1.0 INTRODUCTION

1.1 DOCUMENT SCOPE

This data sheet applies to both the 3.3 volt or 5.0 volt or 3.3 volt and 5.0 volt (mixed voltage) WD76C20ALV device. The WD76C20ALV can be used with either a 5.0 volt power supply or a low voltage 3.3 volt power supply. Some references are included to the WD76C20A which operates only at 5 volts.

1.2 FEATURES

The WD76C20ALV includes these features:

- 84-pin PQFP packages
- 100-pin SQFP packages
- 3.3V or 5.0 volt or 3.3 volt and 5.0 volt VCC operation
- 3.3V nominal battery backup supply for 5.0V V_{CC} device and 2.4V nominal battery backup for 3.3V V_{CC} device. The battery backup supply is used for RTC and 114 byte SRAM
- Implemented in a low-power, high-performance, 1.25 micron CMOS technology process
- Option to interface with external analog PLL device (100-pin SQFP only)
- Option to select and de-select digital PLL internal to chip (100-pin SQFP only)
- Default digital PLL, internal to WD76C20ALV device (84-pin PQFP device only)
- Floppy Disk Controller (FDC) software transparent power-down mode with low standby ICC current. FDC features:
  - 256 tracks support
  - 100% software compatible with NEC 765A
  - Integrated high-performance DPLL data separator:
- 125, 250, 300, 500 Kb/sec and 1 Mb/sec data rates
- Option to select 150 Kb/sec FM and 300 Kb/sec MFM data rates only
  - Automatic Write Precompensation:
    - Defeat option
    - Inner track value of 125 or 187 ns pin selectable
  - On chip clock generation:
    - 2 TTL clock inputs, or
    - Single 16 MHz crystal circuit and one TTL clock input
- PQR circuitry- power qualified reset circuitry
  - PQR disabled in 3.3 volt application, 84-pin package
  - PQR enabled in 5.0 volt application, 84-pin package
  - PQREN external pin to enable and disable PQR circuitry internal to chip (only in 100-pin SQFP package and 5.0 volt application)
  - Host interface read/write accesses compatible with 80286 microprocessors at speeds of 12 MHz with 0 wait states
  - Direct floppy disk drive interface - no buffers needed
    - 48 mA sink output drivers
    - Schmitt Trigger input line receivers
  - FDC direct PC XT/AT interface compatibility
    - Floppy Control and Operations Registers on chip
    - In PC/AT mode, provides required signal qualification to DMA channel
    - IBM BIOS compatible
    - Dual-speed spindle drive support
  - PS/2 type drive support
- Real Time Clock (RTC) features:

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- Software compatible with Motorola MC146818A.
- Internal time base and oscillator circuitry
- Counts seconds, minutes, and hours
- Counts days of the week, date, month, and year
- Time base input for 32.768 KHz square wave
- Time base oscillator for parallel resonant crystals
- Binary or BCD representation of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight savings time option
- Automatic leap year compensation
- Interfaced with software as 128 RAM locations
- 114 bytes of general purpose RAM
- Status bit indicates data integrity
- Bus compatible interrupt signals (IRQ)
- Three interrupts are separately software maskable and testable:
  - Time-of-day alarm - once-per-second to once-per-day
  - Periodic interrupt rates from 122 us to 500 ms
  - End-of-clock update cycle

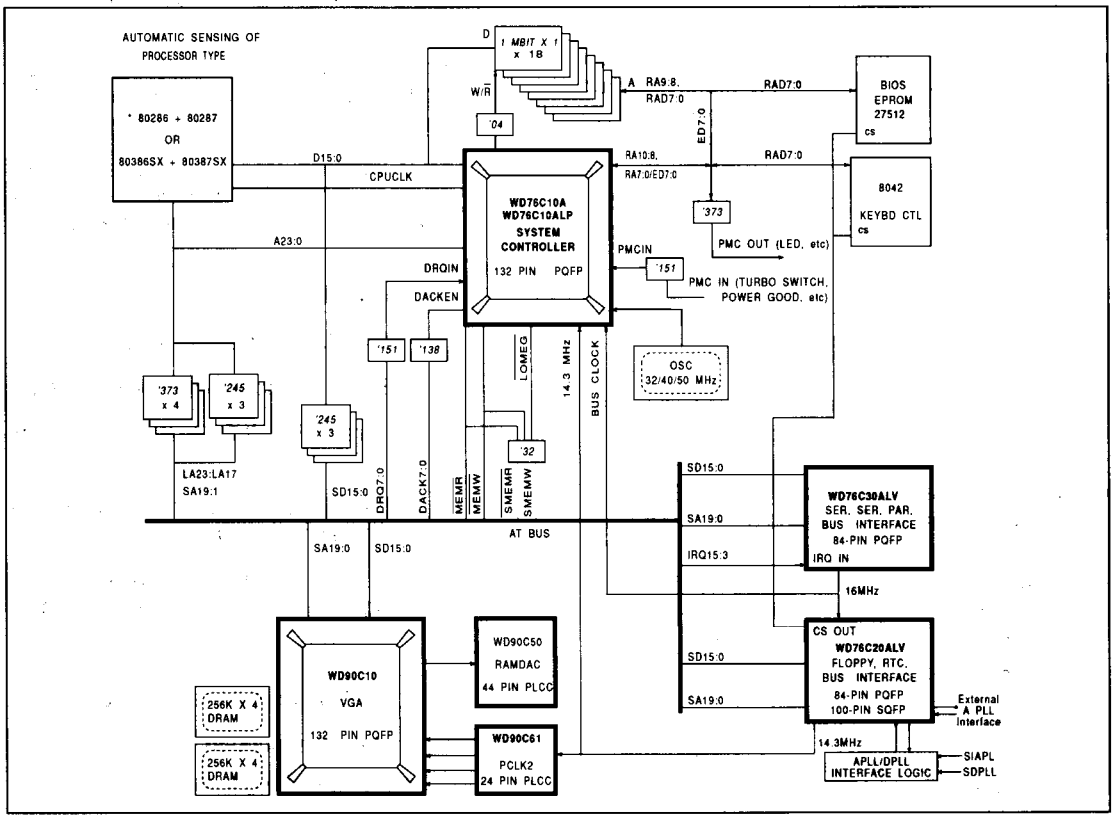

FIGURE 1-1. SYSTEM LEVEL FUNCTIONAL BLOCK DIAGRAM

1.3 GENERAL DESCRIPTION

The WD76C20ALV is a member of the WD7600 chip set which provides a cost-effective, power-efficient solution to PC systems design, especially those relating to "lap-top" devices. The set includes the WD76C10, the WD76C20ALV, and the WD76C30ALV as shown in Figure 1-1. Together these chips provide all necessary logic to build a fully integrated system board for several varieties of IBM PC/AT compatibles including systems using 80286, 80386SX, and 80C286 processors.

As part of this chip set, the WD76C20ALV provides these integral functions:

- Bus Interface Logic
- IDE Interface
- Chip Select Logic
- Floppy Disk Controller
- Real Time Clock
- Suspend/Resume Logic

The Floppy Disk Controller (FDC) component provides necessary timing and signalling between the host processor peripheral bus and a floppy disk drive through a cable connector.

The Real Time Clock component provides calendar and clock information for the system.

The IDE Interface controls buffering between the system's AT Bus and PC/AT compatible IDE drive interface.

The Bus Interface Logic controls buffering of data between the system's AT Bus and the WD76C20ALV.

The Chip Select Logic section provides decoding for selected chip functions both within the WD76C20ALV and on the PC/AT motherboard.

Suspend/Resume Logic provides support for chip set power-down and resume sequences.

The remainder of this manual contains the following information:

Section 2 discusses the basic system architecture.

Section 3 provides signal descriptions.

Section 4 discusses the Chip Select Logic in more detail.

Section 5 discusses the Floppy Disk Controller in more detail.

Section 6 provides additional information on the IDE Interface.

Section 7 provides information on the Real Time Clock and SRAM.

Section 8 gives more information on the Suspend/Resume Logic.

Section 9 provides DC Operating Characteristics.

Section 10 provides AC Interface Timing.

Section 11 shows several package diagrams.

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1.4 FEATURE DIFFERENCES BETWEEN WD76C20ALV 84-PIN PQFP AND 100-PIN SQFP PACKAGES

- The WD76C20ALV (84-pin PQFP package) is backward compatible to the WD76C20 device for 5.0 volt and 3.3 volt applications.

- The WD76C20ALV (100-pin SQFP package) has two new programmable chip select outputs, they are PROG2 and PROG3 signals.

- The WD76C20ALV has integrated internal to the chip the level translators for interfacing directly to 5.0 volt or 3.3 volt signals. The WD76C20ALV can operate in 5.0 volt or 3.3 volt or mixed voltage (3.3 volt and 5.0 volt) environment.

- PQR (Power Qualified Reset). The PQR is disabled in 3.3 volt and mixed voltage operation. The PQR can be enabled in 5.0 volt VCC operation for a 100-pin SQFP packaged device by the PQREN pin. Also PQR is enabled as a default in the 5.0 volt, 84-pin PQFP packaged device.

- WD76C20ALV (100-pin SQFP) provides an interface to the external PLL (phase lock loop) device as an option. This is an option and can be selected by SIAPL and SDPLL input signals to the device. See details in the Signal Description section. This feature is provided in the 100-pin SQFP device only.
  - The default for the 84-pin PQFP device is digital PLL selection, which is internal to the WD76C20ALV device.

2.0 ARCHITECTURE

The WD76C20ALV has three principal functions as illustrated in Figure 2-1. First, it exchanges control signals with the WD76C10 System Controller. Second, under control of the WD76C10, it exchanges data and qualified operation/status information with the Host via the system's AT Bus. Third, it provides complete control and data read/write services for one to four floppy disk units.

Internally, the WD76C20ALV has the following functional components:

- Bus Interface Logic
- Chip Select Logic
- IDE Drive Interface
- Floppy Disk Controller
- Real Time Clock and associated SRAM
- Suspend/Resume Logic

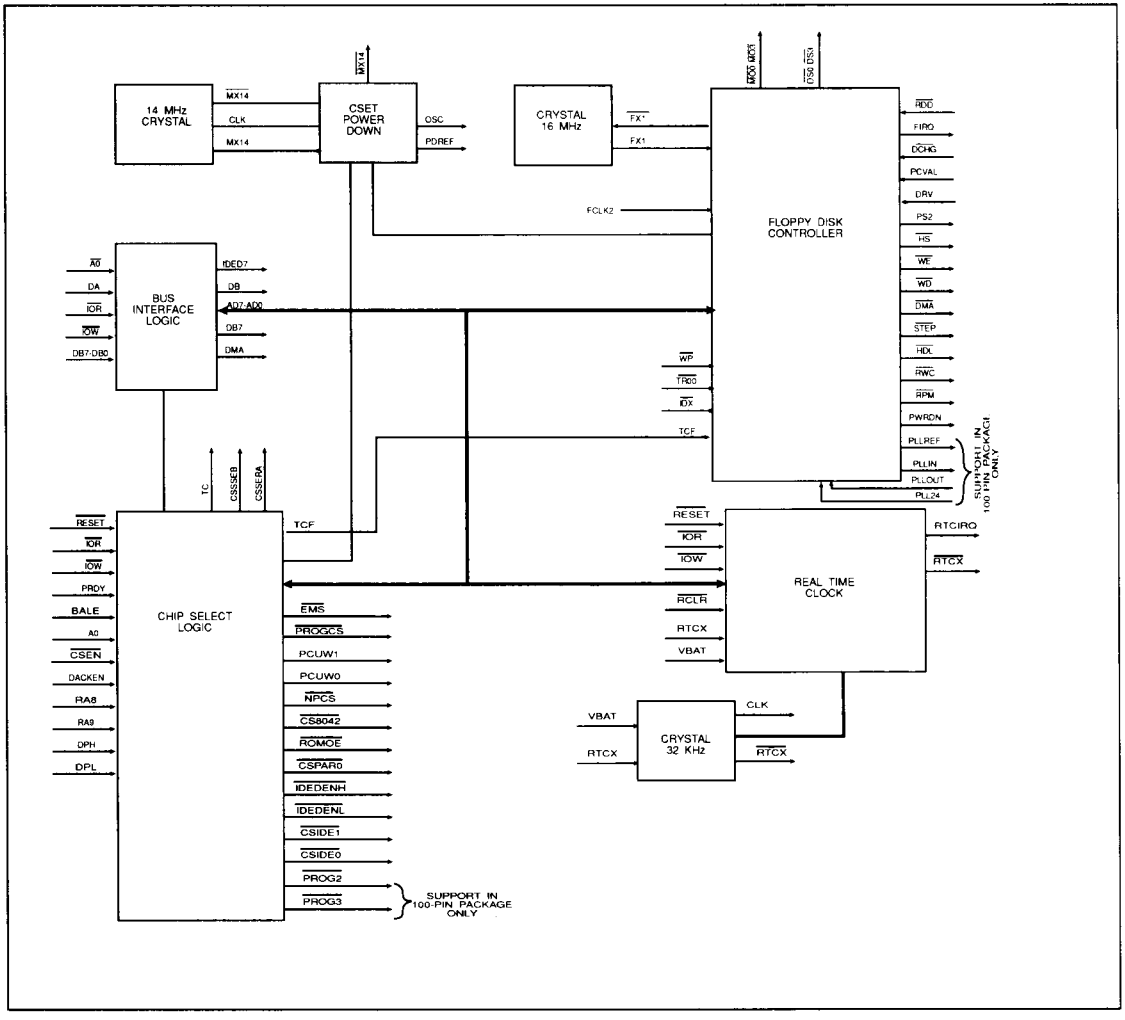

FIGURE 2-1. WD76C20ALV FUNCTIONAL BLOCK DIAGRAM

These functional components are described briefly in the following sections.

For a more detailed description of Chip Select Logic, IDE Interface Support, Floppy Disk Controller, Real Time Clock, and the Suspend/Resume Logic, refer to Sections 4 through 9. Signals mentioned in the following discussion are listed and described in Section 3.

2.1 BUS INTERFACE LOGIC

The chip's Bus Interface controls the buffering of bits D0-D7 passing between the system's AT Bus and any WD76C20ALV internal source/destination 8-bit storage cell via the internal bus. The Bus Interface receives the $\overline{IOR}$ and $\overline{IOW}$ signals from the WD76C10, and with the appropriate chip selects from the Chip Select Logic (CSL), it parallel-passes D0-D7 from the AT Bus to an internal WD76C20ALV cell, or vice versa. The internal cells which the Bus Interface Logic reads/writes to are:

- The Control, Master Status, Status, Data, or Operation Registers in the Floppy Disk Controller
- The 128 registers in the SRAM affiliated with the Real Time Clock.

The Bus Interface Logic also provides a controlled bidirectional path for bit D7 between the AT Bus and the IDE Drive Port.

2.2 CHIP SELECT LOGIC

The Chip Select Logic (CSL) component of the WD76C20ALV provides the decoding needed both for selecting chip functions within the WD76C20ALV and on the PC/AT motherboard. It receives the DPL, DPH, and RA8-RA10 signals from the WD76C10 Systems Controller and outputs appropriately decoded chip select signals (detailed in Section 3). Overall control of the decoding processes is accomplished using the $\overline{CSEN}$ and DACKEN signals from the WD76C10. CSEN enables the decoded output, while DACKEN causes the CSL to ignore the inputs from the WD76C10.

2.3 FLOPPY DISK CONTROLLER

The Floppy Disk Controller (FDC) portion of the WD76C20ALV is a VLSI Super Cell that provides all functions required between the host processor peripheral bus and the cable connector to the floppy disk drive. This provides a comprehensive solution to floppy subsystem control. Among its many features, the FDC possesses a software-transparent power-down mode which facilitates the chip's use in lap-top and portable systems. For more information on this component, see Section 5.

2.4 REAL TIME CLOCK AND SRAM

The Real Time Clock (RTC) component of the WD76C20ALV, in conjunction with the 128-byte register file, provides both calendar (day-of-week, day-of-month, month, and year) and clock (hours, minutes, and seconds) information, along with clocked alarms and a periodic interrupt. This interface gets signals from the WD76C20ALV Bus Interface and Chip Select Logic functions and appropriately buffers bits D0-D7 between the WD76C20ALV internal bus and the RTC internal bus accessing the SRAM.

2.5 SUSPEND/RESUME LOGIC

This functional block is used in conjunction with the RTC time base to provide a 14.318 MHz clock output to the WD76C10. This can switch to a 32.768 KHz clock during the low-power Suspend mode. This logic supports the WD7600 power-down and resume sequencing required to run the Floppy Disk Controller and other components during low power.

2.6 DIGITAL/ANALOG PLL (PHASE LOCK LOOP) INTERFACE SUPPORT

Only the WD76C20ALV in the 100-pin SQFP package supports the interface to the external analog PLL device. The interface provided is for the standard external PLL interface as an option.

The default condition for the 84-pin PQFP package is digital PLL selection, which is internal to the WD76C20ALV device. See the table on the next page for details.

NUMBER	DESCRIPTION	SIAPL	SDPLL
1	Selects digital PLL internal to the WD76C20ALV device. (84-pin PLCC/PQFP package)	NC	NC
2	Selects digital PLL internal to the WD76C20ALV device. (100-pin SQFP package)	1	1
3	Selects internal PLL interface logic to provide interface to analog external analog PLL device. (100-pin SQFP package)	1	0

TABLE 2-1. DIGITAL/ANALOG PLL INTERFACE SUPPORT

3.0 SIGNAL DESCRIPTION

Figure 3-1 illustrates the signal names and pin locations on the 84-pin PQFP WD76C20ALV package. Figure 3-2 shows the signal locations and Table 3-1 lists the signal names for the 100-pin SQFP package. Table 3-2 lists the signal names and descriptions grouped by function.

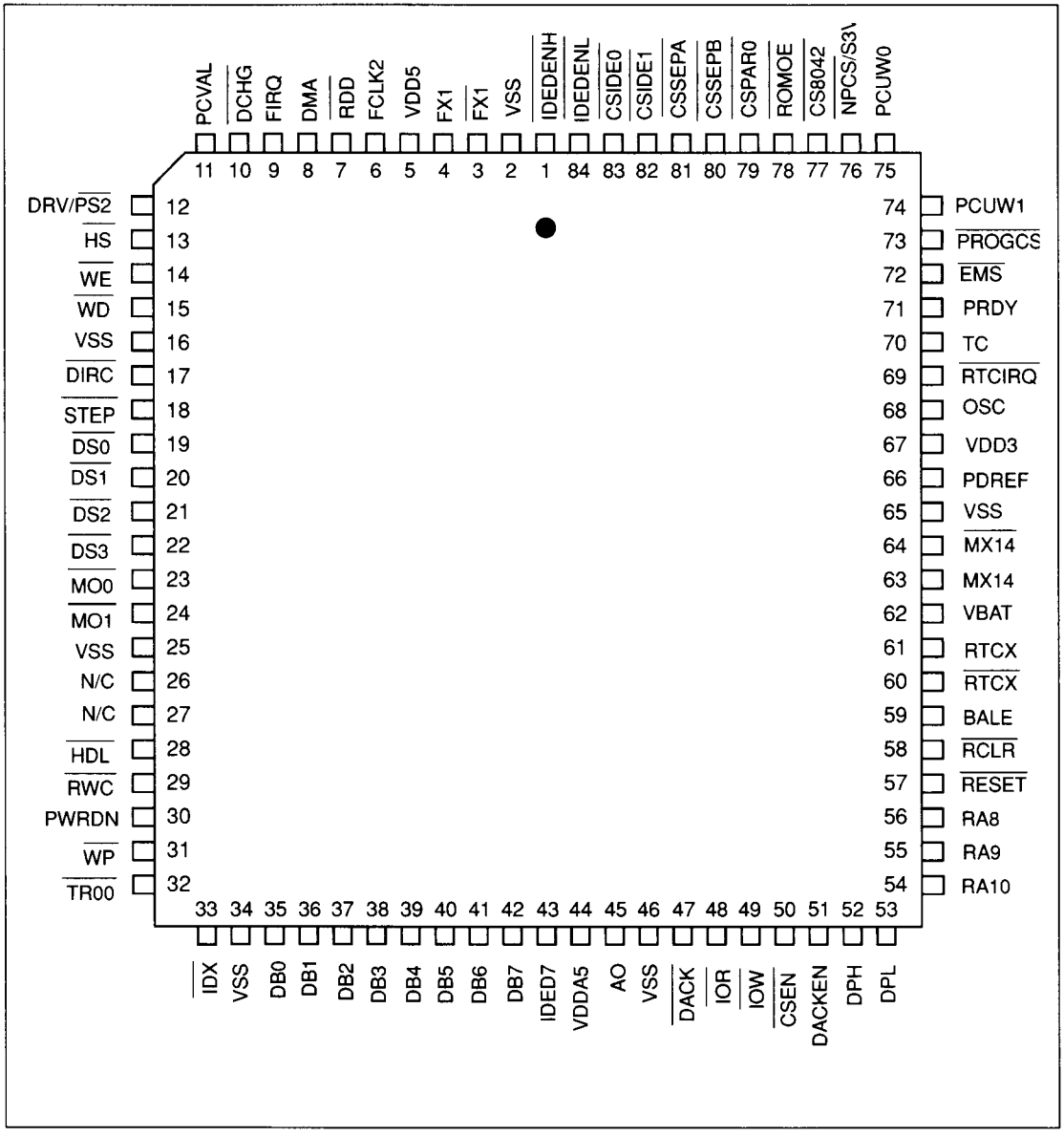

FIGURE 3-1. 84-PIN PQFP DIAGRAM

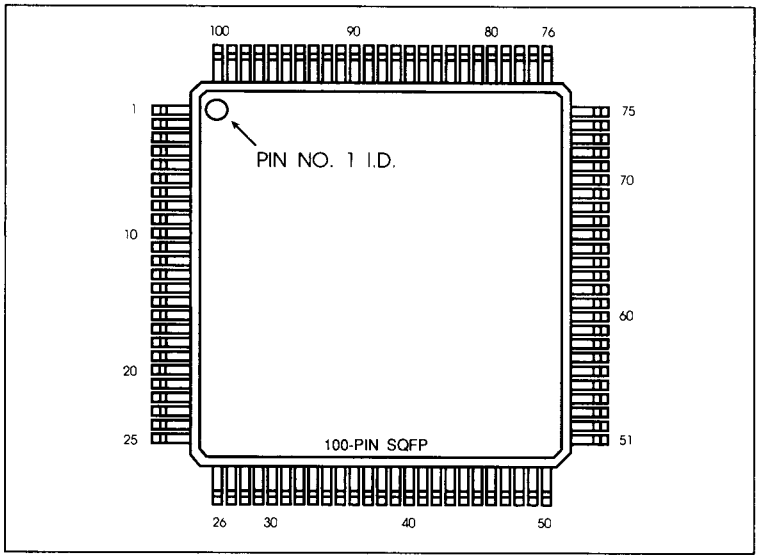

FIGURE 3-2. 100-PIN SQFP DIAGRAM

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PIN-NAME	PIN-NAME	PIN-NAME	PIN-NAME
1-PCUW0	26-VDD3	51-NC	76-NC
2-NPCS/S3V	27-DRV/PS2	52-IDX	77-RA10
3-CS8042	28-HS	53-VSS	78-RA9
4-ROMOE	29-WE	54-DB0	79-RA8
5-CSPAR0	30-WD	55-DB1	80-RESET
6-CSSERB	31-PLLOUT	56-DB2	81-RCLR
7-CSSERA	32-VSS	57-DB3	82-BALE
8-CSIDE1	33-DIRC	58-DB4	83-RTCX
9-CSIDE0	34-STEP	59-DB5	84-RTCX
10-IDEDENL	35-DS0	60-DB6	85-VBAT
11-IDEDENH	36-DS1	61-DB7	86-MX14
12-PLLREF	37-DS2	62-IDED7	87-MX14
13-PLLIN	38-DS3	63-VDDA5	88-VSS
14-VSS	39-MO0	64-PROG2	89-PQREN
15-FX1	40-MO1	65-PROG3	90-PDREF
16-FX1	41-VSS	66-A0	91-VDD3
17-VDDD5	42-SIAPL	67-VSS	92-OSC
18-FCLK2	43-SDPLL	68-DACK	93-RTCIRQ
19-RDD	44-HDL	69-IOR	94-TC
20-PLL24	45-RWC	70-IOW	95-PRDY
21-DMA	46-PWRDN	71-CSEN	96-EMS
22-FIRQ	47-WP	72-DACKEN	97-PROGCS
23-DCHG	48-TR00	73-DPH	98-PCUW1
24-PCVAL	49-NC	74-DPL	99-NC
25-NC	50-NC	75-NC	100-NC

TABLE 3-1. WD76C20ALV PIN ASSIGNMENTS (100 PIN)

84-PIN*	100-PIN**	MNEMONIC	I/O	DESCRIPTION
INTEGRATED DRIVE ELECTRONICS (IDE) INTERFACE				
1	11	$\overline{\text{IDEDENH}}$	O	**IDE Drive Enable High Byte** TTL level output goes active low to enable the IDE drive interface bus transceivers for the high byte of the 16-bit Interface. The signal is used with the $\overline{\text{CSIDE0}}$ 1 card select output signal to the IDE drive only during 16-bit IDE data transfers.
43	62	IDED7	I/O	**IDE Data Bit 7** TTL level I/O providing a data path for bit 7 between the Host and the IDE drive interface. IDED7 is an output, passing data to the IDE drive from DB7 of the Host data bus whenever an $\overline{\text{IOW}}$ to the IDE drive interface is detected. IDED7 is an input, passing data from the IDE drive to DB7 of the Host data bus whenever an $\overline{\text{IOR}}$ of the IDE drive interface is detected, except when reading from address 3F7H. During an $\overline{\text{IOR}}$ of 3F7H, the floppy DCHG status is output on the Host data bus pin DB7.
82	8	$\overline{\text{CSIDE1}}$	O	**IDE Card Select 1** TTL level output is used by the Host to address and communicate with the IDE drive auxiliary registers. Host activates the signal through a decode in the CSL logic block, while at the same time asserting $\overline{\text{IDEDENL}}$.
83	9	$\overline{\text{CSIDE0}}$	O	**IDE Card Select 0** TTL level output is used by the Host to address and communicate with the IDE drive on the I/O channel. The Host activates the signal through a decode in the CSL logic block, while at the same time asserting $\overline{\text{IDEDENL}}$ or both $\overline{\text{IDEDENL}}$ and $\overline{\text{IDEDENH}}$.
84	10	$\overline{\text{IDEDENL}}$	O	**IDE Drive Enable Low Byte** TTL level output goes active low to enable the IDE drive interface bus transceivers for the low byte of the 16-bit Interface. The signal is used with the $\overline{\text{CSIDE0}}$ and $\overline{\text{CSIDE1}}$ card select outputs to the IDE drive.

TABLE 3-2. SIGNAL DESCRIPTIONS

NOTE:
* Pin numbers are for the 84-pin package
** Pin numbers are for the 100-pin package

84-PIN*	100-PIN**	MNEMONIC	I/O	DESCRIPTION
		HOST INTERFACE		
8	21	DMA	O	**DMA Request** (FDC) In PC AT mode, this pin is tristated, enabled by DMAEN signal from the operations register.
45	66	A0	I	**Address Line 0** Address signal selecting data (=1) or status (=0) information for the FDC. A0=0 during the $\overline{IOW}$ is illegal except when using user initiated FDC power down mode.
47	68	$\overline{DACK}$	I	**DMA Acknowledge** Used by DMA controller to transfer data from FDC onto the bus. Logical equivalent to $\overline{FDCS}$ and A0=1. In PC AT mode, this signal is qualified by DMAEN from the operations register.
48	69	$\overline{IOR}$	I	**Input/OutputRead** Read enable allowing data or status information to be transferred onto data bus by the WD76C20ALV.
49	70	$\overline{IOW}$	I	**Input/Output Write** Write enable latching data from the bus into WD76C20ALV buffer register.
57	80	$\overline{RESET}$	I	**Reset** TTL input resets the WD76C20ALV with the exception of the normal timekeeping operations which will remain uninterrupted. Resets all device outputs. Resets FDC controller, placing microsequencer in idle PC/AT mode.

TABLE 3-2. SIGNAL DESCRIPTIONS (CONTINUED)

NOTE:
* Pin numbers are for the 84-pin package
** Pin numbers are for the 100-pin package

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84-PIN*	100-PIN**	MNEMONIC	I/O	DESCRIPTION
FLOPPY DISK CONTROLLER INTERFACE				
3	15	$\overline{FX1}$	O	**Floppy Crystal Oscillator Output** This pin is an oscillator drive output for a 16 MHz parallel resonant crystal. FX1 should be left floating if a TTL level clock is used at pin FX1.
4	16	FX1	I	**Floppy Crystal Oscillator Input** A crystal oscillator input requiring a 16 MHz parallel resonant crystal. This oscillator is used for all standard data rates, and may be driven with a 16 TTL level signal instead of using the crystal circuitry.
6	18	FCLK2	I	**Floppy Clock** TTL level input used for non-standard data rates, can be driven with a 9.6 MHz clcok for 300kb/s MFM data rate and only be selected from the control register.
7	19	$\overline{RDD}$	I	**FDC Read Disk Data** This is the raw serial bit stream from the disk drive. Each falling edge of the pulses represents a flux transition of the encoded data.
9	22	FIRQ	O	**Floppy Interrupt Request** Interrupt request indicating completion of command execution or data transfer requests (non-DMA mode). In PC AT mode, this pin is tristated, enabled by the DMAEN signal from the operations register.
10	23	$\overline{DCHG}$	I	**FDC Disk Changed** This Schmitt Trigger (ST) input senses status from the disk drive indicating active low as the drive door is opened or that the diskette has possibly changed since the last drive selection. The pin has an internal pull-up resistor.
11	24	PCVAL	I	**Precompensation Value** This pin determines the amount of write precompensation used on the inner tracks of the diskette. Logic 1=125 ns, 0=187 ns. In the defeat option, the PCVAL input is a don't care and internally the precompsation value is disabled.
12	27	DRV/$\overline{PS2}$	I/O	**Drive Set (PS2)** In the input mode, a logic 0 indicates to the FDC that a 2-speed spindle motor is present and that FCLK2 should be grounded because it will not be used. As an option this pin can be defined as an output to support the floppy drive connector pin 2 for PS2 style drives, indicating that the FDC is set internally for a single spindle motor. The pin has an internal pull-up resistor.

TABLE 3-2.SIGNAL DESCRIPTIONS (CONTINUED)

NOTE:
* Pin numbers are for the 84-pin package
** Pin numbers are for the 100-pin package

84-PIN*	100-PIN**	MNEMONIC	I/O	DESCRIPTION
13	28	$\overline{HS}$	O	**Head Select** This high current driver (HCD) output selects the head, i.e., side, of the floppy disk that is being read or written. Logic 1 = side 0, logic 0 = side 1.
14	29	$\overline{WE}$	O	**Write Enable** This HCD output becomes true, active low, just prior to writing on the diskette. This allows current to flow through the write head.
15	30	$\overline{WD}$	O	**Write Data** This HCD is the write data output. Each falling edge of the encoded data pulse stream causes a flux transition on the media.
17	33	$\overline{DIRC}$	O	**Direction (Stepper)** This HCD output determines the direction of head stepper motor. Logic 1 = outward motion, logic 0 =inward motion.
18	34	$\overline{STEP}$	O	**Stepper** This HCD output issues an active low pulse for each track to track movement of the head.
29	45	RWC/RPM	O	**Reduced Write Current or RPM Select** This HCD output, when active low, causes a reduced write current when bit density is increased toward the inner tracks, becoming active when tracks greater than 28 are accessed. In PC/AT mode, this signal can be used on 2-speed drives to select 300 RPM, active low, when 250 MFM or 125 FM Kb/s data rate is selected and DRV=0.
30	46	PWRDN	O	**Power Down** TTL compatible output when active high indicates that the FDC portion of the WD76C20ALV has gone into power-down mode. This signal can be used to power-down the floppy drive if supported.
31	47	$\overline{WP}$	I	**Write Protect** This Schmitt Trigger (ST) input senses status from the disk drive indicating, active low, when a diskette is write protected.
32	48	$\overline{TR00}$	I	**Track 00** This ST input senses status from the drive indicating, active low, when the head is positioned over the outermost track, track 00.
33	52	$\overline{IDX}$	I	**Index** This ST input senses status from the drive indicating, active low, when the head is positioned over the beginning of a track, marked by an index hole.

TABLE 3-2. SIGNAL DESCRIPTIONS (CONTINUED)

NOTE:
* Pin numbers are for the 84-pin package
** Pin numbers are for the 100-pin package

84-PIN*	100-PIN**	MNEMONIC	I/O	DESCRIPTION
CHIP SELECT INTERFACE				
50	71	$\overline{\text{CSEN}}$	I	**Chip Select Enable** The chip select enable TTL input line is used to output enable the appropriate CSL control line as decoded from the RA8, RA9, RA10, DPL, and DPH inputs. When DACKEN is asserted low, the function of $\overline{\text{CSEN}}$ is negated. When used to enable and disable the WD76C30ALV 48 MHz clock, $\overline{\text{CSEN}}$ acts as a strobe to a latch. When it and DACKEN are both asserted, the TC output will go high.
51	72	DACKEN	I	**DMA Acknowledge Enable** TTL input that indicates the Host is performing a DMA transfer unrelated to the WD76C20ALV. When active low, it is used to disqualify all CSL input lines.
52	73	DPH	I	**Chip Select Address Parity High** Decoded chip select TTL input, bit CS4.
53	74	DPL	I	**Chip Select Address Parity Low** Decoded chip select TTL input, bit CS3.
54	77	RA10	I	**Chip Select Address Line 10** Decoded chip select TTL input, bit CS2.
55	78	RA9	I	**Chip Select Address Line 9** Decoded chip select TTL input, bit CS1.
56	79	RA8	I	**Chip Select Address Line 8** Decoded chip select TTL input, bit CS0.
59	82	BALE	I	**Chip Select Bus ALE** TTL input when active high, causes latches on the CLS input lines ($\overline{\text{CSEN}}$, RA8, RA9, RA10, DPL, and DPH) to become transparent. When BALE is forced low, the data in the transparent latches is latched. This pin has an internal pull-up resistor so the pin can be left unconnected and the latches are transparent.
70	94	TC	O	**Terminal Count** TTL level output used to indicate that the final count has been reached during a Host DMA transfer unrelated to the WD76C20ALV. It is also used internally by the FDC to indicate that a DMA transfer to the floppy drive is complete. TC asserts high when both DACKEN and $\overline{\text{CSEN}}$ are asserted. (DACKEN=1, $\overline{\text{CSEN}}$=0)

TABLE 3-2. SIGNAL DESCRIPTIONS (CONTINUED)

NOTE:
* Pin numbers are for the 84-pin package
** Pin numbers are for the 100-pin package

84-PIN*	100-PIN**	MNEMONIC	I/O	DESCRIPTION
71	95	PRDY	I	**Processor Ready** Schmitt Trigger input senses processor ready status to help latch the CSL inputs correctly during system byte swapping activities. This pin has an internal pull-up resistor so that it can be left unconnected when not used. The PRDY input should be used in system designs that use the BALE pin.
72	96	$\overline{EMS}$	O	**External EMS** TTL card select output decoded from CSL input lines and issued to select external EMS.
73	97	$\overline{PROGCS}$	O	**CMOS Chip Select Program Chip** CMOS chip select output decoded from CSL input select lines and issued as a programmable chip select.
NA	64	$\overline{PROG2}$	O	**CMOS Chip Select Program Chip** CMOS chip select output decoded from CSL input select lines and issued as a programmable chip select 2.
NA	65	$\overline{PROG3}$	O	**CMOS Chip Select Program Chip** CMOS chip select output decoded from CSL input select lines and issued as a programmable chip select 3.
74	98	PCUW1	O	**Power Control Unit Write Strobe 1** TTL write strobe output decoded from CSL input lines and issued to write to the PCU #1.
75	1	PCUW0	O	**Power Control Unit Write Strobe 0** TTL write strobe output decoded from CSL input lines and issued to write to the PCU #0.
76	2	NPCS	O	**Numerical Processor Chip Select** TTL chip select output decoded from CSL input lines and issued to select the numerical processor, the 80287.
		S3V	I	**Sense 3.3V or 5.0V VCC Operation** This signal is used to latch the information on this pin during system reset or power-up reset. Internally all input buffers are configured to accept TTL levels for 3.3 volt or 5.0 volt VCC operation. (VCC=VDD3) When S3V=0, the input threshold is set for 3.3 volt VCC.† When S3V=1, the input threshold is set for 5.0 volt VCC.†
77	3	$\overline{CS8042}$	O	**8042 Chip Select** TTL chip select output decoded from CSL input lines and issued to select the 8042.
78	4	$\overline{ROMOE}$	O	**ROM Output Enable** TTL chip select output decoded from CSL input lines and issued to output enable the BIOS ROM.

TABLE 3-2. SIGNAL DESCRIPTIONS (CONTINUED)

NOTE:
* Pin numbers are for the 84-pin package
** Pin numbers are for the 100-pin package
† The VCC here denotes VDD3 power pin. All input receivers are powered by a VDD3 power pin.

84-PIN*	100-PIN**	MNEMONIC	I/O	DESCRIPTION
79	5	$\overline{\text{CSPAR0}}$	O	**CSL Parallel Port#0 Chip Select** TTL chip select output decoded from CSL input lines and issued as a chip select to the WD76C30ALV to enable the parallel port #0.
80	6	$\overline{\text{CSSERB}}$	O	**CSL Serial Port B Chip Select** TTL chip select output decoded from CSL input lines and issued as a chip select to the WD76C30ALV to enable the serial port B.
81	7	$\overline{\text{CSSERA}}$	O	**CSL Serial Port A Chip Select** TTL chip select output decoded from CSL input lines and issued as a chip select to the WD76C30ALV to enable the serial port A.
REAL TIME CLOCK INTERFACE				
58	81	$\overline{\text{RCLR}}$	I	**Real Time Clock RAM Clear** TTL input used to clear all 114 bytes of the general purpose RAM. None of the clock, calendar, or RAM functions are interrupted, and the 14 registers that are used by the RTC are left unchanged. This pin has an internal pull-up so it **must** be left unconnected.
60	83	$\overline{\text{RTCX}}$	O	**Real Time Clock Time Base XTAL Out** Crystal oscillator output for parallel resonant AT cut crystal at 32.768 KHz.
61	84	RTCX	I	**Real Time Clock Time Base XTAL In** Crystal oscillator input (32.768 KHz) for use with crystal oscillator circuit.
62	85	VBAT	NA	**Battery Backup** Battery backup power supply V_{DD} pin. A 3.3/2.0-volt battery connector can be attached here to maintain the RTC timekeeping functions and SRAM integrity during system power downs. The 3.3/2.0-volt based on the 5.0/3.3-volt systems respectively.
69	93	$\overline{\text{RTCIRQ}}$	O	**Real Time Clock Interrupt Request** TTL output that is set to tristate unless the RTC needs to interrupt the processor, during which time the pin goes low and stays low until register C is read, or the part is reset through the RESET pin.

TABLE 3-2. SIGNAL DESCRIPTIONS (CONTINUED)

NOTE:
* Pin numbers are for the 84-pin package
** Pin numbers are for the 100-pin package

84-PIN*	100-PIN**	MNEMONIC	I/O	DESCRIPTION
SUSPEND /RESUME SUPPORT INTERFACE				
63	86	14MX	I	**14 MHz Crystal Oscillator Input** Crystal oscillator input for the 14.318 MHz oscillator.
64	87	$\overline{14MX}$	O	**14 MHz Crystal Oscillator Output** Crystal oscillator output for the 14.318 MHz oscillator.
66	90	PDREF	O	**Power Down Refresh** External DRAM refresh line used to support the WD76C10 when the WD76C10 goes into hibernation mode. During hibernation mode, this signal provides a 1.0 µs ± 5 µs pulse once every 122.1 µs (using a 50% duty cycle), and is used to maintain the DRAM integrity with as little power as possible. Hibernation mode is entered when a CSL address of 15H is detected, and hibernation mode is exited when a CSL of 16H is issued.
68	92	OSC	O	**Oscillator (WD76C10 Clock Driver)** TTL clock driver output used to support the WD76C10. When not in the WD76C10's "hibernation" mode, the output waveform is a 14.318 MHz square wave, and when in hibernation mode it becomes a 32.768 KHz square wave. The WD76C10 hibernation mode is entered when a CSL address of 15H is detected, and hibernation mode is exited when a CSL address of 16H is issued.
DATA BUS				
35-42	54-61	DB(0:7)	I/O	**Data/Address Bus** 8-bit bi-directional, tristateable data bus.

TABLE 3-2. SIGNAL DESCRIPTIONS (CONTINUED)

NOTE:
* Pin numbers are for the 84-pin package
** Pin numbers are for the 100-pin package

84-PIN*	100-PIN**	MNEMONIC	I/O	DESCRIPTION
		MOTOR CONTROL		
23	39	$\overline{MO0}$	O	**Motor On #0** This HCD output, when active low, is motor on enable bit 0. The proper motor enable signal can be decoded externally if required.
24	40	$\overline{MO1}$	O	**Motor On #1** This HCD output, when active low, is motor on enable bit 1. The proper motor enable signal can be decoded externally if required.
26	42	SIAPL	I	**Select Analog PLL Device** This input signal is used to select the analog PLL interface logic internal to the WD76C20ALV device as an option in the 100-pin SQFP package. This signal is used in conjunction with the SDPLL input signal. See detailed description of options in section 2.6. This feature is only supported in the 100-pin SQFP package. SIAPL=1 selects the internal analog PLL interface logic for the external PLL device. SIAPL=1 selects the internal digital PLL logic and disables the external analog PLL interface. It has an internal pull-up and can be a no connect in the 84-pin PQFP device.
27	43	SDPLL	I	**Select Digital PLL Logic** This input signal is used to select the digital PLL internal to the WD76C20ALV device. This input signal in conjunction with SIAPL determines the option of DPLL or APLL selection. See detailed description in section 2.6. SDPLL=1 selects DPLL . SDPLL=0 selects the internal analog PLL interface for the external PLL device This feature is only supported in the 100-pin SQFP package. The default for the 84-pin PQFP is digital PLL selection. This signal has an internal pull-up and can be a no connect in the 84-pin PQFP device.

TABLE 3-2. SIGNAL DESCRIPTIONS (CONTINUED)

NOTE:
* Pin numbers are for the 84-pin package
** Pin numbers are for the 100-pin package

84-PIN*	100-PIN**	MNEMONIC	I/O	DESCRIPTION
		DRIVE SELECT		
19	35	$\overline{DS0}$	O	**Drive Select #0** This HCD output, when active low, is Drive #0 select in PC/AT mode, enabling the interface in the disk drive. The signal is qualified by the MOEN0 signal.
20	36	$\overline{DS1}$	O	**Drive Select #1** This HCD output, when active low, is Drive #1 select in PC/AT mode, enabling the interface in the disk drive. The signal is qualified by the decoded MOEN1 signal.
21	37	$\overline{DS2}$	O	**Drive Select #2** This HCD output, when active low, is Drive #2 select in PC/AT mode, enabling the interface in the disk drive. The signal is qualified by the decoded MOEN2 signal.
22	38	$\overline{DS3}$	O	**Drive Select #3** This HCD output, when active low, is Drive #3 select in PC/AT mode, enabling the interface in the disk drive. The signal is qualified by the decoded MOEN3 signal.
28	44	$\overline{HDL}$	O	**Head Load** This HCD output when active low causes the Head to be loaded against the media in the selected drive.
		EXTERNAL ANALOG PLL INTERFACE (OPTIONAL)		
NA	12	PLLREF	O	**Phase Lock Loop Ref** Interface to external PLL signal input.
NA	13	PLLIN	O	**Phase Lock Loop In** Interface to external PLL comparator input.
NA	20	PLL24	I	**Phase Lock Loop Clock** This is the 24 MHz clock input. Tie to ground if not used.
NA	31	PLLOUT	I	**Phase Lock Loop Out** VCO output from the external PLL to the WD76C20ALV PLL interface logic. Tie to ground if not used.
		POWER QUALIFY RESET		
NA	89	PQREN	I	**Power Qualifed Reset** This input when active high enables the floppy disk controller internal power-up reset circuitry. This applies only to 5.0 volt applications.

TABLE 3-2. SIGNAL DESCRIPTIONS (CONTINUED)

NOTE:
* Pin numbers are for the 84-pin package
** Pin numbers are for the 100-pin package

84-PIN*	100-PIN**	MNEMONIC	I/O	DESCRIPTION
POWER, GROUND, MISCELLANEOUS				
67	26, 91	VDD3	NA	**3.3V Power or 5.0 V Power** Power to device core and I/O
44	63	VDDA5	NA	**+5V Power or 3.3 V Power** 5 volt or 3.3 volt power for AT bus interface
5	17	VDDD5	NA	**+5V Power or 3.3 V Power** 5 volt or 3.3 volt power for drive interface
2, 16, 25, 34, 46, 65	14, 32, 41, 53, 67, 88	VSS	NA	**Ground**
NA	25, 49, 50, 51, 75, 76, 99, 100	NC	NA	**Not Connected and Not Defined**

TABLE 3-2. SIGNAL DECRIPTIONS (CONTINUED)

NOTE:
* Pin numbers are for the 84-pin package
** Pin numbers are for the 100-pin package

3.1 MAPPING OF POWER PINS TO I/O SIGNALS AND DEVICE CORE

This section summarizes the mapping of device signal pins to a particular power pin connected to a 3.3 volt or 5.0 volt board power plannar.

There are three VDD pins in the WD76C20ALV device. Table 3-3 shows one of the mixed mode power pin distribution examples for mapping the power pins to the signals. The VDD pin description and pin numbers for 84-pin PQFP and 100-pin SQFP packages are included.

Table 3-4 shows the group of signals associated with a particular VDD power pin.

POWER PIN NAME	DESCRIPTION	84-PIN PQFP#	100-PIN SQFP#
VDD3	3.3 volt power pin	67	26, 91
VDDA5	5.0 volt power pin	44	63
VDDD5	5.0 volt power pin	5	17

TABLE 3-3. EXAMPLE MAPPING OF I/O POWER PINS TO SIGNALS

Note: VDDA5 can be connected to either 5.0 volts or 3.3 volts
VDDD5 can be connected to either 5.0 volts or 3.3 volts
VDD3 can be connected to either 5.0 volts or 3.3 volts
All the input receivers are powered by VDD3 power pin
The device can be powered by all 5.0 volt VDDs or 3.3 volt VDDs or 5.0 volt and 3.3 volt mixed mode VDDs as long as the device interface requirements are met.

7

GROUP#	DESCRIPTION	SIGNAL NAMES	BUFFER TYPE	VDD TYPE
GROUP 1, VDD3: 5.0 VOLT OR 3.3 VOLT DEVICE CORE AND I/O				
1	Chip core and	chip core	N/A	VDD3
	IDE Interface	IDEDENH, IDEDENL	O	VDD3
	FDC Interface	FX1	O	VDD3
		FX1, DCHG, PCVAL,	I	VDD3*
		WP, TR00, IDX, RDD, FCLK2	I	VDD3*
		DRV/PS2	I/O (OC)	VDD3*
		HS, WE, WD, DIRC, STEP, HDL	OC	VDD3*
		RWC/RPM, MO0-1, DS(0-3)	OC	VDD3*
		PWRDN	O	VDD3
		PQREN, SIAPL, S3V, SDPLL	I	VDD3
	AT Interface	RESET	I	VDD3
	Chip Select Interface	CSEN, DACKEN, DPH, DPL,	I	VDD3
		RA8, RA9, RA10, PRDY	I	VDD3
		EMS, PROG2, PROG3,	O	VDD3
		PROGCS, PCUW1, PCUW0,	O	VDD3
		NPCS, ROMOE, CS8042,	O	VDD3
		CSPAR0, CSSERB, CSSERA	O	VDD3
	RTC Interface	RCLR, RTCX	I	VDD3
		RTCIRQ, RTCX	O	VDD3
	Suspend/Resume Interface	MX14	I	VDD3
		MX14, PDREF	O	VDD3
GROUP 2, VDDD5: 5. 0 VOLT OR 3.3 VOLT DRIVE INTERFACE				
2	IDE Interface	CSIDE1, CSIDE0	O	VDDD5
		* IDED7	I/O	VDDD5
GROUP 3, VDDA5: 5.0 VOLT OR 3.3 VOLT AT BUS AND APLL INTERFACE				
3	AT Bus Interface	* A0, IOR, IOW, DACK, BALE	I	VDDA5
		FIRQ, TC, OSC	O	VDDA5
		* DB(0-7), DMA	I/O	VDDA5
	APLL Interface Separator	* PLL24, PLLOUT	I	VDDA5
		PLLIN, PLLREF	O	VDDA5

TABLE 3-4. SIGNAL GROUPS

* Input protection and internal pull-ups applicable to these signals are connected to VDDA5 or VDDD5 power pin.
Input receivers for these signals are powered by VDD3 power pin.

4.0 CHIP SELECT LOGIC

The Chip Select Logic is handled cooperatively by all the chips in the chip set, with each chip contributing its part to the logic. The WD76C10 and WD76C20ALV are particularly interrelated. Many of the decoding operations begun by the WD76C10 are handed to the WD76C20ALV for completion, and vice versa. For this reason, it is necessary to read both this section and section 7 of the WD76C10 for the fullest possible understanding of this function.

The Chip Select Logic of the WD76C20ALV provides decoding of five CSL input lines, DPH, DPL, RA10-8, into 17 output lines.

Figure 4-1 provides a block diagram of the inputs and outputs associated with this component.

Before the decoder can function, it must be enabled by $\overline{CSEN}$ going active low and remains open until it is disabled by DACKEN going active high. Optionally, the chip select inputs ($\overline{CSEN}$, DPH, DPL, RA10, RA9, RA8) can be latched by dropping the BALE from 1 to 0. These latches are transparent when BALE is held high or left unconnected.

Once enabled, the Chip Select Logic provides decoding for the following signals, as shown in Table 4-1.

Table 4-2 lists the I/O addresses and chip selects generated for each fixed port. Address bits A15 through A10 are ignored for the I/O addresses listed with three digits. The ports are listed in the sequence of the chip select value.

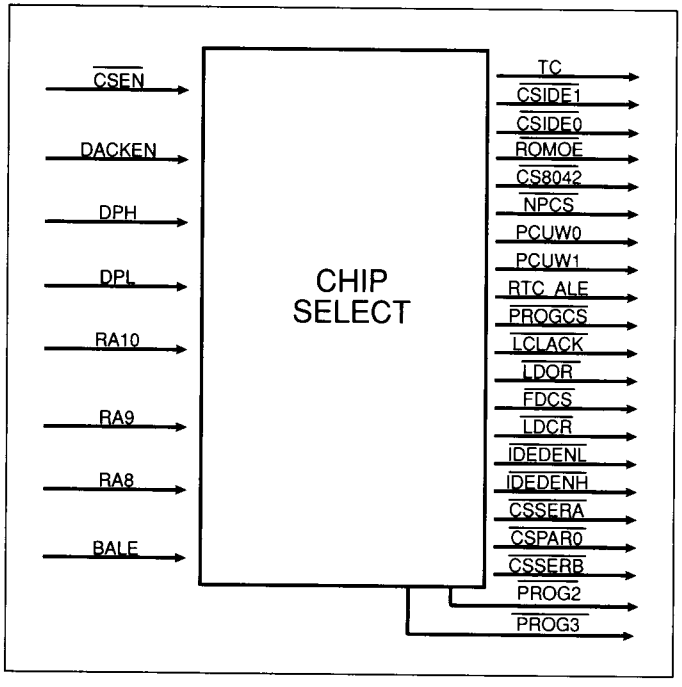

FIGURE 4-1. CHIP SELECT BLOCK DIAGRAM

CS#	CSL INPUT LINES DPH	DPL	RA10	RA9	RA8	FUNCTION
00H	0	0	0	0	0	Assert $\overline{\text{ROMOE}}$ to Output Enable the ROM BIOS[1]
01H	0	0	0	0	1	Assert $\overline{\text{CS8042}}$ to Chip Select the Keyboard Control[1]
02H	0	0	0	1	0	Assert $\overline{\text{NPCS}}$ to Chip Select the Numeric Processor[1]
03H	0	0	0	1	1	Assert PCUW0 to Write Strobe PCU #0
04H	0	0	1	0	0	Assert $\overline{\text{LCLACK}}$ to acknowledge Keyboard Processor[1]
05H	0	0	1	0	1	Assert RTC ALE for RTC I/O[1]
06H	0	0	1	1	0	Assert RTC Write Strobe Gated by $\overline{\text{CSEN}}$ & $\overline{\text{IOW}}$[1]
07H	0	0	1	1	1	Assert RTC Read Stobe Gated by $\overline{\text{CSEN}}$ & $\overline{\text{IOR}}$[1]
08H	0	1	0	0	0	Assert FDC $\overline{\text{LDOR}}$ Register Select Line[1]
09H	0	1	0	0	1	Assert FDC $\overline{\text{FDCS}}$ Chip Select Line[1]
0AH	0	1	0	1	0	Assert FDC $\overline{\text{LDCR}}$ Register (Read/Write) Select Line[1]
0BH	0	1	0	1	1	Assert FDC $\overline{\text{LDCR}}$ Register (Read/Write) Select Line & assert IDEDENL and CSIDE1 IDE Card Select Lines[1]
0CH	0	1	1	0	0	Assert $\overline{\text{IDEDENL}}$ and $\overline{\text{CSIDE0}}$ IDE Card Select Line & assert $\overline{\text{IDEDENH}}$ if A0 = 0[1]
0DH	0	1	1	0	1	Assert $\overline{\text{IDEDENL}}$ and $\overline{\text{CSIDE1}}$ IDE Card Select Line[1]
0EH	0	1	1	1	0	Assert $\overline{\text{CSSERA}}$ to Chip Select Serial Port A[1]
0FH	0	1	1	1	1	Assert $\overline{\text{CSPAR0}}$ to Chip Select Parallel Port 0[1]
10H	1	0	0	0	0	Assert $\overline{\text{CSSERB}}$ to Chip Select Serial Port B[1]
11H	1	0	0	0	1	Assert $\overline{\text{PROGCS}}$[1]
14H	1	0	1	0	0	Assert $\overline{\text{EMS}}$ to signify external EMS memory access[1]
15H	1	0	1	0	1	WD76C30ALV 48 MHz Clk Disable , CSL Latches Code OSSERA, $\overline{\text{CSSERB}}$ & $\overline{\text{CSPAR0}}$ stay asserted[2]
16H	1	0	1	1	0	48 MHz Clk Enable for WD76C30ALV, CSL unlatches code, so $\overline{\text{CSSERA}}$, $\overline{\text{CSSERB}}$ & $\overline{\text{CSPAR0}}$ deassert[3]
17H	1	0	1	1	1	Assert PCUW1 to Write Strobe PCU #1
18H	1	1	0	0	0	Reserved
19H	1	1	0	0	1	Reserved
1AH	1	1	0	1	0	Assert $\overline{\text{PROG2}}$ programmable chip select 2
1BH	1	1	0	1	1	Assert $\overline{\text{PROG3}}$ programmable chip select 3

TABLE 4-1. CHIP SELECT LINE DECODER

[1] These signals are generated using latched CSL inputs if BALE is used.
[2] Suspend Mode is entered by asserting code 15H on the CSL inputs, while qualifying it by $\overline{\text{CSEN}}$=0, $\overline{\text{IOW}}$=0, and the falling edge of OSC.
[3] Suspend Mode is left by asserting code 16H on the CSL inputs, while qualifying it by an OSC falling edge.

PORT	I/O ADDRESS	CS#	FUNCTION
ROM Chip Select	N/A	00	Chip Select for BIOS ROM
Keyboard Control	060 - 06E Even	01	Chip Select For 8042
80287	00E0 - 00FF	02	Chip Select for Numeric Processor
Power Control	7072	03	PMC Write Strobe 0
Reserved		04	Reserved
Real Time Clock	070	05	RTC ALE
Real Time Clock	071	06	RTC Write Stroke
Real Time Clock	071	07	RTC Read Strobe
Floppy Operation Chip Select	3F2 372	08	Primary Address Secondary Address
Floppy Chip Select	3F4, 3F5 374, 375	09	Primary Address Secondary Address
Floppy Control Chip Select	3F7 377	0A	Primary Address Secondary Address (Floppy Enabled, HD Disabled)
Floppy And HD Control Chip Select	3F7 377	0B	Primary Address Secondary Address (Floppy Enabled, HD Enabled)
Hard Disk Chip Select	1F0, 1F1 - 1F7 170, 171 - 177	0C	Primary Address Secondary Address
Hard Disk Chip Select	3F6, 3F7[1] 376, 377[1]	0D	Primary Address, IDE Mode Only Secondary Address, IDE Mode Only
Serial Port A Chip Select	2E8 - 2EF 2F8 - 2FF 3E8 - 3EF 3F8 - 3FF	0E[2]	
Parallel Port 0 Chip Select	278 - 27F 378 - 37F 3BC - 3BF	0F	
Serial Port B Chip Select	2E8 - 2EF 2F8 - 2FF 3E8 - 3EF 3F8 - 3FF	10[2]	
Program Chip Select	PROG	11	
SCSI	3530 - 353X	12	
Cache Flush	F872	13	
EMS		14	External EMS
	F072	15	48 MHz Clock Disabled
	F472	16	48 MHz Clock Enabled
Power Control	7872	17	PMC Write Strobe 1
Reserved		1E, 1F	Reserved
Program Chip Select 2,3	PROG2,PROG3	1A, 1B	

TABLE 4-2. I/O ADDRESS AND CHIP SELECT ASSIGNMENTS

[1] IDE Hard Disk enabled, floppy disabled
[2] CS# is the decoded value of CS4-CS0.

5.0 FLOPPY DISK CONTROLLER

This section discusses the Floppy Disk Controller in detail. The Floppy Disk Controller (FDC) consists of several logical and/or physical blocks, as illustrated in Figure 5-2.

These components are:

- The 765A-compatible Core
  - Clock & Timing Generator
- Drive Interface
  - Data Separator
  - Write Precompensator
- Host Interface
  - Control Register
  - Operations Register
  - Master Status Register
  - Disk Interface Control Register
  - Data Register

Each of these topics is discussed in the following sections.

5.1 765A-COMPATIBLE CORE

The WD76C20ALV maintains the core attributes of the 765A floppy disk controller. The micro-sequencer is functionally equivalent and all commands will execute identically, assuring software compatibility with the 765A standard. The floppy control state machine on the front-end is also functionally equivalent. The micro-sequencer and control state machine operate at 8 times the selected bit data rate in MFM and 16 times the bit data rate in FM.

5.1.1 Clock and Timing Generator

The FDC portion of the WD76C20ALV provides all clock generation necessary for the floppy disk subsystem including SCLK (Sampling Clock), WCLK (Write Clock) and MCLK (Master Clock).

A 16 MHz crystal oscillator circuit provides the necessary signals for internal timing when external clocks are unavailable. The 16 MHz signal handles all standard data rates (500 and 250 Kb/sec) used in PC/AT designs, and a non-standard data rate (300 Kb/sec.). If neither the board space nor the 16 MHz TTL clock is available, FCLK1/FX1 can be driven with a 16 MHz TTL-level clock, and FCLK2 with a 9.6 MHz TTL clock. This will handle standard data rates (500, 250, and 125 Kb/sec.), and a non-standard data rate (300 Kb/sec.).

5.1.1.1 SCLK

SCLK is the clock which drives the digital phase lock loop data separator during data recovery. This clock frequency is always 32 times the selected data rate, and is exactly the frequency of the signals on FX1 (FCLK1) and FCLK2, whether or not standard data rates are being used (see Table 5-1).

FCLK		SCLK	
FCLK1	**FCLK2**	**Standard**	**Non-Stan.**
16 MHz TTL	9.6 MHz TTL	16 MHz	9.6 MHz
16 MHz TTL	Tied Low	16 MHz	Disabled

TABLE 5-1. FDC SAMPLING (SCLK) CLOCK

If the oscillator is not used, a 16 MHz TTL clock should be applied at FCLK1 (FX1) as shown in Figure 5-1. Data rates for this crystal are shown in Table 5-2.

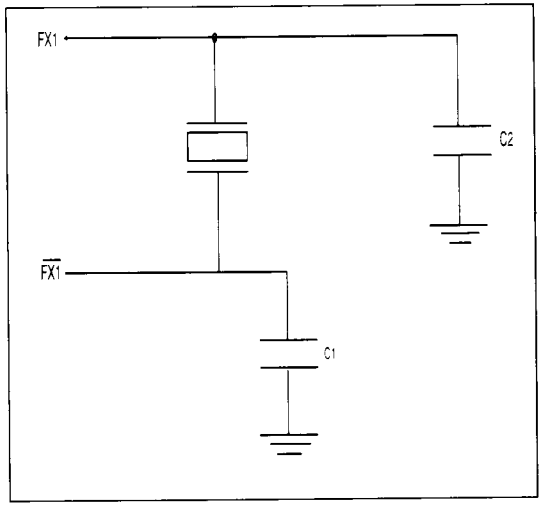

FIGURE 5-1. 16 MHZ CRYSTAL

DATA RATE	CODE	SCLK	MCLK	WCLK
125 Kb/sec	FM	4 MHz	2 MHz	250 KHz
500 Kb/sec	MFM	16 MHz	4 MHz	1 MHz
250 Kb/sec	FM	8 MHz	4 MHz	500 KHz
250 Kb/sec	MFM	8 MHz	2 MHz	500 KHz
300 Kb/sec	MFM	9.6 MHz	2.4 MHz	600 KHz

TABLE 5-2. FDC MCLK & WCLK GENERATION

5.1.1.2 WCLK

WCLK is used by the encoder logic to place MFM or FM on the serial Write Data stream to the disk. WCLK always has a frequency twice the selected data rate. See Table 5-2 for WCLK data rates.

5.1.1.3 MCLK

MCLK is used by the micro-sequencer. Both the MCLK and $\overline{\text{MCLK}}$ clocks latch in a 2-phase scheme. One micro-instruction cycle is 4 MCLK cycles. MCLK has a frequency equal to 8 times the selected MFM data rate or 16 times the FM data rate. See Table 5-2 for MCLK data rates.

5.1.1.4 Automatic Power-Down Mode

In this mode, the FDC powers down all circuitry except for the Data Register, the Operations Register, the Control Register, the Master Status Register and the I/O path leading to and from the data bus. Since the crystal oscillator controller circuitry and all non-essential linear circuitry is turned off, the controller will draw very low current. The FDC can return from power-down mode by simply polling the Master Status Register, after which the crystal oscillator turns on along with the other circuitry.

To resume on power-up, the FDC turns on the crystal oscillator, which in turn activates all the clock circuitry on the chip.

For more information on the Power-Down Modes, refer to Section 7.

5.2 DRIVE INTERFACE

The FDC's disk drive interface includes data separation and write precompensation in addition to the usual formatting, encoding/decoding, stepper motor control and status sensing functions. All inputs are TTL compatible, and outputs are high-current, open-drain drivers that conform to the ANSI specification of 48 mA.

The FDC no longer supports certain pin functions provided for in the 765 predecessor. The output RW/SEEK is used in the 765-based subsystem as a multiplexer select line to allow a pin to have 2 functions depending on whether a read, write, or seek type command is under execution. This signal is no longer available externally but is used within the WD76C20ALV to assure that no improper pin functionality occurs.

The LCT function has been renamed $\overline{\text{RWC}}$ and resides on a pin of its own with slightly altered active conditions and in the PC/AT mode is $\overline{\text{RPM}}$. $\overline{\text{DIRC}}$ is the only function on that pin and is enabled only during seeks as a power conservation measure.

$\overline{\text{STEP}}$ is also only enabled during seeks and a fault rest (FR) is no longer needed since FLT, fault detects, are not sensed. FLT status - status register #3, bit 7 - will always be a logic 0 state. Also, track zero status, $\overline{\text{TR00}}$, is only sensed during seeks.

Two-sided drive status, TS, is no longer supported, and Status Register #3, bits 6 and 3 will both now reflect Write Protect status. The FDC device assumes the drive is ready all the time since DRDY signal is set to logic 1 internally. This will still result in an FIRQ. This action is acknowledged as a change in status and demands a Sense Interrupt Status command execution in order to clear the FIRQ. Signals MFM, RDW, WCK and VCO are no longer needed since all logic associated with these is now contained within the FDC.

5.2.1 Data Separator

The FDC incorporates the patented digital phase lock loop used in the WD92C32 product. The sample clock rate, SCLK, must be 32 times the data rate.

As an option, the interface signals are provided for an external anlog PLL.

5.2.2 Write Precompensation

The FDC maintains the standard first level algorithm to determine when write precompensation should be applied. The EARLY and LATE signals are used internally to select the appropriate delay in the Write Data pulse stream. The encoded write data signal is synchronized to the 16 MHz clock, if this is the frequency on pin FCLK1, and clocked through a shift register, FX1. Signals EARLY, NOM, and LATE determine the amount of delay through the shift register before a multiplexer gates the chosen bit to the output. The output data pulse width has 25% duty cycle which equals 1/4 of the bit cell period or 1/2 the WCLK period.

When PCVAL is set to 1, all data will be precompensated by ±125 ns regardless of track number and data rate, but only for MFM encoding (no write precomp for FM). If PCVAL is 0, and if a track inside number 28 is accessed, then ±187 ns of precomp will be generated. For frequencies other than 16 MHz on FX1, these precomp values will be 2 and 3 SCLK clock cycles respectively.

When a non-standard data rate using FCLK2 is chosen, the precompensation logic is run from this frequency. In this case, the PCVAL function is disabled. Hence precomp values will always be 2 clock cycles. For 9.6 MHz this value is ±208 ns. The write precomp can be disabled by the use of bit 2 of Control register for PC AT. With no write precomp, the PCVAL input to the chip is ignored.

5.3 HOST INTERFACE

The host access signals are identical to a 765A floppy disk controller, but timings have been enhanced. The host interface has been designed to support up to 12 MHz bus speeds without the use of wait states. Input strobes are Schmitt Triggers. The data bus drive capability is 12 mA IOL, and 5 mA IOH, allowing, in most applications, direct interconnection to bus structures without the use of buffers or transceivers. For PC and PC/AT applications, qualification of interrupt request and DMA request is provided.

Traditionally, data rate selection, drive selection, and motor control have been output ports of the host processor architecture; however, in the PC AT these functions are latched into registers addressed within the system's I/O mapping. These registers, Operations and Control, are incorporated into the FDC.

The FDC has 8 internal registers.

- Control Register is a write register that provides support logic for selection of desired data rates and write precompensation logic.
- Disk Interface Control Register provides a read only register for determining the Disk Change status signal.
- Operations Register provides all the control signals required to select the drive and the spindle motor.
- Master Status Register is an 8-bit read/write register comprised of these two parts:
  - MSR is an 8-bit read only register containing FDC status information and may be accessed at any time.
  - MSR1 is an 8-bit write only register containing support for the Power Down Mode and the PS/2 drive type select.
- Status Registers 0-3 are four read only registers under system control providing various status and error information.
- Data Register is an 8-bit read/write register which stores data, commands, parameters, and FDD status information.

Selection of these registers is handled through the decoding of 7 lines as shown in Table 5-3.

ADDRESS MAP	$\overline{CS}$	A0	$\overline{LDCR}$	$\overline{LDOR}$	R/W/RW
MASTER STATUS REGISTER	0	0	–	–	R
MASTER STATUS REGISTER1	0	0	–	–	W
DATA REGISTER	0	1	–	–	R/W
OPERATIONS REGISTER	–	–	–	0	W
CONTROL REGISTER	–	–	0	–	W
DISK INTERFACE REGISTER	–	–	0	–	R

TABLE 5-3. FDC REGISTER MAP

5.3.1 Control Register

The Control Register is a Write register.

Address 3F7, $\overline{LDCR}$ = 0, $\overline{IOW}$ = 0 - Write only

The Control Register is used to set the data transfer rate and disable write precomp. On receiving an $\overline{IOW}$, the WD76C20ALV latches the three LSB's of the data bus. These bits, along with CR1 and CR0 in the Control Register, are used as shown in Table 5-1 to select the desired data rate which, in turn, controls the internal clock generation. Clock switchover is internally corrected, allowing continuous operation after changing data rates. Switching this clock must be errorless or the device must be reset. For all non-standard transfer data rates, use Table 5-2.

As an option, FDC also supports a 150 Kb/sec FM data transfer rate. The Control Register is used to set the transfer data rate as shown in Table 5-2. FX1 (pin 4) can be driven with a TTL level 9.6 MHz signal. With this setup, only 150 Kb/sec (FM) and 300 Kb/sec (MFM) data transfer rates can be selected. If the Control Register is not used, the data rate is governed by the supplied clock, or crystal, frequency and must be 64 times the desired MFM data rate. This provides a maximum frequency of 16 MHz for the data rate of 250 Kb/sec.

In PC/AT mode, precomp can be disabled by the use of the No Write Precomp (NWP) bit in the Control Register as shown in Figure 5-3.

7	6	5	4	3	2	1	0
					NWP	CR1	CR0

Signal Name	Default At Reset
NWP	0
CR1	0
CR0	0

Bits 7-3 - Reserved, not defined.

Bit 2 - NWP, No Write Precomp
In PC/AT mode, precomp can be disabled. This enables the PCVAL input pin.

NWP = 0 -
Write Precomp enabled.

NWP = 1 -
Write Precomp disabled.

Bit 1 - CR1, Data Rate 1
CR1 = 0 -
Refer to Tables 5-4.

CR2 = 1 -
Refer to Tables 5-4.

Bit 0 - CR0, Data Rate 0

CR0 = 0 -
Refer to Table 5-4.

CR0 = 1 -
Refer to Tables 5-4.

7

DATA RATE	PC/AT RPM	MODE	CR1	CR0	DRV
16 MHZ					
500 Kb/sec	1	MFM	0	0	X
250 Kb/sec	1	FM	0	0	X
250 Kb/sec	0	MFM	0	1	0
300 Kb/sec	0	MFM (9.6 MHz)	0	1	1
250 Kb/sec	0	MFM (Reset Default)	1	0	X
125 Kb/sec	0	FM (Reset Default)	1	0	X
125 Kb/sec	0	FM	1	1	X
9.6 MHZ					
300 Kb/sec	1	MFM	0	0	X
150 Kb/sec	1	FM	0	0	X

TABLE 5-4. FCLK1 DATA RATE DECODER

5.3.2 Disk Interface Control Register

The Disk Interface Control Register is a Read only register. It shares the same address as the Control Register but is accessed to indicate the state of $\overline{DCHG}$. This signal helps decode Disk Interface Control logic by sensing status from the disk drive. It senses low if the drive door is open or the diskette has changed since the last drive selection.

Address 3F7, $\overline{LDCR}$ = 0 - Read only

During the Read Mode, bit 7 indicates the state of the Disk Change Status signal, $\overline{DCHG}$. Bits 6 through 0 are tristated and used by the hard disk during this read.

7	6	5	4	3	2	1	0
$\overline{DCHG}$	Tristated						

Signal Name	Default At Reset
Bit 6-0	Tristated
Bit 7	0

Bit 7 - D_CHG, Disk Changed status signal

D_CHG = 0 -

$\overline{DCHG}$ has not changed state.

D_CHG = 1 -

$\overline{DCHG}$ has changed state.

Bits 6-0 - Tristated

5.3.3 Operations Register

Address 3F2, $\overline{LDOR}$ = 0, $\overline{IOW}$ = 0, PCAT Mode - Write only

When the Operations Register receives an $\overline{IOW}$, the data on the data bus is latched into the Operations Register. This register replaces the typical latched port seen in floppy subsystems used to control disk drive spindle motors and select desired drive.

7	6	5	4	3	2	1	0
MOEN				DMAEN	$\overline{SRST}$	DSEL	
3	2	1	0			1	0

Signal Name	Default At Reset
MOEN3-0	0
DMAEN	0
$\overline{SRST}$	1
DSEL1-0	0

Bits 7-4 - MOEN3-0, Motor On Enable 3-0

MOEN3 through MOEN0 produce the inverted outputs $\overline{MO3}$, $\overline{MO2}$, $\overline{MO1}$, and $\overline{MO0}$.

Bit 3 - DMAEN, DMA Enable

In PC/AT mode, FIRQ and DMA are tristated and qualified by DMAEN. The data bus is designed to handle 20 LSTTL loading.

Bit 3 = 0 -

DMA and FIRQ outputs and $\overline{DACK}$ input disabled.

Bit 3 = 1 -
DMA and FIRQ outputs and $\overline{DACK}$ input enabled.

Bit 2 - $\overline{SRST}$, Soft Reset

Bit 2 = 0 -
The Floppy Disk Controller will be reset. After the Soft Reset has occurred, bit 2 is returned to a 1.

Bit 2 = 1 -
Normal or default state.

Bit 1, 0 - DSEL1, 0, Drive Select

The DSEL 1,0 drive select bits are valid only when in the PC/AT Mode.

DS1	DS0	DRIVE SELECT
0	0	$\overline{DS0}$ Active
0	1	$\overline{DS1}$ Active
1	0	$\overline{DS2}$ Active

TABLE 5-5. DRIVE SELECT DECODE

5.3.4 Master Status Registers

The Master Status Register (MSR) is a Read/Write register. The Write Mode and Read Mode of the Master Status Register provide different functions and are discussed separately in this section.

The Write Mode MSR, called MSR1, sets the conditions for drive select and motor enable signals. It also checks for correct polarity on the DRV/PS2 pin for PS/2 drive types.

Table 5-6 shows the sequence to select the PS/2 type of drives and the polarity on DRV/PS2 pin which is tied to pin 2 on the floppy disk drive connector. If this register is not programmed for PS/2 configuration, the $\overline{RWC}$ output from FDC should go to pin 2 of the floppy disk drive connector. The default is AT mode which means that the $\overline{RWC}$ output from the FDC should be tied to Pin 2 of the FDC connector.

A0	$\overline{IOR}$	$\overline{IOW}$	Function
0	0	1	Read from Main Status Register (MSR)
0	1	0	Write into Main Status Register (MSR1)
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

TABLE 5-6. MSR/DDR DECODE

The WD76C20ALV decodes for both the Master Status Register and the Data Register based on five signals: A0, $\overline{RD}$, $\overline{WR}$, $\overline{RD}$, and $\overline{WR}$ as shown in Table 5-5.

5.3.4.1 MSR1: Power-Down and PS/2 Support

Address 3F4, A0 = 0, $\overline{IOW}$ = 0 - Write only

In the Write Mode, the MSR1 register contains support for the Power-Down Mode and the PS/2 drive type select. You may write to this register to enable the Power-Down Mode (option 1), to disable user transparent Power-Down Mode (option 2), and set up the PS/2 type drive configuration. The Power Down-Mode is discussed in more detail in section 7.

7	6	5	4	3	2	1	0
Reserved	Reserved	PSSEL				PD2ENAB	PDM1
		3	2	1	0		

Bit	Signal Name	Default At Reset
Bit (5-2)	PSSEL3-0	0
Bit 1	PD2ENAB	1
Bit 0	PDM1	0

Bit 7-6 - Reserved

Bit 5 - PSSEL3

PSSEL3 = 1 -
PS2 drive 3 is selected.

Bit 4 - PSSEL2

PSSEL2 = 1 -
PS2 drive 2 is selected.

Bit 3 - PSSEL1

PSSEL1 = 1 -
PS2 drive 1 is selected.

Bit 2 - PSSEL0

PSSEL0 = 1 -
PS2 drive 0 is selected.

Bit 1 - PD2_ENAB, FDC Power-Down Option 2

PD2_ENAB = 0 -
User-transparent Power-Down Mode option 2 is disabled.

PD2_ENAB = 1 -
User-transparent Power-Down Mode option 2 is enabled. A hard reset also enables the PDM option 2. Refer to section 7 for more details.

Bit 0 - PDM, FDC Power-Down Mode Option 1

PDM = 0 - Disabled
PDM is set to 0 by a hard or soft reset.

PDM = 1 -
The FDC immediately enters the user-initiated Power-Down Mode. Refer to section 7 for more details.

5.3.4.2 MSR: FDC Status Information

Address 3F4, A0 = 0, $\overline{IOR}$= 0 - Read only

In the Read Mode, MSR contains FDC status information and can be accessed at any time.

7	6	5	4	3	2	1	0
RQM	DI/O	EXM	CB	D3B	D2B	D1B	D0B

Signal Name	Default At Reset
Bits 7-0	0

Bit 7 - RQM, Request For Master

RQM = 0 -
The FDC is busy.

RQM = 1 -
The Data Register is ready to send to or receive data from the processor. RQM and DI/O should be used to perform handshaking functions specifying the ready status and signal direction to the processor.

STEP	CODE	REGISTER VALUE	DESCRIPTION	RWC	DRV
1.	3F4	00	Disable FDC Sleep Mode	–	–
2.	3F7	00	Select 500 Kb/sec data rate and 3.5" 1.44 MB in AT Mode	1	1
3.	3F2	1C	Disable $\overline{SRST}$, enable $\overline{DS0}$, $\overline{MO0}$, and DMAEN bits of Operations Register	1	1
4.	3F4	04	Enable bit 2 of MSR and select PS2 drive 0 (1.44 MB)	1	1
5.	3F2	1C	Disable $\overline{SRST}$, enable $\overline{DS0}$, $\overline{MO0}$, and DMAEN bits of Operations Register	1	0
6.	3F4	08	Enable bit 3 of MSR and select	–	–
7.	3F7	02	Select 250 Kb/sec data rate and 3.5" 720 KB	0	0
8.	3F2	2D	Disable $\overline{SRST}$, enable $\overline{DS1}$, $\overline{MO1}$and DMAEN bit of the Operations Register PSSEL1 (3.5" 720 KB)	0	1

TABLE 5-7. PS/2 SUPPORT SEQUENCE

Bit 6 - DI/O, Data Input

DI/O indicates the direction of the data transfer between the FDC and the processor.

DI/O = 0 -
Transfer is from the processor to the Data Register.

DI/O = 1 -
Transfer is from the Data Register to the processor.

Bit 5 - EXM

EXM operates only during the Execution phase in non-DMA mode.

EXM = 0 -
Execution Phase has ended and the Results Phase has started.

EXM = 1 -
Performing Execution Phase in non-DMA mode.

Bit 4 - CD, Floppy Disk Controller Busy

CB = 0 -
The FDC is not busy.

CB = 1 -
A Read or Write Command is in progress. The FDC will not accept any other command.

Bit 3 - D3B, Floppy Disk Drive 3 Busy

D3B = 0 -
Floppy Drive 3 is not in Seek Mode.

D3B = 1 -
Floppy Drive 3 is in Seek Mode. If the Floppy Drive is in the Seek Mode, the FDC will not Read or Write commands.

Bit 2 - D2B, Floppy Disk Drive 2 Busy

D2B = 0 -
Floppy Drive 2 is not in Seek Mode.

D2B = 1 -
Floppy Drive 2 is in Seek Mode. If the Floppy Drive is in the Seek Mode, the FDC will not Read or Write commands.

Bit 1 - D1B, Floppy Disk Drive 1 Busy

D1B = 0 -
Floppy Drive 1 is not in Seek Mode.

D1B = 1 -
Floppy Drive 1 is in Seek Mode. If the Floppy Drive is in the Seek Mode, the FDC will not Read or Write commands.

Bit 0 - D0B, Floppy Disk Drive 0 Busy

D0B = 0 -
Floppy Drive 0 is not in Seek Mode.

D0B = 1 -
Floppy Drive 0 is in Seek Mode. If the Floppy Drive is in the Seek Mode, the FDC will not Read or Write commands.

5.3.4.3 Overrun Error Status Reporting

The WD76C20ALV has the capability to detect and flag data overruns during DMA operations. This situation may occur, for example, when a floppy operation, DRAM refresh, and DMA channel 2 transfer occur simultaneously. Should a data overrun occur, D4 (OR) in Status Register 1 (SR1) will be set.

Versions of the WD76C20ALV which contain this feature can be distinguished easily by reading RTC RAM location 66H after reset. If the device contains the overrun flag feature, the LSB location 66H is 1. In these devices, 66H is read only.

Address 66 - Read only

7	6	5	4	3	2	1	0
							Flag

Signal Name	Default At Reset
Bit 0	1

Bits 7-1 - Not defined

Bit 0 - Flag, Overrun Flag

Flag = 0 -
There is no overrun flag feature supported by this version of the WD76C20ALV device.

Flag = 1 -
The overrun flag feature is supported by this version of the WD76C20ALV device.

5.3.5 Status Registers

Address 3F4, A0 = 1, $\overline{CS}$ = 0, $\overline{IOR}$ = 0

There are four read only status registers that are part of the Floppy result phase and contain a variety of status information. They can only be accessed after the execution phase and must be read sequentially, starting with SR0 and going through SR3.

These four status registers are explained on the following pages.

5.3.5.1 Status Register 0

7	6	5	4	3	2	1	0
IC		SE	EC	NR	HS	US1	US0

Signal Name	Default At Reset
All signals	0

Bits 7 - 6 - IC, Interrupt Code

IC 7	6	
0	0	Normal termination of command was completed and properly executed
0	1	Abnormal termination of the command (AT). Execution was started but was not successfully completed
1	0	Invalid command issue (IC). Issued command was never started
1	1	Not defined

Bit 5 - SE, Seek End

SE = 0 -
The FDC has not completed the SEEK command.

SE = 1 -
The FDC has completed the SEEK command.

Bit 4 - EC, Equipment Check

EC = 0 -
Track 0 signal occurred within 77 step pulses per Recalibrate Command.

EC = 1 -
Track 0 signal failed to occur after 77 step pulses per Recalibrate Command and set this flag.

Bit 3 - NR, Not Ready

NR = 0 -
Drive is ready. This is always assumed to be logic 0.

Bit 2 - HS, Head Select

This flag is used to indicate the state of the head at interrupt.

Bit 1 - US1, Unit Select 1

This flag is used to indicate a Drive Unit Number at interrupt.

Bit 0 - US0, Unit Select 0

This flag is used to indicate a Drive Unit Number at interrupt.

5.3.5.2 Status Register 1

7	6	5	4	3	2	1	0
EN	0	DE	OR	0	ND	NW	MA

Signal Name	Default At Reset
All signals	0

Bit 7 - EN, End of Cylinder

EN = 1 -
When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.

Bit 6 - Not used. This bit is always low.

Bit 5 - DE, Data Error

DE = 1 -
The FDC has detected a Cyclic Redundancy Check (CRC) error in either the ID field or the data field and set this flag.

Bit 4 - OR, Overrun

OR = 0 -

The FDC was serviced by the Host during data transfers within a specified time interval.

OR = 1 -
The FDC was not serviced by the Host during data transfers within a specified time interval and this flag was set.

Bit 3 - Not used. This bit is always low.

Bit 2 - ND, No Data

When this bit is high, it can indicate one of several problems with FDC tracking or reading.

ND = 0 -
This flag is not set.

ND = 1 -
During execution of READ DATA, WRITE DELTED DATA, or SCAN, the FDC could not find the section specified in the Internal Data Register (IDR) and this flag was set.

During execution of the READ ID command, the FDC could not read the ID field without an error and this flag was set.

During execution of the READ A TRACK command, the starting sector could not be found and this flag was set.

Bit 1 - NW, Not Writeable

NW = 0 -
This flag is not set.

NW = 1 -
During execution of WRITE DATA, WRITE DELETED DATA, or FORMAT A TRACK, the FDC detected a WP from the Floppy Disk Drive and this flag was set.

Bit 0 - MA, Missing Address Mark

MA = 0 -
This flag is not set.

MA = 1 -
If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.

If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. At the same time, the Missing Address Mark in the data field (MD) of Status Register 2 is set.

5.3.5.3 Status Register 2

7	6	5	4	3	2	1	0
0	CM	DD	WC	SH	SN	BC	MD

Signal Name	Default At Reset
All signals	0

Bit 7 - Not used. This bit is always low.

Bit 6 - CM, Control Mark

CM = 0 -
This flag is not set.

CM = 1 -
During execution of the READ DATA or SCAN command, the FDC encountered a section that contained a Deleted Data Address Mark and this flag was set.

Bit 5 - DD, Data Error

DD = 0 -
FDC detected no CRC error in the data field.

DD = 1 -
FDC detected a CRC error in the data field and set this flag.

Bit 4 - WC, Wrong Cylinder

This bit is related to the ND bit.

WC = 0 -
This flag is not set.

WC = 1 -
When the contents of Cylinder (C) on the medium is different from that stored in the IDR, this flag is set.

Bit 3 - SH, Scan Equal

SH = 0 -
During execution of the SCAN command, the condition of equal is not satisfied.

SH = 1 -
During execution of the SCAN command, the condition of equal is satisfied and this flag is set.

Bit 2 - SN, Scan Not

SN = 0 -
This flag is not set.

SN = 1 -
The FDC cannot find a sector on the cylinder meeting the condition of SCAN and this flag is set.

Bit 1 - BC, Bad Cylinder

This bit is related to the ND bit.

BC = 0 -
This flag is not set.

BC = 1 -
When the contents of C on the medium does not agree with the IDR and the contents of C is FF, this flag is set.

Bit 0 - MD, Missing Address Mark In Data Field

MD = 0 -
This flag is not set.

MA = 1 -
When data is read from the medium, if the FDC cannot detect a Data Address Mark or Deleted Data Address Mark, then this flag is set.

5.3.5.4 Status Register 3

7	6	5	4	3	2	1	0
0	$\overline{WP}$	RY	T0	$\overline{WP}$	HS	US1	US0

Signal Name	Default At Reset
Bit 7	0
$\overline{WP}$	1
RY	1
T0	0
$\overline{WP}$	1
HS	0
US1	0
US0	0

Bit 7 - Not used. This bit is always low.

This differs from the NEC765.

Bit 6 - $\overline{WP}$, $\overline{WRITE\ PROTECTED}$

This bit is used to indicate the status of the $\overline{WP}$ signal from the Floppy Disk Drive.

$\overline{WP}$ = 0 -
$\overline{WP}$ is asserted.

$\overline{WP}$ = 1 -
$\overline{WP}$ is not asserted.

Bit 5 - RY, Ready

This differs from the 765 standard.

RY = 1 -
This bit is always set to this value because the drive is presumed to be ready.

Bit 4 - T0, Track 0

This bit is used to indicate the status of the Track 0 signal from the FDD.

T0 = 0 -
T0 is not asserted.

T0 = 1 -
T0 is asserted.

Bit 3 - $\overline{WP}$, $\overline{WRITE\ PROTECTED}$

This bit is used by the WD76C20ALV to indicate the status of the $\overline{WRITE\ PROTECTED}$ signal from the FDD.

$\overline{WP}$ = 0 -
$\overline{WP}$ is asserted.

$\overline{WP}$ = 1 -
$\overline{WP}$ is not asserted.

Bit 2 - HS, Head Select

This bit is used to indicate the status of the Side Select signal to the FDD.

HS = 0 -
Side Select signal is not asserted.

HS = 1 -
Side Select signal asserted.

Bit 1 - US1, Unit Select 1

This bit is used to indicate the status of the Unit Select 1 signal to the FDD.

US1 = 0 -
Unit Select 1 signal is not asserted.

US1 = 1 -
Unit Select 1 signal is asserted.

Bit 0 - US2, Unit Select 2

This bit is used to indicate the status of the Unit Select 2 signal to the FDD.

US0 = 0 -
Unit Select 2 signal is not asserted.

US0 = 1 -
Unit Select 2 signal is asserted.

5.3.6 Data Register

The eight-bit Data Register is a Read/Write register controlling the flow of data that stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain results after a particular command.

The Data Register is selectively decoded by four signals – A0, RD, WR, and FDCS (CSL code 09) – as follows.

A0	$\overline{RD}$	$\overline{WR}$	FDCS	FUNCTION
1	0	1	0	Read Data Register
1	1	0	0	Wrote to Data Register

TABLE 5-8. DATA REGISTER DECODE

Address 3F5 - Read and Write

Two bits within the MSR (address 3F4), RQM (bit 7) and DIO (bit 6) are used to perform the handshaking function and transfer data between the Data Register and the processor. All disk data transfer goes through this register. Once the FDC enters the command execution phase, it clears the Data Register of all data to ensure that no invalid data is transferred.

7	6	5	4	3	2	1	0
Register Data							

7

6.0 IDE DRIVE INTERFACE

This section discusses the components of the WD76C20ALV that control and oversee the function of the Integrated Drive Electronics (IDE) interface logic. While most of the traditional hard disk controller functions reside on the drive itself, the chip set must still interact at several points with the drive in order to coordinate the transmission of data and address information across the bus.

6.1 IDE DRIVE SIGNAL LOGIC

The WD76C20ALV provides multiplexing and data path buffering for IDE drive data. Internally, these functions are achieved using pads DB7 and IDED7.

6.2 CHIP SELECT

IDE drive support is handled by the WD76C10 and WD76C20ALV cooperatively, utilizing chip select logic. Table 6-1 provides a table of the chip select assignments integral to the IDE support. For more information on Chip Select Logic, see Section 4.

6.3 IDE/FDD DRIVE SELECTION

The WD76C20ALV determines whether the IDE drive or the FDD is using the bus. When the CSL decodes for 0A, any reads or writes to address 3F7 or 377 indicate that the Floppy Disk Drive is chosen. When the CSL decodes for 0B, reads to 3F7 indicate the FDD and writes specify the IDE drive. When the CSL decodes for 0C, reads and writes are always selected for a hard disk drive at addresses 1F0 through 1F7 and 170 through 177. When the CSL decodes for 0D, reads and writes are always selected for the hard disk (IDE drive only), at addresses 3F6 - 3F7 and 376 - 377.

6.4 IDE READ/WRITE

The read or write status of the IDE drive is determined by the IDED7 signal which provides a data path for bit 7 between the host and the IDE drive interface. IDED7 becomes an output, writing data from the host to the drive, when $\overline{IOW}$ is driven low. IDED7 is an input signal, reading data from the drive to the host, when $\overline{IOR}$ is low.

The exception to this rule is when the chip is reading from address 3F7. As previously explained, when $\overline{IOR}$ is detected at this location, the floppy DCHG status is output on the host data bus pin DB7.

6.5 IDE DRIVE SELECT

The WD76C20ALV can support a maximum of two drives. Drive selection is determined by the $\overline{CSIDE0}$ and $\overline{CSIDE1}$ signals. Normally, when $\overline{CSIDE0}$ is driven low, it indicates that drive 0 is on the bus; when $\overline{CSIDE1}$ is driven low, this indicates that drive 1 is on the bus. Both of these signals are activated through a decode in the CSL and are asserted in conjunction with either $\overline{IDEDENL}$ or both $\overline{IDEDENH}$ and $\overline{IDEDENL}$. CSL 0B decodes for $\overline{CSIDE1}$ and 0C decodes for $\overline{CSIDE0}$.

6.6 DATA PATH SELECT

The IDE data path can either be 8- or 16-bits wide. Recognition of this width is made possible using the $\overline{IDEDENL}$ and $\overline{IDEDENH}$ signals. When asserted low, $\overline{IDEDENL}$ and $\overline{IDEDENH}$ indicate a 16-bit path exists. $\overline{IDEDENH}$ is asserted only when A0 is driven low and the CSL has decoded for 0C. $\overline{IDEDENL}$ is asserted when CSL is decoded for 0C or 0D.

PORT	I/O ADDRESS	CS#	FUNCTION
Floppy/Hard Disk Chip Select	3F7 377	0B	Primary Address Secondary Address (Floppy Enabled, HD Enabled)
Hard Disk Chip Select	1F0, 1F1 - 1F7 170, 171 - 177	0C	Primary Address Secondary Address
IDE Hard Disk Chip Select	3F6, 3F7[1] 376, 377[1]	0D	Primary Address, IDE Mode Only Seconary Address, IDE Mode Only

TABLE 6-1. IDE CHIP SELECT ASSIGNMENTS

[1] IDE Hard Disk enabled, floppy disabled.

7.0 REAL TIME CLOCK

This section describes the Real Time Clock and its associated registers. A block diagram of the RTC is shown in Figure 7-1.

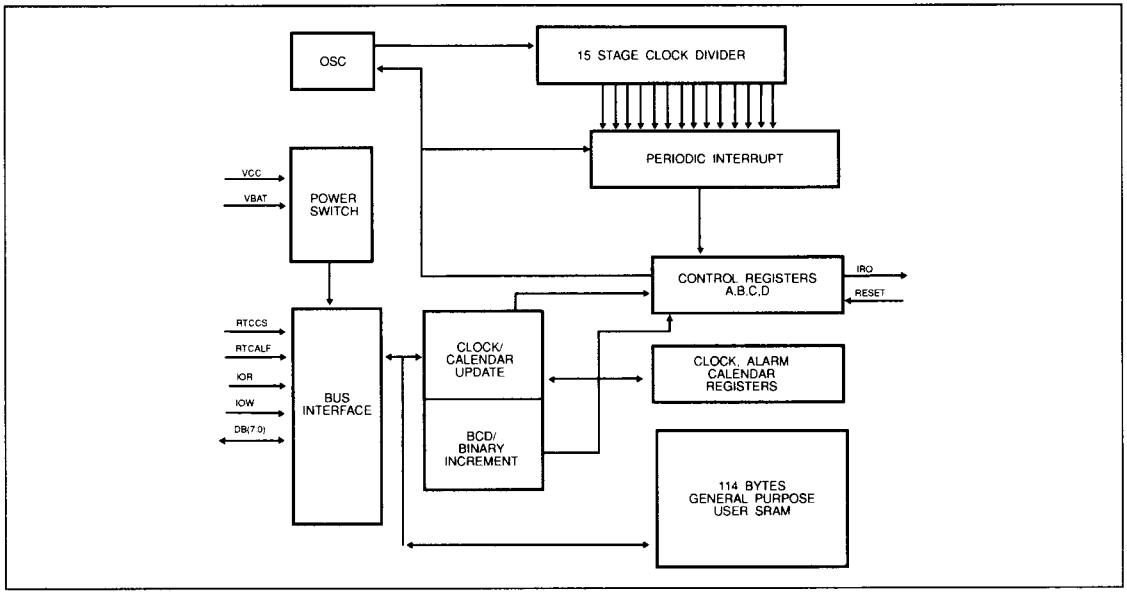

FIGURE 7-1. RTC BLOCK DIAGRAM

Ten SRAM data registers (Registers 00-09) contain all the calendar/clock/alarm information with the RTC crystal-controlled oscillator and frequency divider providing the appropriate timing updates to keep them accurate. Control and status information for the RTC is contained in Registers A-D of the SRAM. Remaining SRAM registers, with a total capacity of 114 bytes, are available to the user.

Read and/or write access to the SRAM (control/status, calendar/clock/alarm, and general purpose registers) is through the RTC bus interface. This interface gets signals from the WD76C20ALV Bus Interface and Chip Select Logic functions and appropriately buffers bits D0-D7 between the WD76C20ALV internal bus and the RTC internal bus accessing the SRAM.

Calendar/clock/alarm information is processed through Update Logic that:

- Increments calendar/clock counts based on "ticks" received from the Frequency Divider,
- Attends to Daylight/Standard Time and Leap Year adjustments, and
- Formats/deformats the information as straight binary or binary coded decimal data, as selected.

Input power to the RTC component is from the VBAT pin. Switching from System VDD to battery power is accomplished through two diodes as shown in Figure 7-1.

Power on Reset: Note that CMOS SRAM must **not** be written no earlier than 100 ms after power on reset.

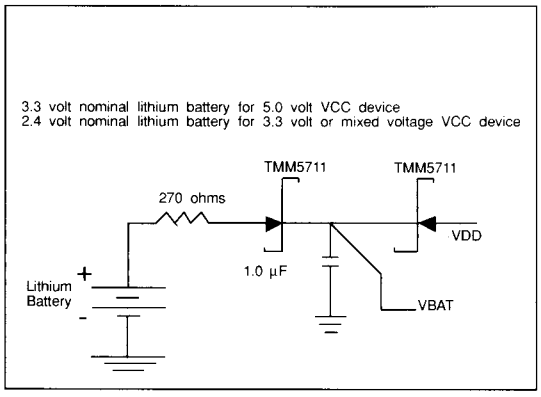

FIGURE 7-2. VBAT EXTERNAL SUPPORT

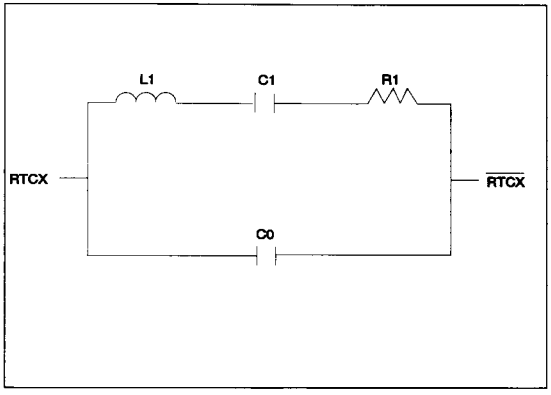

FIGURE 7-4. RTC CRYSTAL PARAMETERS

7.1 TIME BASE OSCILLATOR CIRCUIT

The oscillator that provides the time base for the RTC requires the external circuit shown in Figure 7-2 and the values listed in Table 9-2. The crystal used in parallel with the on-chip oscillator should be an AT-cut crystal with a 32.768 KHz resonant frequency as shown in Figure 7-3, using signals listed in Table 9-2. When in battery backup mode, this circuit is still active, providing the rest of the RTC with a valid time base. See Table 9-2 for the crystal component values.

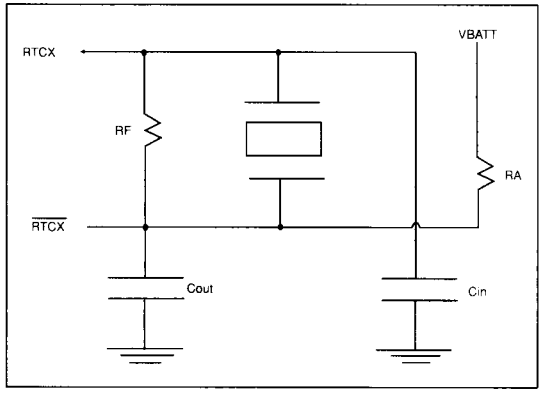

FIGURE 7-3. RTC CRYSTAL EXTERNAL CIRCUITRY

7.2 POWER SWITCH

This functional block is used to detect when the system power is shutting down and the RTC needs to go into battery backup mode. In the event of a full chip power-down without a battery backup, the VRT bit of register D will be reset to zero, indicating that the contents of the SRAM and RTC operational registers are not guaranteed. In order to reset the bit, register D must be read after a full power-up.

7.3 BUS INTERFACE

The RTC Bus Interface block is used to access the internal bus for the WD76C20LV. Protocol is maintained between the BIL block (Bus Interface Logic) and the RTC Bus Interface. The BIL block generates the $\overline{RD}$ and $\overline{WR}$ strobes, and the $\overline{CS}$ signals are decoded from the external bus by the Chip Select Logic.

7.4 CLOCK DIVIDER

This functional block uses clock divider logic to split the 32.768 KHz time base down to a 1 Hz signal that can be used by the timekeeping blocks. It also provides the periodic interrupt block with access to all stages of the division.

7.5 PERIODIC INTERRUPT

This functional block has access to the various stages of the Clock Divider. Using these signals under the direction of register A, an RTCIRQ pulse can be generated periodically for the processor, varying from once every 122 µS to once every 500 ms. The Periodic Interrupt function is enabled by the PIE bit in register B.

7.6 BCD/BINARY INCREMENT & CLOCK/CALENDAR UPDATE

This dual purpose logic block is used to increment and update the 10 timing registers and to check for the existence of an alarm condition. Several register bits are used to control this block, preventing contention between a processor seeking access to the information registers and the occurrence of an update cycle.

7.7 OPERATIONAL REGISTERS

Shown in Figure 7-2 is a memory map of the RTC, SRAM and operational registers. Under normal conditions all these registers are Read/Write except:

- Registers C and D are Read Only.
- Bit 7 of register A is Read Only.
- The high order bit of the seconds byte is Read Only.

7.7.1 Setting Correct Time

Writing the correct time to the RTC is done using this sequence:

1. Program the SET bit in register B to 1 and the Data Mode bit (DM) of Register B to the appropriate level.
2. Load the 10 bytes representing the current time and alarm status from the host into the RTC by addressing the appropriate memory locations and performing a normal I/O Write operation.
3. After all 10 timing bytes and the DM bit have been written to the RTC, the SET bit should be cleared.

After this, the DM bit cannot be changed without reinitializing all 10 registers.

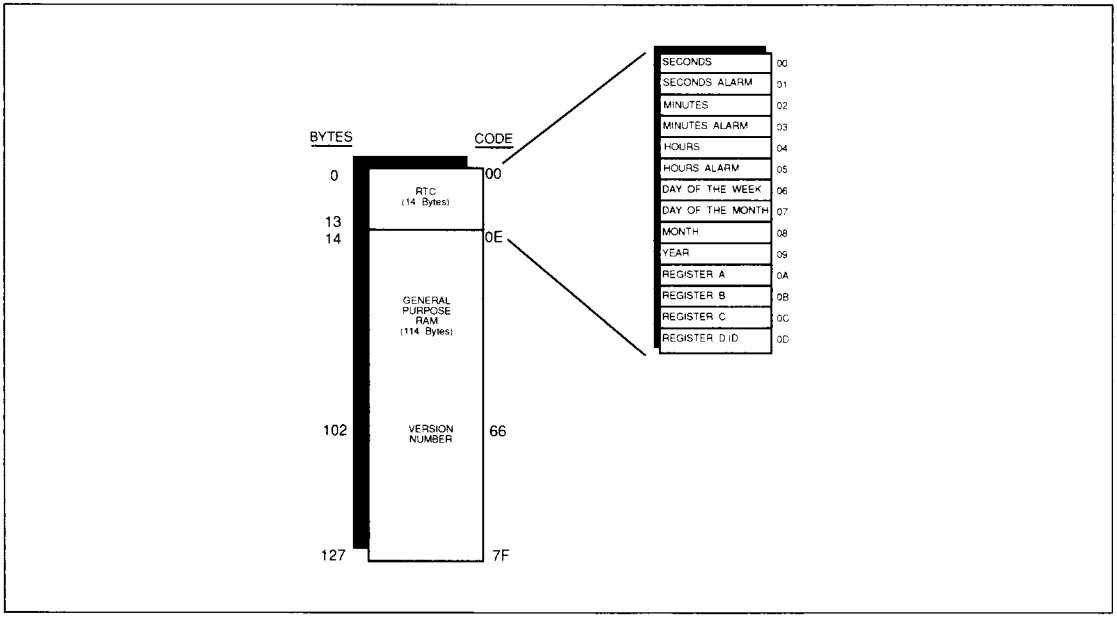

FIGURE 7-5. RTC ADDRESS MAP

ADDRESS	FUNCTION	RANGE		
		DECIMAL	BINARY	BCD DATA
00	SECONDS	0 - 59	00 - 3B	00 - 59
01	SECONDS ALARM	0 - 59	00 - 3B	00 - 59
02	MINUTES	0 - 59	00 - 3B	00 - 59
03	MINUTES ALARM	0 - 59	00 - 3B	00 - 59
04	HOURS - 12 HOUR MODE HOURS - 24 HOUR MODE	1 - 12 0 - 23	01-0C am,81-8C pm 00 - 17	01-12, 81-92 00 - 23
05	HOURS ALARM - 12 HOUR MODE HOURS ALARM - 24 HOUR MODE	1 - 12 0 - 23	01-0C am,81-8C pm 00 - 17	01-12, 81-92 00 - 23
06	DAY OF THE WEEK (SUNDAY = 1 etc.)	1 - 7	01 - 17	01 - 17
07	DATE	1 - 31	01 - 1F	01 - 31
08	MONTH	1 - 12	01 - 0C	01 - 12
09	YEAR	0 - 99	00 - 63	00 - 99

TABLE 7-1. RTC DATA MODES

Table 7-1 shows the Binary and BCD formats of the time, calendar and alarm locations. When the 12-hour format is selected, the high order bit of the hours byte represents AM when it is 0, and PM when it is 1. Once a second, the 10 bytes are updated and checked for alarm conditions. If a Host Read of the time occurs during an update, the hours, minutes, and seconds may not agree. Methods to avoid this possibility are covered later.

7.7.2 Setting Alarm Intervals

Alarms can be set to interrupt the Host in a variety of ways, designating intervals ranging from once a second to once a day. To set periodicity: any value from C0 to FF into the appropriate alarm registers. In this way, an alarm scheduled to interrupt the Host only once a day would have all alarm registers programmed to the proper values. An alarm scheduled to go off once an hour would have a don't care value in the hour register. One scheduled to go off every minute would have don't care values programmed into hours and minutes. An alarm will go off every second if all three registers are programmed to don't cares.

7.7.3 RTC Register A

Address 0A - Bit 7 Read only, Bits 6-0 Read/Write

7	6	5	4	3	2	1	0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

Signal Name	Default At Reset
UIP	None
DV2-0	None
RS3-0	None

Bit 7 - UIP, Update In Progress

Used by the Host to determine when updates are not going to occur.

UIP = 0 -
The Host can assume that a transfer is not going to happen for at least another 244 µs, during which time registers 9 through 0 are fully available. Writing 1 to the SET bit (Register B, bit 7) inhibits any further updates and clears the UIP bit.

UIP = 1 -
An update is in progress during which time registers 9 through 0 are not available.

Bits 6-4 - DV2-0, Oscillator Control 2-0

DV2, DV1 and DV0 enable and disable the oscillator for use during product shipping. The code 010 will turn the oscillator on and start dividing.

Bits 6-4 - DV2-0, Oscillator Control 2-0

RS3, RS2, RS1 and RS0 are used to select the periodic interrupt rate as shown in Table 7-2. Once the rate is selected, use the PIE bit (Register B, bit 6) to enable the interrupt. Functionally, these pins are decoded to select which spot on the divider chain should be tapped in order to generate interrupts.

REGISTER A BITS				PERIODIC
RS3	RS2	RS1	RS0	INTERRUPT RATE
0	0	0	0	None
0	0	0	1	3.90625 ms
0	0	1	0	7.8125 ms
0	0	1	1	122.070 µs
0	1	0	0	244.141 µs
0	1	0	1	488.281 µs
0	1	1	0	976.5625 µs
0	1	1	1	1.953125 ms
1	0	0	0	3.90625 ms
1	0	0	1	7.8125 ms
1	0	1	0	15.625 ms
1	0	1	1	31.25 ms
1	1	0	0	125 ms
1	1	0	1	250 ms
1	1	1	0	500 ms
1	1	1	1	

TABLE 7-2. RTC PERIODIC INTERRUPT RATE DECODER

7.7.4 RTC Register B

Address 0B - Read and Write

7	6	5	4	3	2	1	0
SET	PIE	AIE	UIE	0	DM	24/12	DSE

Signal Name	Default At Reset
SET	0
PIE	0
AIE	0
UIE	0
Bit 3	0
DM	None
24/12	None
DSE	None

Bit 7 - SET, Write to registers 9-0 in progress

SET = 0 -
Normal operation.

SET = 1 -
A Write to registers 9 through 0 can proceed without the possibility of an update cycle occurring part way through.

Bit 6 - PIE, Period Interrupt Enable

PIE = 0 -
Normal operation.

PIE = 1 -
The Host is interrupted whenever the Periodic Interrupt Flag (PIF at Register C, bit 6) is set to 1.

Bit 5 - AIE, Alarm Interrupt Enable

AIE = 0 -
The Host is not interrupted as a result of the AF.

AIE = 1 -
The Host is interrupted whenever the Alarm Flag (AF at Register C, bit 5) is set to 1.

Bit 4 - UIE, Update Interrupt Enable

UIE = 0 -
The Host is not interrupted as a result of the UF.

UIE = 1 -
The Host is interrupted whenever the Update Flag (UF at Register C, bit 4) is set to 1.

7

Bit 3 - Reserved, should be set to zero (default state at reset)

DM, Data Mode

The DATA Mode control bit sets and indicates whether the time is stored in binary or BCD format.

DM = 0 -
Binary coded decimal data.

DM = 1 -
Binary data.

Bit 1 - 24/12, 24- or 12-hour format

24/12 = 0 -
The time is set to a 12-hour AM, PM format.

24/12 = 1 -
The time is set to a 24-hour format.

Bit 0 - DSE, Daylight Savings Enable

The Daylight Savings Enable bit allows the RTC to perform adjustments required to maintain daylight savings: on the first Sunday in April, the time increments from 1:59:59 AM to 3:00:00 AM, and on the last Sunday in October at 1:59:59 AM, it changes to 1:00:00 AM

DSE = 0 -
Daylight savings time is not enabled.

DSE = 1 -
Daylight savings time is enabled.

7.7.5 RTC Register C

Address 0C - Read only

7	6	5	4	3	2	1	0
IRQF	PIF	AIF	UP	Reserved			

Signal Name	Default At Reset
IRQF	0
PIF	0
AIF	0
UF	0
Bits3-0	0

Bit 7 - IRQF, Interrupt Request Flag

IRQF = 0 -
The RTC is not issuing a Host service interrupt request.

SET = 1 -
The RTC is issuing a Host service interrupt request. The Boolean equation for the flag is:

$$IRQ = PF\ PIE + AF\ AIE + UF\ UIE$$

Bit 6 - PIF, Period Interrupt Flag

The PIF bit is independent of the PIE bit, but the PIE bit still controls whether or not an RTCIRQ pulse is generated.

PIF = 0 -
The divider tap determined by the decoded RSX lines did not change state.

PIF = 1 -
The divider tap determined by the decoded RSX lines changed state. The bit is cleared by reading Register C or resetting the WD76C20ALV.

Bit 5 - AIF, Alarm Interrupt Flag

AIF = 0 -
An alarm condition has not occurred.

AIF = 1 -
An alarm condition has occurred, either because of a timing match or "don't care" conditions. AIF is cleared by reading Register C or resetting the WD76C20ALV.

Bit 4 - UF, Update Ended Interrupt Flag

UIE = 0 -
UF is reset during each update cycle.

UIE = 1 -
UF is set after each update cycle.

Bit 3-0 - Reserved, 0 default at reset

7.7.6 RTC Register D

Address 0D - Read only

7	6	5	4	3	2	1	0
IRQF	PIF	AIF	UP	Reserved			
				ID3	ID2	ID1	ID0

Signal Name	Default At Reset
VRT	None
Bits6-4	0
ID3-0	None

Bit 7 - VRT, Valid RAM and Time

The RTC uses Valid RAM and Time to indicate the possibility of corruption in the SRAM memory locations.

VRT = 0 -

The time and calendar are not valid. An interrupt in the power occurred during which neither VBAT or VDD provided sufficient voltage.

VRT = 1 -

The time and calendar are valid. An interrupt in power either did not occur, or VBAT or VDD provided sufficient voltage.

Bits 6-4 - Not used, state is ignored

Bit 3-0 - ID3-0, Revision ID Code

ID3, ID2, ID1, and ID0 are used to indicate the device ID code. This code identifies the chip during board-level testing.

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8.0 POWER MANAGEMENT: SUSPEND/RESUME LOGIC

Suspend/Resume Logic is used in conjunction with the RTC time base to provide a 14.318 MHz clock output to the WD76C10. This can switch to a 32.768 KHz clock during the Suspend mode. While in Suspend mode, the WD76C20ALV typically draws less than 2 mA.

The Suspend/Resume Logic also provides the external DRAM refresh signal, PDREF, that pulses active low once every 15.26 µs. This logic also supports a latched signal that causes $\overline{\text{CSSERA}}$, $\overline{\text{CSSERB}}$ and $\overline{\text{CSPAR0}}$ to remain low during Suspend mode, signaling the WD76C30ALV to disable the 48 MHz crystal.

Like several other functions discussed in this databook, the Suspend/Resume function is supported by the entire chip set, especially the WD76C20ALV and WD76C30ALV. In the discussion that follows, much of the material can also apply to other members of the chip set. To see the interconnection of chips during this process, look at Figure 8-2.

8.1 OVERVIEW: FDC POWER-DOWN MODE OPTIONS

The WD76C20ALV has multiple power-down mode options to save power and enhance the system battery life. The power-down modes are as follows:

- **FDC Power-Down Mode Option 1** (user initiated power-down mode)
- **FDC Power-Down Mode Option 2** (user transparent power-down mode)
- **Suspend/Resume Chip Set** (chip set power-down mode)

FDC Power-Down Mode Option 1 - The WD76C20ALV should enter in Power-Down Mode Option 1 when Bit 0 of MSR1 register (OPT1) is set to logical 1 and the following conditions are met:

- The PD bit of the MSR1 write only register is set to logic 1
- The RST pin to FDC is inactive
- The Bit 2 of Operations Register $\overline{\text{SRST}}$=1
- FDC is waiting command from Host

The FDC will return from Power-Down Mode Option 1 when the WD76C20ALV RESET is active and the FDC is reset. This will also reset Bit 0 of MSR1 register to logic 0. The crystal oscillator will turn on automatically once the chip is reset, but may need 20 ms to stabilize. The FDC standby current during the mode is maximum 100 uA. During this time through the normal Master Status register protocol the "request for master" (RQM) Bit 7 in the MSR will be inactive. (ROM bit indicates that data register is ready to send or receive data to or from the processor). The FDC can also be brought out from Power-Down mode by asserting a soft reset which assures that an internal reset is generated, and the reset is active long enough for the internal clocks and oscillator to start cleanly. If the mode is ever exited by merely writing to the MSR, then it is recommended that a soft reset be issued and a time out be instituted to allow the oscillator to stabilize (20 msec.). The soft reset can be released after this stabilization wait period.

FDC Power-Down Mode Option 2 - This is a user transparent Power-Down mode. The FDC has been designed to enter in Power-Down Mode automatically 1 second after the beginning of the IDLE state (based on the 500 Kb/s data rate). During this time the crystal oscillator, all the internal clocks, drive interface signals and all the interface signals to FDC will be shut off. The host interface path to FDC will be active during this time; for low power consumption the host interface signals should be held to DC logic levels 1 or 0.

The FDC will come out from PDM by any host access to FDC. The crystal oscillator will turn on automatically and need at least 20 ms for the oscillator to stabilize and during this time bit 7 of Master Status Register will be logic = 0. Once the Bit 7 of the MSR is set to logic 1, the FDC will be ready to receive any command from the host. During power-down mode, the contents of FDC registers will not be affected, and FDC will come up in the same mode as it was before it entered into PDM. The power-down mode can be disabled by writing a logic 0 in Bit 1 of the MSR. The default is power-down mode enabled all the time after hard reset or chip power-up.

Chip Set Power-Down - The following denotes I/O status during three different power-down options:

- **#1 - FDC Core and disk interface I/O Only**
  - During this power-down mode, all the input signals to floppy core, except RESET input to floppy core are shut off. All the floppy disk interface input and output pins are either disabled or tristated.
  - The WD76C20ALV host interface input and output pins, all the input and output pins not related to FDC core are left unaffected by this mode.
  - All the analog circuitry, the crystal oscillator and clock internal to FDC are shut off.
- **#2 - FDC Core and Disk Interface I/O Only**
  - This is a user transparent power-down mode for the FDC core and all the FDC disk interface pins. The host interface to and from FDC core and also at WD76C20ALV pins is not affected by this power-down mode.
  - All the analog circuitry, the crystal oscillator and clock internal to FDC are shut off.
- **#3 - WD7600 Core Chip Set Power-Down Mode**
  - For FDC core, this mode is exactly the same as Option 2.

Only signals which must be active in suspend mode remain active. All other pins are shut off, disabled or tristated.

The WD7600's power management saves power whenever possible without degrading the system's performance. Whenever the system perceives itself as not doing anything "useful," it powers down. This both slows the clock speed and cuts down on power consumption. The full power-down sequence is called system Suspend. The power-up sequence from system Suspend is called Resume.

8.1.1 Suspending the System

Suspend is initiated by a change in the state of certain Power Management Control (PMC) input(s). This change can either be programmed to generate a NMI or a Local Attention. If a PMC input is programmed to cause a Local Attention, the Local Attention signal has to be tied to an IRQ level. Once tied to interrupts, it can be determined when a system is performing an "idle" task. When it is known that the system is performing such a task, the processor can be safely powered down. The processor is then awakened on the next unmasked DRQ, IRQ, or NMI.

Once the processor is halted, it is awakened by an IRQ, which means that it will come out of power down on every IRQ0 once every 55 µs.

Several conditions are used by the processor to confirm an "idle" state. These are:

- Low battery condition
- External switch tied to a PMC interrupt enable that generates an IRQ
- Software-initiated suspend corresponding to a hardware interrupt (for example, an INT77H for IRQ15H)
- Watchdog timer generates a PMC interrupt to the WD76C10 (which in turn generates an IRQ) whenever it recognizes it is not being used.

Any of the preceding reasons are valid for ascertaining that the system is idle. The following is a general description of the Suspend sequence:

1. Any change in PMC input signals the WD76C10 to generate a Local Attention which is tied to an IRQ leading to the processor.

   The processor vectors to the power-down routine and the processor saves its internal states and the states of all peripherals attached to it that are to power down.

   The processor saves the states into a protected area of the system DRAM (similar to the shadowed BIOS).

2. The power down routine (in a loadable driver) writes to the full-power-down bit in the WD76C10 which enables the power-down sequence. The WD76C10 switches to sampling of the PMC inputs with the 14.318 MHz clock instead of the AT BUS clock.
3. The processor then writes to an I/O register in the WD76C10 that switches a PMC output connected to the PWRDN input pin of the WD90C20. On assertion of the PWRDN signal, the VGA controller enters the Power-Down

mode which refreshes the video DRAM via the AT BUS REFRESH signal. This is done so that the PIXCLK clock generator can later be powered down and the VGA controller can continue refresh. CAS before RAS refresh is the preferred way of refreshing the DRAMs because it allows lower power operation without the generation of a DRAM refresh address.

4. The processor then writes to the KILL 48 MHz register which sends a CSL address code of 15H to the WD7600 encoded Chip Select Bus (ENCSBUS). The WD76C20ALV decodes the 15H (qualified by an IOW) and disables its 16 MHz oscillator, errorlessly switches the 14.318 MHz oscillator signal to a 32 KHz, 50% duty cycle signal, then disables the 14.318 MHz oscillator. The WD76C20ALV also asserts the CSSERA, CSSERB, and CSPAR signals simultaneously which signals the WD76C30 to disable its 48 MHz oscillator. When this oscillator is disabled, the AT BUS CLOCK, KEYBOARD CLOCK, and 80287 CLOCK are disabled. The processor executes a halt instruction and the WD76C10 detects the halt status from the processor and switches from the AT compatible refresh to the PDREF controlled refresh. The WD76C10 then switches the AT bus compatible REFRESH output signal to mimic the PDREF input signal.

   The PDREF input is a CMOS level clock signal that has a 124 µs period and a low going pulse of 200 ns to 1 µs. This signal is always active and should be adequate for refreshing low power DRAMs. This signal is generated by the WD76C20ALV.

5. On detecting that the 14.318 MHz clock has been changed to 32 KHz, the WD76C10 tri-states all outputs except the PMC controls, DRAM controls, RAD bus, and AT bus REFRESH signal. The CPURES signal is asserted and then tri-stated and is pulled high through a 200K pull-up resistor. All inputs except RSTIN, CLK14, and the PMC are ignored, and all circuitry except the PMC and refresh logic is stopped.

The power is now turned off to the CPU, PIXCLK, BUS, etc. by the assertion of a PMC output from the WD76C10.

Figure 8-1 illustrates the interconnected concepts of Suspend, Resume, and Sleep Mode cycles.

8.1.2 Resuming the System

Resume is initiated by changes to PMC input(s) similar to the Suspend mode.

1. The WD76C10 samples the PMC inputs at 32 KHz. When it detects a change of any enabled PMC inputs, PMC outputs switch and power up the processor, bus, and so on. After 1 ms (timed by the 32 KHz clock input), the WD76C10 samples the processor-power-good PMC input. When this is active, the CPURES is driven high and the rest of the WD76C10 control outputs are driven to their correct states.
2. Once the chip detects the power-good signal, the WD76C10 performs a write to the ENABLE 48 HMz register which sends a CSL address code of 16H on the ENCSBUS.
3. The WD76C20ALV receives the 16H address code, enables the 16 MHz and 14.318 MHz oscillators, and deasserts the CSSERA, CSSERB, and CSPAR signals. After approximately 20 ms (stabilizing time for the oscillators), the WD76C20ALV switches the OSC 32 KHz signal to 14.318 MHz.
4. The WD76C30ALV enables its 48 MHz oscillator on the deassertion of its CSSERA, CSSERB, and CSPAR input signals.
5. When the WD76C10 detects that the 32 KHz has been switched to 14.318 MHz, it switches the PMC sampling to the AT BUS CLOCK. The WD76C10 then switches from PDREF- controlled refresh to the AT-compatible refresh. The WD76C10 also switches the AT bus REFRESH sign from PDREF input to AT-compatible refresh rate. The WD76C10 deasserts the CPURESET signal and the processor comes out of reset and checks the shutdown status in the RTC RAM on the WD76C20ALV. This tells the processor that it is coming out of full power-down mode as opposed to a warm or cold boot. The processor then restores the states of the machine.
6. The processor writes to the WD76C10 register that causes the WD76C10 to deassert its PMC output. This output is connected to the PWRDN input of the WD90C20 signaling the WD90C20 to come out of the power-down mode.

Figure 8-2 illustrates how the WD7600 chip set shares the Suspend/Resume/Sleep Mode duties.

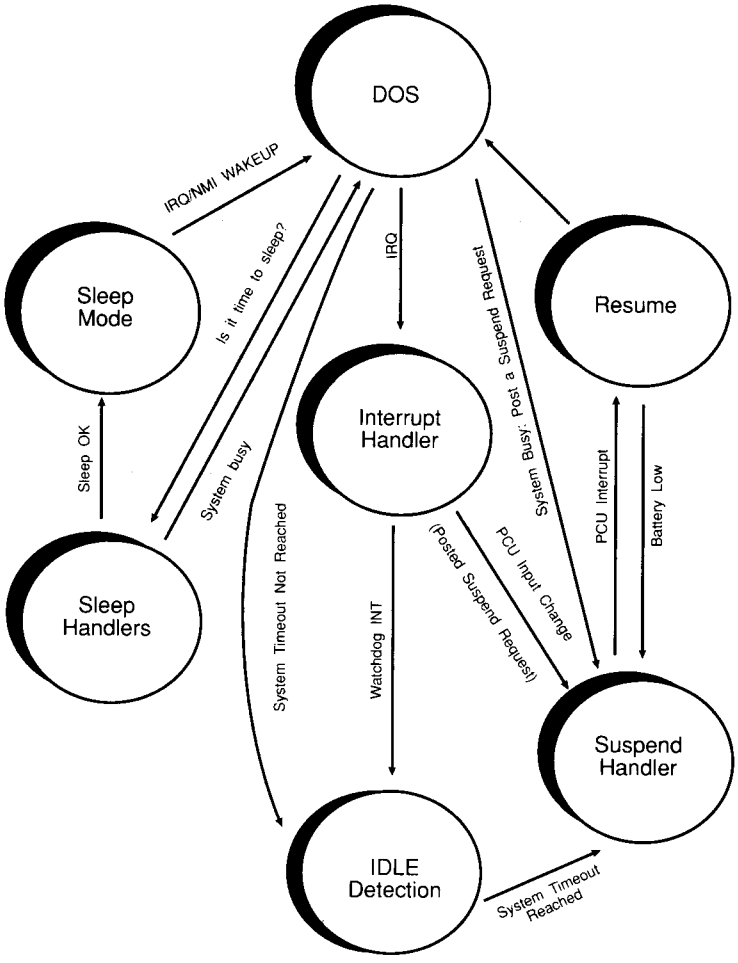

FIGURE 8-1. SUSPEND/RESUME/SLEEP MODE CYCLE

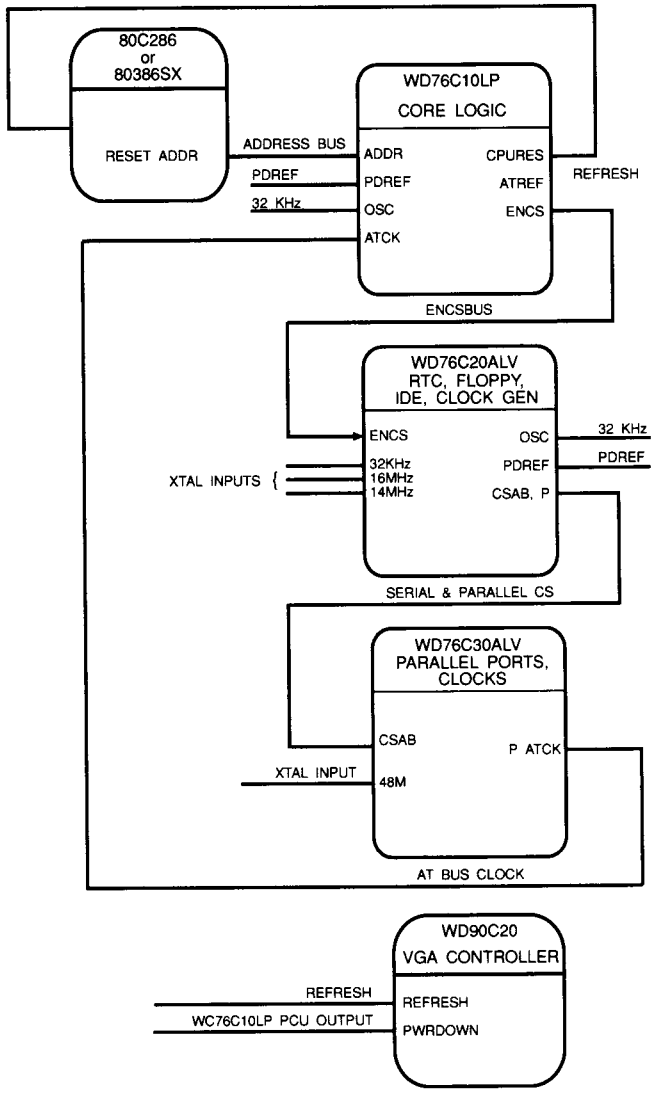

FIGURE 8-2. FULL POWER-DOWN MODE SYSTEM BLOCK DIAGRAM

8.2 PDREF

The PDREF is an external DRAM refresh line used to support the WD76C10 when it goes into Suspend/Resume mode. During Suspend/Resume mode, this pad provides a 1.0 µs pulse once every 15.26 µs (during a 50% duty cycle. This pulse is used to maintain the DRAM integrity with as little power as possible.

8.3 14 MHZ CRYSTAL SPECIFICATIONS

The 14.318 MHz crystal oscillator associated with the Suspend/Resume Logic is shown in Figure 8-3. This timing is maintained through the MX14 and $\overline{MX14}$ pins. MX14 is the input pin for the 14.318 oscillator and $\overline{MX14}$ is the output pin for the oscillator. See Table 9-2 for the crystal component values.

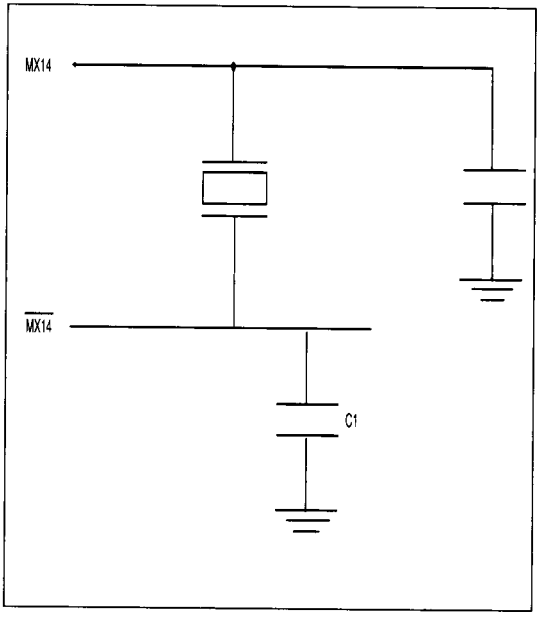

FIGURE 8-3. 14 MHZ CLOCK GENERATION

8.4 PIN STATES DURING POWER DOWN

Table 8-1 shows what happens to the pins during power-down.

84 PIN	100 PIN	SIGNAL	INPUT/ OUTPUT	PD OPT1		PD OPT2		SUSPEND	
				IN	OUT	IN	OUT	IN	OUT
1	11	$\overline{\text{IDEDENH}}$	Output		O		O		Z
2	14	VSS	VSS						
3	15	$\overline{\text{FX1}}$	Output		Z		Z		Z
4	16	FX1	Input	IH		IH		IH	
5	17	VDDD5	VDD (5.0 volt or 3.3 volt)						
6	18	FCLK2	Input	IH		IH		IH	
7	19	$\overline{\text{RDD}}$	Sch Input	IH		IH		IH	
8	21	DMA	Bidirectional (input unused)	IH	Z***	IH	Z***	IH	Z
9	22	FIRQ	Bidirectional	IH	Z***	IH	Z***	IH	Z
10	23	$\overline{\text{DCHG}}$	Sch w/pullup	IH		IH		IH	
11	24	PCVAL	Sch Input	IH		IH		IH	
12	27	DRV	Bidirect ional sch(w/pullup)	IH	Z	IH	Z	IH	Z
13	28	$\overline{\text{HS}}$	Output		Z		Z		Z
14	29	$\overline{\text{WE}}$	Output		Z		Z		Z
15	30	$\overline{\text{WD}}$	Output		Z		Z		Z
16	32	VSS	VSS						
17	33	$\overline{\text{DIRC}}$	Output		Z		Z		Z
18	34	$\overline{\text{STEP}}$	Output		Z		Z		Z
19	35	$\overline{\text{DS0}}$	Output		Z		Z		Z
20	36	$\overline{\text{DS1}}$	Output		Z		Z		Z
21	37	$\overline{\text{DS2}}$	Output		Z		Z		Z
22	38	$\overline{\text{DS3}}$	Output		Z		Z		Z
23	39	$\overline{\text{MO0}}$	Output		Z		Z		Z
24	40	$\overline{\text{MO1}}$	Output		Z		Z		Z
25	41	VSS	VSS						
26	42	SIAPL	Input	I		I		I	
27	43	SDPLL	Input	I		I		I	
28	44	$\overline{\text{HDL}}$	Output		Z		Z		Z
29	45	$\overline{\text{RWC}}$	Output		Z		Z		Z
30	46	PWRDN	Output		OH		OH		OH
31	47	$\overline{\text{WP}}$	Input	IH		IH		IH	

TABLE 8-1. PIN STATES DURING POWER-DOWN

84 PIN	100 PIN	SIGNAL	INPUT/ OUTPUT	PD OPT1		PD OPT2		SUSPEND	
				IN	OUT	IN	OUT	IN	OUT
32	48	$\overline{TR00}$	Input	IH		IH		IH	
33	52	$\overline{IDX}$	Input	IH		IH		IH	
34	53	VSS	VSS						
35	54	*DB0	Bidirectional	I	O	I	O	IH	Z
36	55	*DB1	Bidirectional	I	O	I	O	IH	Z
37	56	*DB2	Bidirectional	I	O	I	O	IH	Z
38	57	*DB3	Bidirectional	I	O	I	O	IH	Z
39	58	*DB4	Bidirectional	I	O	I	O	IH	Z
40	59	*DB5	Bidirectional	I	O	I	O	IH	Z
41	60	*DB6	Bidirectional	I	O	I	O	IH	Z
42	61	*DB7	Bidirectional	I	O	I	O	IH	Z
43	62	IDED7	Bidirectional	I	O	I	O	IH	Z
44	63	VDDA5	VDD (5.0 volt or 3.3 volt)						
45	66	A0	Input	I		I		IH	
46	67	VSS	VSS						
47	68	$\overline{DACK}$	Input	I		I		IH	
48	69	$\overline{IOR}$	Input	I		I		IH	
49	70	$\overline{IOW}$	Input	I		I		IH	
50	71	$\overline{CSEN}$	Input	I		I		I	
51	72	DACKEN	Input	I		I		I	
52	73	DPH	Input	I		I		I	
53	74	DPL	Input	I		I		I	
54	77	RA10	Input	I		I		I	
55	78	RA9	Input	I		I		I	
56	79	RA8	Input	I		I		I	
57	80	$\overline{RESET}$	Input	I		I		I	
58	81	$\overline{RCLR}$	Input	I		I		IH	
59	82	BALE	Input (w/ pullup)	I		I		IH	
60	83	$\overline{RTCX}$	Output		O		O		O
61	84	RTCX	Input	I		I		I	
62	85	VBAT	VDD						
63	86	MX14	Input	I		I		IH	
64	87	$\overline{MX14}$	Output		O		O		Z
65	88	VSS	VSS						
66	90	PDREF	Output		O		O		O
67	26, 91	VDD3	VDD (5.0 volt or 3.3 volt)						
68	92	OSC	Output		O		O		O

TABLE 8-1. PIN STATES DURING POWER-DOWN (CONTINUED)

84 PIN	100 PIN	SIGNAL	INPUT/ OUTPUT	PD OPT1		PD OPT2		SUSPEND	
				IN	OUT	IN	OUT	IN	OUT
69	93	RTCIRQ	Output		O		O		O
70	94	TC	Output		O		O		O
71	95	PRDY	Input	I		I		IH	
72	96	$\overline{EMS}$	Output		O		O		Z
73	97	$\overline{PROGCS}$	Output		O		O		Z
74	98	PCUW1	Output		O		O		O
NA	64	$\overline{PROG2}$	Output		O		O		Z
NA	65	$\overline{PROG3}$	Output		O		O		Z
75	1	PCUW0	Output		O		O		O
76	2	$\overline{NPCS}$/S3V	Bidirectional	I	O	I	O	IH	Z
77	3	$\overline{CS8042}$	Output		O		O		Z
78	4	$\overline{ROMOE}$	Output		O		O		Z
79	5	$\overline{CSPAR0}$	Output		O		O		O
80	6	$\overline{CSSERB}$	Output		O		O		O
81	7	$\overline{CSSERA}$	Output		O		O		O
82	8	$\overline{CSIDE1}$	Output		O		O		Z
83	9	$\overline{CSIDE0}$	Output		O		O		Z
84	10	$\overline{IDEDENL}$	Output		O		O		Z
NA	89	PQREN	Input	I		I		I	
NA	20	PLL24	Input	IH		IH		IH	
NA	31	PLLOUT	Input	IH		IH		IH	
NA	13	PLLIN	Output		Z		Z		Z
NA	12	PLLREF	Output		Z		Z		Z

TABLE 8-1. PIN STATES DURING POWER-DOWN (CONTINUED)

NOTES:

IH = Input High, internally forced high

IL = Input Low, internally forced low

OH = Output High, internally forced high

Z = Output tri-stated; 1 = Input active; 0 = Output active

* DB is always powered down and Z-state unless chip access is in progress

** Z only if DMAEN = 0; 0 if DMAEN = 1

9.0 SPECIFICATIONS

9.1 MAXIMUM RATINGS

Absolute maximum ratings—all voltages referenced to VSS

V_{CC}	7.0 volts
Voltage at any pin	-0.3 to VCC+0.3 volts
Storage Temperature	-55°C to 150°C
Operating Temperature	0°C to 70°C

9.1 DC OPERATING CHARACTERISTICS

TA=0°C (32°F) to 70°C (158°F)
VCC = 5V ±10%/ 3.3V ±10%
CL =100 pf; C_{in} =10 pf; C_{inclk} = 20 pf
VIL/VOL referenced to 0.8V
VIH/VOH referenced to 2.0V
CY specifies FX1 period; MCY specifies MCLK period, dependent on selected data rate; WCY specifies MCLK period, dependent on selected data rate

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
VCC	Power Supply	4.5/3.0	5.5/3.6	V
VBAT	Battery Backup Voltage	2.6/2.0	VDD	V
VIL	Input Low Voltage - Data Bus and XTOCS	0/-0.3	0.8	V
VIH	Input High Voltage - Data Bus and XTOCS	2.0	-/VCC+.3	V
VILT	Input Low Threshold - Schmitt Trigger	0.8		$V_{typical}$
VIHT	Input High Threshold - Schmitt Trigger		2.0	$V_{typical}$
VHYS	Schmitt Trigger Hysteresis	0.45		$V_{typical}$
VOLAT*	Output Low - DBus, TC, $\overline{EMS}$; I_O=12mA		0.4	V
VOHAT*	Output High - DBus, TC, $\overline{EMS}$; I_O=-5.0mA	2.8		V
VOLHC	Output Low - Drive Interface: I_O=48mA		0.4	V
VOL	Output Low - All Others: I_O=4mA		0.4	V
VOH	Output High - All Others: I_O=400µA	2.8/2.4		V
ILUL	Latch Up Current Low	40		mA
ILUH	Latch Up Current High	-40		mA
ILL	Leakage Current Low		10	µA
ILH	Leakage Current High		-10	µA
ILL	32 KHz Input Leakage Current		1	nA
ICC	Supply Current - 100µA source loads		70/50	mA
ICC	Supply Current - 5mA source loads		140/100	mA
ICCPDM1	Supply Current in Power-Down Mode (Option 1)[1]		200/100	$\mu A_{typical}$
ICCPDM2	Supply Current in Power-Down Mode (Option 2)[1]		2/1	$mA_{typical}$
ICCPDM3	Supply Current in Chip Set Power-Down Mode		2/1	mA
ICCBAT	Supply Current in Battery Backup Mode[1]		50/25	µA
PD	Power Dissipation - ICC max[3]		700/300	mW
PDHL	Power Dissipation - ICCHL max[2, 3]		850/350	mW
VPQR**	Power Qualified Reset Threshold	2.8/NA	4.35/NA	V

TABLE 9-1. DC CHARACTERISTICS

* See Tables 3-3 and 3-4 for the signals/pins associated with these DC levels.
** VPQR is enabled in 5.0V application (84-pin package)
VPQR is pin selectable by the PQREN pin for 5.0V application in 100-pin SQFP package
[1] Vin = VCC or GND, I_O=0 mA; NA- not apply
[2] Includes DBx; I_O=-5.0 mA source loads
[3] Includes open drain high current drivers at Vol=0.4V

9.3 CRYSTAL CIRCUIT SPECIFICATION

SYMBOL	CHARACTERISTICS	MIN	MAX	UNITS
	*RTC CRYSTAL**			
R1	Crystal Motional Resistance		40	K ohm
C0	Crystal Shunt Capacitance		1.7	pF
C1	Crystal Motional Capacitance		0.0035	pF
Q	Crystal Quality Factor	50		K
CI_{IN}	Crystal Circuit Input Capacitance	30	±5%	pF
C_{OUT}	Crystal Output Capacitance	30	±5%	pF
RA	Crystal Circuit Drive Level Resistor	330	±1%	K ohm
RF	Crystal Circuit Feedback Resistor	15	22	M ohm
	16 MHZ CRYSTAL			
Rseries	Crystal Circuit Resistors	30		ohm
Cshunt	Crystal Output	10		pF
C1	Crystal Input Capacitance	47	±5%	pF
C2	Crystal Output Capacitance	15	±5%	pF
	14MHZ CRYSTAL			
Rseries	Crystal Circuit Resistors	30		ohm
Cshunt	Crystal Output	10	±5%	pF
C1	Crystal Input Capacitance	22	±5%	pF
C2	Crystal Output Capacitance	22		pF

TABLE 9-2. CRYSTAL CIRCUIT SPECIFICATION

* RTC crystal components specified are valid for crystals with A(CL) load capacitance of 12.5 pF to 18 pF typical.

9.4 RTC CRYSTAL COMPONENTS LAYOUT

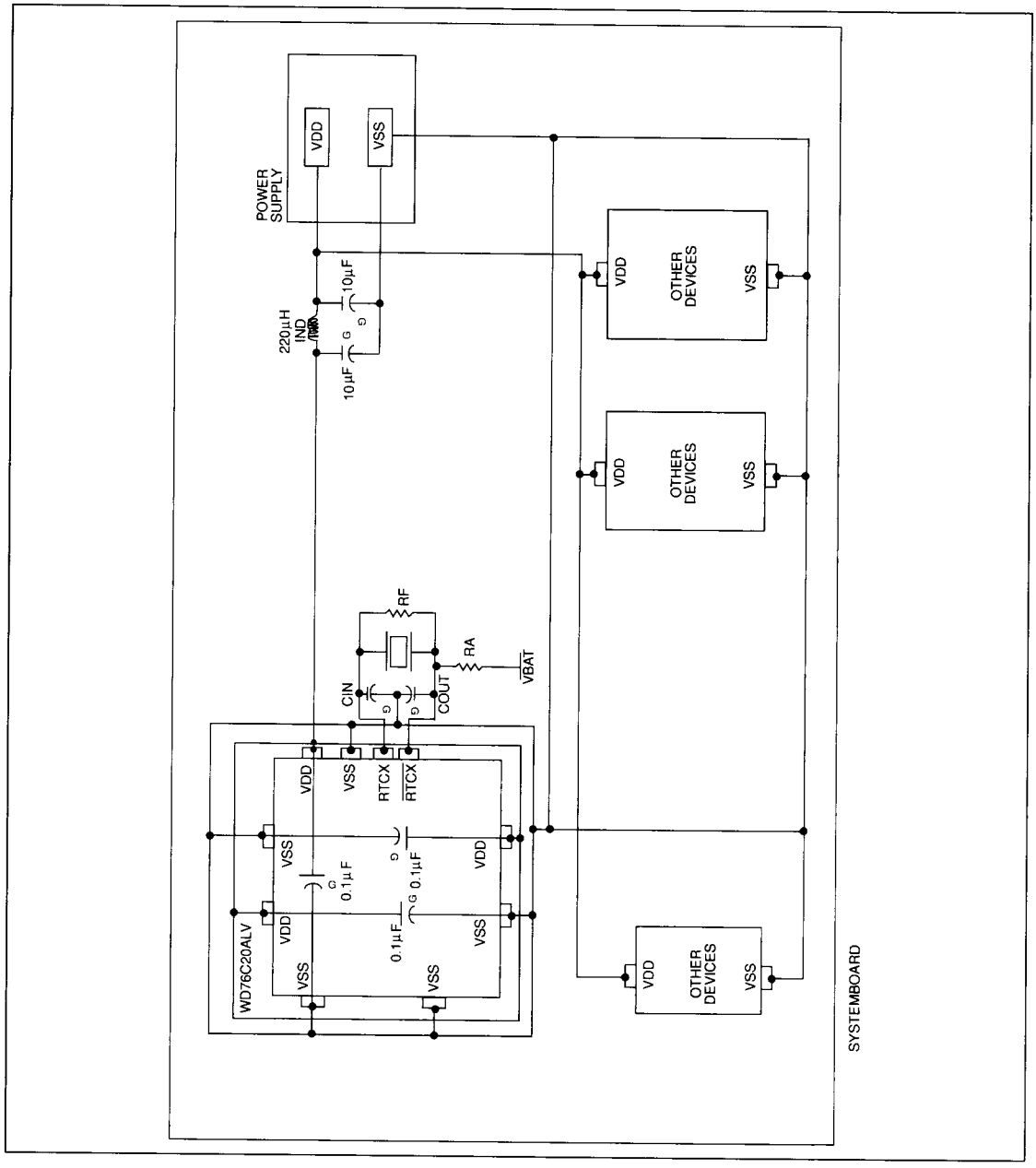

FIGURE 9-1. RTC CRYSTAL COMPONENTS LAYOUT

10.0 AC OPERATING CHARACTERISTICS

The AC Operating Characteristics are divided into four main categories:

- Floppy Disk Controller Specification
- Real Time Clock Specifications
- IDE Interface Timing
- Suspend/Resume Support Timing
- Chip Select Logic Decode Timing

Each table provides timing specifications which are followed by a figure displaying a timing diagram.

10.1 FLOPPY DISK CONTROLLER SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSS	CSL Input Address[1] Set Up to $\overline{IOR}$ Low	35		ns
pwRR	$\overline{IOR}$ Pulse Width	180		ns
tCSH	CSL Input Address[1] Hold Time from $\overline{IOR}$ High	10		ns
tRD	Data Access Time from $\overline{IOR}$ Low		175	ns
tDF	DB to Float Delay from $\overline{IOR}$ High	10	80	ns
tRI	FIRQ Reset Delay Time from $\overline{IOR}$ High		1MCY + 150	ns

TABLE 10-1. FDC READ TIMING SPECIFICATION

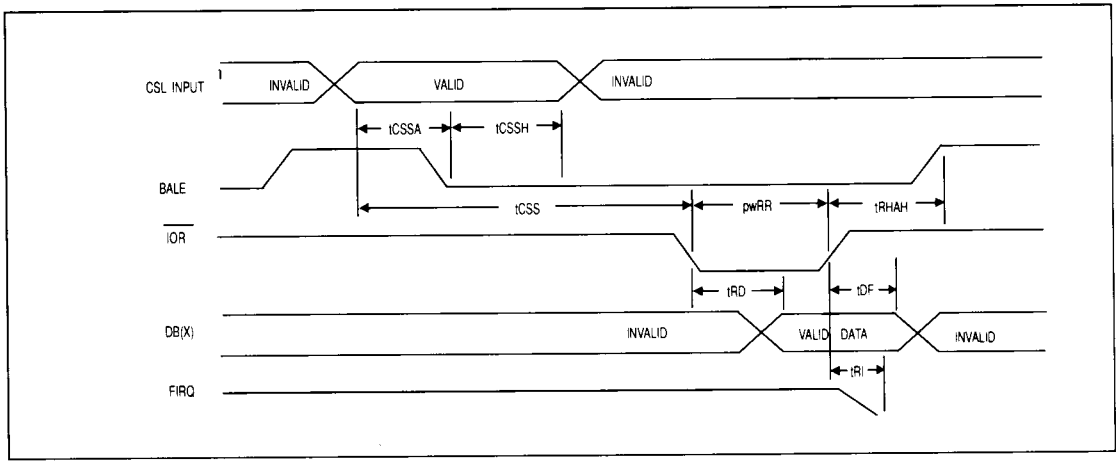

FIGURE 10-1. FDC READ TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tCSSH	CSL Input Address[1] Hold Time from BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IOR}$ Low	35		ns
pwRR	$\overline{IOR}$ Pulse Width	180		ns
tRHAH	$\overline{IOR}$ High to BALE High	10		ns
tRD	Data Access Time from $\overline{IOR}$ Low		175	ns
tDF	DB(x) to Float Delay from $\overline{IOR}$ High	10	80	ns
tRI	FIRQ Reset Delay Time from $\overline{IOR}$ High		1 MCY +150	ns

TABLE 10-2. FDC READ W/BALE TIMING SPECIFICATION

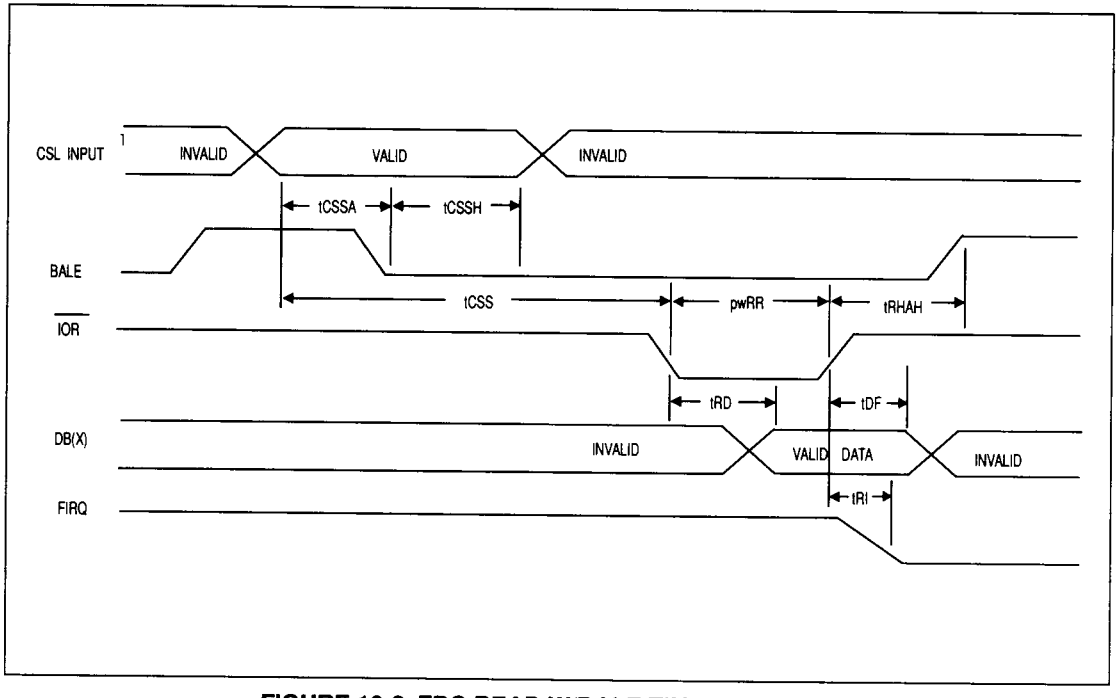

FIGURE 10-2. FDC READ W/BALE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSS	CSL Input Address[1] Set Up to $\overline{IOW}$ Low	35		ns
pwWW	$\overline{IOW}$ Pulse Width	180		ns
tCSH	CSL Input Address[1] Hold Time from $\overline{IOW}$ High	10		ns
tDW	Data Set Up Time to $\overline{IOW}$ High	100		ns
tWD	Data Hold Time from $\overline{IOW}$ High	10		ns
tWI	FIRQ Reset Delay from $\overline{IOW}$ High		1MCY + 150	ns

TABLE 10-3. FDC WRITE TIMING SPECIFICATION

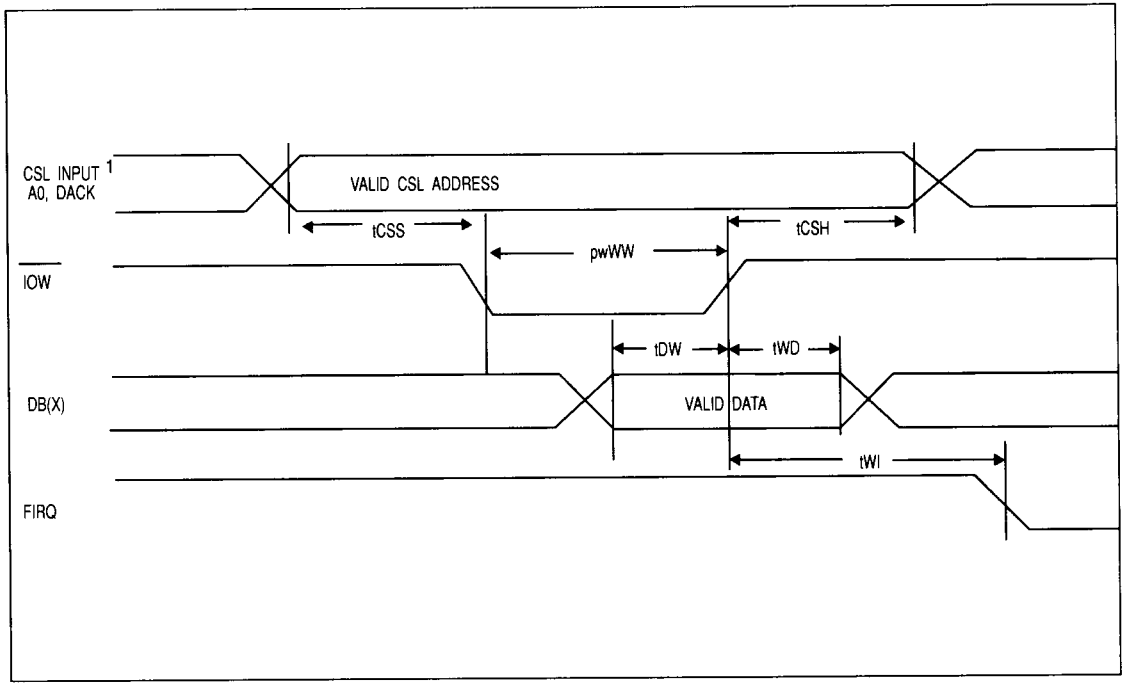

FIGURE 10-3. FDC WRITE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tCSSH	CSL Input Address[1] Hold Time from BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IO}$ Low	35		ns
pwWW	$\overline{IOW}$ Pulse Width	180		ns
tWHAH	$\overline{IOW}$ High to BALE High	10		ns
tDW	Data Set Up Time to $\overline{IOW}$ High	100		ns
tWD	Data Hold Time from $\overline{IOW}$ High	10		ns
tWI	FIRQ Reset Delay from $\overline{IOW}$ High		1 MCY +150	ns

TABLE 10-4. FDC WRITE W/BALE TIMING SPECIFICATION

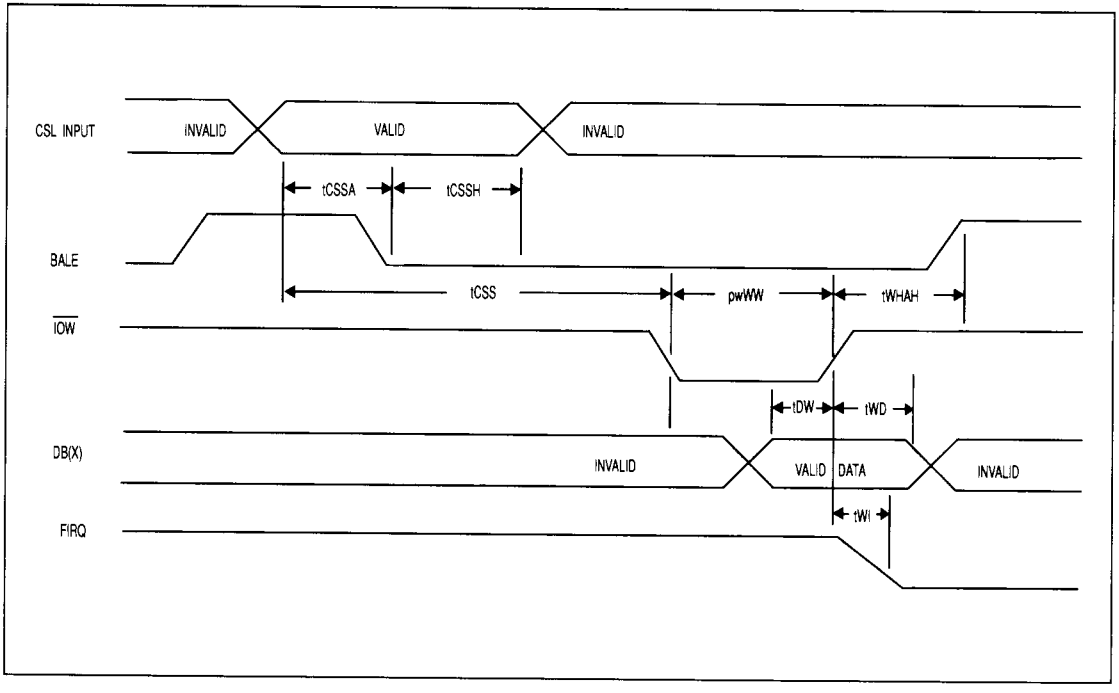

FIGURE 10-4. FDC WRITE W/BALE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tMCY	DMA Cycle Time	52		MCY
tMA	$\overline{DACK}$ Delay Time from DMA High	0		ns
tAM	DMA Reset Delay Time from $\overline{DACK}$ Low		140	ns
tAA	$\overline{DACK}$ Width	125		ns
tMRW	$\overline{IOR}$ or $\overline{IOW}$ Response from DMA High		48	MCY
tMtMR	$\overline{IOR}$ Delay from DMA	0		ns
tMW	$\overline{IOW}$ Delay from DMA	0		ns
tRD	Data Access Time from $\overline{IOR}$ Low		120	ns
tDW	Data Set Up Time to $\overline{IOW}$ High	100		ns
tDF	DB to Float Delay from $\overline{IOR}$ High	10	80	ns
tWD	Data Hold Time from $\overline{IOW}$ High	10		ns

TABLE 10-5. FDC DMA TIMING SPECIFICATION

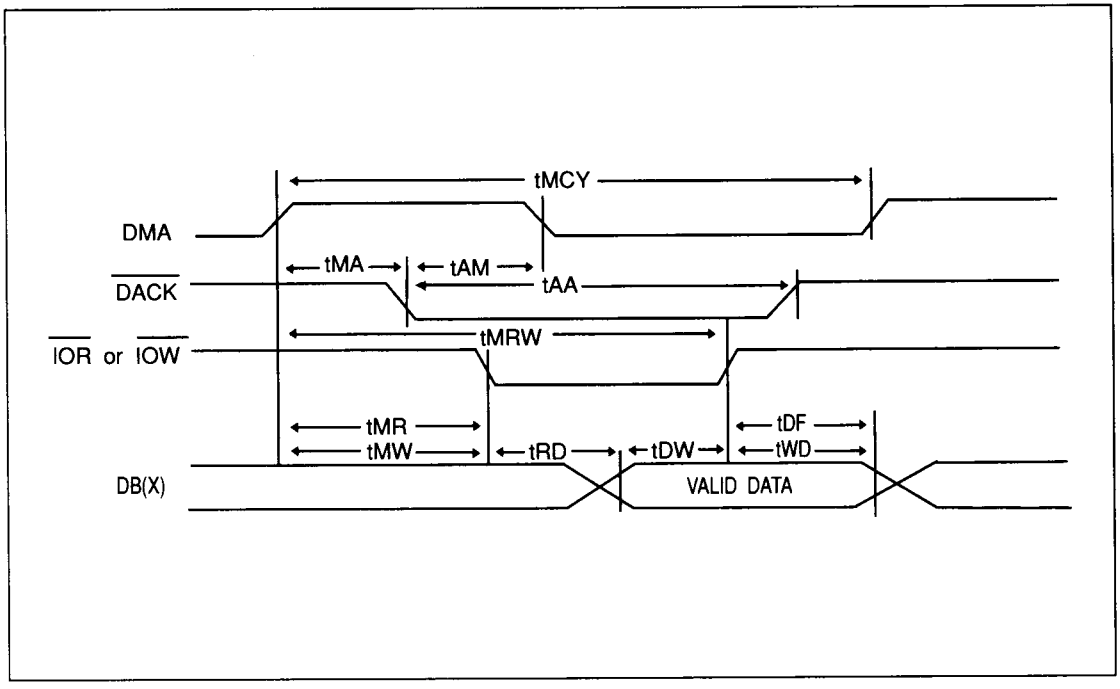

FIGURE 10-5. FDC DMA TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tTCR	DACKEN, $\overline{CSEN}$ Delay from Last DMA or FIRQ, $\overline{IOR}$	0	192	MCY
tTCW	DACKEN, $\overline{CSEN}$ Delay from Last DMA or FIRQ, $\overline{IOW}$	0	384	MCY
tTC	DACKEN High, $\overline{CSEN}$ Low Pulse Width	60		ns
tTCA	DACKEN High, $\overline{CSEN}$ Low to TC Asserted	0	30/40	ns
tTCD	DACKEN Low, $\overline{CSEN}$ High to TC De-Asserted	0	30	ns

TABLE 10-6. FDC TERMINAL COUNT TIMING SPECIFICATION

Note: The AC timing tTCA= 30 ns max for WD76C20A (5.0 Volts)
40 ns max for WD76C20ALV (3.3 volts)

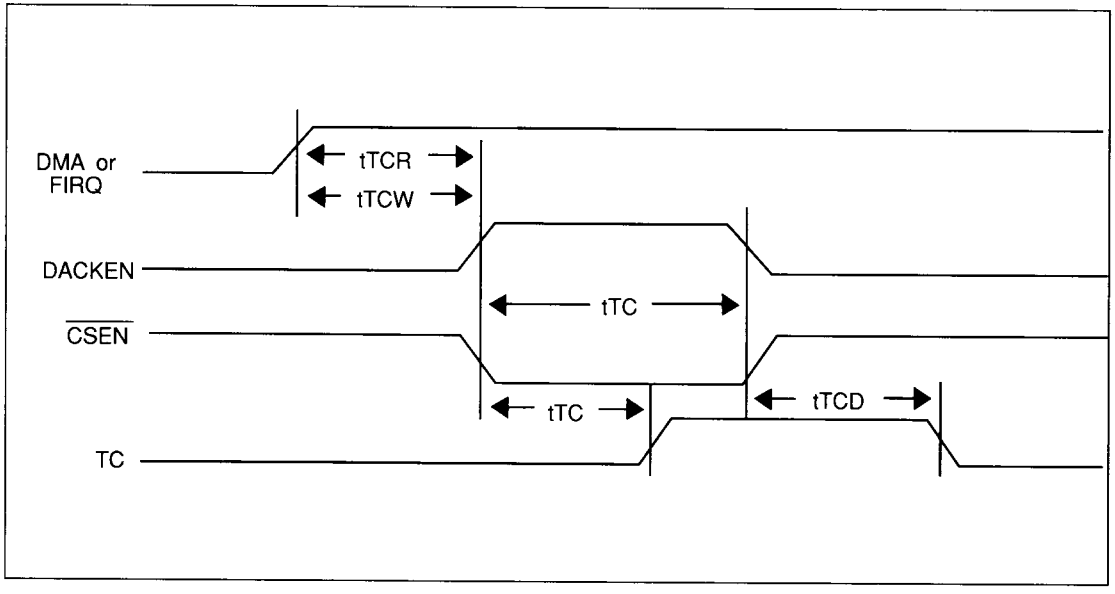

FIGURE 10-6. FDC TERMINAL COUNT TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCY	Clock Period	60		ns
tR	Clock Rise Time		5	ns
tF	Clock Fall Time		5	ns
tPH	Clock Active (High or Low)	25		ns

TABLE 10-7. FDC 16 MHZ CLOCK TIMING SPECIFICATION

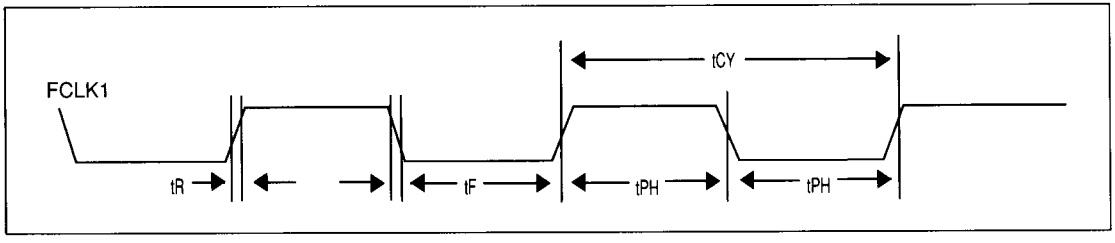

FIGURE 10-7. FDC 16 MHZ CLOCK TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tDST	$\overline{\text{DIRC}}$ Set Up to $\overline{\text{STEP}}$ Low	4		MCY
tSTP	STEP Active Time Low	24		MCY
tSTD	DIRC Hold Time from STEP High	96		MCY
tSC	STEP Cycle Time	132		MCY
tSTU	DS(x) Hold Time from STEP Low	20		MCY
tIDX	IDX Index Pulse Width	1		MCY
tRDD	RDD Active Time Low	40		ns
tWDD	WD Write Data Width Low	1/2		WCY

TABLE 10-8. FDC DISK DRIVE TIMING SPECIFICATION

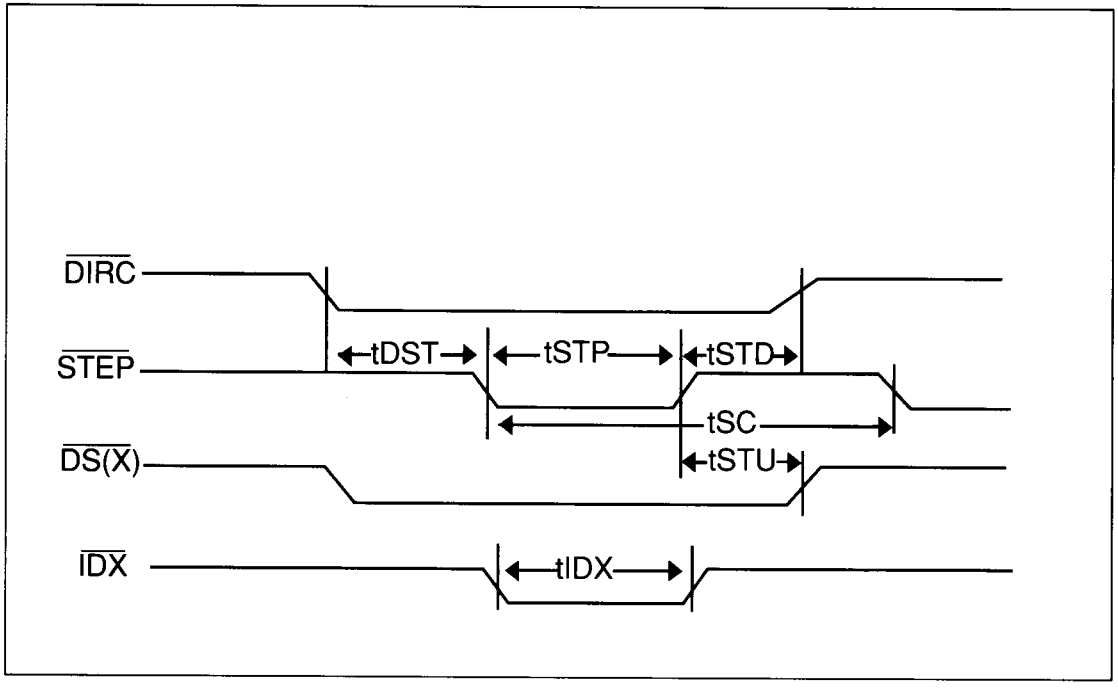

FIGURE 10-8. FDC DISK DRIVE TIMING DIAGRAM

10.2 REAL TIME CLOCK SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tASD	Data Cycle $\overline{IOW}$ or $\overline{IOR}$ High to Address Cycle $\overline{IOW}$ Low (not shown)	100		ns
tASED	Address Cycle $\overline{IOW}$ High to Data Cycle $\overline{IOW}$ or $\overline{IOR}$ Low (not shown)	100		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IOR}$ Low	35		ns
pwRS	$\overline{IOR}$ Pulse Width	180		ns
tCSH	CSL Input Address[1] Hold Time from $\overline{IOR}$ High	10		ns
tDDR	Data Access Time from $\overline{IOR}$ Low		175	ns
tDHR	DB to Float Delay from $\overline{IOR}$ High	10	80	ns

TABLE 10-9. RTC AND RAM READ TIMING SPECIFICATION

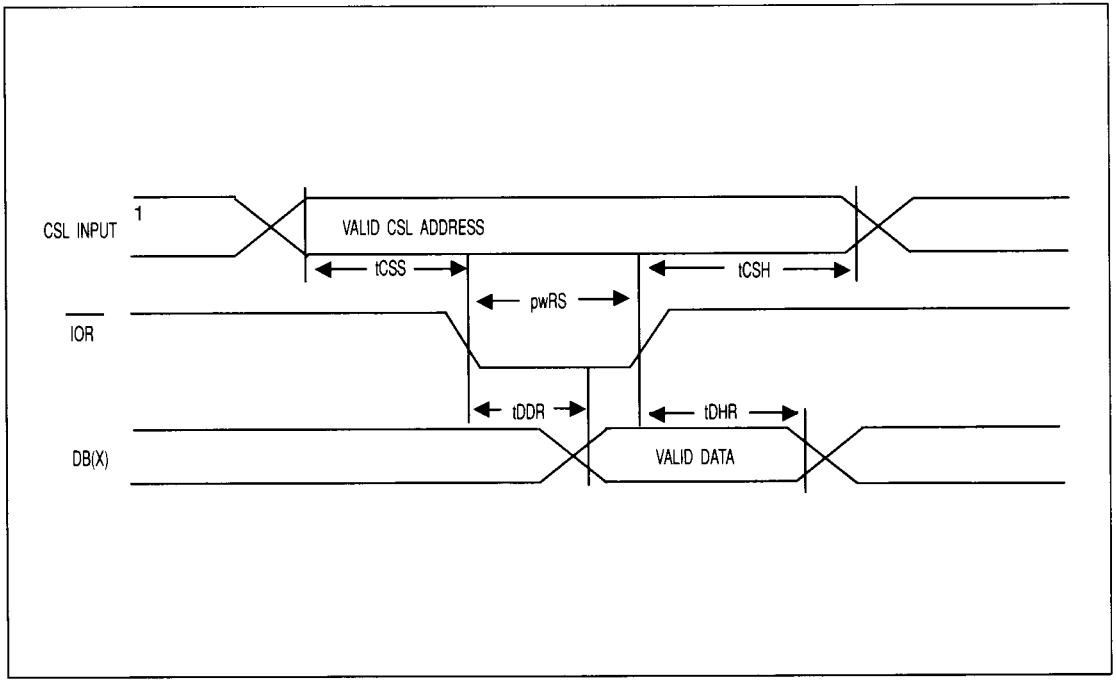

FIGURE 10-9. RTC AND RAM READ TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tASD	Data Cycle $\overline{IOW}$ or $\overline{IOR}$ High to Address Cycle IOW Low (not shown)	100		ns
tASED	Address Cycle $\overline{IOW}$ High to Data Cycle IOW or IOR Low (not shown)	100		ns
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tcSSH	CSL Input Address[1] Hold Time from BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IOW}$ Low	35		ns
pwWW	$\overline{IOW}$ Pulse Width	180		ns
tWHAH	$\overline{IOW}$ High to BALE High	10		ns
tDSW	Address or Data Setup Time to $\overline{IOW}$ High	100		ns
tDHW	Address or Data Hold Time from $\overline{IOW}$ High	10		ns

TABLE 10-10. RTC AND RAM WRITE W/BALE TIMING SPECIFICATION

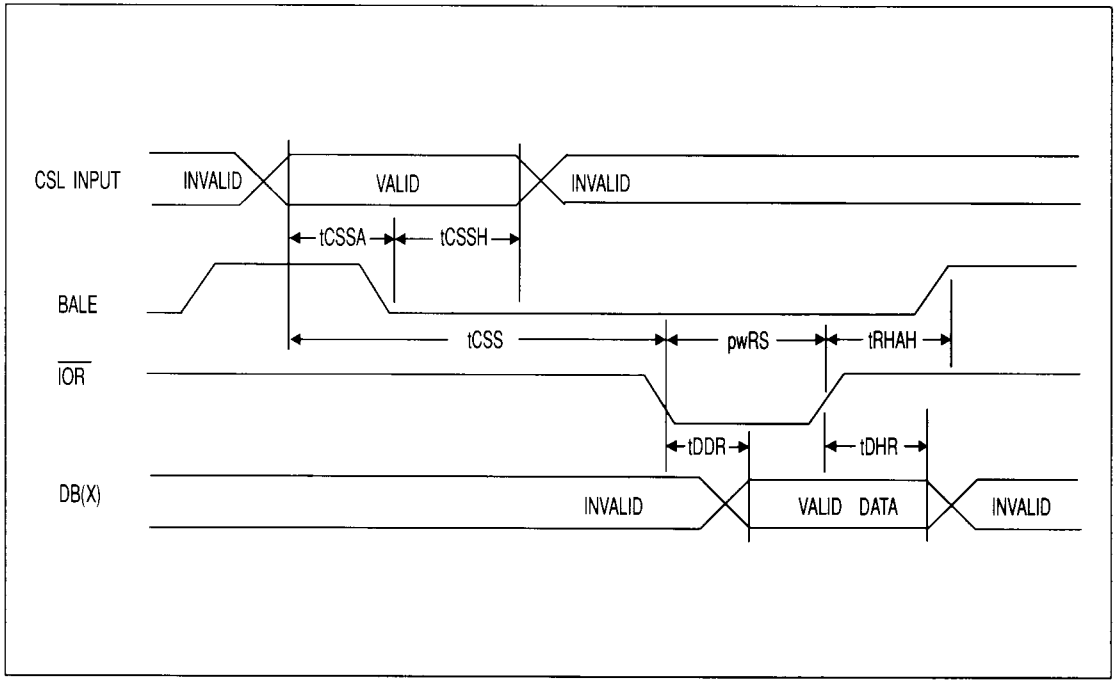

FIGURE 10-10. RTC AND RAM READ W/BALE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tASD	Data Cycle $\overline{IOW}$ or $\overline{IOR}$ High to Address Cycle $\overline{IOW}$ Low (not shown)	100		ns
tASED	Address Cycle $\overline{IOW}$ High to Data Cycle $\overline{IOW}$ or $\overline{IOR}$ Low (not shown)	100		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IOW}$ Low	30		ns
pwWW	$\overline{IOW}$ Pulse Width	180		ns
tCSH	CSL Input Address[1] Hold Time from $\overline{IOW}$ High	10		ns
tDSW	Address or Data Set Up Time to $\overline{IOW}$ High	100		ns
tDHW	Address or Data Hold Time from $\overline{IOW}$ High	10		ns

TABLE 10-11. RTC AND RAM WRITE TIMING SPECIFICATION

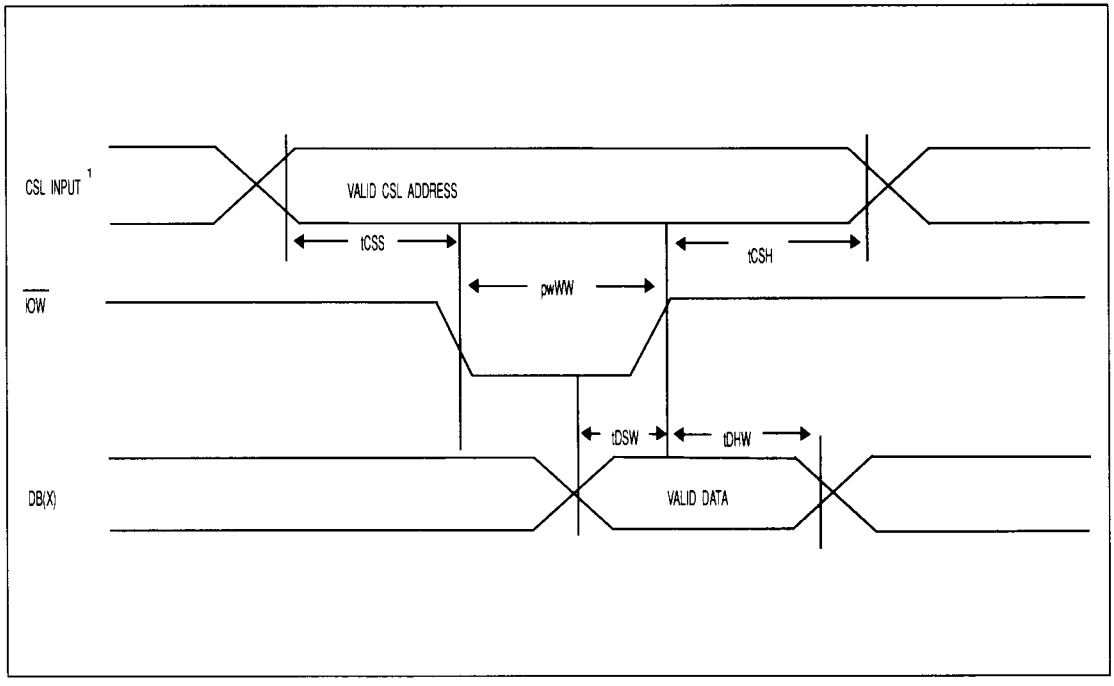

FIGURE 10-11. RTC AND RAM WRITE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tASD	Data Cycle $\overline{IOW}$ or $\overline{IOR}$ High to Address Cycle IOW Low (not shown)	100		ns
tASED	Address Cycle $\overline{IOW}$ High to Data Cycle IOW or $\overline{IOR}$ Low (not shown)	100		ns
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tcSSH	CSL Input Address[1] Hold Time from BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IO}$ Low	30		ns
pwRS	$\overline{IOR}$ Pulse Width	180		ns
tRHAH	$\overline{IOR}$ High to BALE High	10		ns
tDDR	Data Access Time from $\overline{IOR}$ Low		175	ns
tDHR	DB(x) to Float Delay from $\overline{IOR}$ High	10	80	ns

TABLE 10-12. RTC AND RAM READ W/BALE TIMING SPECIFICATION

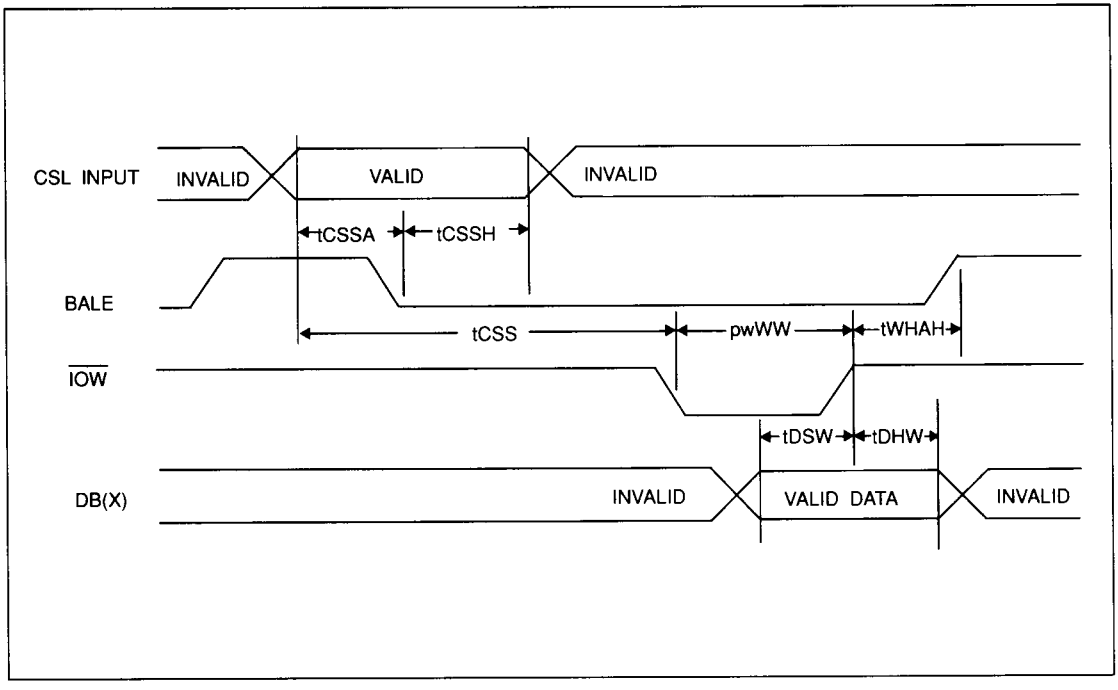

FIGURE 10-12. RTC AND RAM WRITE W/BALE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tRLIQ	$\overline{\text{RTCIRQ}}$ Release from $\overline{\text{IOR}}$ (Qualified by RECS)		2	µs
tRLIH	$\overline{\text{RTCIRQ}}$ Release from $\overline{\text{RESET}}$		2	µs

TABLE 10-13. RTC IRQ RELEASE TIMING SPECIFICATION

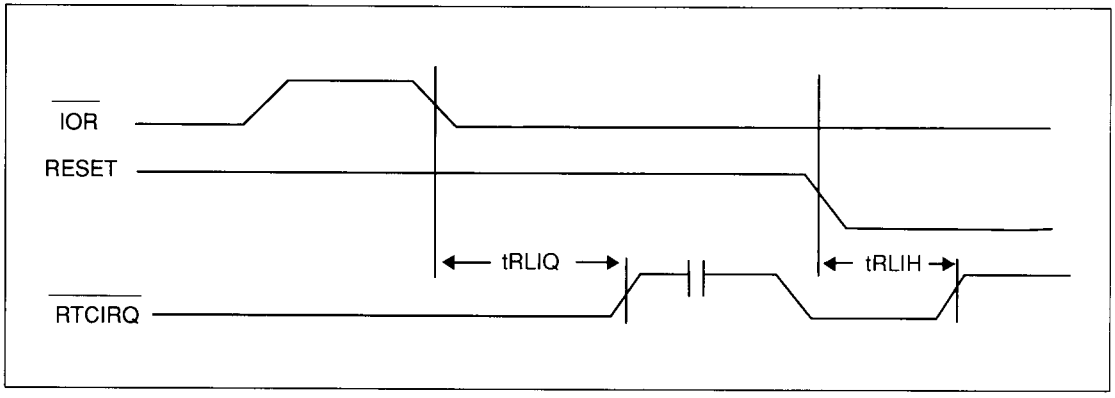

FIGURE 10-13. RTC IRQ RELEASE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tPRST	Power on Reset Width	200		ns
tRST	Reset Width	5		µs
tCA	Chip Access Delay from $\overline{\text{RESET}}$ High	32		MCY

TABLE 10-14. RESET TIMING SPECIFICATION

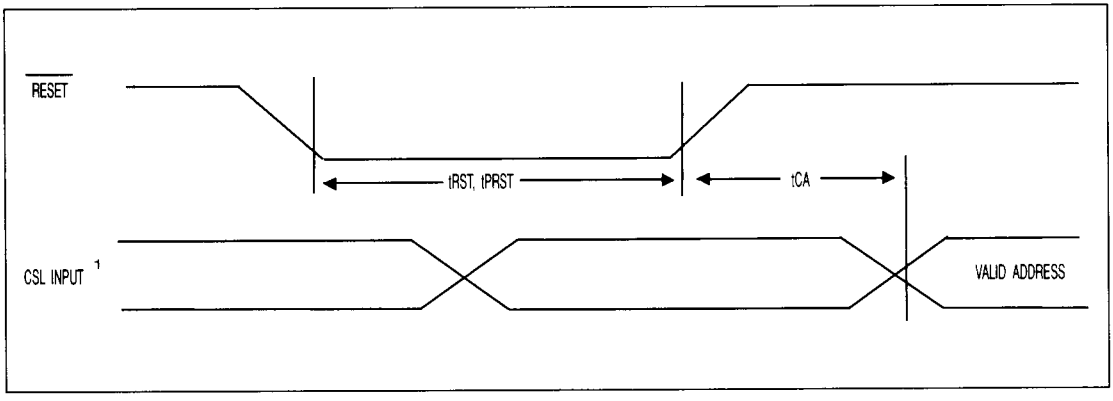

FIGURE 10-14. RESET TIMING DIAGRAM

10.3 IDE INTERFACE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSA	CSL Input Valid to CSL Output Asserted		35/40	ns
tCSD	CSL Input Invalid to CSL Output De-Asserted		35	ns
tD7D	Propagation Delay from IDED7 to DB7		20	ns
tD7HR	DB7 to Float Delay from $\overline{IOR}$ High	10	80	ns

TABLE 10-15. IDE INTERFACE TIMING (IDED7 TO DB7)

Note: The AC timing tCSA= 35 ns max for WD76C20A (5.0 Volts)
40 ns max for WD76C20ALV (3.3 volts)

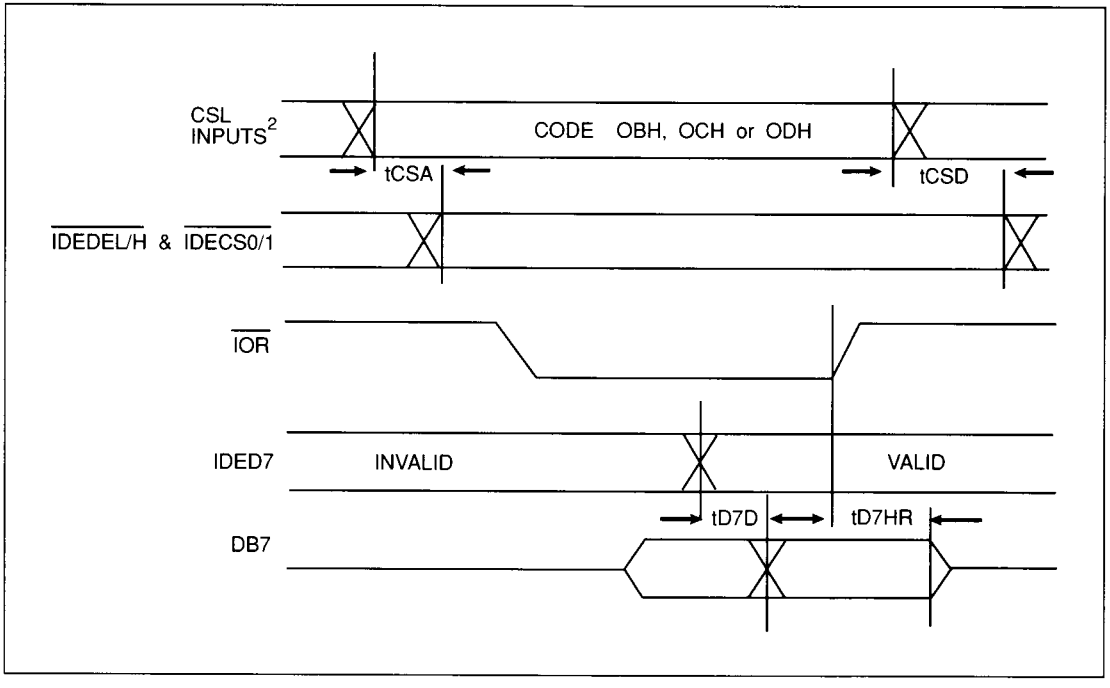

FIGURE 10-15. IDE INTERFACE TIMING DIAGRAM (IDED7 TO DB7)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tCSSH	CSL Input Address[1] Hold Time from BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IO}$ Low	30		ns
tRHAH	$\overline{IOR}$ High to BALE High	10		ns
tD7D	Propagation Delay from IDED7 to DB7		20	ns
tD7HR	DB7 to Float Delay from $\overline{IOR}$ High	10	80	ns

TABLE 10-16. IDE INTERFACE W/BALE TIMING (IDED7 TO DB7)

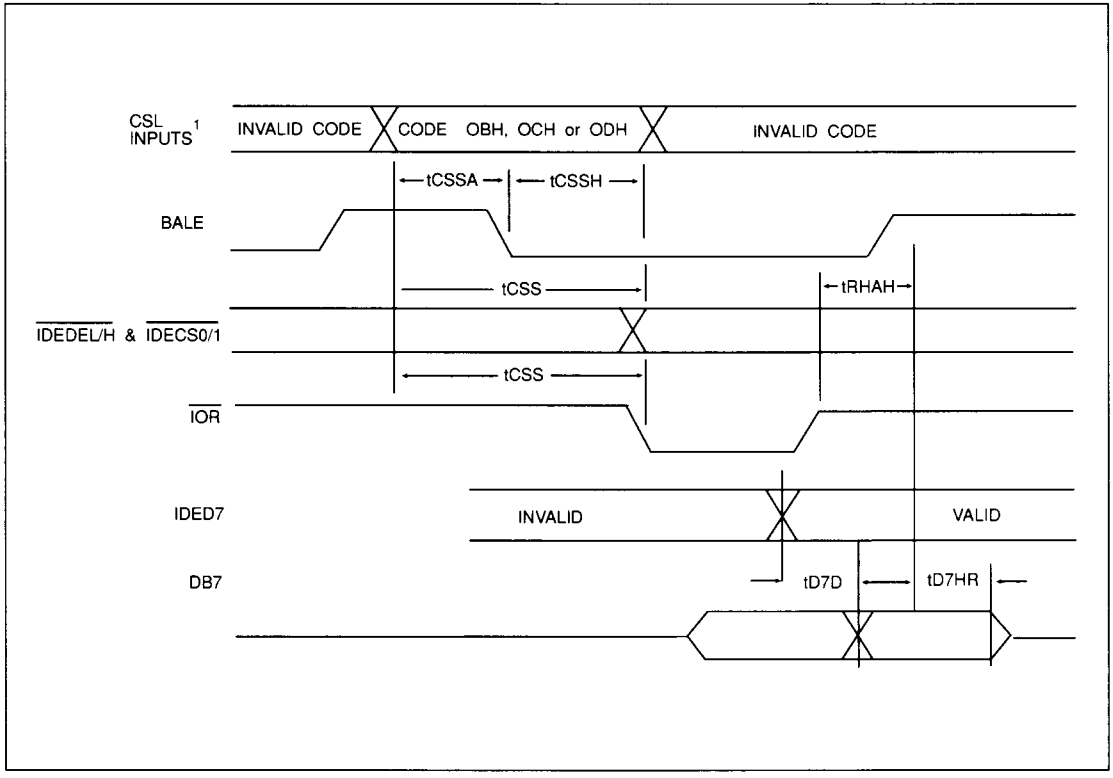

FIGURE 10-16. IDE INTERFACE W/BALE TIMING (IDED7 to DB7)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSA	CSL Input Valid to CSL Output Asserted		35/40	ns
tCSD	CSL Input Invalid to CSL Output De-Asserted		35	ns
tIDDR	IDED7 Enable time from $\overline{IOW}$ low		60	ns
tIDD	Propagation Delay from DB7 to IDED7		60	ns
tIDHR	IDED7 to Float Delay to $\overline{IOW}$ high	20	160	ns

TABLE 10-17. IDE INTERFACE TIMING (DB7 TO IDED7)

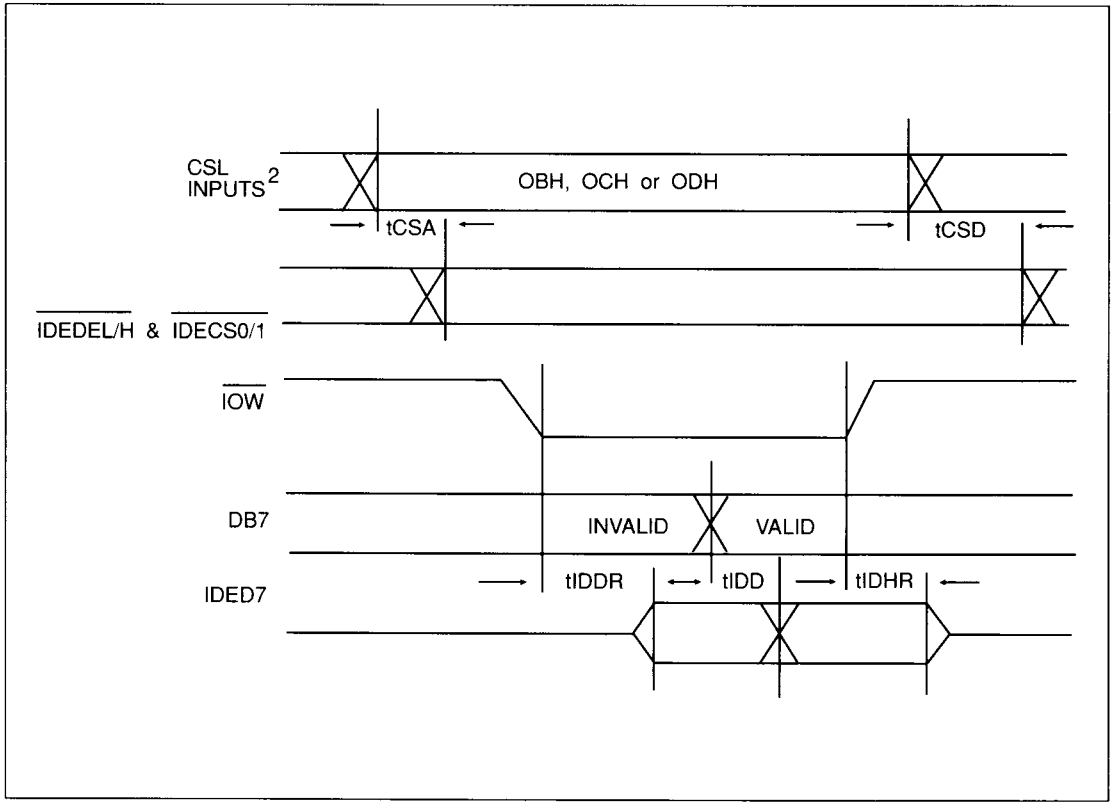

FIGURE 10-17. IDE INTERFACE TIMING (DB7 TO IDED7)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tCSSH	CSL Input Address[1] Hold Time From BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IOW}$ Low	30		ns
tWHAH	$\overline{IOW}$ High to BALE High	10		ns
tIDDR	IDED7 Enable time from $\overline{IOW}$ Low		60	ns
tIDHR	IDED7 to Float Delay from $\overline{IOW}$ High	20	160	ns

TABLE 10-18. IDE INTERFACE W/BALE TIMING (DB7 TO IDED7)

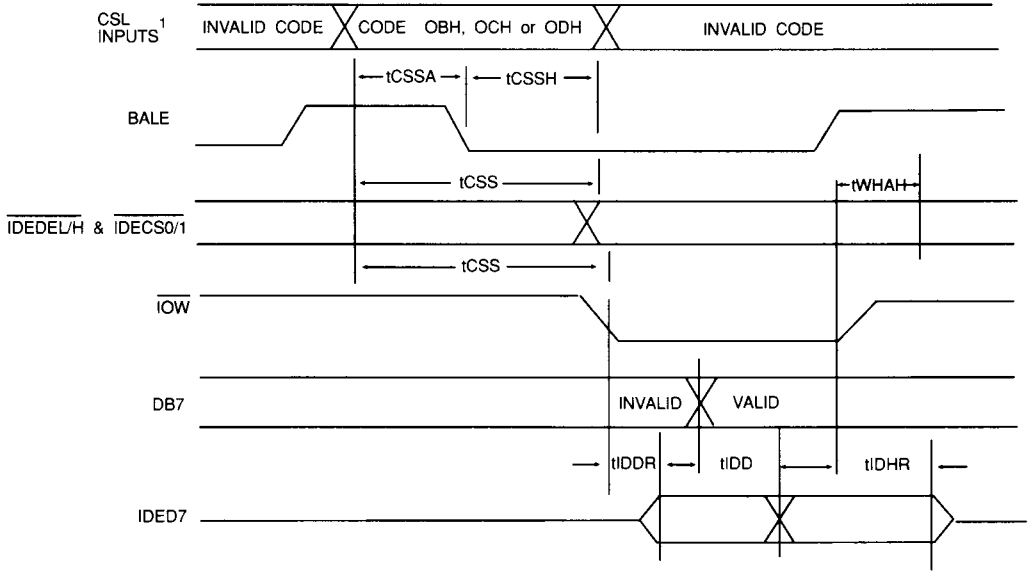

FIGURE 10-18. IDE INTERFACE W/BALE TIMING (DB7 to IDED7)

10.4 SUSPEND/RESUME TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCWSS	CSL Input Valid and $\overline{IOW}$ Low to OSC Transition to Low	30		ns
tCWSR	CSL Input Invalid and $\overline{IOW}$ Low to OSC Transition to Low	30		ns
tOSD	OSC Suspend Initiated to OSC Low Gap	60		µs
tOSL	OSC Low Gap	60		µs

TABLE 10-19. RESUME TO SUSPEND SUPPORT TIMING*

*Note: Code 15 can also be latched in with BALE.

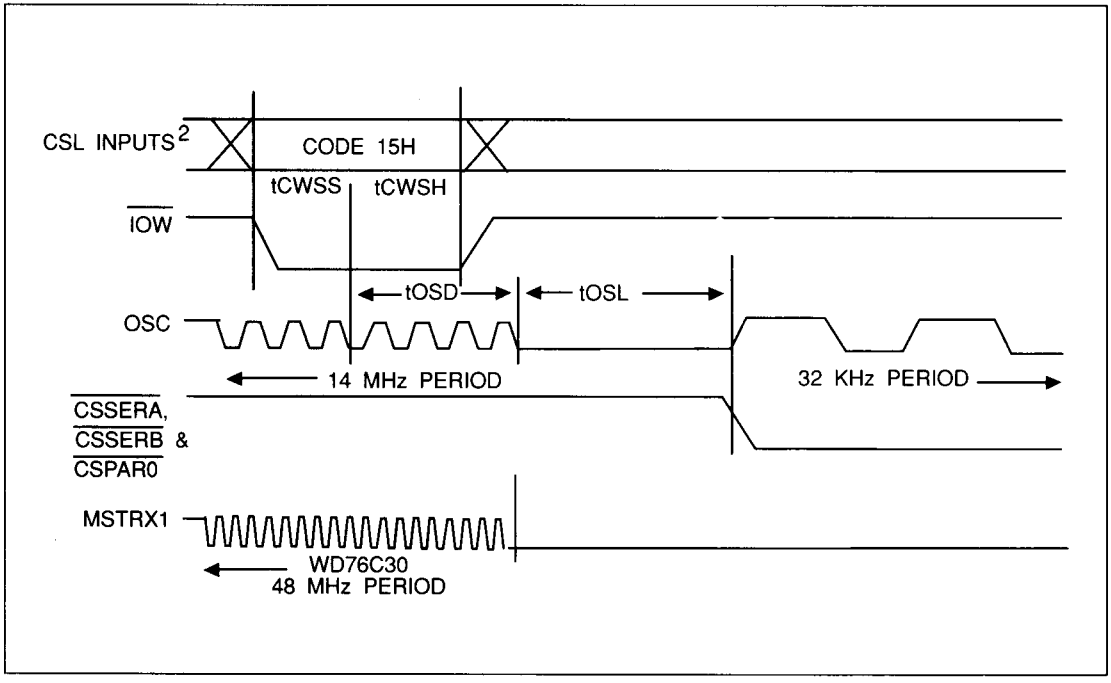

FIGURE 10-19. RESUME TO SUSPEND SUPPORT TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCRS	CSL Input Valid to OSC Transition to Low	30		ns
tCRH	CSL Input Invalid to OSC Transition to Low	30		ns
tCOR	CSL Output De-Assert to Resume WD76C30*	60	91	µs
tOTD	OSC Transition Delay (for XTAL warmup)*	500	501	ms

* CSL Code 16H is latched on the falling edge of OSC.

TABLE 10-20. SUSPEND TO RESUME SUPPORT TIMING

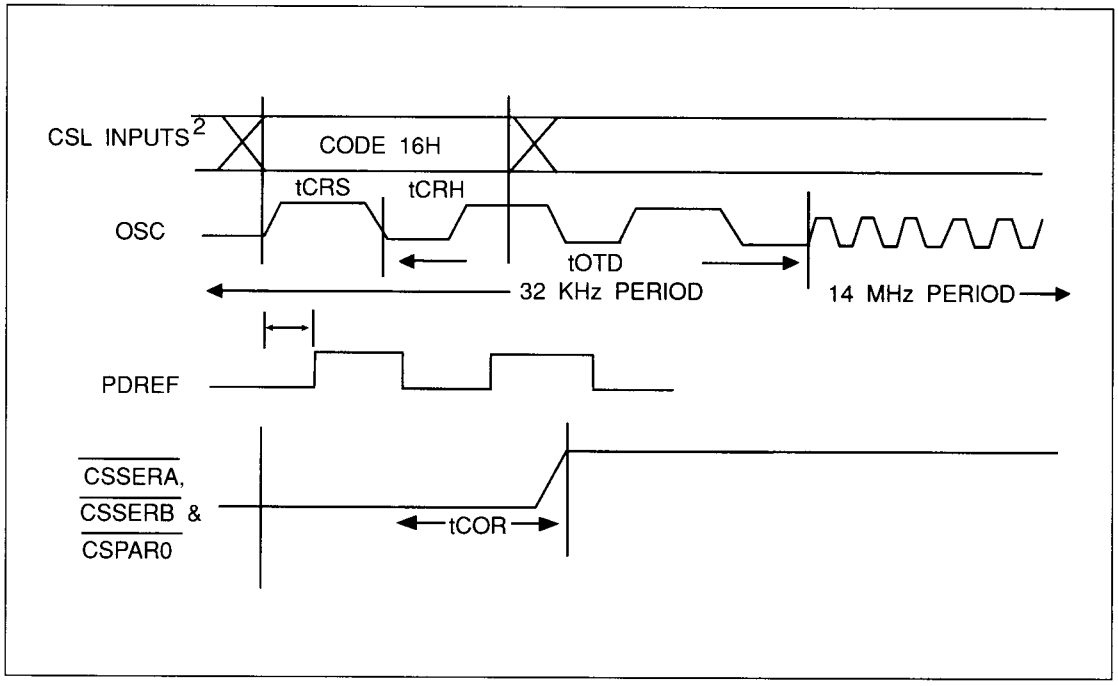

FIGURE 10-20. SUSPEND TO RESUME SUPPORT LOGIC

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSA	CSL Input[2] Valid to CSL Asserted		35	ns
tCSD	CSL Input[2] Invalid to CSL Output De-Asserted		35	ns
tCSH	CSL Input Address[2] Hold Time from $\overline{IOW}$ High	10		ns
tWLPH	$\overline{IOW}$ Low to PCUW0/1 High		35	ns
tWHPH	$\overline{IOW}$ High to PCUW0/1 Low		35	ns

TABLE 10-21. CHIP SELECT LOGIC DECODE TIMING SPECIFICATION

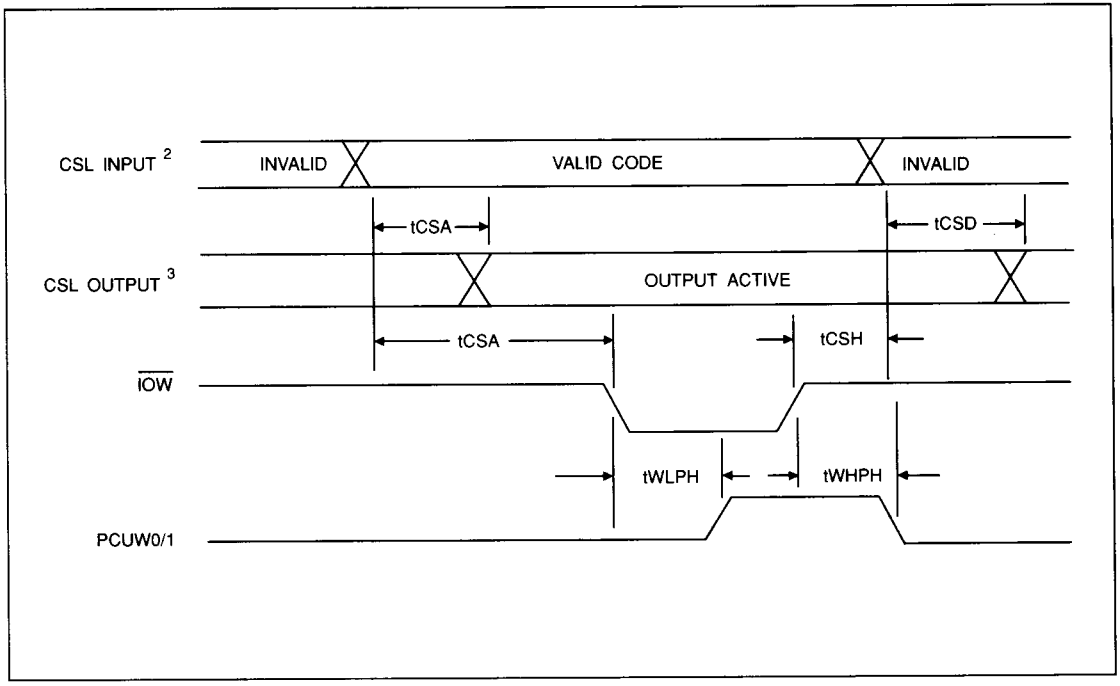

FIGURE 10-21. CHIP SELECT LOGIC DECODE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSSA	CSL Input Address[2] Set Up to BALE Low	10		ns
tCSSH	CSL Inpu Addresst[2] Hold Time from BALE Low	5		ns
tCSA	CSL Input Valid to Output[3]Asserted	35		ns

TABLE 10-22. CSL DECODE W/BALE TIMING SPECIFICATION

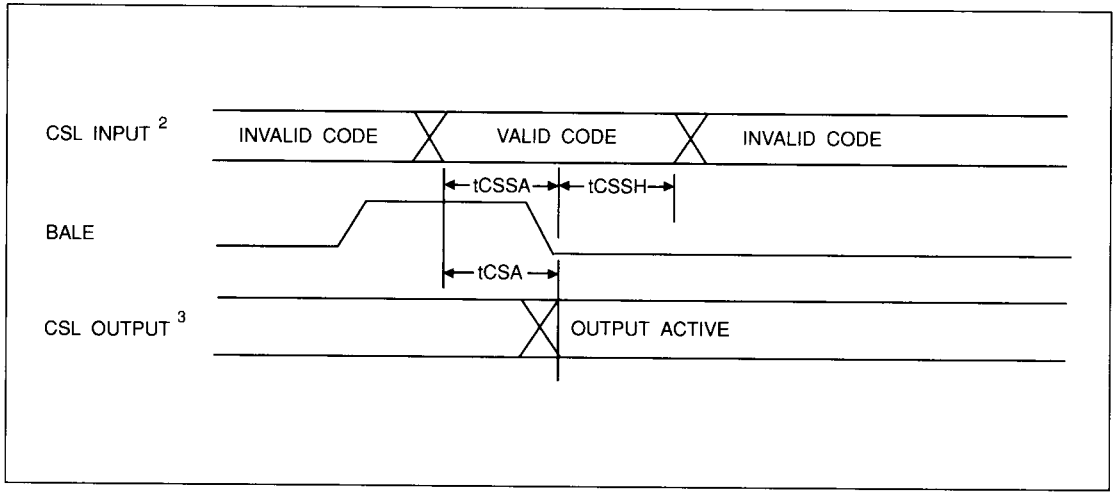

FIGURE 10-22. CHIP SELECT LOGIC DECODE W/BALE TIMING DIAGRAM

Notes

[1] The RTCALE and RTCCS are internal to the WD76C20ALV and are used by the RTC during I/O operations. The CS, LDCR, and LDOR are also internal to the WD76C20ALV and used by the FDC during I/O operations. CSL Inputs decoded in Table 4-1 are comprised of DPH, DPL, RA10, RA9 and RA8. All CSL Input Addresses are qualified by the CSEN signal. The general specification for generating the internal and external signals is presented in Tables 10-21 and 10-22.

[2] CSL Inputs are decoded in Table 4-1 and are comprised of DPH, DPL, RA10, RA9 and RA8. All CSL Input Addresses are qualified by the CSEN signal as shown in Figure 10-21 and 10-22. Also included in this group is DACKEN which must be deasserted (logic=0) in order to allow the decoder to activate any signal other than TC, which is asserted (logic=1) when both DACKEN and CSEN are active.

[3] CSL outputs are control lines used both internally by the WD76C20ALV (FDCCS, FDC LDCR, FDC LDOR, RTC CS, and RTC AEN) and externally by other chips (IDEDENL, IDEDENH, CSIDE0, CSIDE1, CSSERA, CSSERB, CSPAR0, ROMOE, 8042CS, NPCS, PCUW0, PCUW1, PROGCS, EMS and TC). For all but one case, only a single, decoded output is asserted at any given time and is unique as decoded in Table 4-1. Although not mentioned in Table 4-1, TC is asserted when both DACKEN and CSEN are active, as specified in Table 10-6.

11.0 PACKAGE DIMENSIONS

Figure 11-1 shows the 84-pin PQFP package dimension in inches and millimeters.

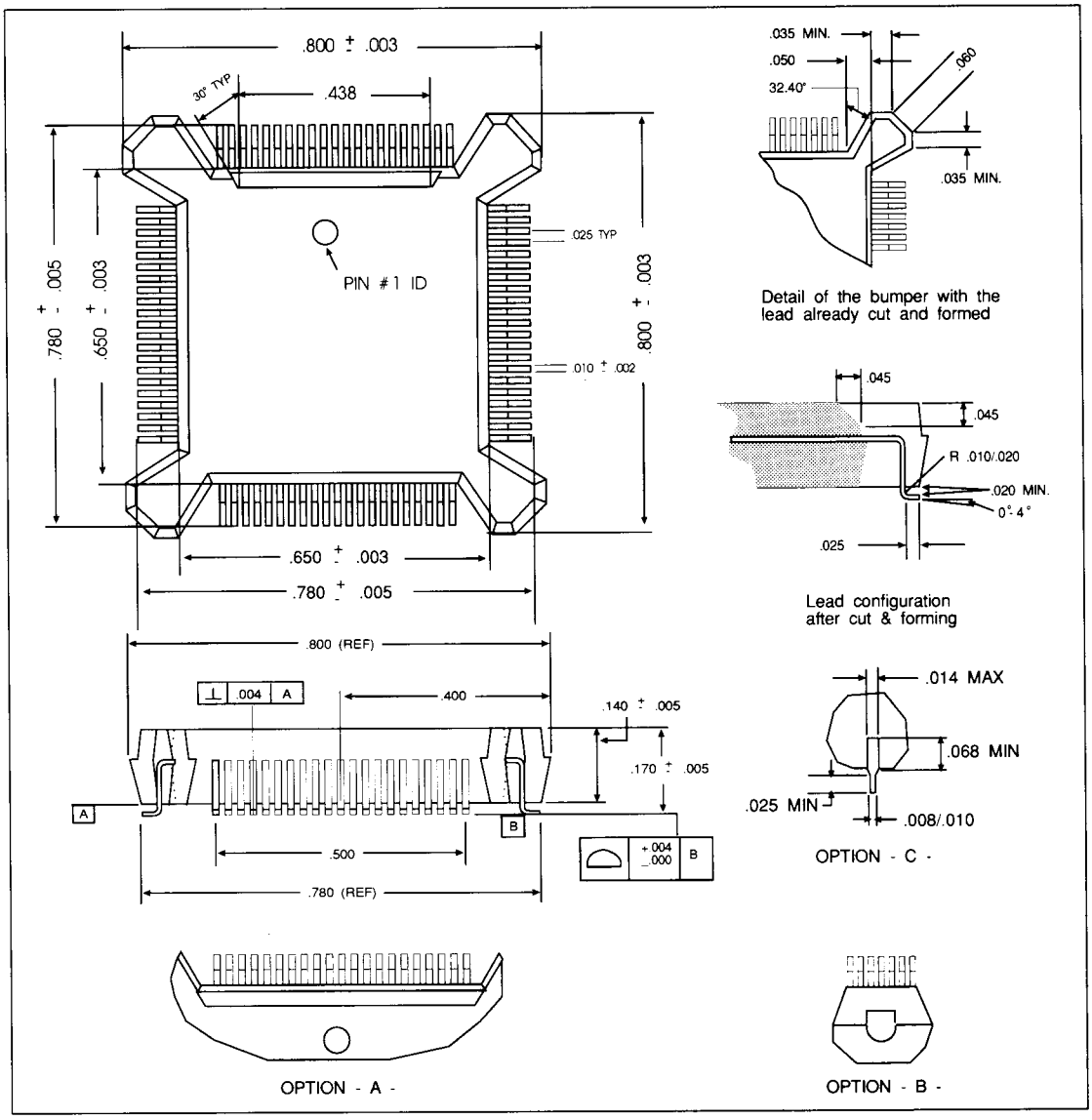

FIGURE 11-1. 84-PIN PQFP PACKAGE DIMENSIONS

Figure 11-2 shows the 100-pin SQFP package dimension in inches and millimeters.

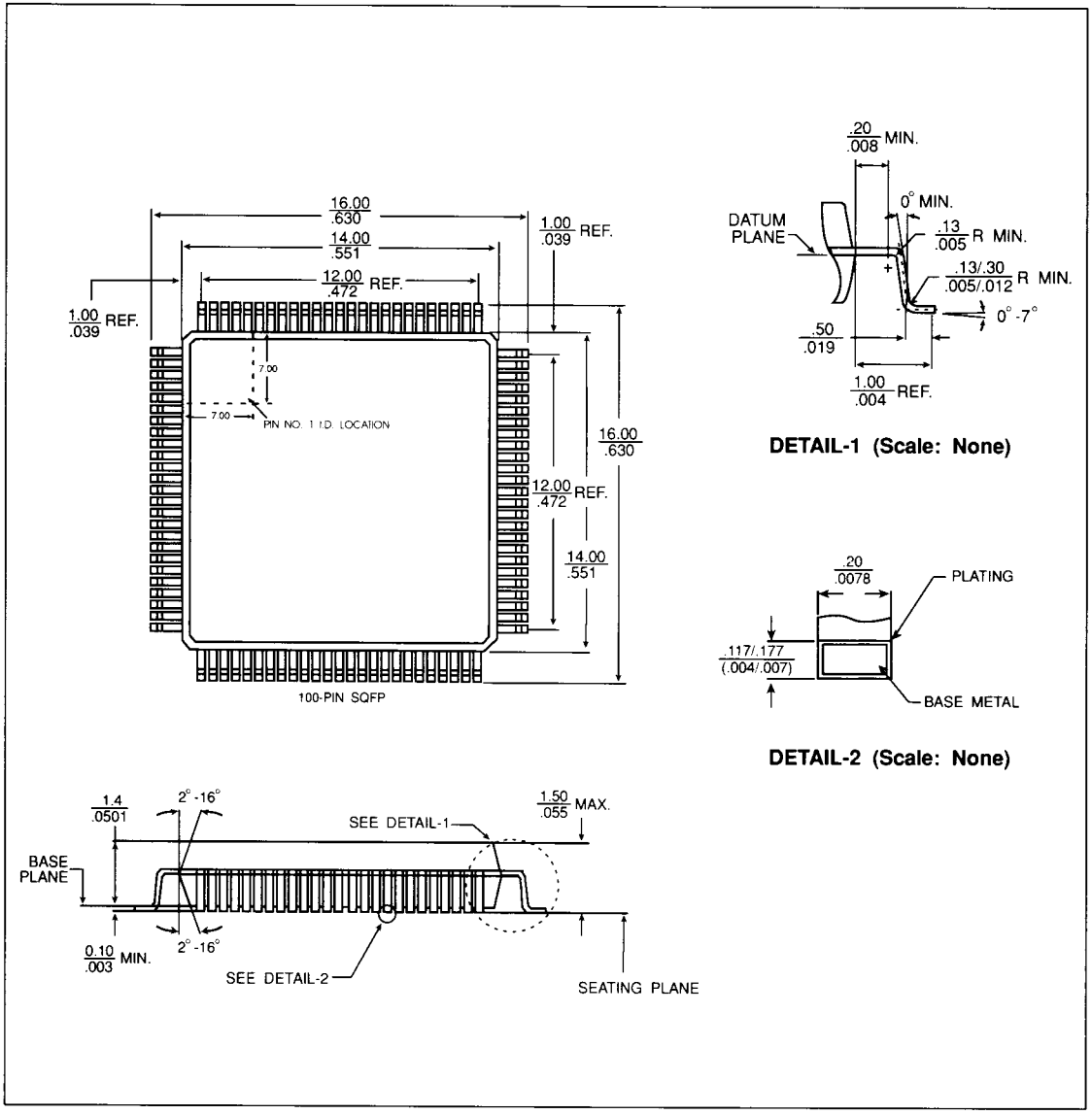

FIGURE 11-2. 100-PIN SQFP PACKAGE DIMENSIONS

A.0 REVISION HISTORY

A.1 INITIAL RELEASE

The initial release of this document was 9/1/92. This appendix will lists the changes between the initial release and the next version of the WD76C20ALV data sheet.