1.0 INTRODUCTION

1.1 GENERAL DESCRIPTION

The WD76C20ALV is a member of the WD7600 chip set which provides a cost-effective, power-efficient solution to PC systems design, especially those relating to "lap-top" devices. The set includes the WD76C10, the WD76C20ALV, and the WD76C30ALV as shown in Figure 1-1. Together these chips provide all necessary logic to build a fully integrated system board for several varieties of IBM PC/AT compatibles including systems using 80286, 80386SX, and 80C286 processors.

This document applies to both the 3.3 volt or 5.0 volt or 3.3/5.0 mixed voltage WD76C20ALV device. The WD76C20ALV can be used with either a 5.0 volt power supply or a low voltage 3.3 volt power supply. Some references are included to the WD76C20A which operates only at 5 volts.

As part of this chip set, the WD76C20ALV provides these integral functions:

- Bus Interface Logic
- IDE Interface
- Chip Select Logic
- Floppy Disk Controller
- Real Time Clock
- Suspend/Resume Logic

The Floppy Disk Controller (FDC) component provides necessary timing and signalling between the host processor peripheral bus and a floppy disk drive through a cable connector.

The Real Time Clock component provides calendar and clock information for the system.

The IDE Interface controls buffering between the system's AT Bus and PC/AT compatible IDE drive interface.

The Bus Interface Logic controls buffering of data between the system's AT Bus and the WD76C20ALV.

The Chip Select Logic section provides decoding for selected chip functions both within the WD76C20ALV and on the PC/AT motherboard.

Suspend/Resume Logic provides support for chip set power-down and resume sequences.

1.2 FEATURES

The WD76C20ALV includes these features:

- 84-pin PQFP packages
- 100-pin SQFP packages
- 3.3V or 5.0 volt or 3.3 volt and 5.0 volt VCC operation
- 3.3V nominal battery backup supply for 5.0V V_{CC} device and 2.4V nominal battery backup for 3.3V V_{CC} device. The battery backup supply is used for RTC and 114-byte SRAM
- Implemented in a low-power, high-performance, 1.25 micron CMOS technology process
- Option to interface with external analog PLL device (100-pin SQFP only)
- Option to select and de-select digital PLL internal to chip (100-pin SQFP only)
- Default digital PLL, internal to WD76C20ALV device (84-pin PQFP device only)
- Floppy Disk Controller (FDC) software transparent power-down mode with low standby ICC current. FDC features:
  - 256 tracks support
  - 100% software compatible with NEC 765A
  - Integrated high-performance DPLL data separator:
- 125, 250, 300, 500 KB/s and 1 MB/s data rates
- Option to select 150 KB/s FM and 300 KB/s MFM data rates only
  - Automatic Write Precompensation:
    - Defeat option
    - Inner track value of 125 or 187 ns, pin- selectable
  - On-chip clock generation:
    - 2 TTL clock inputs, or

  - Single 16 MHz crystal circuit and one TTL clock input
- PQR circuitry- power qualified reset circuitry
  - PQR disabled in 3.3 volt application, 84-pin package
  - PQR enabled in 5.0 volt application, 84-pin package
  - PQREN external pin to enable and disable PQR circuitry internal to chip (only in 100-pin SQFP package and 5.0 volt application)
  - Host interface read/write accesses compatible with 80286 microprocessors at speeds of 12 MHz with 0 wait states
  - Direct floppy disk drive interface - no buffers needed
    - 48 mA sink output drivers
    - Schmitt Trigger input line receivers
  - FDC direct PC XT/AT interface compatibility
    - Floppy Control and Operations Registers on chip
    - In PC/AT mode, provides required signal qualification to DMA channel
    - IBM BIOS compatible
    - Dual-speed spindle drive support
  - PS/2 type drive support
- Real Time Clock (RTC) features:

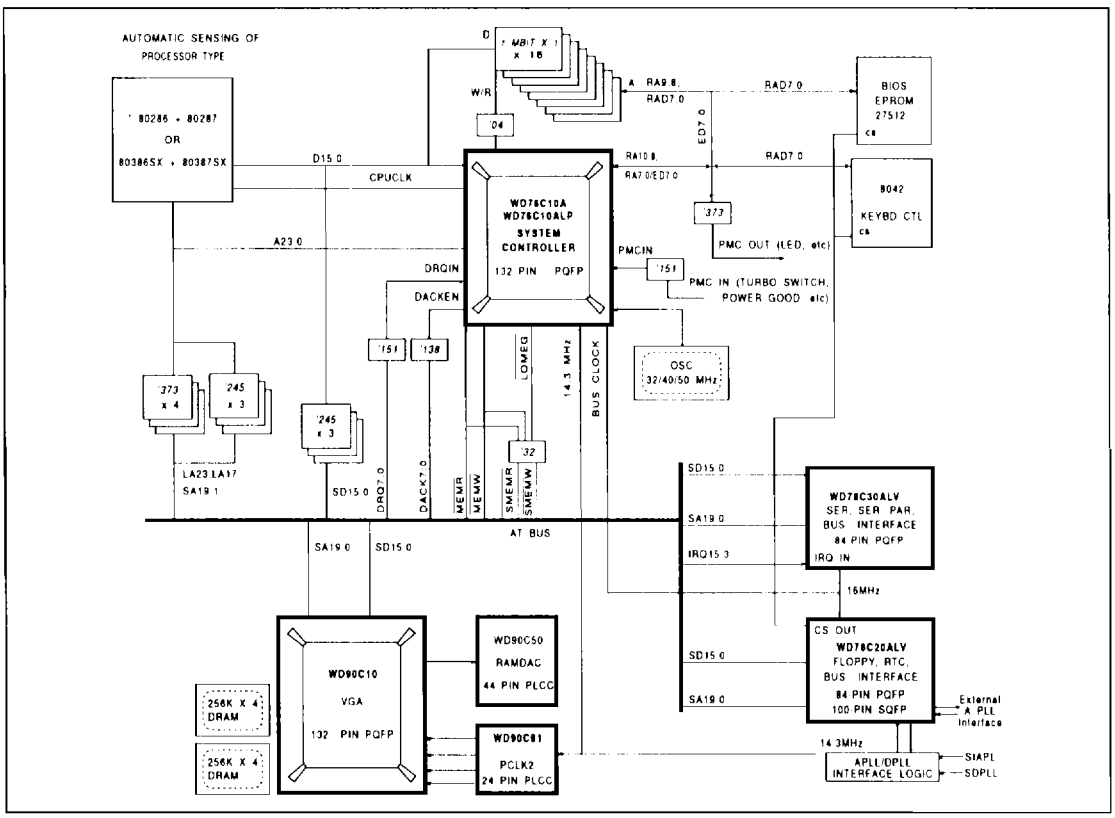

FIGURE 1-1. SYSTEM LEVEL FUNCTIONAL BLOCK DIAGRAM

- Software compatible with Motorola MC146818A.
- Internal time base and oscillator circuitry
- Counts seconds, minutes, and hours
- Counts days of the week, date, month, and year
- Time base input for 32.768 KHz square wave
- Time base oscillator for parallel resonant crystals
- Binary or BCD representation of time, calendar, and alarm
- 12- or 24-hour clock with AM and PM in 12-hour mode
- Daylight savings time option
- Automatic leap year compensation
- Interfaced with software as 128 RAM locations
- 114 bytes of general purpose RAM
- Status bit indicates data integrity
- Bus compatible interrupt signals (IRQ)
- Three interrupts are separately software maskable and testable:
  - Time-of-day alarm - once-per-second to once-per-day
  - Periodic interrupt rates from 122 µs to 500 ms
  - End-of-clock update cycle

1.3 FEATURE DIFFERENCES BETWEEN WD76C20ALV 84-PIN PQFP AND 100-PIN SQFP PACKAGES

- The WD76C20ALV (84-pin PQFP package) is backward compatible to the WD76C20 device for 5.0 volt and 3.3 volt applications.
- The WD76C20ALV (100-pin SQFP package) has two new programmable chip select outputs, they are PROG2 and PROG3 signals.
- The WD76C20ALV has integrated internal to the chip the level translators for interfacing directly to 5.0 volt or 3.3 volt signals. The WD76C20ALV can operate in 5.0 volt or 3.3 volt or mixed voltage (3.3 volt and 5.0 volt) environment.
- PQR (Power Qualified Reset). The PQR is disabled in 3.3 volt and mixed voltage operation. The PQR can be enabled in 5.0 volt VCC operation for a 100-pin SQFP packaged device by the PQREN pin. Also PQR is enabled as a default in the 5.0 volt, 84-pin PQFP packaged device.
- WD76C20ALV (100-pin SQFP) provides an interface to the external PLL (phase lock loop) device as an option. This is an option and can be selected by SIAPL and SDPLL input signals to the device. See details in the Signal Description section. This feature is provided in the 100-pin SQFP device only.
  - The default for the 84-pin PQFP device is digital PLL selection, which is internal to the WD76C20ALV device.