T-52-33-21

FARADAY
A Western Digital Company

Advance Information

FE5030

Advanced Memory Controller

- 100% Hardware (Register Level) and Software Compatible with the IBM* Personal System/2* Models 50 and 60
- Contains the following functions:
  - Address Multiplexer
  - DRAM Controls
  - Cache Controls
  - Memory Configuration Registers
  - EMS Registers
  - RAM Data Buffers and Parity Generation/Detection
- Complete DRAM Support
- Supports 256K, 1MB, 4MB DRAMs
- Page Mode DRAM Access with Interleaved Memory Banks
- Controls up to 4 Banks (up to 16MB) of Memory
- Supports EMS Expanded Memory (LIM 4.0)
- Programmable Wait States
- Shadow RAM for Fast BIOS Execution
- Extended Setup Facility ™ (ESF™)
- Low Power 1.25 Micron CMOS Technology
- 132-Lead JEDEC Plastic Quad Flat Pack

As part of the Faraday® FE5400 Chip Set, the FE5030 Memory Control Logic device significantly facilitates the design and implementation of Model 50 and 60 compatible system boards. By combining functionality normally implemented in gate arrays and discrete components, the FE5030 decreases design complexity, saves space, reduces system cost, and increases system reliability.

The Extended Setup Facility (ESF) is a fully compatible enhancement that allows designers to add more functionality (e.g., Winchester Controller, LAN Adapter, Additional Serial Port) to the system board. This facility helps reduce costs and provides system level product differentiation. Figure 1 shows a typical system diagram using the FE5400 Chip Set.

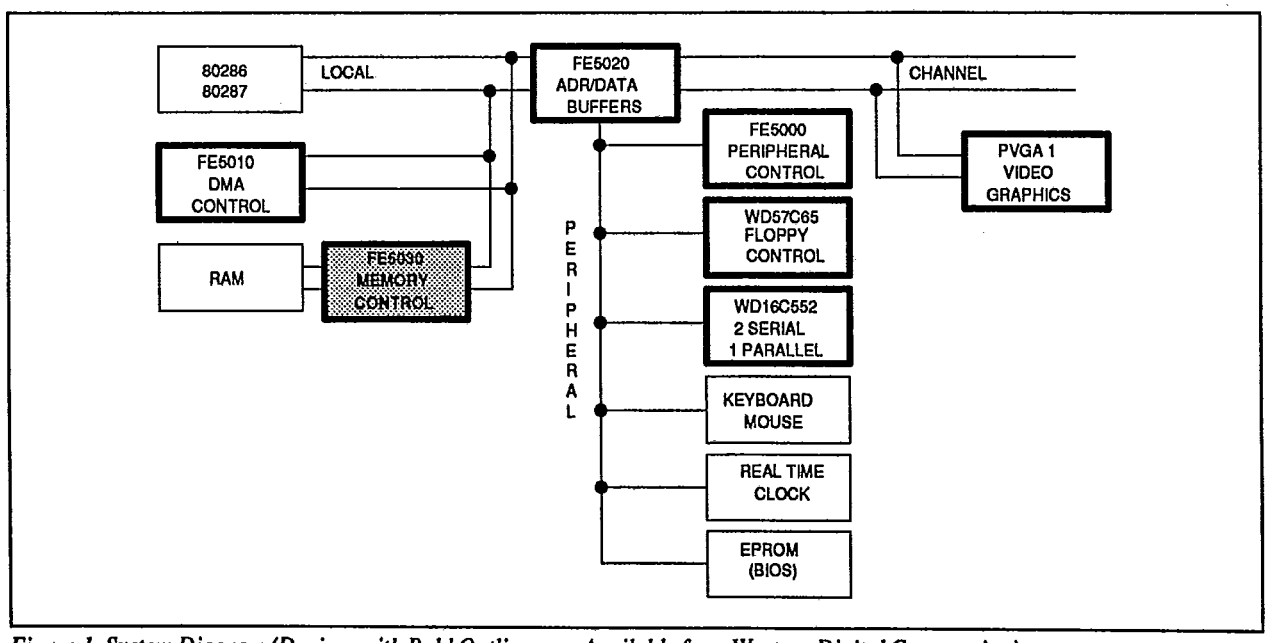

Figure 1. System Diagram (Devices with Bold Outlines are Available from Western Digital Corporation)

Release 1.0

January 31, 1988

Additional References

IBM PS/2 Model 50/60 Technical Reference Manual
Intel Microprocessor and Peripheral Handbook*

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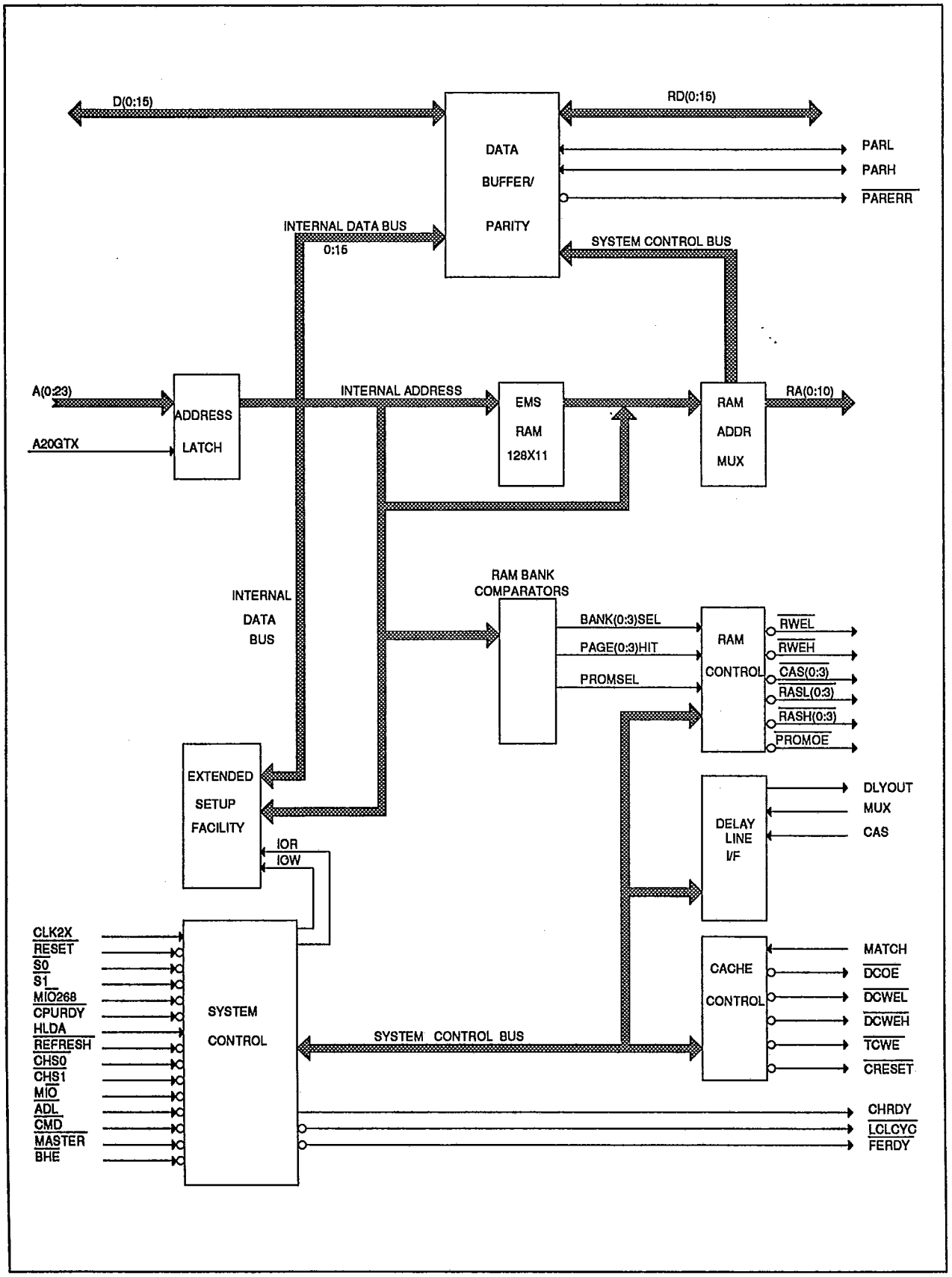


Figure 2. FE5030 Block Diagram

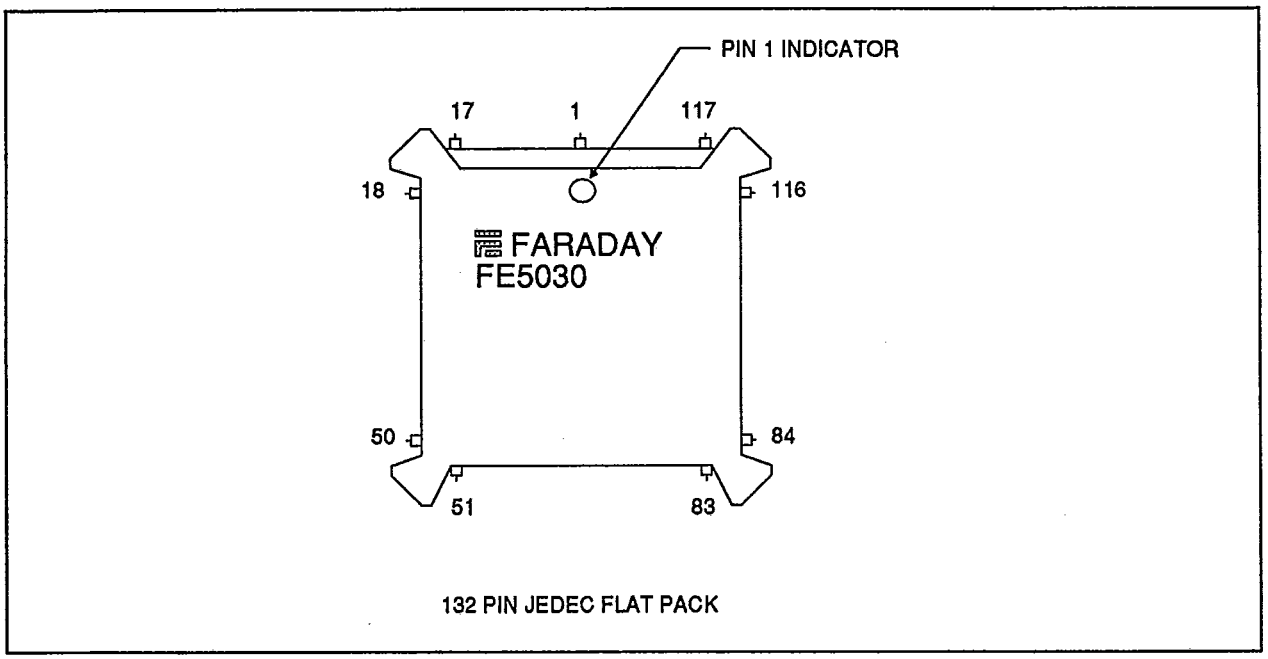


Figure 3. Pin Diagram

PIN – NAME	PIN – NAME	PIN – NAME	PIN – NAME
1 – A0	34 – RD6	67 – RA5	100 – D8
2 – A1	35 – RD7	68 – RA4	101 – $V_{DD}2$
3 – A2	36 – RD8	69 – $V_{SS}6$	102 – D7
4 – A3	37 – RD9	70 – RA3	103 – D6
5 – A4	38 – RD10	71 – RA2	104 – D5
6 – A5	39 – RD11	72 – RA1	105 – D4
7 – A6	40 – RD12	73 – $V_{SS}5$	106 – D3
8 – A7	41 – RD13	74 – RA0	107 – D2
9 – A8	42 – RD14	75 – $V_{DD}3$	108 – D1
10 – A9	43 – $V_{DD}5$	76 – PARH	109 – D0
11 – A10	44 – RD15	77 – PARL	110 – $V_{SS}1$
12 – A11	45 – $V_{SS}10$	78 – $\overline{WREH}$	111 – DLYOUT
13 – A12	46 – $\overline{CAS0}$	79 – $\overline{WREL}$	112 – $\overline{CAS}$
14 – A13	47 – $\overline{CAS1}$	80 – $\overline{TCWE}$	113 – MATCH
15 – A14	48 – $\overline{CAS2}$	81 – $\overline{DCWEH}$	114 – MUX
16 – A15	49 – $\overline{CAS3}$	82 – $\overline{DCWEL}$	115 – $\overline{CMD}$
17 – $V_{SS}12$	50 – $V_{SS}9$	83 – $V_{SS}4$	116 – $V_{DD}1$
18 – A16	51 – $\overline{RASL0}$	84 – $\overline{CRESET}$	117 – $\overline{ADL}$
19 – A17	52 – $\overline{RASL1}$	85 – $\overline{PARERR}$	118 – $\overline{MIO}$
20 – A18	53 – $\overline{RASL2}$	86 – $\overline{PROMOE}$	119 – $\overline{CHS1}$
21 – A19	54 – $\overline{RASL3}$	87 – CHRDY	120 – $\overline{CHS0}$
22 – A20	55 – $\overline{RASH0}$	88 – $\overline{FERDY}$	121 – $\overline{REFRESH}$
23 – A21	56 – $\overline{RASH1}$	89 – $\overline{DCOE}$	122 – $\overline{MASTER}$
24 – A22	57 – $\overline{RASH2}$	90 – $\overline{LCLYC}$	123 – A2OGTX
25 – A23	58 – $V_{DD}4$	91 – $V_{SS}3$	124 – $\overline{MIO}$286
26 – $V_{SS}11$	59 – $\overline{RASH3}$	92 – D15	125 – $\overline{S1}$
27 – RD0	60 – $V_{SS}8$	93 – D14	126 – $\overline{S0}$
28 – $V_{DD}6$	61 – RA10	94 – D13	127 – $\overline{CPURDY}$
29 – RD1	62 – RA9	95 – D12	128 – HLDA
30 – RD2	63 – RA8	96 – D11	129 – $\overline{BHE}$
31 – RD3	64 – RA7	97 – D10	130 – $\overline{RESET}$
32 – RD4	65 – $V_{SS}7$	98 – D9	131 – CLK2X
33 – RD5	66 – RA6	99 – $V_{SS}2$	132 – $V_{SS}12$

1.0 PIN DESCRIPTION

PIN NO.	NAME	TYPE	FUNCTION
109	D0	I/O	DATA—These signals are the local data bus signals connected to the CPU.
108	D1		
107	D2		
106	D3		
105	D4		
104	D5		
103	D6		
102	D7		
100	D8		
98	D9		
97	D10		
96	D11		
95	D12		
94	D13		
93	D14		
92	D15		
1	A0	I	ADDRESS—These signals are the local address bus signals connected to the CPU.
2	A1		
3	A2		
4	A3		
5	A4		
6	A5		
7	A6		
8	A7		
9	A8		
10	A9		
11	A10		
12	A11		
13	A12		
14	A13		
15	A14		
16	A15		
18	A16		
19	A17		
20	A18		
21	A19		
22	A20		
23	A21		
24	A22		
25	A23		
129	$\overline{BHE}$	I	$\overline{BUS\ HIGH\ ENABLE}$—This signal and A0 indicates which byte(s) of data are being transferred on the data bus. 80286 Interface: $\overline{BHE}$ / A0 / FUNCTION 0 / 0 / Word transfer 0 / 1 / Byte transfer on upper byte (8:15) 1 / 0 / Byte transfer on lower byte (0:7) 1 / 1 / Will not occur

O = Output, I = Input, I/O = Bidirectional

PIN NO.	NAME	TYPE	FUNCTION
126 125 124	$\overline{S0}$ $\overline{S1}$ M$\overline{IO}$286	I	$\overline{BUS\ CYCLE\ STATUS}$—These three lines from the system CPU encode the bus cycle type information. 80286 Interface: M$\overline{IO}$286 $\overline{S1}$ $\overline{S0}$ TYPE 0 0 1 I/O Read 0 1 0 I/O Write 1 0 1 Memory Read 1 1 0 Memory Write
131	CLK2X	I	SYSTEM CLOCK—This signal from the FE5010 provides fundamental timing.
127	$\overline{CPURDY}$	I	$\overline{CPU\ READY}$—This signal connects to the 80286 Ready line.
128	HLDA	I	HOLD ACKNOWLEDGE—This signal indicates a CPU HOLD. 80286 Interface: System Interface
123	A20GTX	I	ADDRESS 20 GATE—controls A20 enable.
86	$\overline{PROMOE}$	I	$\overline{PROM\ ENABLE}$—This signal is connected to the BIOS EPROM.
130	$\overline{RESET}$	I	$\overline{SYSTEM\ RESET}$—This signal is the system power-on reset (POR).
121	$\overline{REFRESH}$	I	$\overline{REFRESH}$—This signal indicates a system refresh.
85	$\overline{PARERR}$	O	$\overline{PARITY\ ERROR}$—This output is generated when a read to DRAM generates erroneous data.
90	$\overline{LCLCYC}$	O	$\overline{LOCAL\ CYCLE}$—This signal indicates an access to the FE5030 RAM, PROM, or register.
88	$\overline{FERDY}$	O	$\overline{FE\ READY}$—This signal is generated to end a CPU access to the FE5030 RAM or ESF registers.
87	CHRDY	O	CHANNEL READY—This signal is generated to end a channel access to the FE5030 RAM.
122	$\overline{MASTER}$	I	$\overline{MASTER}$—This signal indicates a Channel master operation.
120 119 118	$\overline{CHS0}$ $\overline{CHS1}$ M$\overline{IO}$	I	$\overline{SYSTEM\ BUS\ STATUS}$—These signals indicate the Channel status. 80286 Interface: M$\overline{IO}$ S0 S1 FUNCTION 1 0 1 Memory Write 1 1 0 Memory Read
117	$\overline{ADL}$	I	$\overline{ADDRESS\ DECODE\ LATCH}$—This signal indicates a valid address on the Channel.
115	$\overline{CMD}$	I	$\overline{COMMAND}$—This signal defines when data is valid on the Channel.
27 29 30 31 32 33 34 35 36 37 38 39 40 41 42 44	RD0 RD1 RD2 RD3 RD4 RD5 RD6 RD7 RD8 RD9 RD10 RD11 RD12 RD13 RD14 RD15	I/O	RAM DATA BUS—These signals are connected to the data pins of all the DRAMs.

O = Output, I = Input, I/O = Bidirectional

PIN NO.	NAME	TYPE	FUNCTION
77	PARL	I/O	PARITY DATA LOW BYTE—This signal is the data parity low byte.
76	PARH	I/O	PARITY DATA HIGH BYTE—This signal is the data parity high byte.
74 72 71 70 68 67 66 64 63 62 61	RA0 RA1 RA2 RA3 RA4 RA5 RA6 RA7 RA8 RA9 RA10	O	RAM ADDRESS—This signal is connected to the RAM address lines.
46 47 48 49	$\overline{CAS0}$ $\overline{CAS1}$ $\overline{CAS2}$ $\overline{CAS3}$	O	$\overline{COLUMN\ ADDRESS\ STROBE}$—This signal is connected to Banks 0, 1, 2, and 3 of DRAM.
51 52 53 54	$\overline{RASL0}$ $\overline{RASL1}$ $\overline{RASL2}$ $\overline{RASL3}$	O	$\overline{ROW\ ADDRESS\ STROBE\ LOW}$—These signals are connected to the low byte of Banks 0–3 of DRAM.
55 56 57 59	$\overline{RASH0}$ $\overline{RASH1}$ $\overline{RASH2}$ $\overline{RASH3}$	O	$\overline{ROW\ ADDRESS\ STROBE\ HIGH}$—These signals are connected to the high byte of Banks 0–3 of DRAM.
78 79	$\overline{WREH}$ $\overline{WREL}$	O	$\overline{WRITE\ ENABLE}$—The signals are connected to the WE pin of the DRAM array.
111	DLYOUT	O	DELAY LINE OUT—This signal is the sync signal to the delay line.
114	MUX	I	ADDRESS MULTIPLEX—This signal sets the RAS/CAS address mux time.
112	$\overline{CAS}$	I	$\overline{CAS}$—This signal sets CAS active time from RAS.
89	$\overline{DCOE}$	O	$\overline{DATA\ CACHE\ OUTPUT\ ENABLE}$—This signal controls the output enable of the data cache SRAMs.
82	$\overline{DCWEL}$	O	$\overline{DATA\ CACHE\ WRITE\ ENABLE\ LOW}$—This signal writes data to the low data byte of the data cache.
81	$\overline{DCWEH}$	O	$\overline{DATA\ CACHE\ WRITE\ ENABLE\ HIGH}$—This signal writes data to the high data byte of the data cache.
80	$\overline{TCWE}$	O	TAG CACHE WRITE ENABLE—This signal writes address information to the tag cache SRAM.
113	MATCH	I	TAG RAM MATCH—This signal is an input from the tag RAM that indicates a cache hit from the tag cache SRAM.
84	$\overline{CRESET}$	O	$\overline{CACHE\ RESET}$—This signal sets all addresses of the tag RAM to a non-match condition. It is generated by a system reset or by a software controlled bit in ESF:1F.
28, 43, 58, 75, 101, 116	V_{DD}	I	+5V Power Supply

O = Output, I = Input, I/O = Bidirectional

PIN NO.	NAME	TYPE	FUNCTION
17, 26, 45, 50, 60, 65, 69, 73, 83, 91, 99, 110, 132	Vss	I	0V Ground

O = Output, I = Input, I/O = Bidirectional

2.0 DRAM CONTROLLER

2.1 Memory Organization

The FE5030 organizes memory into four banks of sixteen bits each (see Figure 4). Total size is dependent on the type of memory used and the number of banks populated (see Table 1). Each bank can have a different type of RAM for maximum versatility.

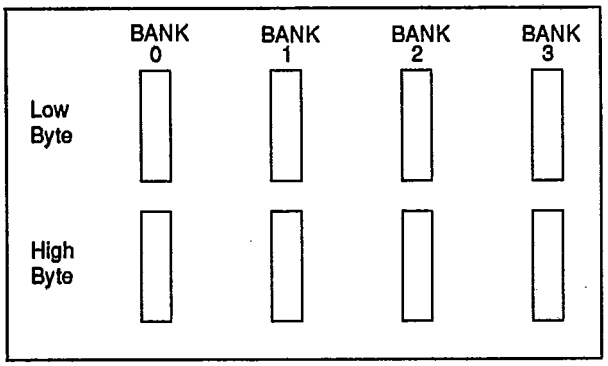


Figure 4. Memory Bank Organization

MEMORY TYPE	SIZE
256K x 1	512K, 1MB, 1.5MB, 2MB
1Mb x 1	2MB, 4MB, 6MB, 8MB
4Mb x 1	8MB, 16MB

Table 1. Memory Size Options vs. Memory Type

Each bank can be enabled or disabled by programming bits in the memory configuration registers ESF:16 ESF:1C. In addition, banks can be swapped in order to map around one or more defective banks.

2.1.1 Memory Map

Figure 5 shows the memory map for the system architecture. The first 640K is system RAM. Additional banks of RAM are mapped in contiguous blocks, starting at 1MB. The 384K of extra RAM from the first 1MB is the Split RAM. It is remapped to the top of the last block of memory on the system board after the BIOS software determines the total memory size.

The software can copy the EPROM to a 128K segment of the Split RAM for faster code execution. The segment is then mapped into the PROM area (E0000H–FFFFFH) and the EPROM is disabled. In this case, the SRBR value is decreased by 128K.

2.1.2 Memory Configuration

Figure 6 provides details of the RAM Control Register (ESF:16) format, Bits 0 through 8 of which are used to program the RAM type in each bank. The programming is done by the BIOS at power-up. Enabling Page mode results in better performance; enabling Interleaved Mode ensures an even higher performance. Interleaved banks must have the same RAM type for proper operation.

The Shadow RAM feature on the FE5030 speeds up BIOS execution by moving the BIOS EPROM code to the top of Split Memory and setting the Swap Bit (Bit 12) to active. This enables the RAM and disables the EPROM at Location E000H. The area can then be write-protected by setting Bit 13 of the RAM Control Register.

The four boundary registers illustrated in Figure 7, ESF:17–ESF:1A, can locate each of the four memory banks on a 512K address boundary. The registers can also be used to map out a defective memory map. All memory above 1 Mb must be contiguous. Banks that are populated with the largest RAM type must be located first on the memory map.

After the BIOS has determined the total RAM addressed by the FE5030, it can calculate the address at which to locate the split memory. This address is loaded into ESF:1B, illustrated in Figure 8. For example, if the BIOS finds 2 Mb of DRAM, ESF:1B would be loaded with the value 04H (2 Mb). Bit 5 of the register is then set to enable the split RAM area.

The SRBR register (ESF:1C) defines the upper limit of the DRAM addressed by the FE5030. In the case of the example above, the SRBR register would be loaded with the value 13H (2.384 Mb).

To disable the DRAM entirely, load the System Board Setup Register (Port 94H) with the value 80H. This allows the System RAM Enable Register (Port 103H) to be altered. Bit 1 can then be set to disable all FE5030 RAM. Figure 9 depicts both these registers.

2.1.3 Page Mode

Page Mode operation permits fast access to 512-byte, 1Kb, or 2Kb locations (depending on the memory type) within a single RAS active cycle. Any location within the page can be accessed by strobing the new CAS address. Since a CAS access is much faster than a normal RAS/CAS cycle, wait states can be saved for a program executing within the page.

Interleaving in page mode increases the number of page "hits", thus improving performance. It does this by allowing each bank to have its own page. New page locations are determined by the state of address bits 10, 11 or 12, depending on RAM type. This increases the probability that a program can execute out of multiple page localities.

Page sizes for different RAM types are shown below.

256K DRAMs — 512-byte page
1MB DRAMs — 1K-byte page
4MB DRAMs — 2K-byte page

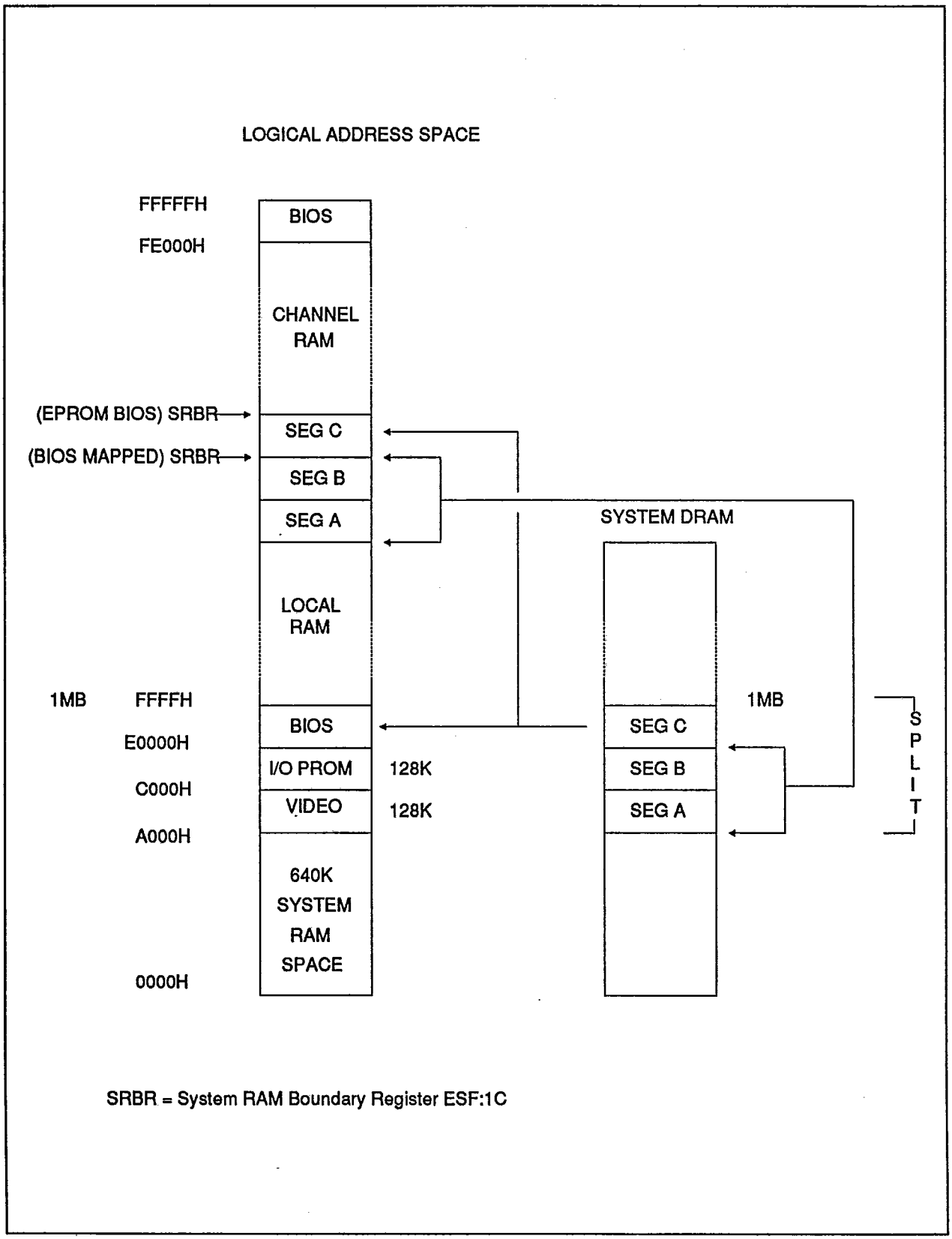


Figure 5. System RAM Address Map

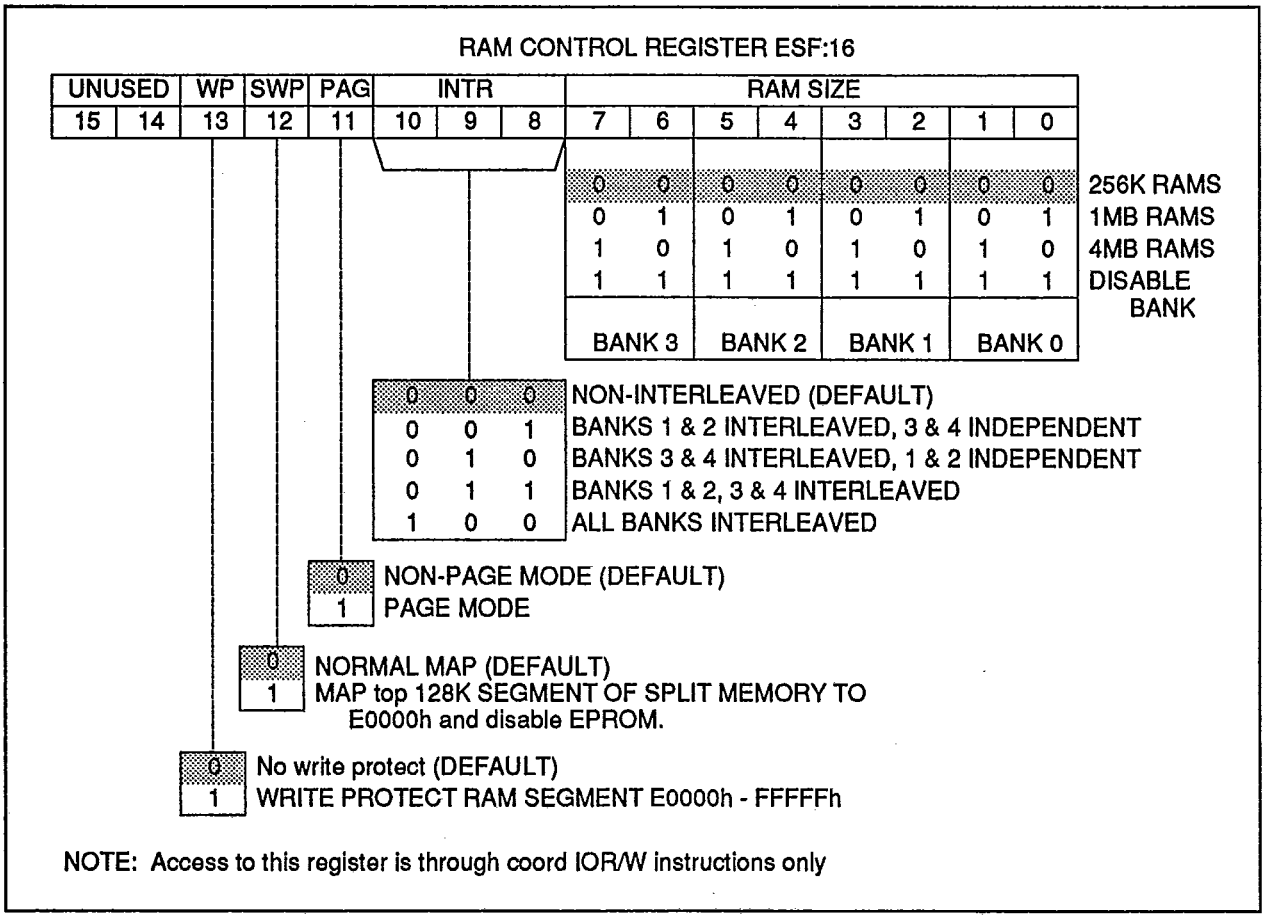


Figure 6. RAM Control Register Format

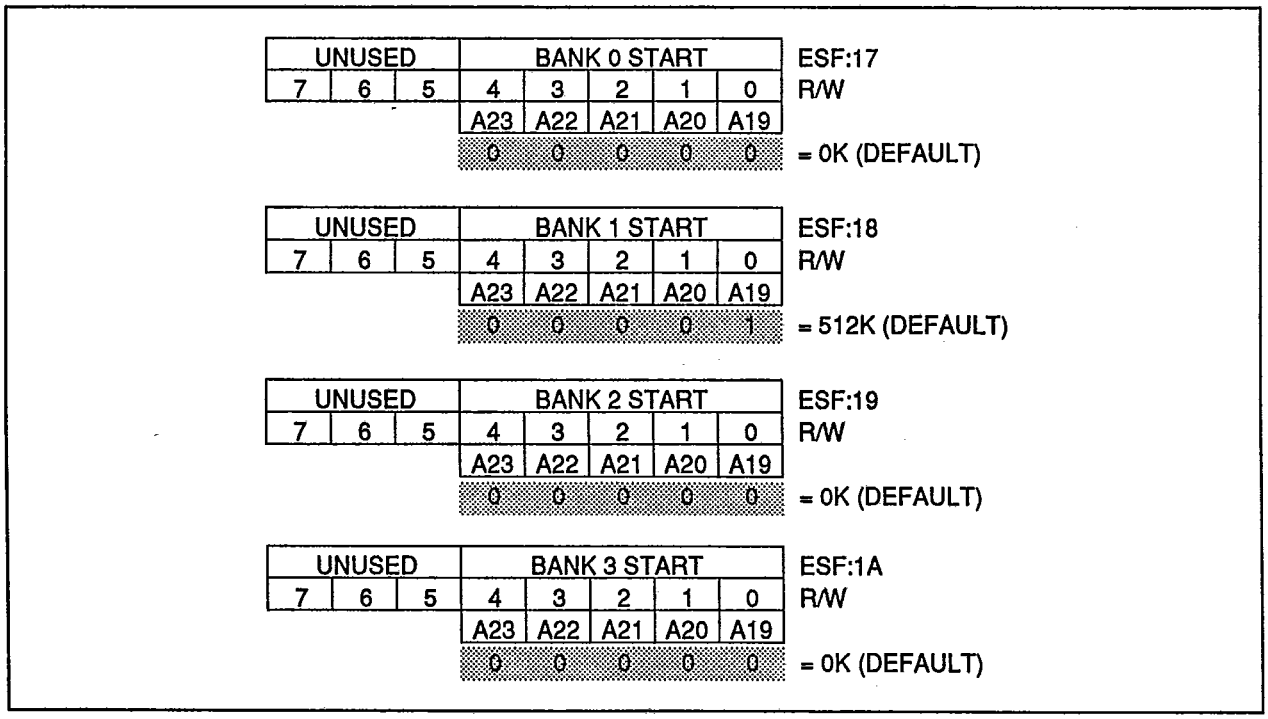


Figure 7. Bank Boundary Registers Format

UNUSED		SPLIT MEMORY ADDRESS						ESF:1B
7	6	5	4	3	2	1	0	R/W
		EN	A23	A22	A21	A20	A19	
		1	0	0	0	1	0	= 1M (DEFAULT) 22h

A19 - A23: Selects address to address to locate 384K split address.

SRBR ESF:1C

	A23	A22	A21	A20	A19	A18	A17	R/W
7	6	5	4	3	2	1	0	
0	0	0	0	1	0	1	1	DEFAULT = OBh (1.384M)

A17 - A23 Defines the top RAM Address of the the 5030. All RAM Memory accessed above this will be directed to the channel.

Figure 8. Split Memory Address Register Format/SRBR Register

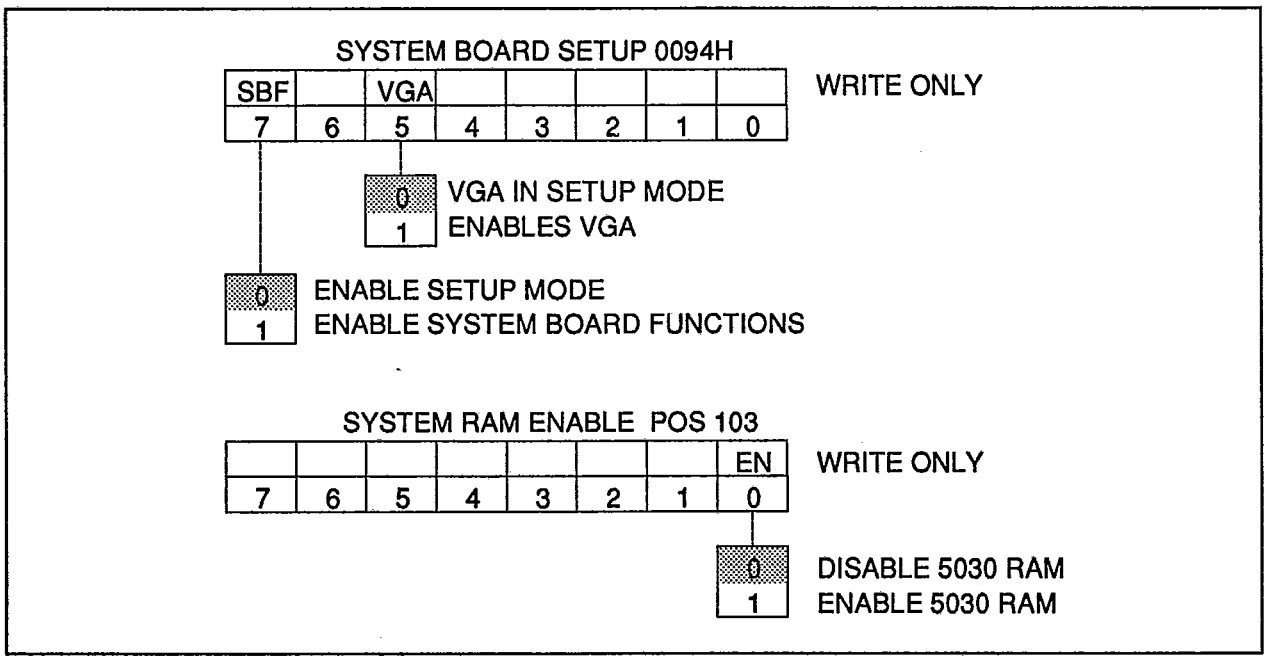


Figure 9. RAM Enable Function

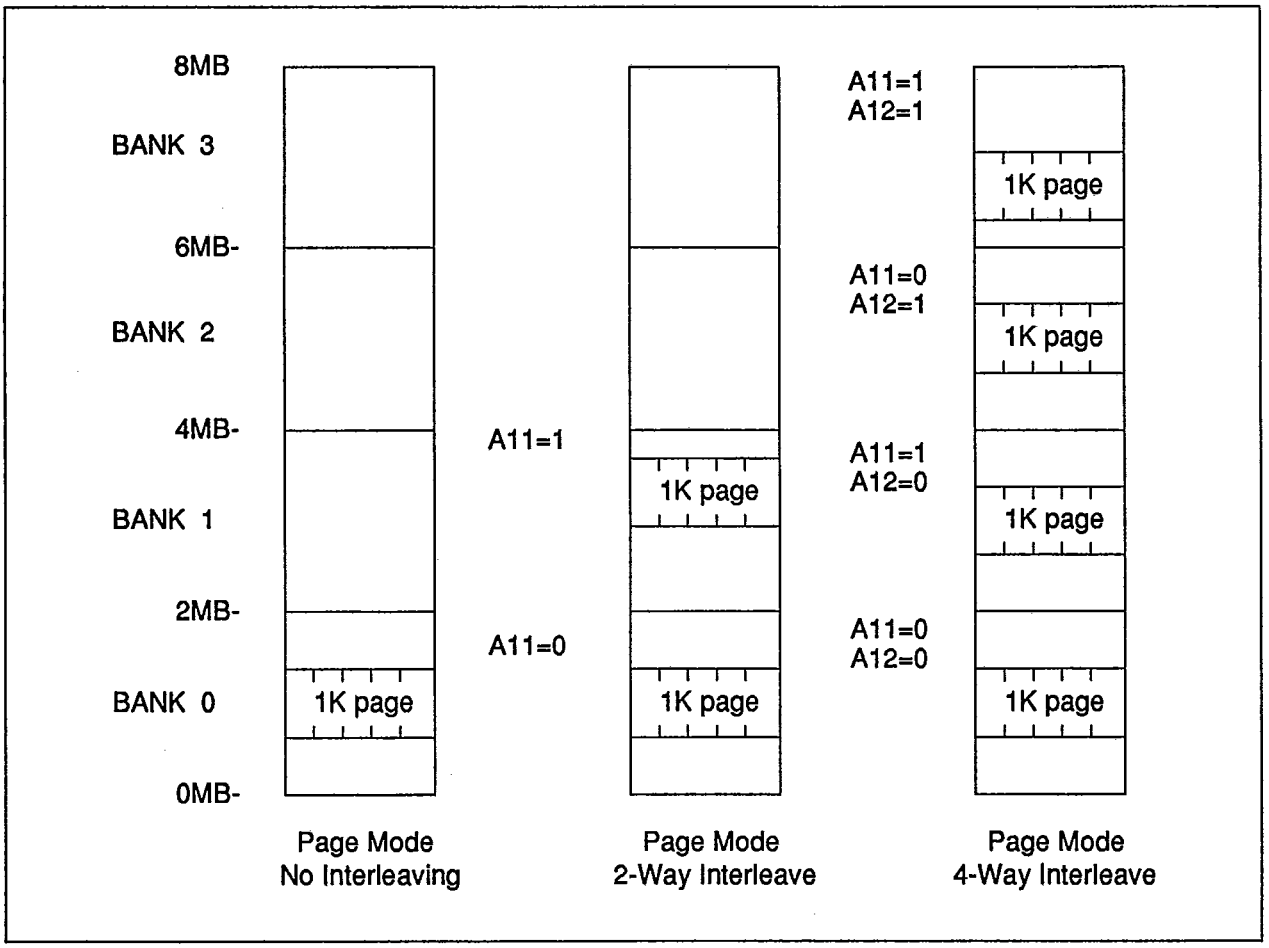


Figure 10. 8MB Interleaved Page Mode (IMB DRAM Example)

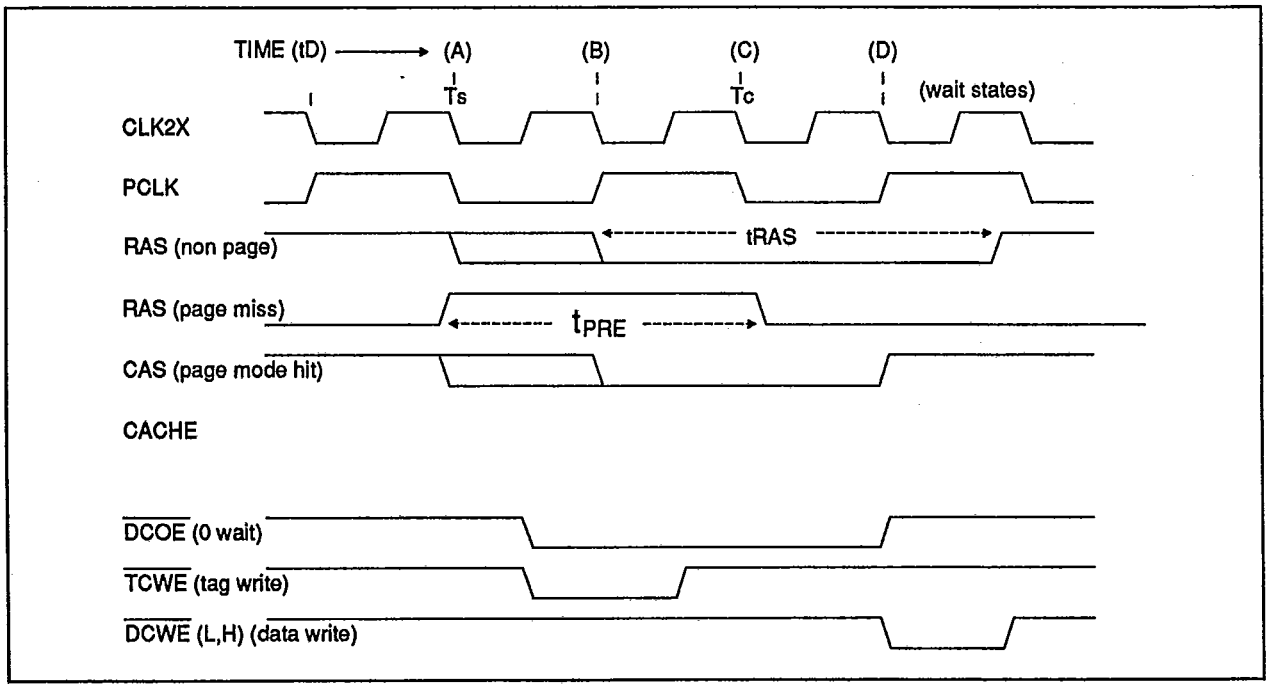


Figure 11. Programmable DRAM Timing

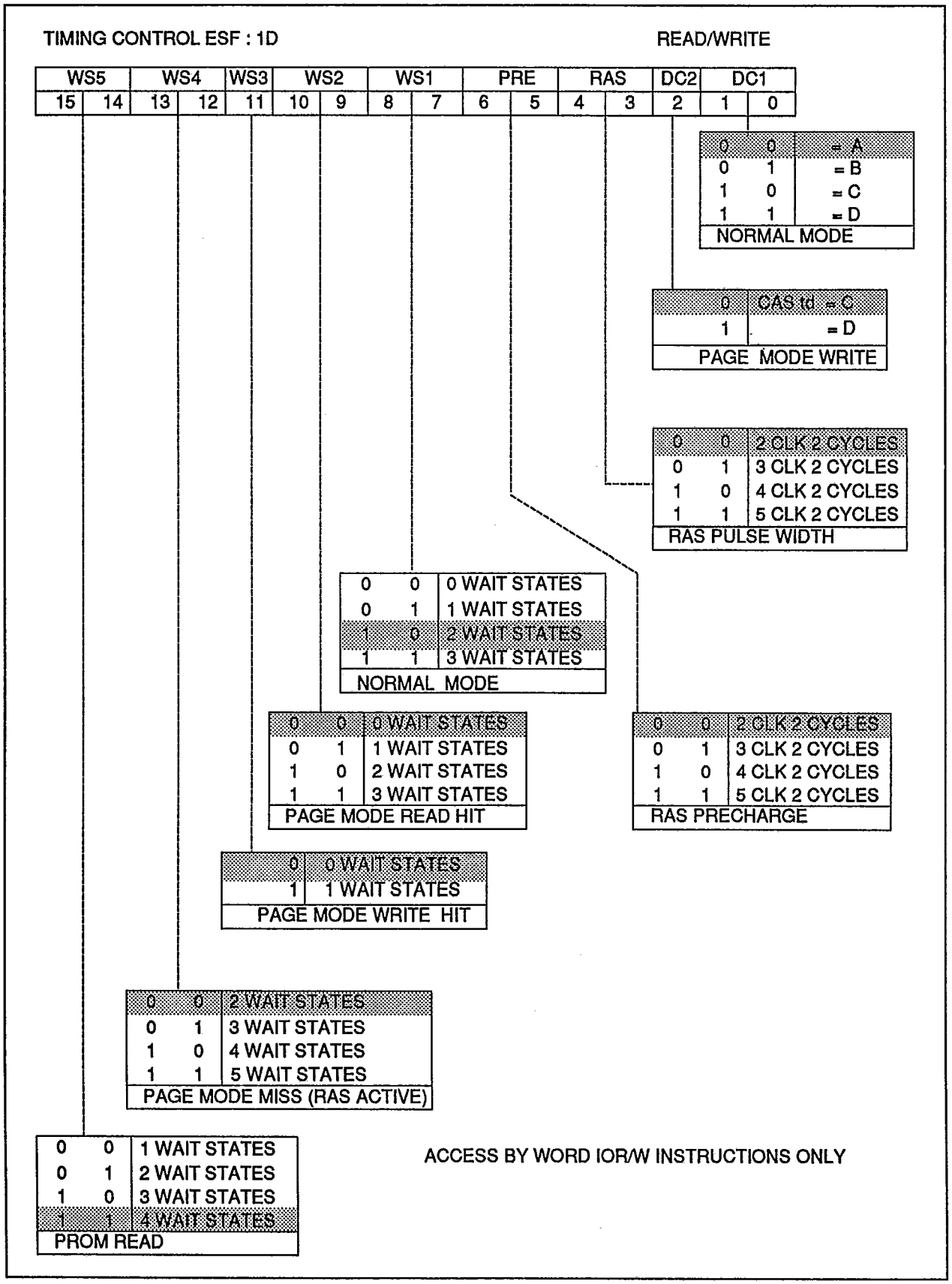


Figure 12. Timing Control Register Format

2.2 Timing Control

The FE5030 uses a combination of programmable clocked and delay line timings. This ensures optimum performance at different CPU and memory speeds. Table 2 lists the recommended program parameters at different CPU speeds.

	CPU SPEED			
	10	12	16	20
DC1–RAS Start Time	A	B	B	B
DC2–Page Write CAS Start Time	C	C	C	C
RAS–RAS Pulse Width	2	3	3	4
PRE–RAS Precharge Time	2	2	3	4
WS1–Normal Mode Wait States	0	1	2	2
WS2–Page Mode Read Hit Wait States	0	0	0	1
WS3–Page Mode Write Hit Wait State	0	0	1	1
WS4–Page Mode Miss Wait States	1	1	2	3

Table 2. Typical RAM Program Parameters

All other parameters must be calculated at the appropriate CPU frequency and RAM specification. Table 3 shows the delay line tap selections for a 100ns DRAM. These are hardwired outside the FE5030, typically using a 50ns 10-tap delay line.

PIN	FUNCTION	TIME	TAP
DLYOUT	Reference out	0	—
MUX	RAS/CAS address mux	30	10
$\overline{CAS}$	Read CAS assertive	60	30

Table 3. Delay Line Timing

2.3 Performance

Table 4 shows memory performance (in wait states) over a range of CPU processor speeds and memory modes. The performance values shown are based on the following assumptions about the RAM specifications:

CPU SPEED	MEMORY MODE	READ WAIT STATES
10 Mhz	normal	0
	page (Hit)	—
	cache (Hit)	—
12 Mhz	normal	1
	page (Hit)	0
	cache (Hit)	0
16 Mhz	normal	2
	page (Hit)	0
	cache (Hit)	0
20 Mhz	normal	2
	page (Hit)	1
	cache (Hit)	0

Table 4. Memory Performance Table

ESF:1D is used to configure timing for the selected DRAM type, as Figures 11 and 12 illustrate. The shaded areas in the timing control register parameters in Figure 12 represent the default values at power-up. The BIOS software must program them to meet the specifications of the installed RAMs. The Page Mode Write Hit parameter (Bit 11) must be set at one. Parameters DC1 and DC2 specify the clock cycle at which the RAS/CAS signals become assertive. Determined by internal delays of the FE5030, the parameter timings are as follows:

DC1 = A 10 MHz, 12 MHz
B 16 MHz, 20 MHz, EMS enabled at 10 MHz
C EMS enabled at 12 MHz, 16 MHz
D EMS enabled at 20 MHz

DC2 = C All normal cycles
D All EMS cycles

- 100 ns RAM access time
- 40 ns page access time
- 80 ns RAS precharge time
- 35 ns Data cache access time

Table 5 shows the effect of different RAM speeds on performance, measured in wait states.

CPU SPEED	DRAM SPEED	NORMAL W. S.	WAIT STATES (Page Mode)
10 MHz	100 ns	0	—
12 MHz	70 ns	0	—
12 MHz	100 ns	1	.8
16 MHz	120 ns	2	1.2
16 MHz	80 ns	1	.8
20 MHz	100 ns	2	1.6

Table 5. RAM Speeds and Performance

2.4 DRAM Interface

The FE5030 directly controls eight SIMM modules without external buffers. Series-terminating resistors should be used for the RAS, CAS, and WE lines to the DRAMS. External buffers could prove useful to decrease the address propagation delay (MA0–MA10) time at high speeds.

Figure 13 describes the multiplexed output of the FE5030. Note that some address bits are not used for the larger DRAM sizes

2.5 Extended Memory Subsystem (EMS) Control

Programs that operate in the Real Mode (less than 1MB), can use EMS mapping to make use of up to 16MB of DRAM. The FE5030 supports EMS LIM 4.0 when the device driver is loaded under DOS.

When EMS Mode is enabled (see Figure 14), the lower 640K of DRAM is remapped into 16MB of physical memory. This is done by dividing the 1MB Real Mode range into 64 16k segments called page frames; an EMS Page Register is associated with each page frame (see

MEMORY MODE	MUX	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
256K DRAM ADDRESS MULTIPLEXER CONFIGURATION												
Normal	RAS	NA	NA	A9	A8	A7	A6	A5	A4	A3	A2	A1
	CAS	NA	NA	A12	A11	A10	A18	A17	A16	A15	A14	A13
Page Mode	RAS	NA	NA	A12	A11	A10	A18	A17	A16	A15	A14	A13
	CAS	NA	NA	A9	A8	A7	A6	A5	A4	A3	A2	A1
Page Mode 2-Way Intlv	RAS	NA	NA	A12	A11	A19	A18	A17	A16	A15	A14	A13
	CAS	NA	NA	A9	A8	A7	A6	A5	A4	A3	A2	A1
Page Mode 4-Way Intlv	RAS	NA	NA	A12	A20	A19	A18	A17	A16	A15	A14	A13
	CAS	NA	NA	A9	A8	A7	A6	A5	A4	A3	A2	A1
1MB DRAM ADDRESS MULTIPLEXER CONFIGURATION												
Normal	RAS	NA	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	CAS	NA	A20	A12	A11	A19	A18	A17	A16	A15	A14	A13
Page Mode	RAS	NA	A20	A12	A11	A19	A18	A17	A16	A15	A14	A13
	CAS	NA	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
Page Mode 2-Way Intlv	RAS	NA	A20	A12	A21	A19	A18	A17	A16	A15	A14	A13
	CAS	NA	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
Page Mode 4-Way Intlv	RAS	NA	A20	A22	A21	A19	A18	A17	A16	A15	A14	A13
	CAS	NA	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
4MB DRAM ADDRESS MULTIPLEXER CONFIGURATION												
Normal	RAS	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
	CAS	A22	A20	A12	A21	A19	A18	A17	A16	A15	A14	A13
Page Mode	RAS	A22	A20	A12	A21	A19	A18	A17	A16	A15	A14	A13
	CAS	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
Page Mode 2-Way Intlv	RAS	A23	A20	A22	A21	A19	A18	A17	A16	A15	A14	A13
	CAS	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
Page Mode 4-Way Intlv	RAS					NA						
	CAS					NA						
256K, 1MB, 4MB REFRESH ADDRESSES												
Refresh	RAS	A10	A9	A0	A8	A7	A6	A5	A4	A3	A2	A1

Figure 13. RAM Address Multiplexer

Figure 15). When enabled, a 24-bit real address is formed by taking the 10-bit address from the page register (A14–A23) and appending the 14-bit lower address. The resulting 24-bit address is then used to access up to 16MB of memory. See Figure 16 for an illustration of EMS mapping.

Multi-tasking programs are supported by loading the alternate (Set B) page register. This is done by enabling the MAP bit in the EMS Control Register.

2.6 Cache Controller

To ensure the best possible performance at higher speeds, the FE5030 supports an external cache of any size, with direct-mapped, write-through architecture. When the cache is enabled, all DRAM memory locations addressed by the FE5030 are mapped to the cache. The BIOS is not cached, except when the shadow RAM is enabled. The cache does not operate in EMS Memory Mode.

Performance versus cache size is shown in the chart below, assuming zero wait states for a hit, and two wait states for a normal RAM cycle. These figures are approximate, and may vary with the software being run.

CACHE SIZE	HIT RATE	AVG. WAIT STATES
16K byte	.80	.9
32K byte	.84	.76
64K byte	.88	.72

Table 6 shows the caching algorithm for the FE5030.

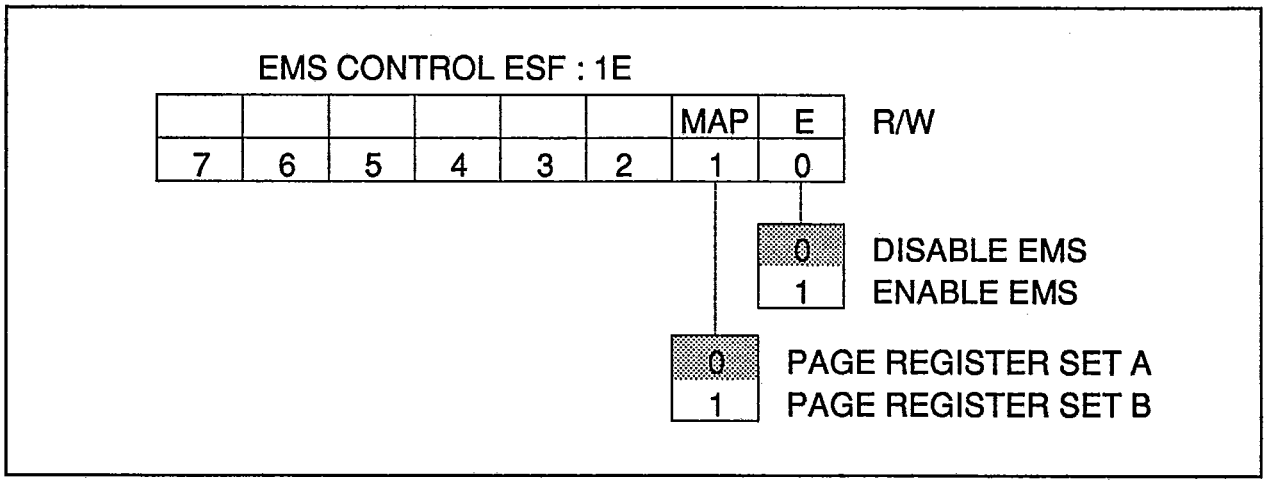


Figure 14. EMS Control Register Format

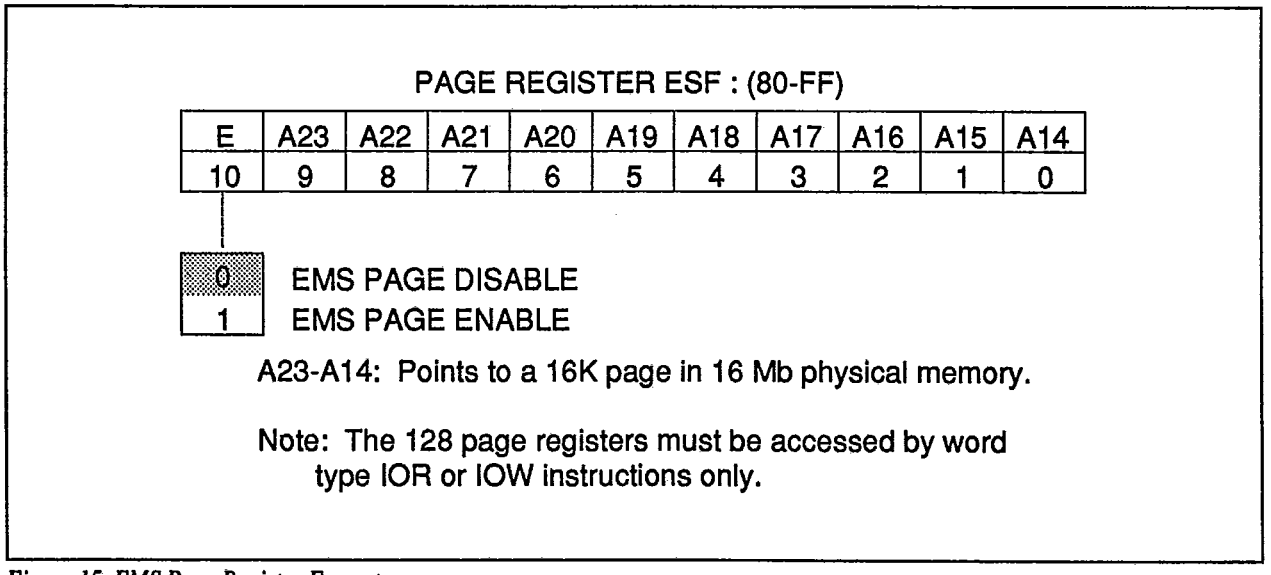


Figure 15. EMS Page Register Format

2.6.1 Cache Design

The external devices needed for the cache are the Tag RAM, Data RAM, and a 16-bit latch for the Data RAM. The Tag RAM would need a 22-bit latch if the "Fast Cache" cycle is not selected. This programmable option allows the tag cache address to be latched before the processor address changes. The SRAM speeds needed to operate at different processor speeds are tabulated to the right. Numbers in parantheses are for the "Fast Cache" option.

CPU	TAG RAM	DATA RAM
16 MHz	35 ns (30 ns)	45 ns
20 MHz	25 ns (25 ns)	35 ns

2.6.2 Cache Initialization

The Tag RAM contains invalid match addresses on power-up. The cache must be initialized by reading consecutive bytes in memory equal to the size of the cache.

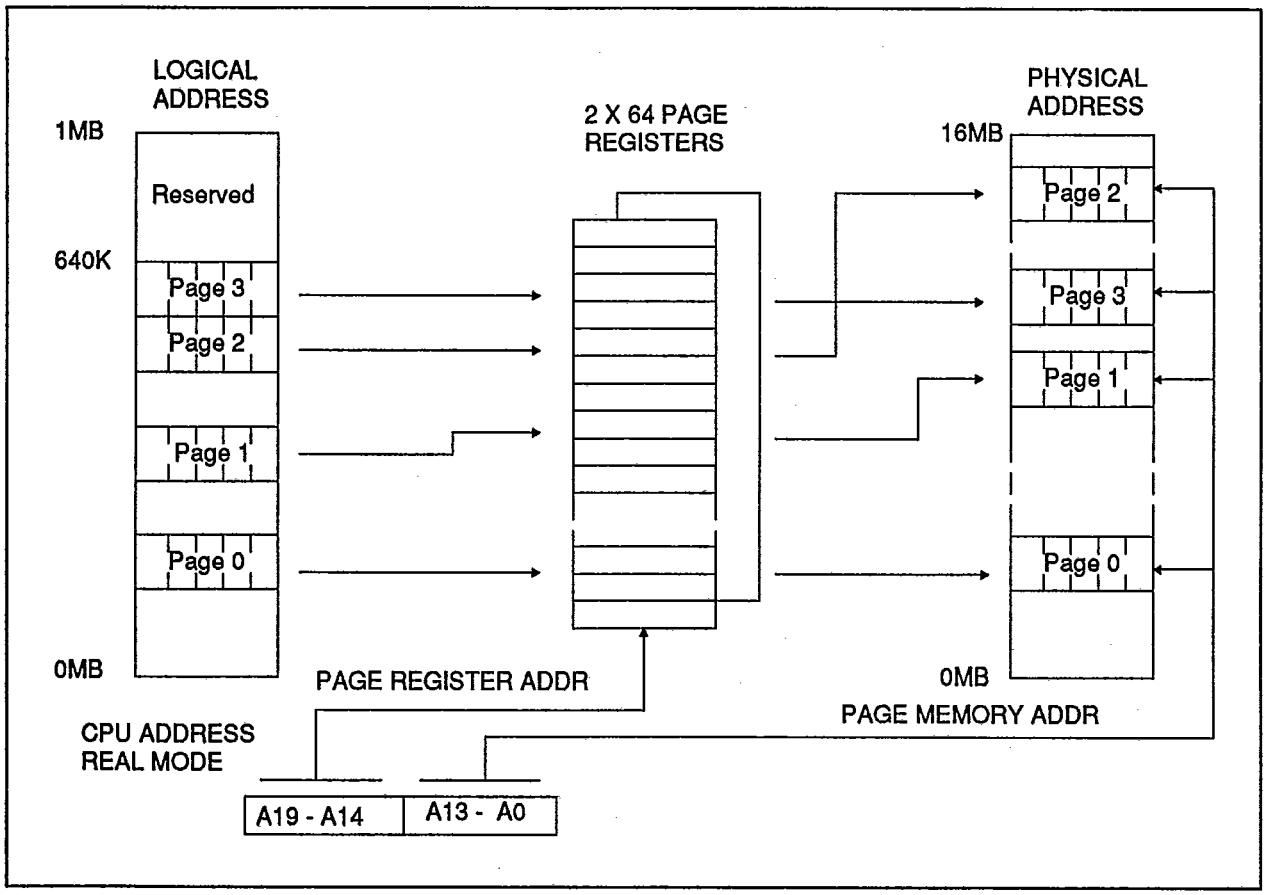


Figure 16. EMS Mapping

OPERATION	HIT/MISS	DRAM	CACHE
CPU Memory Read	HIT MISS	— Read	Read Update
CPU Memory Write	HIT MISS	Write Write	Write —
DMA/MASTER Memory Read	HIT MISS	— Read	Read —
DMA/MASTER Memory Write	HIT MISS	Write Write	Write —
NOTE: "—" represents no operation, EPROM writes are ignored			

Table 6. Cache Algorithm

If the Tag RAM contains a tag reset function, the reset pin on the RAM can be connected to the CRESET pin on the FE5030, and the tags can be reset by an output instruction to the cache control register (ESF:1F). The cache is then enabled by another instruction to ESF:1F. See Figure 17. To test the cache, Bit 2 of the cache control register is set to disable all writes to the cache excepting for read misses, which are still updated. The diagnostic software can then test the integrity of the data cache.

2.7 Extended Setup Facility (ESF)

The ESF is designed to extend the congfiguration architecture established with the POS features. See Figure 18 for an overview of the ESF function.

All communication with setup registers in the FE5030 is accomplished indirectly through the ESF function. To access an ESF register, EAR0 at 0074H and EAR1 at 0075H are loaded with one of the 138 FE5030 ESF addresses (see Table 7). The ESF Pointer Register (EPR) in the FE5030 is loaded with the ESF Data Register (EDR) address which is then used to read or write any of the FE5030 ESF registers. The EPR default value is 0700H.

PORT	REGISTER FUNCTION
0070H	NMI, CMOS Enable
0074H	EAR0
0075H	EAR1
0094H	System Board Setup
0103H	System RAM Enable
EPR	ESF Access (Default = 0700H)
ESF:16	RAM Control
ESF:17	Bank 0 Boundary
ESF:18	Bank 1 Boundary
ESF:19	Bank 2 Boundary
ESF:1A	Bank 3 Boundary
ESF:1B	Split Memory Address
ESF:1C	SRBR
ESF:1D	Timing Control
ESF:1E	EMS Control
ESF:1F	Cache Control
ESF:80-FF	EMS Mode Page Register

Table 7. ESF System Address Map

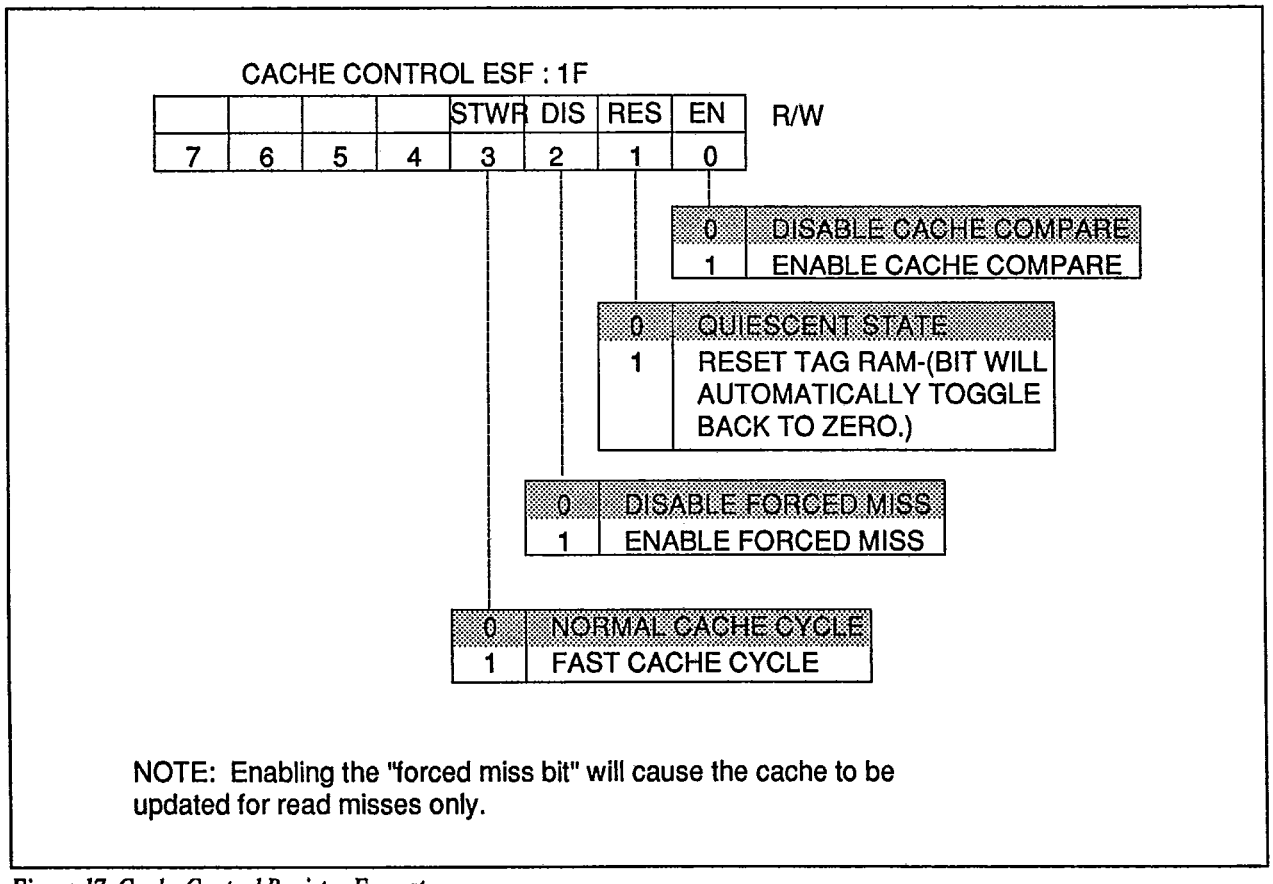


Figure 17. Cache Control Register Format

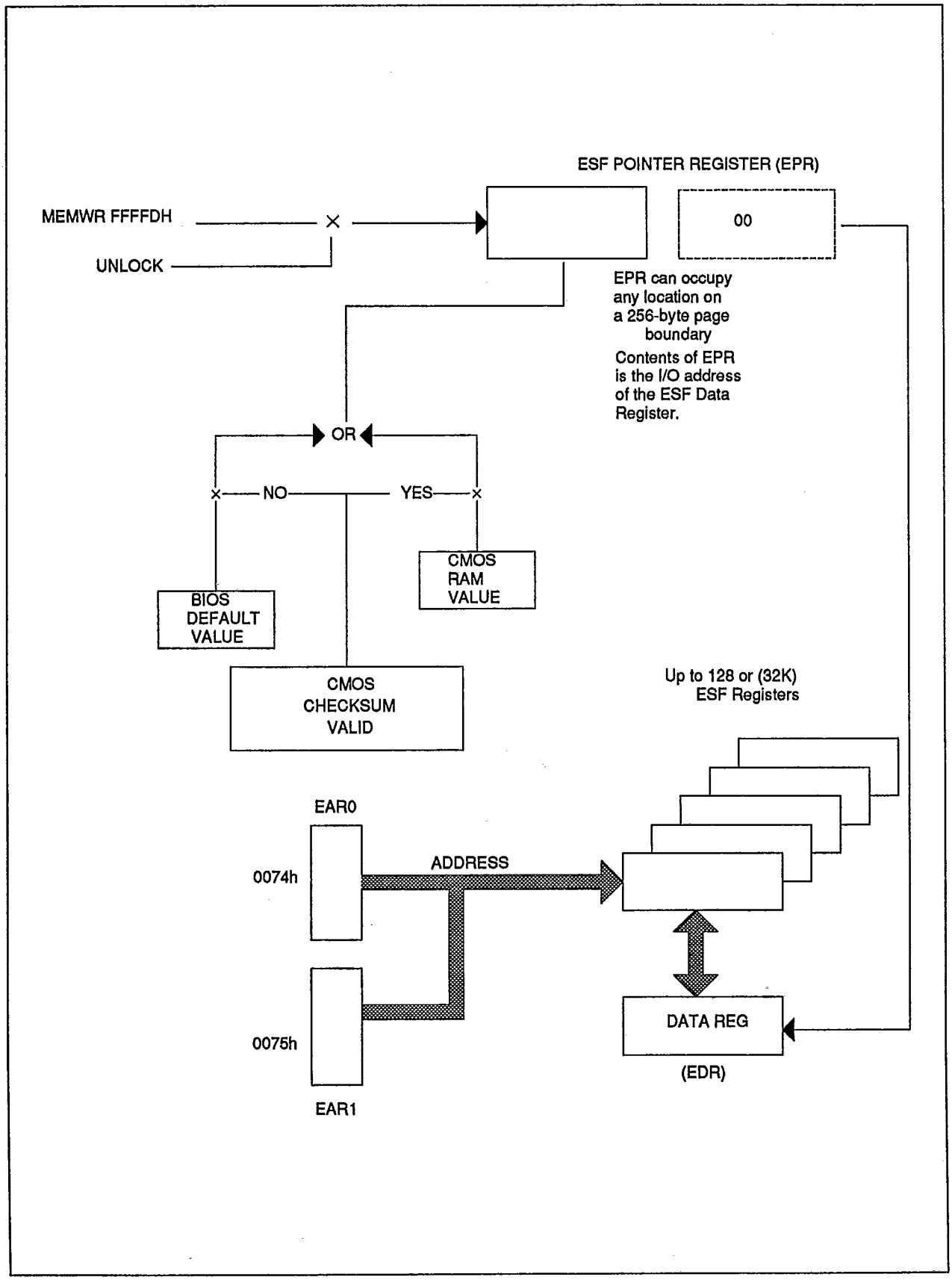


Figure 18. Extended Setup Facility Overview

2.7.1 ESF Access

ESF is based on an "alternate I/O space" concept similar to the way in which IBM implemented their Extended CMOS RAM feature. ESF space (128 locations expandable to 32K) is accessed through a single "real I/O space" window called the ESF Data Register (EDR). ESF space may be implemented as either word or byte-wide, at the discretion of the designer.

The EDR is pointed to by the software-configurable (write-only) ESF Pointer Register (EPR), located in the FE5010 and duplicated in the FE5030. The EPR is loaded by writing to memory location FFFFDH or FFFFFDH (normally PROM). The power-on default location for the EDR is at I/O address 0700H.

The following procedure is recommended to modify the EPR:

1. Set the value 8DH in Port 0070H to disable NMI.

2. Read System Control Port B at 0061H, and test for a change in the state of Bit 4 (Refresh Toggle) to synchronize to the refresh circuitry.

3. Read EAR0 at 0074H (normally write-only) to unlock the EPR.

4. Write the new value into the EPR (FFFFDH). This locks the EPR again.

5. Enable NMI if required.

Note that the EPR is locked when written or on the next refresh cycle, whichever occurs first.

The value in the EPR becomes the new 8-bit address of the EDR. The EDR can reside at any of 256 locations in the 64K I/O space of the CPU from 0400H to FF00H.

To address the ESF I/O space:

1. Write the value 8DH to Port 0070H to disable NMI.

2. Write the address value to EAR0 at 0074H. If expanded ESF is being used, the value should also be written to EAR1.

3. Issue an I/O read or write command to the EDR address. The selected ESF register is determined by decoding the EAR0 (and EAR1) address value. Figure 19 shows the format for EAR0 and EAR1.

2.7.2 ESF Address Map

The lower sixty-four bytes (EAR0 = 00H–3FH) are reserved for Faraday functions and features. The upper sixty-four bytes (EARO = 40H–7FH) are for customer use (see Table 8). All functions using ESF must include Bit 7 in the decode. Bit 7 of EAR0 must be 0 when addressing only 128 ESF registers. To expand the ESF to 32,768 locations, set EAR0 Bit 7 to 1 and write the second ESF address byte to EAR1.

ESF ADDRESS	DEFINITION
00H–0FH	System Reserved
10H–1FH	System board core functions
20H–3FH	System board peripheral functions
40H–7FH	Customer Specified
0080H–FFFFH	Expansion (EAR0 bit 7 must be 1)

Table 8. ESF General Usage Map

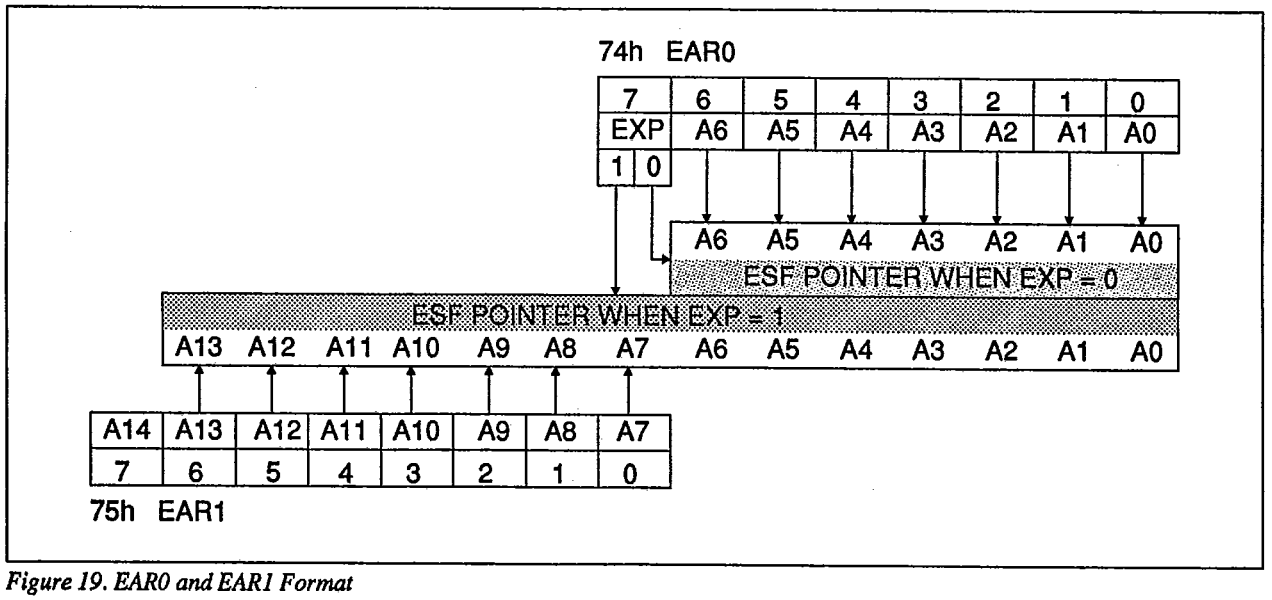


Figure 19. EAR0 and EAR1 Format

3.0 TECHNICAL SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS

These are absolute maximum stress ratings for the device. Permanent device damage can result from exposing the device to conditions exceeding these ratings.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	(V_{DD}–V_{SS})	0	7	V
Input Voltage	V_{IABS}	V_{SS}–0.3	V_{DD}+0.3	V
Bias on Output Pin	V_{OABS}	V_{SS}–0.3	V_{DD}+0.3	V
Storage Temperature	T_S	–40	125	°C

3.2 NORMAL OPERATING CONDITIONS

Exposure of the device to conditions exceeding the normal operating conditions for extended periods of time can affect the long-term reliability of the device.

(V_{SS} = 0 V)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power Supply Voltage	V_{DD}	4.5	5.5	V
Ambient Temperature	T_A	0	70	°C
Input Voltage	V_{IN}	–0.3	V_{DD}+0.3	V
Power Dissipation	P_W	—	TBD	mW
Supply Current	I_{DD}	—	TBD	mA

3.3 DC CHARACTERISTICS (UNDER NORMAL OPERATING CONDITIONS)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Capacitance @ f_C= 1 MHz	C_I	—	10	pF
I/O Capacitance	C_{IO}	—	15	pF
Input Leakage	I_{IL}	—	±10	uA
Tri-state Output Leakage	I_{OL}	—	±30	uA
I/O Pin Leakage	I_{IOL}	—	±40	uA
INPUT CLK2				
Logic High Input Voltage	V_{IH}	3	—	V
Logic Low Input Voltage	V_{IL}	—	0.6	V
ALL OTHER INPUTS				
Logic High Input Voltage	V_{IH}	2.0	—	V
Logic Low Input Voltage	V_{IL}	—	0.8	V
OUTPUTS $\overline{\text{RASL}}$ (0:3), $\overline{\text{RASH}}$ (0:3), $\overline{\text{CAS}}$ (0:3), LCLCYC				
Source Current @ V_{OH} = 2.4 V	I_{OH}	4	—	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	12	—	mA
OUTPUT D (0:15)				
Source Current @ V_{OH} = 2.4 V	I_{OH}	4	—	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	8	—	mA
OUTPUTS $\overline{\text{PARERR}}$ and $\overline{\text{CRESET}}$				
Source Current @ V_{OH} = 2.4 V	I_{OH}	4	—	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	6	—	mA
ALL OTHER OUTPUTS				
Source Current @ V_{OH} = 2.4 V	I_{OH}	1	—	mA
Sink Current @ V_{OL} = 0.4 V	I_{OL}	4	—	mA

4.0 TIMING

PARAM	DESCRIPTION	MIN	MAX	NOTES
T1	CLK2 Period	31	—	—
T2	$\overline{S0}$, $\overline{S1}$ Setup	8	—	—
T3	$\overline{LCLCYC}$ Setup	—	38	—
T4	$\overline{LCLCYC}$ Hold	10	32	—
T5	RA (0:10) Delay	18	52	—
T6	$\overline{RAS}$ (L,H) Active Delay	—	22	2
T7	$\overline{RAS}$ (L,H) Inactive Delay	8	20	—
T8	DLYOUT Active Delay	7	20	—
T9	DLYOUT to MUX Delay	—	—	1
T10	MUX to CAS Address Valid	12	35	—
T11	DLYOUT to CAS Delay	—	—	1
T12	DLYOUT Inactive Delay	8	22	—
T13	CAS to $\overline{CAS}$ (0:3) Active Delay	10	28	—
T14	$\overline{CAS}$ (0:3) Inactive Delay	8	22	—
T15	$\overline{CAS}$ (0:3) Active Delay	—	25	—
T17	$\overline{RWE}$ (L, H) Active Delay	—	22	—
T18	$\overline{RWE}$ (L, H) Inactive Delay	9	26	—
T19	$\overline{PROMOE}$ Active Delay	—	24	—
T20	$\overline{PROMOE}$ Inactive Delay	7	20	—
T21	$\overline{FERDY}$ Active Delay	—	28	—
T22	$\overline{FERDY}$ Inactive Delay	8	22	—
T23	D (0:15) to RD (0:15), PAR (L, H) Delay Valid	—	25	—
T24	RD (0:15), PAR (L, H) Inactive Delay	10	—	—
T25	RD (0:15) to D (0:15) Valid Delay	—	24	—
T26	D (0:15) Inactive Delay	10	—	—
T27	ESF Register Read Data Delay	—	85	—
T28	$\overline{CMD}$ Setup Delay	10	—	—
T29	A (0:23) to CHRDY Delay	—	60	—
T30	CHRDY to Valid Data	—	30	—
T31	$\overline{CMD}$ Inactive to D(0:15) Inactive	—	20	—
T32	$\overline{DCOE}$ Active Delay	—	20	—
T33	$\overline{DCOE}$ Inactive Delay	5	10	—
T34	$\overline{DCWE}$ Active Delay		26	—
T35	$\overline{DCWE}$ Inactive Delay	8	22	—
T36	$\overline{TCWE}$ Active Delay	—	16	—
T37	$\overline{TCWE}$ Inactive Delay	8	20	—

T38	MATCH Setup Time (Fast)	10	—	—
T39	MATCH Setup Time	10		—

Notes:
1. This delay is determined by an external delay line.
2. This signal is programmed to be active at different CLK2 edges.

Table 9. CPU to Channel Cycles (in nsec)

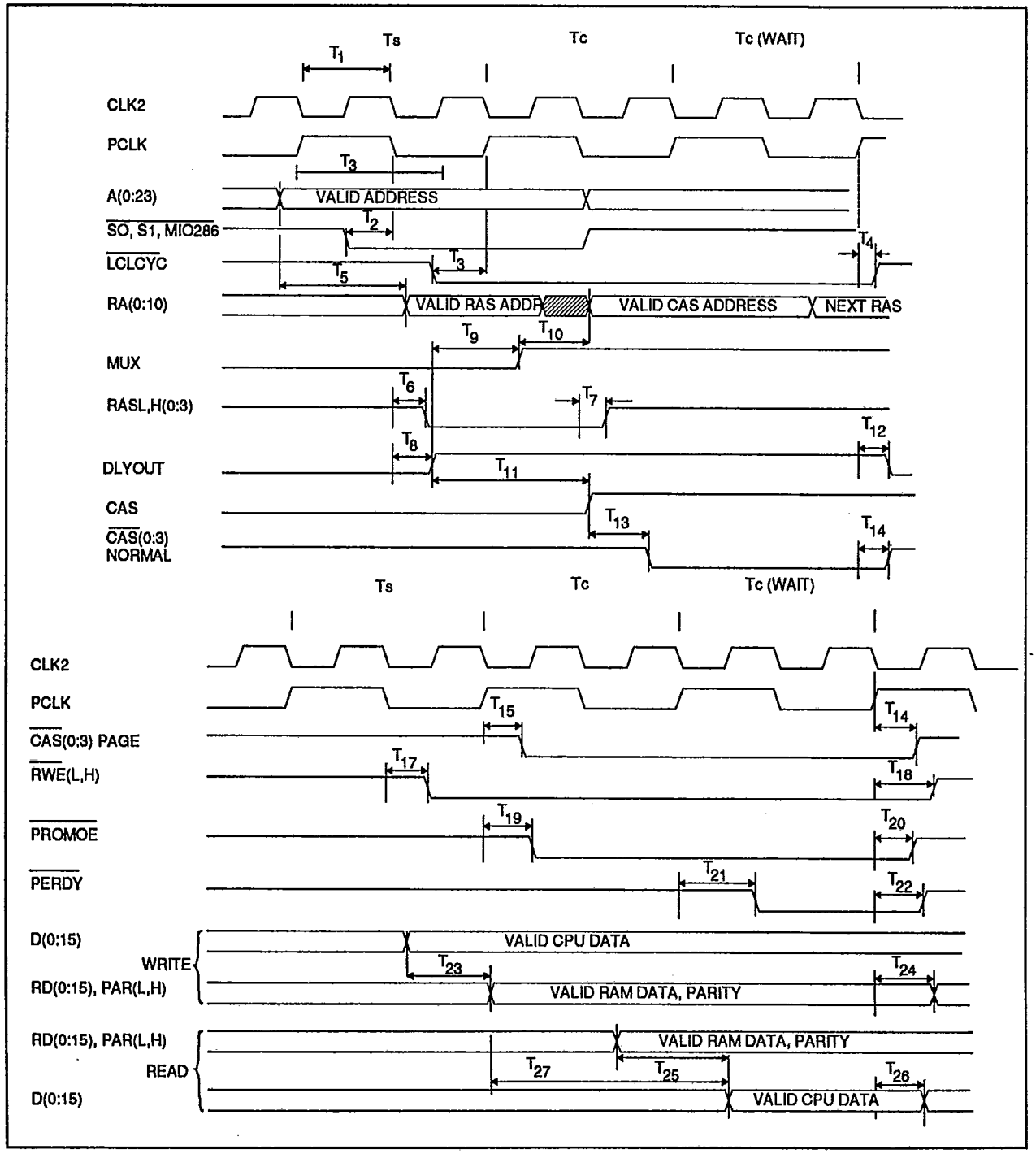


Figure 20. Basic Cycle

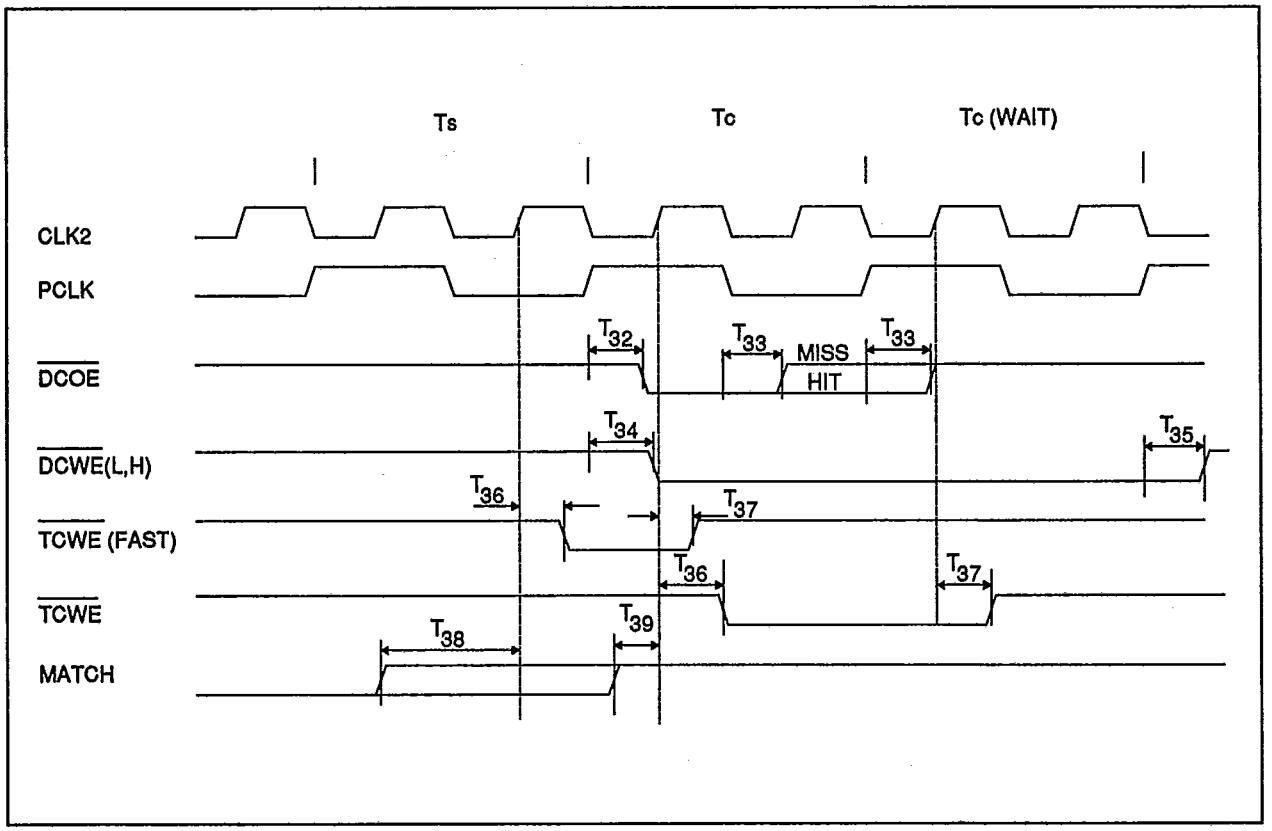


Figure 21. Cache Cycle

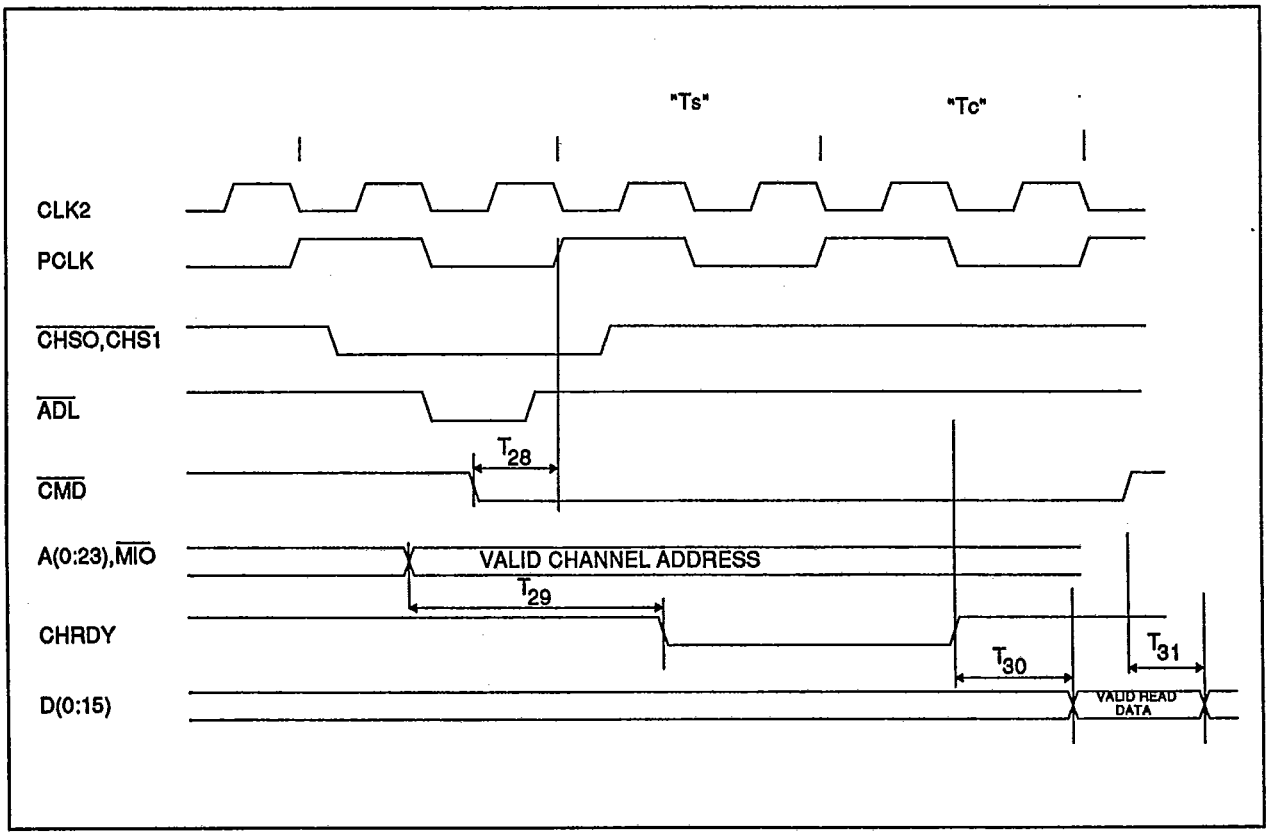


Figure 22. Channel Master Cycle

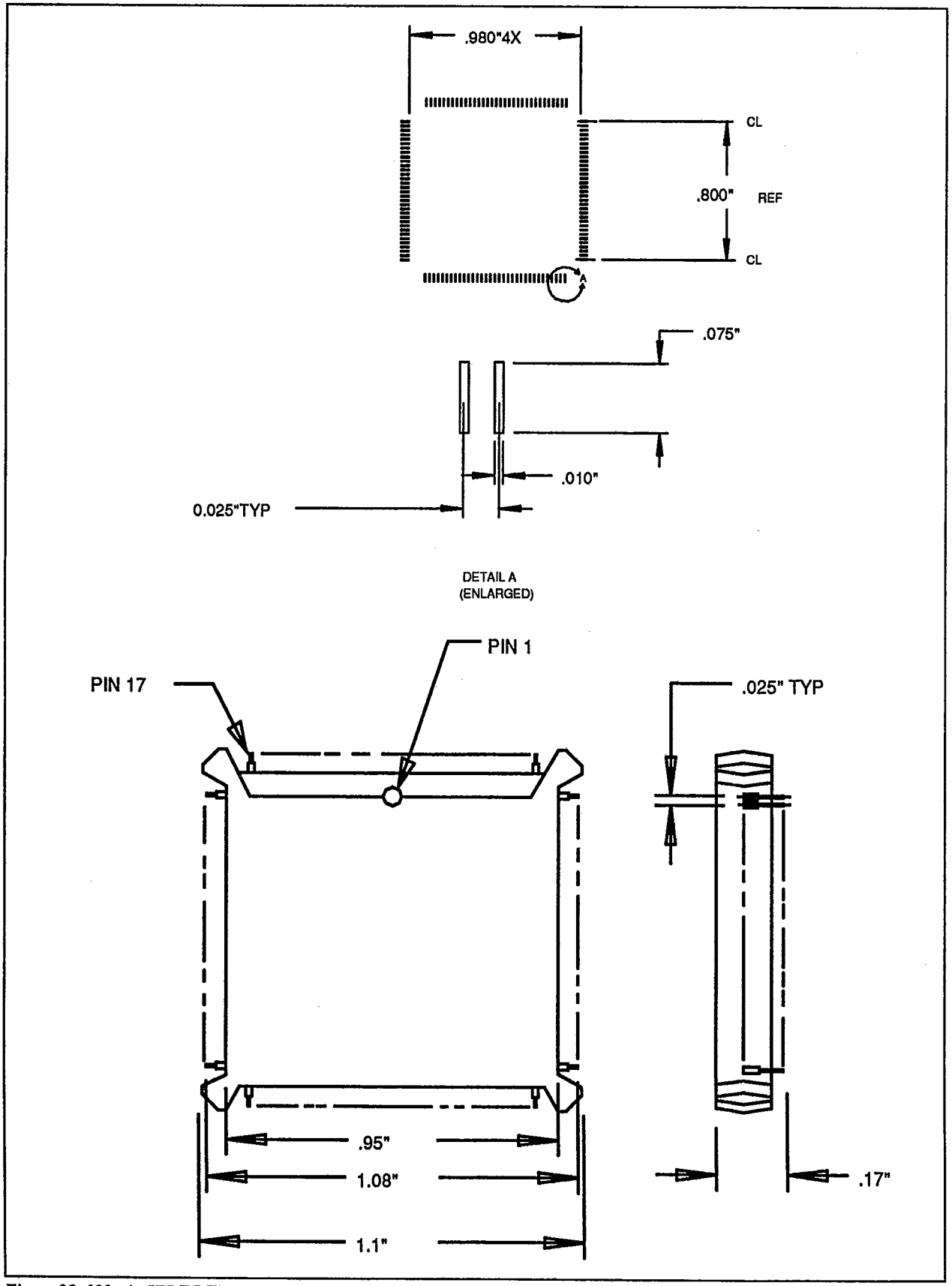
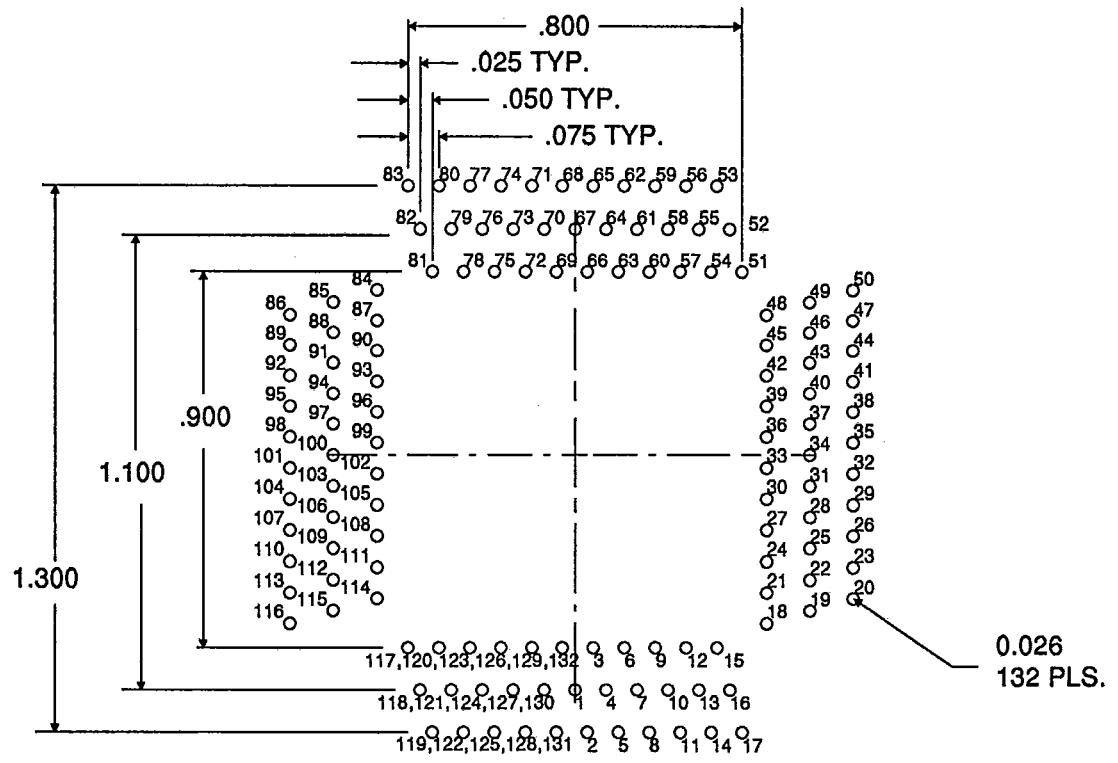


Figure 23. 132-pin JEDEC Flat Pack Packaging Diagram



RECOMMENDED P.C. BOARD HOLE PATTERN
SOCKET SIDE
132 POSN

Amp Incorporated
Harrisburg PA
Part No. 821932-5

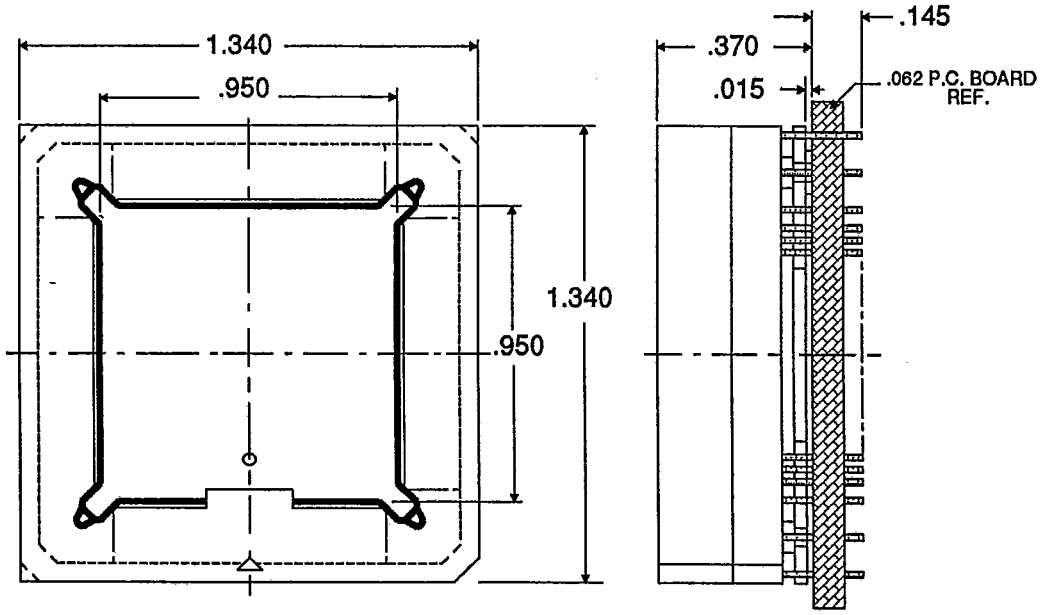


Figure 24. Socket Diagram