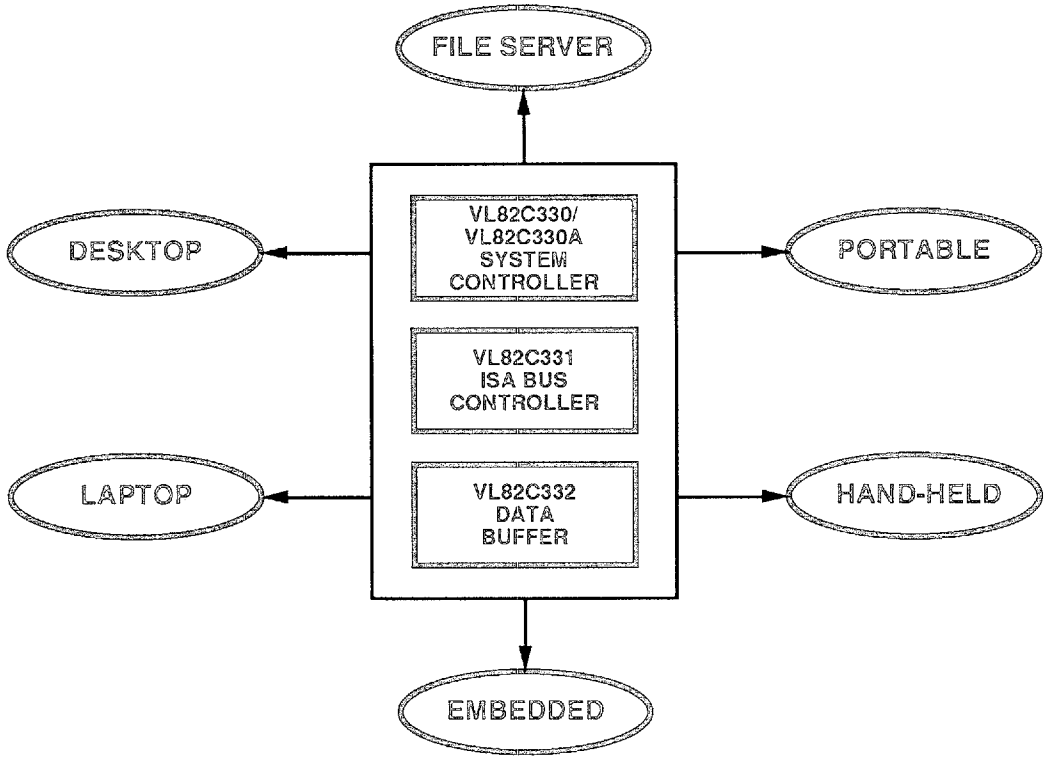
Product Bulletin

T-49-17-01

"TOPCAT 386DX" PC/AT-COMPATIBLE CHIP SET



OVERVIEW

The TOPCAT 386DX chip set from VLSI Technology, Inc., is a very high-integration chip set for use in the design of PC/AT®-compatible based systems. This chip set is intended for use in 80386DX microprocessor-based systems with clock speeds from 16 to 33 MHz.

The TOPCAT 386DX chip set provides design engineers with a very flexible, high-performance, low-cost board design solution for IBM PC/AT-compatible desktop, laptop, portable, and hand-held computers.

The TOPCAT 386DX three-device chip set has been designed with the highest integration consistent with economic and reliable system design. It provides a complete board design using only 10 non-memory devices including the microprocessor.

VLSI's TOPCAT 386DX chip set was designed with seven goals.

- Lowest system board cost
- Smallest board area requirement
- Highest performance in both cached and non-cached systems
- Single board design for:
  - 16 to 33 MHz operation
  - Cache or non-cache
  - 1M byte to 64M byte memory using 256K, 1M, and 4M bit DRAM
  - Laptop or desktop applications
- Full hardware LIM EMS 4.0® support for the highest possible performance
- Built-in, in-circuit test modes for easy board level testing
- The VL82C330A interfaces to the VL82C335 "look-aside" Cache Controller

With VLSI's TOPCAT 386DX chip set, you can be assured that your high-performance system design needs are met.

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System Controller

The VL82C330/VL82C330A System Controller is highly configurable via software; no hardware jumpers are required. Defaults on reset for the configuration registers mimic the compatibility requirements of the original IBM PC/AT as closely as possible. These power-up defaults allow any possible configuration of the system to boot at the CPU's rated speed.

Built-in page mode operation, two- or four-way interleaving, and fully programmable memory timing allow the system designer to maximize system performance by using low-cost DRAMs, standard or custom. These adjustments can often be made without incurring the penalty of additional wait states.

The System Controller handles system board refresh directly and controls the timing of slot bus refresh that is actually performed by the VL82C331 ISA Bus Controller. Refresh may be performed in coupled or decoupled mode. Both may be programmed for independent, slower than normal rates. This allows the use of low-power, slow refresh DRAMs. In all cases, refreshes are staggered to minimize power supply loading and attendant noise on the VDD and ground pins. Full 72 register hardware LIM EMS 4.0 support is included on-chip to provide the highest possible performance.

ISA Bus Controller

The 160-lead VL82C331 ISA Bus Controller provides the functions of DMA, page address register, timer, interrupt control, port B logic, slot bus refresh address generation, and real-time clock.

To avoid problems with sensitive slot bus add-in cards, the Bus Controller features "Bus Quiet" mode operation. When no valid slot bus accesses are occurring, none of the slot bus data, address, or control lines are driven.

Built-in "sleep" mode features work together with System Controller sleep features to provide a low-power system idle state for extension of battery life in portable, laptop, and hand-held systems. If an interrupt occurs due to an external source or dedicated, internal programmable timer, the Bus Controller "wakes up" and resumes normal operation.

The DMA channels have been upgraded to provide a superset of AT functionality by allowing DMA to the entire 32M byte memory range of the TOPCAT 386DX chip set. Additional performance is provided via DMA wait state, clock and MEMR timing programmability.

Bus buffers can be externally strapped to provide for 12 mA or 24 mA drive to the slot bus. This allows systems designed with one to four slots to select a lower drive level and reduce bus ringing.

Data Buffer

The VL82C332 contains the Data Buffer functions in a 128-lead package and performs all of the data buffering functions for an 80386DX processor-based PC/AT system.

The VL82C332 supports posted writes from a cache controller or non-posted writes to the MD bus. The VL82C332 provides the data conversion necessary for 32- or 16-bit writes to 16- to 8-bit devices on the XD or SD buses.

In slower systems (≤16 MHz), true 0 wait state operation is possible with available 60 ns DRAMs. Faster non-cached systems can come close to 0 wait state performance using 80 ns - 100 ns DRAMs and page mode interleaving.

System Support

VLSI Technology offers extensive support for system designers to assist them in their design applications.

- Sample kits of the TOPCAT 386DX chip set
- Evaluation Board
  - VLTC386DX-SB1C - 12 to 33 MHz with cache

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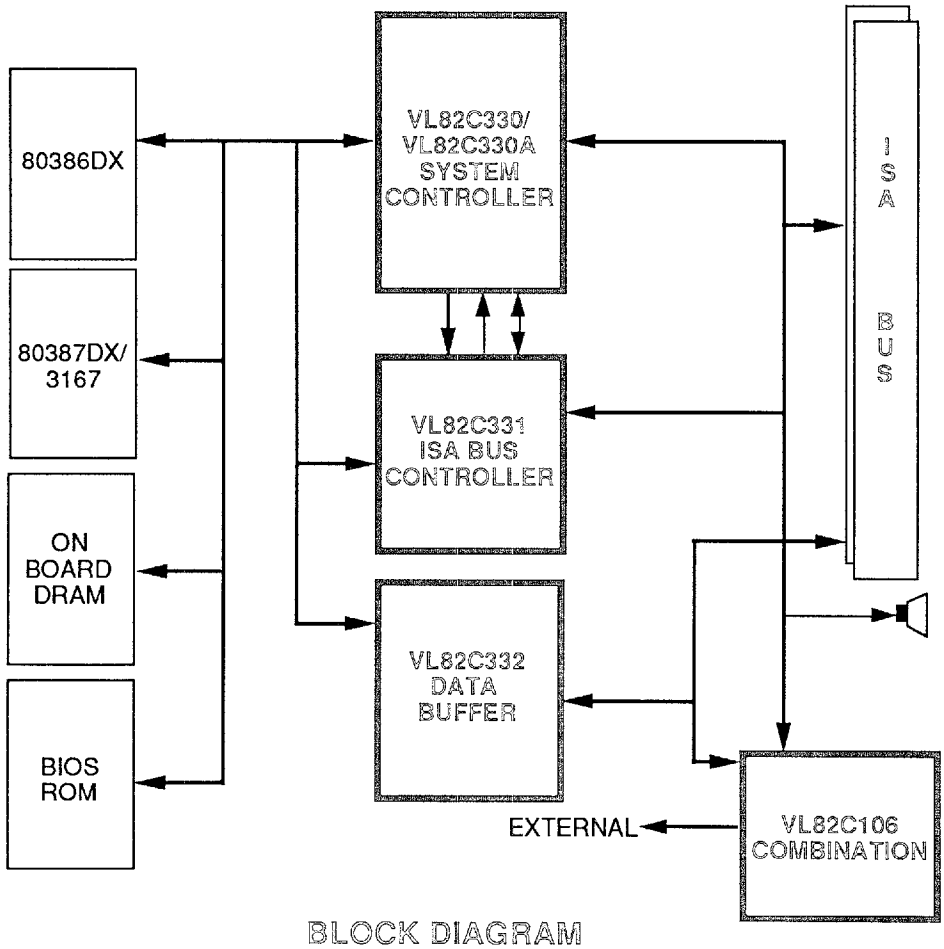

BLOCK DIAGRAM

PACKAGING

PART NUMBER	DESCRIPTION	PACKAGE
VL82C386-SET:	*Three-Chip Set:*	
1-VL82C330/ VL82C330A-FC	System Controller	128-lead Plastic Quad Flatpack
1-VL82C331-FC	ISA Bus Controller	160-lead Plastic Quad Flatpack
1-VL82C332-FC	Data Buffer	128-lead Plastic Quad Flatpack
NOTE: Operating temperature range is 0°C to +70°C		

"TOPCAT 386DX" PC/AT-COMPATIBLE CHIP SET

SYSTEM SUPPORT (Cont.)

- Documentation
  - TOPCAT Data Manual
  - User's manual
  - Sample schematics
    - 16 to 33 MHz 80386DX System Board with DRAM on MD Bus
    - Austek Cache Controller daughter board for 33 MHz 80386DX System Board with DRAM on MD Bus
    - 33 MHz 80386DX System Board with DRAM on D Bus
    - 33 MHz 80386DX System Board with integral Austek Cache Controller
    - 33 MHz 80386DX System Board with integral Intel Cache Controller
  - Schematic databases and netlists available on PC disk
  - Evaluation board artwork available
- Software
  - Quadtel BIOS provided by VLSI Technology (others supported by BIOS vendor)
  - Quadtel EMS driver provided by VLSI Technology
  - BIOS support from Phoenix Technologies (617-551-4282), AMI (404-263-8181), and AWARD Software (408-370-7979)
- Support
  - BIOSEDIT from Quadtel allows OEM BIOS customization

RELATED PRODUCTS LISTING

VL82C286-SET – The TOPCAT 286/386SX is a very high-integration two-chip set for use in the design of PC/AT-compatible based systems. This chip set is intended for use in 80286 and 80386SX microprocessor-based systems with clock speeds from 12 to 25 MHz.

VL82C310/VL82C311 – The SCAMP Controller chips are very cost-effective mid-range featured chips that are designed for use in notebook, laptop, portable, and cached desktop PC/AT-compatible based systems. These chips are intended for use in 80286 and 80386SX microprocessor-based systems with clock speeds from 10 to 20 MHz.

VL82C106 – The Combination I/O chip, when used with the VLSI PC/AT-compatible chip set, allows designers to implement a very cost-effective minimum chip count motherboard containing functions that are common to virtually all PCs.

VL82C107 – The SCAMP Combination I/O chip, when used with the VLSI SCAMP chips, allows designers to implement a very cost-effective minimum chip count motherboard. This chip combines a keyboard controller and a real-time clock with the address latches/buffers and DMA Acknowledge decoders which are normally required in SCAMP-based systems. The VL82C107 additionally contains circuitry necessary to interface PC Memory Cards to the system or provide the chip select and control signals for an external VL16C552 UART I/O device, FDC, and IDE interface.

VL82C312 – The SCAMP Power Management Unit (PMU) chip is intended to be used in conjunction with the VL82C310 SCAMP-LT chip and the VL82C107 SCAMP Combination chip. The PMU dramatically reduces overall system power consumption and provides special features for laptop/notebook PC/AT-compatible computers.

VL82C325/VL82C335 – The VL82C325 and the VL82C335 are high-performance, highly integrated Cache Controllers. The VL82C325 TOPCAT/SCAMP SX Cache Controller is for systems based on VLSI's TOPCAT 286/386SX or SCAMP-LT chip sets up to 25 MHz, and the VL82C335 TOPCAT DX Cache Controller is for systems based on the TOPCAT 386DX chip set up tp 33 MHz.

UART Family – Asynchronous communications elements that serve as serial data input/output interfaces in microcomputer systems. They perform serial-to parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU.

- VL16C450 Single UART
- VL16C451B Single UART (enhanced VL16C451)
- VL16C452B Dual UART (enhanced VL16C452)
- VL16C550 Single enhanced UART (NSC-compatible)
- VL16C551 Single enhanced UART
- VL16C552 Dual enhanced UART
- VL16C554 Quad UART

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"TOPCAT 386DX" PC/AT-COMPATIBLE CHIP SET

FEATURES

- Three chip, PC/AT-compatible chip set capable of use in 80386DX-based systems from 16 to 33 MHz
- Two 128-lead and one 160-lead plastic quad flatpacks, 1.0 and 1.5 micron CMOS
- Memory control of one to four banks of 32-bit DRAM using 256K, 1M, or 4M components allowing 64M bytes on system board
- Two-/four-way page mode interleaving or direct access on system board memory
- Programmable DRAM timing parameters
- Remap option allows logical reordering of system board DRAM banks
- Staggered system board refresh optionally decoupled from slot bus refresh
- Built-in "sleep" mode features, including use of slow refresh DRAMs in power critical operations
- Hardware supports full LIM EMS 4.0 spec over entire 64M byte memory map
- DMA expanded to allow transfers over 64M byte range
- Shadow RAM support in 16K increments
- Support for 80387DX and Weitek 3167 numerical coprocessors
- Internal switching and programmable CPU clock support for PC/AT-compatible and "turbo" modes
- Asynchronous or synchronous slot bus with "Bus Quiet" mode
- Built-in real-time clock and scratchpad RAM
- Additional 64 bytes of battery backed RAM in RTC
- Supports 8- or 16-bit wide BIOS ROMs
- Cache support for posted writes
- In-circuit test modes
- Support for the VL82C335 Cache Controller is provided by the VL82C330A

BENEFITS

- Improves reliability, reduces system size and system cost
- Easy to mount on printed circuit board, inexpensive, and an accepted industry standard
- Allows for extremely flexible memory configuration and expansion
- Allows use of the lowest speed DRAMs possible
- Provides optimum performance for any type of DRAM
- Allows maximum use of memory even if bad DRAMs are present
- Allows optional decoupling of system and slot DRAM, and minimizes power supply peak currents
- Reduces power consumption, and supports laptop and portable applications
- Provides higher performance than by using 80386DX paging registers for EMS
- Allows fast DMA transfers over large memory range and improves system speed
- Allows faster execution of slow ROM code by executing it in faster DRAMs
- Provides the ability to use two coprocessors simultaneously
- Allows timing compatibility with "older" software
- Allows use of older and slower add-in cards and prevents false decoding of bus addresses
- Reduces board chip count
- Provides non-volatile storage of chip set configuration data and user specific information
- Allows user to use less expensive 8-bit ROMs
- Reduces external logic in posted write cache applications
- Allows in-board electrical testing and easy solder joint verification
- High-performance, high-integration cache system

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T-49-17-01

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