VLSI TECHNOLOGY, INC.

ADVANCE INFORMATION

# VL82C110

## FLOPPY DISK CONTROLLER COMBINATION I/O

### FEATURES

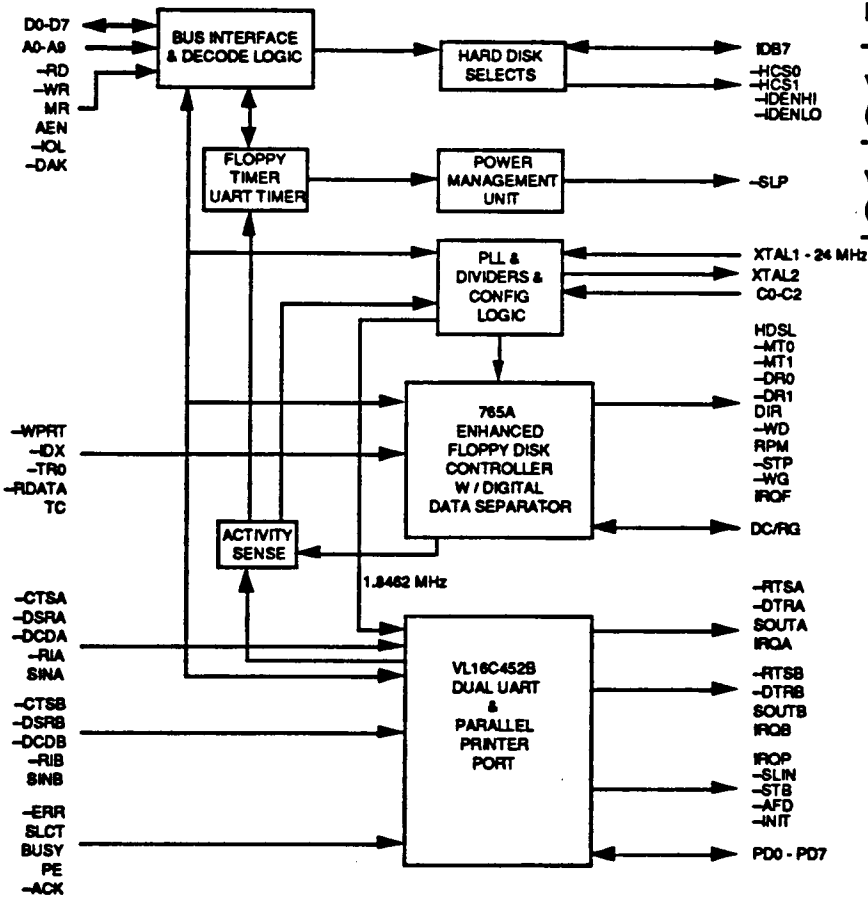
- Combines the functions of the following PC/AT® peripheral chips:
  - Two 16C450 UARTs
  - Parallel printer port
  - 765A compatible floppy disk controller with digital data clock separator
- Serial ports 100% National NS16C450 compatible
- UARTS can be programmed as COM1-COM4
- Bidirectional line printer port
- CMOS direct drive of Centronics-style interface
- Printer Port can be programmed as LPT2, 3
- IDE bus control signals included
- 24 mA bus interface drivers
- 48 mA floppy drive interface
- Single 24 MHz crystal/oscillator
- Internal PMU (power management unit)
- PLL clock circuit for one of seven CPU clock frequencies
- Pin compatible with National PC87310
- Hard disk select logic
- Single 100-pin plastic quad flat package

### DESCRIPTION

The VL82C110 Combination I/O chip replaces several of the commonly used peripherals found in PC/AT-compatible computers. The VL82C110 contains a 765A compatible floppy disk controller with a digital data clock separator, write precompensation logic and the necessary control registers. It also contains two 16C450 compatible UARTs, a Centronics compatible printer port, and an internal PMU (power management unit) which is useful in applications where low power consumption is essential. Additionally, a PLL clock circuit is included to provide one of seven of the commonly used CPU clock frequencies. This 100-pin chip allows designers to implement a very cost effective, minimum chip count motherboard containing functions that are common to virtually all PCs.

The internal PMU provides a Sleep output which is asserted via automatically after a programmable time delay period of inactivity in any of the major on-chip functions. Conversely, the Sleep output will be de-asserted when any activity is detected to any of the major on-chip functions.

### BLOCK DIAGRAM




### ORDER INFORMATION

| Part Number | Package |
|---|---|
| VL82C110-PFC (Prototypes) | Plastic Quad Flat Pack |
| VL82C110-FC (Production) | Plastic Quad Flat Pack |

PC/AT is a registered trademark of IBM Corporation.

## DESCRIPTION (Cont.)

The on-chip UARTs are 100% software compatible with the VL16C450 ACE.

The bidirectional parallel port provides a PS/2® software compatible interface between a Centronics-style printer and the VL82C110. Direct drive is provided so all that is necessary to interface to the line printer port is a resistor-capacitor network. The bidirectional feature (option) is software programmable for backwards PC/AT compatibility.

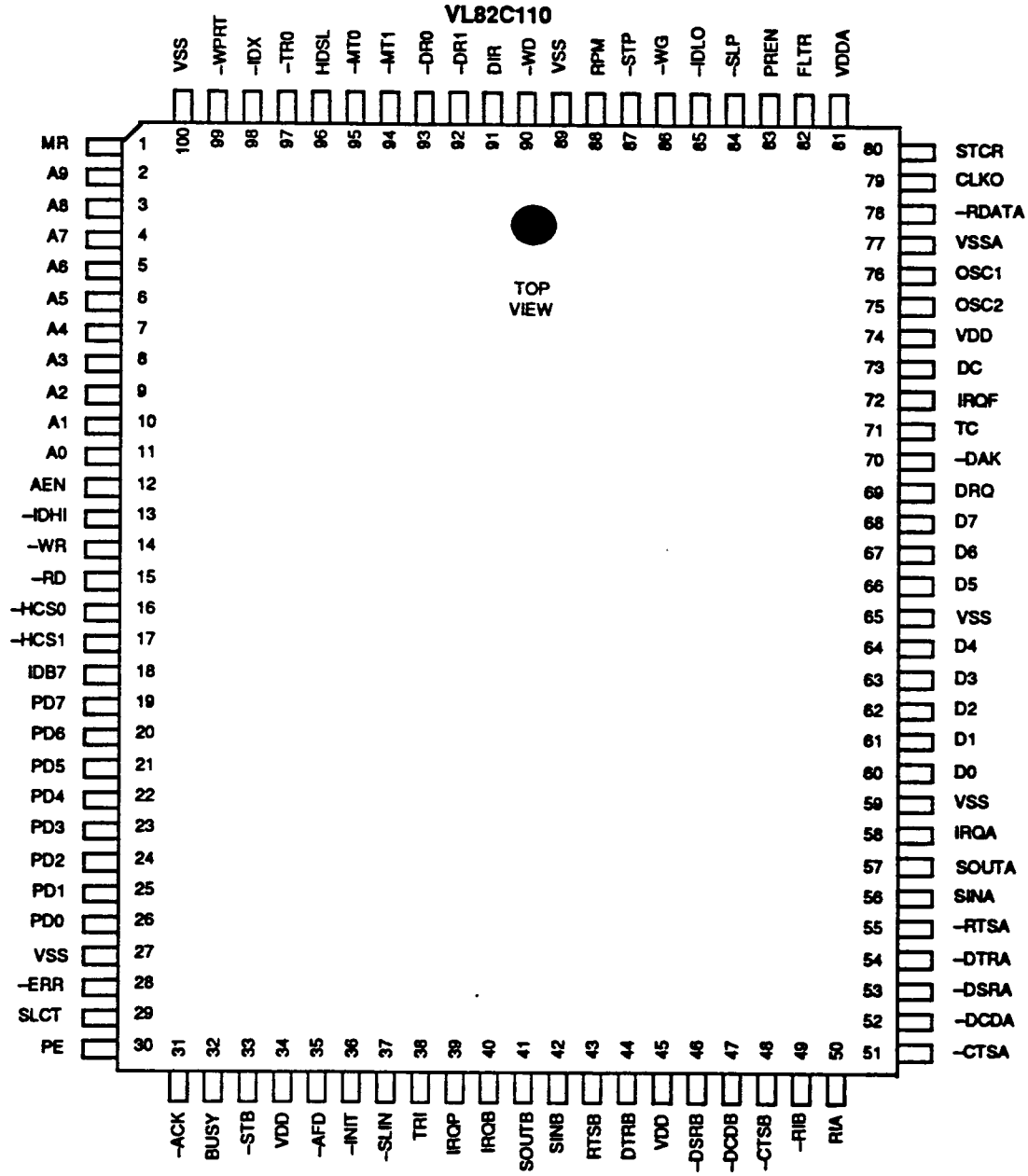
The on-chip floppy disk controller is 100% compatible to the industry standard 765A. The internal digital data separator is capable of operating up to a 500 kb/s data rate. The Controller also implements all of the DP8473 disk controller functions.

The necessary signals are provided to implement the Integrated Drive Electronics (IDE) interface.

A 24 MHz oscillator is included for UART baud rate generation and the floppy disk controller clock. It is also used to generate, via software and hardware control, a 20, 25, 32, 40, 50, 66 or 80 MHz output which can be used as a CPU input clock. This feature may be disabled at power-up reset time.

Software configurable registers are provided to enable and disable major blocks, assign addresses, and control other functions within the VL82C110.

## PIN DIAGRAM




PS2 is a registered trademark of IBM Corporation.

## SIGNAL DESCRIPTIONS

| Signal Name | Pin Number | Signal Type | Signal Description |
|---|---|---|---|
| **COMMUNICATIONS PORT A** | | | |
| –RTSA | 55 | O | RTS output port A - Used at power-up as PLL configuration bit 0. |
| –DTRA | 54 | O | DTR output port A - Used at power-up as PLL configuration bit 1. |
| SOUTA | 57 | O | Serial output port A. |
| –CTSA | 51 | I | CTS input port A. |
| –DSRA | 53 | I | DSR input port A. |
| –DCDA | 52 | I | DCD input port A. |
| –RIA | 50 | I | Ring Indicator input port A. |
| SINA | 56 | I | Serial input port A. |
| IRQO | 58 | O | Interrupt Request ports 1 and 3. |
| **COMMUNICATIONS PORT B** | | | |
| –RTSB | 43 | O | RTS output port B - Used at power-up as PLL configuration bit 2. |
| –DTRB | 44 | O | DTR output port B - Used at power-up as DRTYP. |
| SOUTB | 41 | O | Serial output port B. |
| –CTSB | 48 | I | CTS input port B. |
| –DSRB | 46 | I | DSR input port B. |
| –DCDB | 47 | I | DCD input port B. |
| –RIB | 49 | I | Ring Indicator input port B. |
| SINB | 42 | I | Serial input port B. |
| IRQE | 40 | O | Interrupt Request ports 2 and 4. |
| **PARALLEL PRINTER PORT** | | | |
| PD0 | 26 | I | Printer Data port bit 0. |
| PD1 | 25 | I | Printer Data port bit 1. |
| PD2 | 24 | I | Printer Data port bit 2. |
| PD3 | 23 | I | Printer Data port bit 3. |
| PD4 | 22 | I | Printer Data port bit 4. |
| PD5 | 21 | I | Printer Data port bit 5. |
| PD6 | 20 | I | Printer Data port bit 6. |
| PD7 | 19 | I | Printer Data port bit 7. |
| –INIT | 36 | O | Printer command Initialize. |
| –AFD | 35 | O | Printer command Auto Feed. |
| –STB | 33 | O | Printer command data Strobe. |
| –SLIN | 37 | O | Printer command Select. |
| –ERR | 28 | I | Printer status Error. |
| SLCT | 29 | I | Printer status Select. |
| BUSY | 32 | I | Printer status busy. |
| PE | 30 | I | Printer status Paper Error. |
| –ACK | 31 | I | Printer status ACK. |
| IRQP | 39 | O | Printer Interrupt Request |

## SIGNAL DESCRIPTIONS (Cont.)

| Signal Name | Pin Number | Signal Type | Signal Description |
|---|---|---|---|
| **FLOPPY DISK CONTROLLER** | | | |
| –WPRT | 99 | I | Write Protect - This input indicates that the disk is write protected. |
| –IDX | 98 | I | Beginning of track. |
| –TR0 | 97 | I | Track 0. |
| HDSL | 96 | OD | Active head - Low = head 1, high = head 0. |
| –MT0 | 95 | OD | Motor enable drive 0. |
| –MT1 | 94 | OD | Motor enable drive 1. |
| –DR0 | 93 | OD | Select drive 0. |
| –DR1 | 92 | OD | Select drive 1. |
| DIR | 91 | OD | Direction of head movement. |
| –WD | 90 | OD | Precompensated serial data output to disk drive. |
| RPM | 88 | OD | Dual function pin (see floppy disk controller description). |
| –STP | 87 | OD | Pulse to move drive head during seek. |
| **FLOPPY DISK CONTROLLER** | | | |
| –WG | 86 | OD | Enables disk drive write circuitry. |
| –PREN | 83 | I | Sets precompensation mode. |
| –RDATA | 78 | I | Raw Data from disk. |
| DC | 73 | I | Disk Change (see Floppy Disk Controller description). |
| IRQF | 72 | O | Floppy Disk Controller Interrupt - This pin is also reserved for future use. |
| TC | 71 | I | Terminal Count - DMA terminal count. |
| **COMMON BUS I/O** | | | |
| D0-D7 | 60-64, 66-68 | IO | CPU Data bus bits 0 through 7. |
| A0-A9 | 11-2 | I | CPU Address bus bits 0 through 9. |
| XTAL1 | 76 | XI | Crystal. |
| XTAL2 | 75 | XO | Crystal/Clock (24 MHz). |
| –RD | 15 | In | CPU Read command strobe. |
| –WR | 14 | In | CPU Write command strobe. |
| MR | 1 | In | Master Reset command. |
| AEN | 12 | I-n | Address Enable input. |
| –IDHI | 13 | IO | IDE Enable High, see Hard Disk Interface. |
| –DAK | 70 | In | DMA Acknowledge. |
| DRQ | 69 | Out | DMA Request. |
| **MISCELLENEOUS SIGNALS** | | | |
| –HCS1 | 17 | IO | Hard Drive Chip Select 1 - This is used for the IDE interface, see Hard Disk Interface. |
| –HCS0 | 16 | IO | Hard Drive Chip Select 0, see Hard Disk Interface. |
| –IDLO | 85 | IO | IDE Enable Low - This is the –IDENLO signal for the IDE interface. |
| IDB7 | 18 | IO | IDE Bit 7 - This pin is used as IDE bit 7, see Hard Disk Interface. |
| CLKO | 79 | O | Programmable Clock Output. |
| STCR | 80 | I | Set Current - This is the bias pin for the PLL circuitry. |

## SIGNAL DESCRIPTIONS (Cont.)

| Signal Name | Pin Number | Signal Type | Signal Description |
|---|---|---|---|
| FLTR | 82 | I | Filter- This is the filter pin for the PLL circuitry. |
| SLP | 84 | IOD | This pin is used as the bidirectional SLP pin of the power management unit (PMU), see PMU section. |
| TRI | 38 | I | This pin three-states all outputs when asserted. |
| **POWER AND GROUND PINS** | | | |
| VDDA | 81 | PWR | Power Supply connection for PLL section, nominally +5 V. |
| VDD | 34, 45, 74 | PWR | Power Supply, nominally +5 V connection. |
| VSSA | 77 | GND | Ground connection for PLL section, nominally 0 V. |
| VSS | 27, 59, 65, 89, 100 | GND | Ground, nominally 0 V. |

**SIGNAL LEGEND**

| Signal Type | Description |
|---|---|
| I | Input |
| IX | Input from crystal |
| O | Output |
| OX | Output from crystal |
| OD | Open drain |
| IO | Input/output |
| GND | Ground |
| PWR | Power |

## FUNCTIONAL DESCRIPTION

The following functional blocks are covered:

- Configuration registers
- 16C450 serial ports
- Parallel port
- 765 enhanced floppy disk controller
- PMU (power management unit)
- Programmable clock output

The VL82C110 contains five registers (refer to Table 1) which are used to program the various functions of the chip. These registers are indexed registers and are accessible by first writing the index address to I/O port 0ECH and then by reading or writing data from I/O port 0EDH. For example: To access index register 30H, the software would first write 30H to I/O port 0ECH followed by a read or write to I/O port 0EDH for the register data.

## TABLE 1. CONFIGURATION REGISTERS

| Index Port | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| OECH (R/W) | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

| Data Port | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| OEDH (R/W) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

R/W

| 30H (INDEX) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| MISCSET Register | Drive Select | –HCSx Enable | LPT Enable | LPT Select | –EMODE Bit | Clock Output Control | | |

R/W

| 31H (INDEX) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| FDC Register | RES | RES | –FDC Enable | Drive Format | Motor Control | PMU Timer Control | | |

R/W

| 32H (INDEX) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| UARTA Register | COM3 Address | | UARTA Enable | COM Port Select | | PMU Timer Control | | |

R/W

| 33H (INDEX) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| UARTB Register | COM4 Address | | UARTB Enable | COM Port Select | | PMU Timer Control | | |

R/W

| 34H (INDEX) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| PMU Register | FDC Enable | UARTA Enable | UARTB Enable | FDC SLP Control | UARTA SLP Control | UARTB SLP Control | SLP Enable | OSC Control |

**SERIAL COMMUNICTIONS PORTS**

The chip contains two UARTS based on the VL16C450 ACE. The UART clock is the 24 MHz clock divided by 13. (Please refer to the VL16C452 data sheet for the register descriptions.) The UART's I/O addresses and enables may be programmed via index register 32H (UARTA register) and index register 33H (UARTB register).

In Table 2, UARTA register bits 3 through 7 are used to program the UARTs and are assigned as follows:

Bits 6 and 7: Determine the address range for COM port 3:

- 00 COM port 3 at 3E8H-3EFH (default)
- 01 COM port 3 at 338H-33FH
- 10 COM port 3 at 2E8H-2EFH
- 11 COM port 3 at 220H-227H

Bit 5: When this bit is set to a 0, UARTA is enabled. When this bit is set to a 1, UARTA is disabled, its input clock is stopped and its outputs are three-stated.

Bits 3 and 4: Determine which COM port is assigned to UARTA. If UARTA is assigned to port 1 or 3, then its interrupt is assigned to INTO (odd interrupt), otherwise its interrupt is assigned to INTE (even interrupt). If UARTA is assigned to COM port 3, then its address range is determined by bits 6 and 7 of the UARTA register. If UARTA is assigned to COM port 4, then its address range is determined by bits 6 and 7 of the UARTB register.

- 00 UARTA is assigned to COM port 1 (3F8H-3FFH) (default)
- 01 UARTA is assigned to COM port 2 (2F8H-2FFH)
- 10 UARTA is assigned to COM port 3
- 11 UARTA is assigned to COM port 4

Also in Table 2, UARTB register bits 3 through 7 are used to program the UARTs and are assigned as follows:

Bits 6 and 7: Determine the address range for COM port 4:

- 00 COM port 4 at 2E8H-2EFH (default)
- 01 COM port 4 at 238H-23FH
- 10 COM port 4 at 2E0H-2E7H
- 11 COM port 4 at 228H-22FH

Bit 5: When this bit is set to a 0, UARTB is enabled. When this bit is set to a 1, UARTB is disabled, its input clock is stopped and its outputs are three-stated.

Bits 3 and 4: Determine which COM port is assigned to UARTB. If UARTB is assigned to port 1 or 3, then its interrupt is assigned to INTO (odd interrupt), otherwise its interrupt is assigned to INTE (even interrupt). If UARTB is assigned to COM port 3, then its address range is determined by bits 6 and 7 of the UARTA register. If UARTB is assigned to COM port 4, then its address range is determined by bits 6 and 7 of the UARTB register.

- 00 UARTB is assigned to COM port 1 (3F8H-3FFH)
- 01 UARTB is assigned to COM port 2 (2F8H-2FFH) (default)
- 10 UARTB is assigned to COM port 3
- 11 UARTB is assigned to COM port 4

**LINE PRINTER PORT**

The line printer port contains the functionality of the port included in the VL16C452, but offers a software programmable Extended Mode. This enhancement is the addition of a direction control bit and an interrupt status bit.

Bits 3 through 5 are used to program the parallel port and are assigned as follows:

Bit 5: When set to 0, printer port is enabled.

Bit 4: Determine the address range for the parallel port:

- 00 Parallel port at LPT2 (378H-37AH) (default)
- 01 Parallel port at LPT3 (278H-27AH)
- 10 Parallel port disabled
- 11 Parallel port disabled

Bit 3: When set to 0, the extended features are enabled. When the –EMODE bit is set to 1, the part functions exactly as a PC/AT-compatible printer port.

There are three registers assigned to the parallel port I/O address space, (see Table 3), and are defined in Table 4.

## TABLE 2. SERIAL COMMUNICATION PORTS

R/W

| 32H (INDEX) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| UARTA Register | COM3 Address | | UARTA Enable | COM Port Select | | PMU Timer Control | | |

R/W

| 33H (INDEX) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| UARTB Register | COM4 Address | | UARTB Enable | COM Port Select | | PMU Timer Control | | |

## TABLE 3. LINE PRINTER PORT

R/W

| 30H (INDEX) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| MISCSET Register | Drive Select | –HCSx Enable | LPT Enable | LPT Select | –EMODE Bit | Clock Output Control | | |

## TABLE 4. LPT PORT DEFINITIONS

| Control Pins | | | | |
|---|---|---|---|---|
| –IOR | –IOW | A1 | A0 | Register Selected |
| 0 | 1 | 0 | 0 | Read Data |
| 0 | 1 | 0 | 1 | Read Status |
| 0 | 1 | 1 | 0 | Read Control |
| 0 | 1 | 1 | 1 | Invalid |
| 1 | 0 | 0 | 0 | Write Data |
| 1 | 0 | 0 | 1 | Invalid |
| 1 | 0 | 1 | 0 | Write Control |
| 1 | 0 | 1 | 1 | Invalid |

## TABLE 5. REGISTER 0 - LPT PORT DATA REGISTER

| Control Pins | | | | |
|---|---|---|---|---|
| –IOR | –IOW | A1 | A0 | Register Selected |
| 0 | 1 | 0 | 0 | Read Data |
| 0 | 1 | 0 | 1 | Read Data |

**Register 0 - LPT Port Data Register**
The line printer (LPT) port, a read/write port, is either uni- or bidirectional, depending on the state of the –EMODE (bit 3, MISCSET index register 30H) and the data direction control (bit 5, register 2 LPT port control) bits.

When in non-extended mode, –EMODE = 1, reads to this register return the last data that was written to the LPT port. When in extended mode, –EMODE = 0. Read operations return either the data last written to the LPT data register if the direction bit, (bit 5 register 2), is set to write (0) or the data that is present on the pins of the LPT port if the direction is set to read (1). Write operations latch data into the output register, but only drive the LPT port when the direction bit is set to write.

In either case, the bits of the LPT data register are defined in Table 6.

**Register 1 Read - LPT Port Status Register**
The LPT status register is a read-only register that contains interrupt status and real-time status of the LPT connector pins. The bits are described as follows:

Bit 0: Reserved, read as 1.

Bit 1: Reserved, read as 1.

Bit 2: Interrupt Status Bit - A 0 indicates that the printer has acknowledged the previous transfer with a –ACK handshake (bit 4 of the control register must be set to 1). The bit is set to 0 on the active to inactive transition of the –ACK signal. This bit is changed to a 1 after a read from the status port. The default value for this bit is 1. If the –EMODE bit, (bit 3 index register 30H), is set to a 1, this bit reflects the state of the –ACK pin.

Bit 3: Error Status Bit - When reset (0), indicates that the printer has had an error. A 1 indicates normal operation. This bit follows the state of the –ERR pin.

Bit 4: Select Status Bit - Indicates the current status of the SLCT signal from the printer. When a 0, the printer is currently not selected (off-line). When a 1, the printer is currently selected.

Bit 5: Paper Empty Status Bit - When a 0, indicates normal operation. A 1 indicates that the printer is currently out of paper. This bit follows the state of the PE pin.

Bit 6: Acknowledge Status Bit - When a 0, indicates that the printer has received a character and is ready to accept another. A 1 indicates that the last operation to the printer has not been completed yet. This bit follows the state of the –ACK pin.

Bit 7: Busy Status Bit - When a 0, indicates that the printer is busy and can not receive data. A 1 indicates that the printer is ready to accept data. This bit follows the inversion of the state of the BUSY pin.

## TABLE 6. LPT DATA REGISTER

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| LPT Data Register | Data Bit 7 | Data Bit 6 | Data Bit 5 | Data Bit 4 | Data Bit 3 | Data Bit 2 | Data Bit 1 | Data Bit 0 |

## TABLE 7. LPT PORT STATUS REGISTER (READ ONLY)

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| LPT Status Register | –BUSY | –ACK | PE | SLCT | –ERROR | –IRQ | RES | RES |

## TABLE 8. LPT PORT CONTROL REGISTER

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| LPT Control Register | RES | RES | DIR | IRQ EN | SLCT IN | –INT | AUTO FD XT | STROBE |

**REG 2 - LPT Port Control Register**
This port is a read/write port that is used to control the LPT direction as well as the printer control lines driven from the port. Write operations set or reset these bits while read operations return the status of the last write operation to this register (except for bit 5 which is write-only and is always read back as a 1). The bits in this register are defined as follows:

Bit 0: Printer Strobe (STROBE) Control Bit - When set (1), the –STB signal is asserted on the LPT interface causing the printer to latch the current data. When reset (0), the signal is negated.

Bit 1: Auto Feed (AUTO FD XT) Control Bit - When set (1), the –AFD signal will be asserted on the LPT interface causing the printer to automatically generate a line feed at the end of each line. When reset (0), the signal is negated.

Bit 2: Initialize Printer (–INIT, active low) Control Bit - When set (1), the –INIT signal is negated. When reset (0), the –INIT signal is asserted to the printer, forcing a reset.

Bit 3: Select Input (SLCT IN) Control Bit - When set (1), the SLCT signal is asserted causing the printer to go "on-line". When reset (0), the signal is negated.

Bit 4: Interrupt Request Enable (IRQ EN) Control Bit - When set (1), enables interrupts from the LPT port whenever the –ACK signal is asserted by the printer. When reset (0), disables interrupts.

Bit 5: When –EMODE = 0, (bit 3 index register 30H), this direction (DIR) control

bit, when set (1), disables the output buffers in the LPT port allowing data driven from external sources to be read from the LPT port. When reset (0), the output buffers are enabled forcing the LPT pins to drive the LPT pins. The power-on reset value of this is clear (0). This bit is always read as a 1. When –EMODE = 1, (bit 3 index register 30H), this control bit has no effect on device operation.

Bit 6: Reserved, read as 1.

Bit 7: Reserved, read as 1.

**FLOPPY DISK CONTROLLER**

The VL82C110 contains a floppy disk controller that is compatible with the industry standard 765A and the DP8473. The Controller also contains many software and hardware enhancements . One of the enhancements is the addition of a digital data separator that utilizes precision digital phase lock loop circuitry. Note that when bit 5 of index register 31H is set to 1, the floppy disk controller is disabled (see Drive Control Register Definitions.)

**I/O Address Definition**

Table 11 is the address memory map for the floppy disk controller.

**Reset Control Logic**

When the reset input is asserted this will cause the drive control register to be set to 0s, and the data rate register to be set to 250 kb/s. The Controller will be held reset until the drive control reset bit is set via software. Once this occurs, the Controller may be initialized. The Controller may be software reset by setting then resetting the reset bit in the drive control register. This will not reset the drive control register or the data rate register.

**TABLE 9. I/O ADDRESS DEFINITION**

| I/O Address | R/W | Register |
|---|---|---|
| 3F0H | X | None |
| 3F1H | X | None |
| 3F2H | W | Drive Control (DCR) |
| 3F4H | R | Main Status |
| 3F5H | R/W | Data (DR) |
| 3F6H | X | None |
| 3F7H | W | Data Rate (DDR) |
| 3F7H | R | Disk Changed Bit (DKR)* |

*Bit 7 only.

**REGISTER DEFINITIONS**

**Drive Control Register - 3F2H (write-only)**

If bit 4 of index register 31H is set to 0, and the floppy controller is enabled by setting bit 5 to 0, then the drive control register encodes the drive control output pins as follows:

Bit Definition
B0 - Drive Select 0
B1 - Drive Select 1
B2 - Software Reset
B3 - DMA Enable
B4 - Motor 0 Enable
B5 - Motor 1 Enable
B6 - Not Used
B7 - Not Used

**TABLE 10. DRIVE CONTROL REGISTER**

| 31H (INDEX) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| FDC Register | RES | RES | –FDC Enable | Drive Format | Motor Control | PMU Timer Control | | |

If Bit 4 of index register 31H is set to 1, and the floppy controller is enabled by setting bit 5 to 0, then the drive control register encodes the drive control output pins in Table 11.

**Main Status Register - 3F4H (read-only)**
B0: Drive 0 Seeking - Set after the last byte of the command phase of a seek or recalibrate command is issued for drive 0. Cleared after reading the first byte in the result phase of the sense interrupt command for the drive.

B1: Same as B0 for drive 1.

B2: Same as B0 for drive 2.

B3: Same as B0 for drive 3.

B4: Command In Progress - This bit is set after the first byte of the command phase has been written and cleared after the last byte of the result phase has been read.

B5: Non-DMA Execution - This bit is set only in the non-DMA mode during the execution phase of a command.

B6: Data Direction - Set to indicate the data flow direction of the data register. 0 = written to and 1 = read from.

B7: Request for Master - This bit is set when the data register is ready to send or receive data.

**Data Register - 3F5H (read/write)**
The data register is used for all data, command, and status flow to and from the CPU.

**Data Rate Register - 3F7H (write)**
B0 and B1 are the only bits used when writing to this register. These bits along with the value latched in from the DRTYP (drive type) pin at reset control the data rate. The data rate and precompensation values are in Table 12.

## TABLE 11. DRIVE CONTROL REGISTER BIT PATTERNS

| Drive Control Bits | | | | | | | | Drive Control Pins | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | –DR1 | –DR0 | –MTR1 | –MTR0 | Function |
| | | | 1 | | | 0 | 0 | 0 | 0 | 0 | 0 | EN DRV0 and MTR0 |
| | | 1 | | | | 0 | 1 | 0 | 1 | 0 | 1 | EN DRV1 and MTR1 |
| | 1 | | | | | 1 | 0 | 1 | 0 | 1 | 0 | EN DRV2 and MTR2 |
| 1 | | | | | | 1 | 1 | 1 | 1 | 1 | 1 | EN DRV3 and MTR3 |
| Any other bit pattern | | | | | | | | 1 | 0 | 0 | 1 | Invalid State |

Note: Any other bit patterns should be encoded as invalid states.

## TABLE 12. DATA RATE REGISTER

| B1 | B0 | DRTYP Pin | Data Rate MFM (KB/S) | Precompensation Pren = 0 | Precompensation Pren = 1 | RPM Pin Level |
|---|---|---|---|---|---|---|
| 0 | 0 | X | 500 | 125 ns | 125 ns | High |
| 0 | 1 | 0 | 250 | 125 ns | 250 ns | Low |
| 0 | 1 | 1 | 300 | 208 ns | 208 ns | Low |
| 1 | 0 | 0 | 250 | 125 ns | 250 ns | Low |
| 1 | 0 | 1 | 250 | 125 ns | 250 ns | Low |
| 1 | 1 | 0 | 1000 | 83 ns | 83 ns | High |
| 1 | 1 | 1 | 1000 | 83 ns | 83 ns | Low |

**Disk Changed Bit - 3F7H (read)**
Bit 7 is used when reading this register to indicate the complement of the disk changed input pin. Bits 0 through 6 are three-stated during reads from this register.

**HARD DISK INTERFACE**
When enabled in the VL82C110, it provides the necessary signals to directly implement an IDE interface for the hard disk. The signals are defined as follows:

–HCS0: This signal will be active during all I/O accesses to addresses 1F0H-1F7H.

–HCS1: This signal will be active during all I/O accesses to addresses 3F6H-3F7H.

–IDHI: This signal is used as the enable for the high byte transceiver of the IDE bus. It will be active for all 16-bit operations.

–IDLO: This signal is used as the enable for the low byte transceiver of the IDE bus. It will be active for all IDE operations.

IDB7: This is the input for data bit 7 from the IDE interface. To avoid conflict with the floppy disk controller this signal will be gated off during all I/O accesses to address 3F7H.

**POWER MANAGEMENT UNIT**
The internal power management unit, herein referred to as the PMU, provides several functions which can be utilized in applications where power consumption is critical. The PMU will monitor activity to the serial ports and the floppy disk controller, and if enabled will turn the internal clocks to that block on or off based on this activity.

Bit 7: Enables the PMU Timer for the floppy disk controller when set to 1.

Bit 6: Enables the PMU Timer for UARTA when set to a one.

Bit 5: Enables the PMU Timer for UARTB when set to 1.

Activity for the UARTs is defined as any of the input pins to the UARTs (–CTS, –DSR, –DCD, –RI, SIN), going active, or any of the associated registers being accessed. Activity for the floppy controller is defined as any of its associated registers being accessed. Inactivity would be the absence of any activity. Inactivity time-outs are accomplished via software configurable registers which can be programmed to time the length of inactivity of either of the UARTs or the floppy controller. Upon timing out, the clock to the corresponding block will be turned off.

Bit 4: Allows the PMU Timer for the floppy disk controller to effect the SLP pin when set to 1.

Bit 3: Allows the PMU Timer for UARTA to effect the SLP pin when set to 1.

Bit 2: Allows the PMU Timer for UARTB to affect the SLP pin when set to 1.

Bit 1: Allows the PMU Timers to effect the SLP pin when set to 1.

If bit 1 of index register 34H (PMU) is set to 0, then the SLP pin will be three-stated. If bit 1 of index register 34H (PMU) is set to 1, then the SLP pin will be driven low until all of the enabled PMU Timers have timed out due to inactivity on there respective blocks. Once all of the blocks that are enabled have timed out, the PMU will three-state the SLP output. The SLP output will be driven low upon detection of activity on either UART or the floppy disk controller. The internal timers will always begin timing from the point of inactivity and will be reset upon any resumption of activity. Bit 3 of index register 31H (FDC) is used in conjunction with the floppy disk controller timer (see "UARTs and Floppy Controller Timer" section).

If bit 0 of index register 34H (PMU) is set to 1, then the internal crystal oscillator will be turned off once the SLP pin is high. This will also shut the CLKO, clock out, output off if it is being used. This will be useful in low power applications using a static CPU. The internal crystal oscillator will be turned back on when either the SLP pin goes low or bit 0 of index register 34H (PMU) is set to a 0.

## TABLE 13. HARD DISK INTERFACE

| 30H (INDEX) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| MISCSET Register | Drive Select | –HCSx Enable | Parallel Port Control | | –EMODE Bit | Clock Output Control | | |

## TABLE 14. POWER MANAGEMENT UNIT

| 34H (INDEX) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| PMU Register | FDC Enable | UARTA Enable | UARTB Enable | FDC SLP Control | UARTA SLP CTL | UARTB SLP CTL | SLP Enable | OSC Control |

**UARTS AND FLOPPY CONTROLLER TIMER**

Index registers 31H (FDC), 32H (UARTA), and 33H (UARTB), bits 2-0 are used to set the time-out period for inactivity to the UARTs and floppy disk controller. These may be programmed to one of eight choices from 1 to 256 counts. Each count in the timer is equal to 125 ms, this gives a range from 125 ms to 32 seconds. The timers will begin to count from the point of inactivity and will be reset upon resumption of activity. Once the timer has reached the terminal count it will turn the clock off to the appropriate block.

| | | |
|---|---|---|
| Bits 2-0 | 000 | timer count = 1 |
| | 001 | timer count = 4 |
| | 010 | timer count = 8 |
| | 011 | timer count = 16 |
| | 100 | timer count = 32 |
| | 101 | timer count = 64 |
| | 110 | timer count = 128 |
| | 111 | timer count = 256 |

If bit 3 of index register 31H is set to 1, the floppy motor will be turned off once the floppy timer has reached the terminal count. Upon any subsequent activity, the motor will be turned back on if it was on when the counter reached terminal count. If this bit is set to 0, the motor will remain in the state it was in once the timer reaches terminal count.

**PROGRAMMABLE CLK2 OUTPUT**

The VL82C110 has internal PLL circuitry to provide all necessary internal clocks. When enabled, the VL82C110 also provides a software and hardware configurable clock output that may be used as a CPU input clock. With a single 24 MHz oscillator or crystal input, the VL82C110 will provide a 20, 25, 32, 40, 50, 66, or 80 MHz clock output. This divider is set at power-up through three configuration inputs, C0-C2, or through a software programmable register. This function is also affected by the PMU, see the section "Power Management Unit" for explanation. This function is disabled when the chip is in "compatibility" mode.

| | | |
|---|---|---|
| Bits 2-0 | 000 | Clock output disabled |
| | 001 | 20 MHz clock output |
| | 010 | 25 MHz clock output |
| | 011 | 32 MHz clock output |
| | 100 | 40 MHz clock output |
| | 101 | 50 MHz clock output |
| | 110 | 66 MHz clock output |
| | 111 | 80 MHz clock output |

**OUTPUT DRIVE SELECT**

If bit 7 of index register 30H is set to 1, then D7-D0 will be programmed for 12 mA drive (see Table 17). If this bit is set to 0, these pads will be programmed for 24 mA drive.

**POWER-UP DEFAULTS**

See Table 18 for details.

## TABLE 15. UARTS AND FLOPPY DISK CONTROLLER TIMER

| 31H (INDEX) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| FDC Register | RES | RES | –FDC Enable | Drive Format | Motor Control | PMU Timer Control | | |

| 32H (INDEX) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| UARTA Register | COM3 Address | | UARTA Enable | COM Port Select | | PMU Timer Control | | |

| 33H (INDEX) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| UARTB Register | COM4 Address | | UARTB Enable | COM Port Select | | PMU Timer Control | | |

## TABLE 16. PROGRAMMABLE CLK2 OUTPUT

| 30H (INDEX) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| MISCSET Register | Drive Select | –HCSx Enable | Parallel Port Control | | –EMODE Bit | Clock Output Control | | |

## TABLE 17. OUTPUT DRIVE SELECT

| 30H (INDEX) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| MISCSET Register | Drive Select | –HCSx Enable | Parallel Port Control | | –EMODE Bit | Clock Output Control | | |

## TABLE 18. POWER-UP DEFAULTS

| 30H (INDEX) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| MISCSET Register | 0 | 0 | 0 | 0 | 0 | C2 | C1 | 0 |

| 31H (INDEX) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| FDC Register | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

| 32H (INDEX) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| UARTA Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| 33H (INDEX) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| UARTB Register | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

| 34H (INDEX) | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| PMU Register | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5 V ±5%, VSS = 0 V

"These are preliminary specifications and are subject to change"

| Symbol | Description | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| **Serial Port Transmitter - Figure 1** | | | | | |
| tHR1 | Delay from rising edge of –IOW (WR THR) to reset interrupt | | 175 | ns | 100 pF load |
| tIRS | Delay from THRE reset to transmit start | | 16 | CLK Cycles | Note 2 |
| tSI | Delay from write to THRE | 8 | 24 | CLK Cycles | Note 2 |
| tSTI | Delay from stop to interrupt (THRE) | | 8 | CLK Cycles | Note 2 |
| tIR | Delay from –IOR (RD IIR) to reset interrupt (THRE) | | 250 | ns | 100 pF load |
| **Serial Port Receiver - Figure 2** | | | | | |
| tSINT | Delay from stop to set interrupt | | 1 | CLK Cycles | Note 2 |
| tRINT | Delay from –IOR (RD RBR/RD LSR) to reset interrupt | | 250 | µs | 100 pF load |
| **Serial Port Modem - Figure 3** | | | | | |
| tMDO | Delay from –IOW (WR MCR) to output | | 250 | ns | 100 pF load |
| tSIM | Delay to set interrupt from modem input | | 250 | ns | 100 pF load |
| tRIM | Delay to reset interrupt from –IOR (RS MSR) | | 250 | ns | 100 pF load |
| **Parallel Port - Figure 4** | | | | | |
| tDT | Data time | 1 | | µs | Software controller |
| tSB | Strobe Time | | 500 | µs | Software controller |
| tAD | –ACK delay (busy start to –ACK) | | | µs | Defined by printer |
| tAKD | –ACK delay (busy end to –ACK) | | | µs | Defined by printer |
| tAK | –ACK duration time | | | µs | Defined by printer |
| tBSY | Busy duration time | | | µs | Defined by printer |
| tBSD | Busy delay time | | | µs | Defined by printer |

Notes: 1. All timing specifications apply to pins on both serial channels (e.g., RI refers to both RIA and RIB).
2. CLK cycle refers to external 24 MHz clock divided by 13, e.g., 1.8462 MHz.

**FIGURE 1. SERIAL PORT TRANSMITTER TIMING**

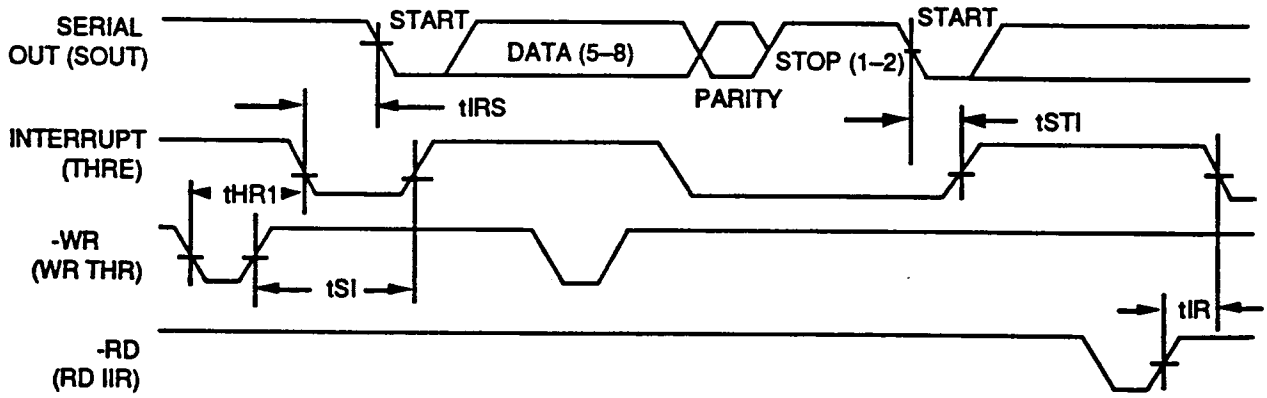



**FIGURE 2. SERIAL PORT RECEIVER TIMING**

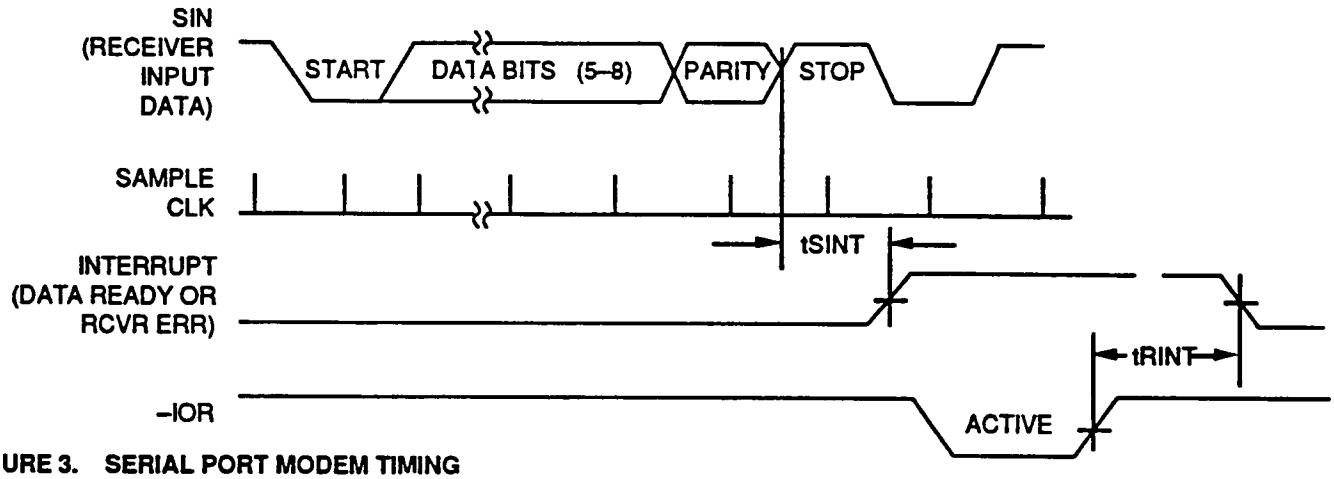



**FIGURE 3. SERIAL PORT MODEM TIMING**

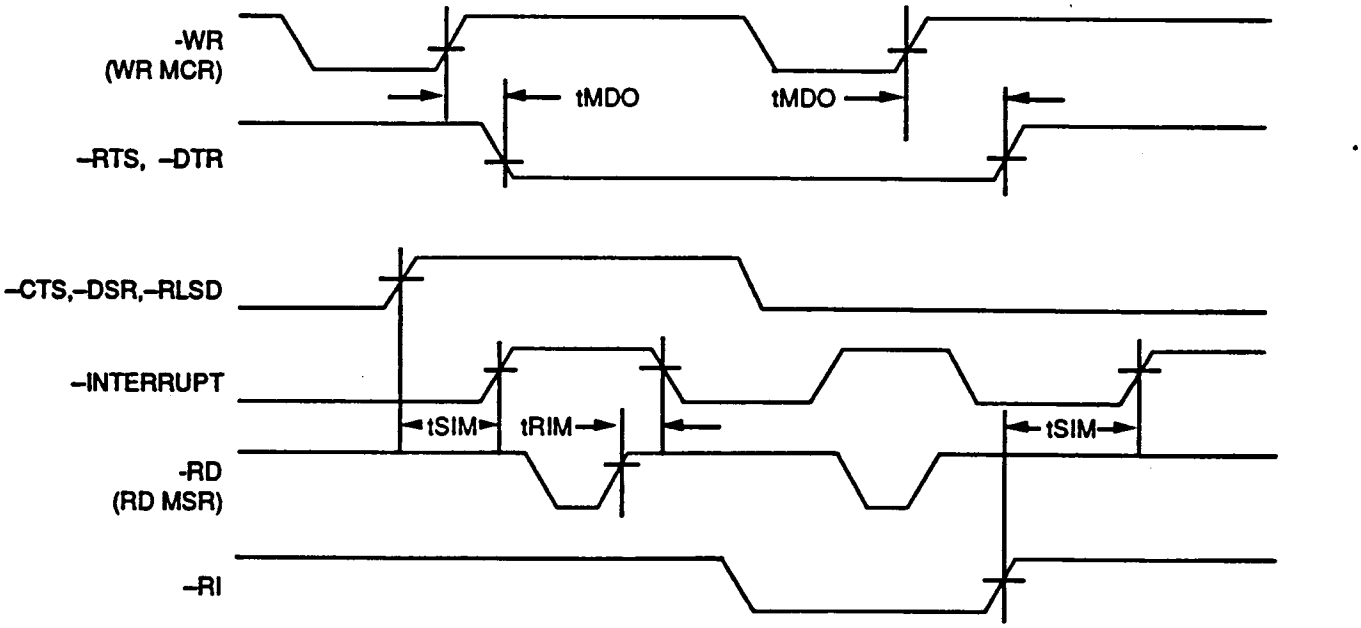


**FIGURE 4. PARALLEL PORT TIMING**

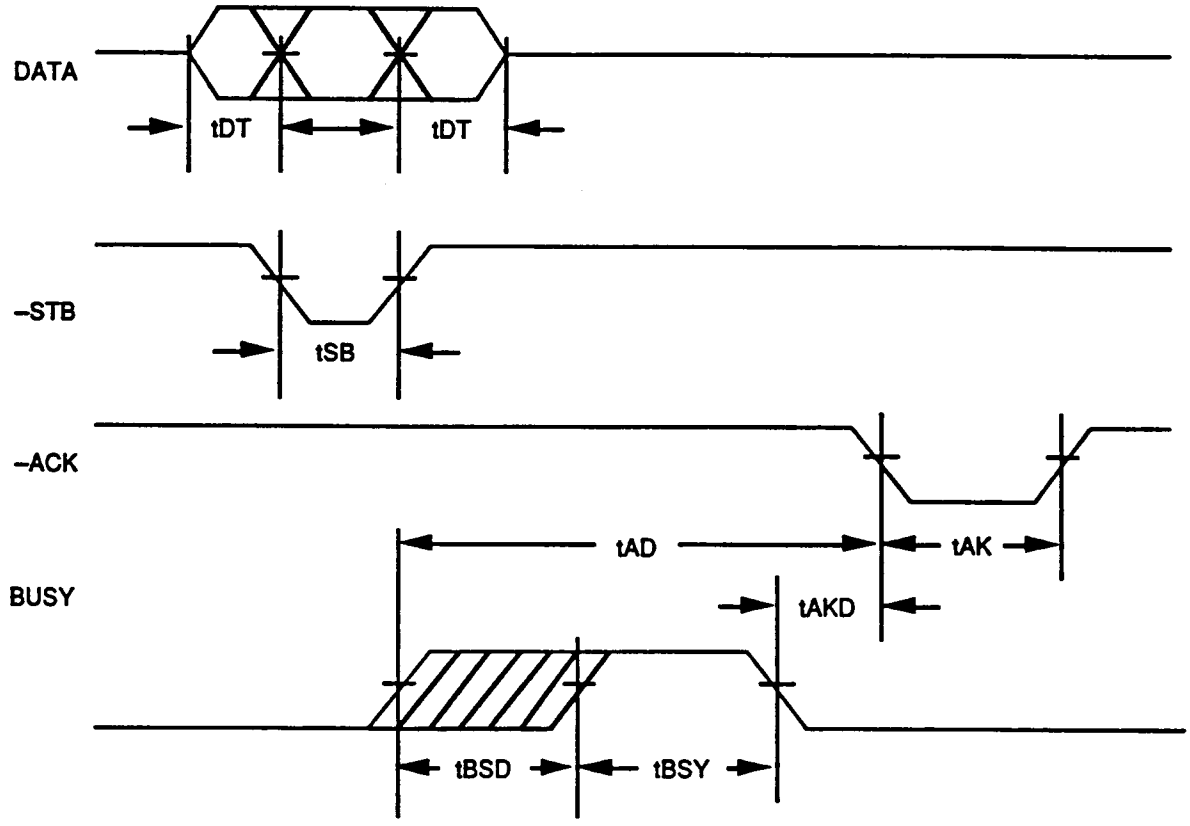
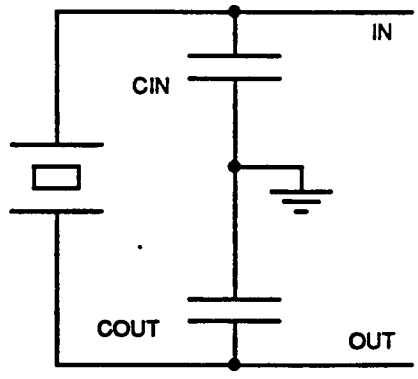



**FIGURE 5. CRYSTAL OSCILLATOR CONFIGURATIONS**




| 24 MHz Parameters | Recommended Crystal |
|---|---|
| CIN = 10 pF | Rs ≤ 50 Ω |
| COUT = 30 pF | Co ≤ 7 pF |
| | Ci ≤ 20 pF |

## ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature: –10°C to + 70°C

Storage Temperature: –65°C to +150°C

Supply Voltage to Ground: –0.5 V to VDD + 0.3 V

Applied Output Voltage: 0.5 V to VDD + 0.3 V

Applied Input Voltage: 0.5 V to 7.0 V

Power Dissipation: 1.0 W

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these on any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## DC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5V ±5 %

| Symbol | Description | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| VILX | Clock input low voltage | –0.5 | 0.8 | V | |
| VIHX | Clock input high voltage | 2.0 | VDD | V | |
| VIL | Input low voltage | –0.5 | 0.8 | V | |
| VIH | Input low voltage | 2.0 | VDD | V | |
| VOL | Output high voltage | | 0.45<br>0.45<br>0.45<br>0.45<br>0.45<br>0.45 | V<br>V<br>V<br>V<br>V<br>V | 8 mA, Note 1<br>12 mA, Note 2<br>12 mA, Note 3, MISCSET7 = 1<br>24 mA, Note 3, MISCSET7 = 0<br>24 mA, Note 4<br>48 mA, Note 5 |
| VOH | Output high voltage | VDD – 0.45<br>VDD – 0.45<br>VDD – 0.45<br>VDD – 0.45 | | V<br>V<br>V<br>V | –2 mA, Note 6<br>–3 mA, Note 2<br>–6 mA, Note 3<br>–8 mA, Note 7 |
| IDDSB | Static supply current | | 10 | mA | VDD = 5.25 V |
| IDDOP | Dynamic supply current | | 3 | mA/MHz | VDD = 5.25 V |
| ILI | Input leakage current | –10 | 10 | µA | VDD = 5.25 V, VSS = 0 V, Note 8 |
| IIL | Input leakage current | –500 | 10 | µA | VDD = 5.25 V, VSS = 0 V, Note 9 |
| IIH | Input leakage current | –10 | 500 | µA | VDD = 5.25 V, VSS = 0 V, Note 10 |

## DC CHARACTERISTICS (Cont): TA = 0°C to +70°C, VDD = 5V ±5 %

| Symbol | Description | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| ILO | Output leakage current | –100 | 100 | µA | VDD = 5.25 V, VSS = 0 V |
| CI | Input or I/O capacitance | | 10 | pF | |
| CO | Output capacitance | | 10 | pF | |

Notes:
1. Pins: –IDHI, SOUTB, –RTSB, –DTRB, –DTRA,–RTSA, SOUTA, CLKO, SLP, –IDLO
2. Pins: PD[7:0], –STB, –AFD, –INIT, –SLIN, IRQP, IRQE, IRQO, IRQF
3. Pins: D7-D0
4. Pins: –HCS0, –HCS1, IDB7, DRQ
5. Pins: –WG, –STP, RPM, –WD, DIR, –DR1, –DR0, –MT1, –MT0, HDSL
6. Pins: –IDHI, SOUTB, –RTSB, –DTRB, –DTRA, –RTSA, SOUTA, –IDLO
7. Pins: CLKO
8. All inputs except for those listed in Notes 9 and 10.
9. Pins: IDB7, –ERR, SLCT, PE, –ACK, BUSY, SINB, –DSRB, –DCDB, –CTSB, –RIB, –RIA, –CTSA, –DCDA, –DSRA, SINA, DC, –RDATA, –PREN, –TR0, –DX, –WPRT
10. Pins: –TRI