



82C556/82C557/82C558N

Viper Notebook Chipset

Data Book

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1.0 Features

CPU Interface

- Fully supports Intel's 3.3V Pentium™ Processor and dual processor configuration at 50, 60, and 66.667MHz
- Supports P54C™, P55C™, K5™, and M1™ processors
- Supports the Cyrix® M1 Processor linear burst mode
- Three chip solution:
 - 82C556 DBC (Data Buffer Controller) in a 160-pin PQFP (Plastic Quad Flat Pack) or 176-pin TQFP (Thin Quad Flat Pack)
 - 82C557 SYSC (System Controller) in a 208-pin PQFP or TQFP
 - 82C558N IPC (Integrated Peripherals Controller) in a 208-pin PQFP or TQFP
- Supports CPU address pipelining

- Support for synchronous and asynchronous SRAMs, pipelined synchronous SRAMs, and Intel standard BSRAMs (BiCMOS SRAMs)
- Support for the Sony SONIC-2WP™ Cache Module
- Programmable cache write policy:
 - Write-back
 - Write-through
 - Adaptive write-back
- Built-in tag auto-invalidation circuitry
- Fully programmable 3-2-2-2 asynchronous cache burst read/write cycles, 3-1-1-1/2-1-1-1 burst read/write support at 66/50MHz
- Options for cacheable, write protected, system and video BIOS

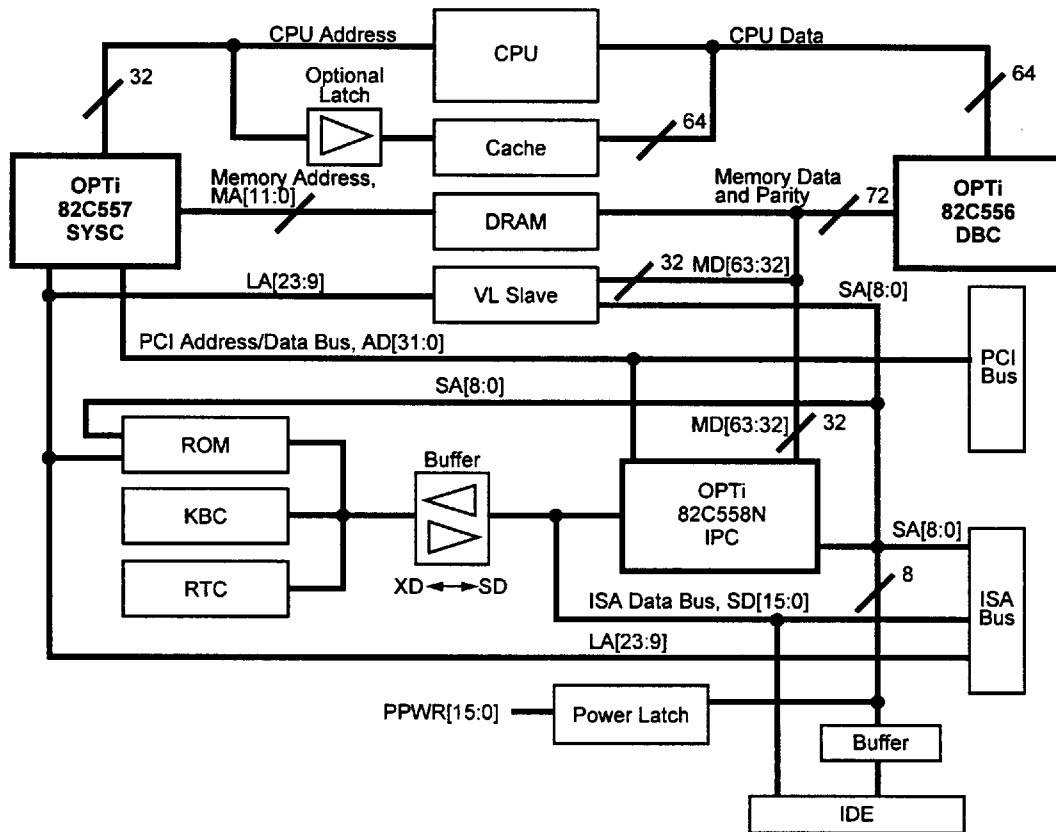
Cache Interface

- Write-back/write-through, direct-mapped cache with size selections: 64KB, 128KB, 256KB, 1MB and 2MB

DRAM Interface

- Supports six banks of 64-bit wide DRAMs with 256KB, 512KB, 1MB, 2MB, 4MB, 8MB and 16MB addressing page mode DRAMs

Figure 1-1 Viper-N System Block Diagram



Features (cont.)

- Supports DRAM configurations up to 512MB
- Supports 3-3-3-3 pipelined DRAM burst cycles
- 64-bit DRAM post write buffer
- Programmable drive currents for the DRAM control signals
- Hidden refresh with CAS-before-RAS refresh supported
- Support for two programmable non-cacheable memory regions

PCI Interface

- Interfaces the CPU and standard buses to both Peripheral Component Interconnect (PCI) and VL bus operating in synchronous/asynchronous modes, with VL bus always running at PCI bus operating frequency
- Supports three PCI masters, one VL slave, and six ISA peripherals
- Supports PCI pre-snoop for PCI masters
- PCI byte/word merge support for CPU accesses to PCI bus, and support for PCI pre-fetch
- Burst mode PCI accesses to local memory supported

Miscellaneous

- Integrated two drive VL-based IDE controller
- Self-refresh supported during Suspend mode
- Support for flash ROM
- Shadow RAM option
- Transparent 8042 emulation for fast CPU reset and Gate A20 generation
- Supports Port 092h, fast Gate A20 and fast reset
- Includes a fully integrated 82C206 with external real-time clock (RTC) interface

2.0 Overview

The OPTi Viper (82C556/557/558N) Notebook Chipset provides a highly integrated solution for fully compatible, high performance PC/AT platforms based on Intel's 3.3V Pentium Processor, Cyrix's M1 Processor, and AMD's K5 Processor. The chipset provides 64-bit core logic, integrated PCI and VL support, and sophisticated power management features. This highly integrated approach supplies the foundation for a cost effective platform without compromising performance. Its feature set furnishes an array of control and status monitoring options that are accessed through a simple and straightforward interface. All major BIOS vendors provide extensive software hooks that allow system designers to integrate their own special features with minimal effort.

The Viper Notebook Chipset is comprised of three chips:

- 82C556 Data Buffer Controller (DBC),
- 82C557 System Controller (SYSC),
- 82C558N Integrated Peripherals Controller (IPC)

2.1 82C556 Data Buffer Controller (DBC)

The 82C556 DBC performs the task of buffering the CPU to the DRAM memory data path. It also performs parity checking.

- CPU to memory data buffer
- CPU to local bus buffer
- Memory to local bus buffer
- 176-pin TQFP or 160-pin PQFP

Figure 4-1 shows a block diagram of the 82C556 DBC.

2.2 82C557 System Controller (SYSC)

The 82C557 SYSC provides the control functions for the host CPU interface, the 64-bit Level-2 (L2) cache, the 64-bit DRAM bus, the VL bus interface, and the PCI interface. The SYSC also controls the data flow between the CPU bus, the DRAM bus, the local buses, and the 8/16-bit ISA bus. The SYSC interprets and translates cycles from the CPU, PCI bus master, ISA master, and DMA to the host memory, local bus slave, PCI bus slave, or ISA bus devices.

- 3.3V CPU interface
- DRAM controller
- L2 cache controller
- L1 cache controller
- PCI interface

- Arbitration logic
- Data bus buffer control (memory data bus to and from host data bus)
- VL bus interface
- 208-pin PQFP or TQFP

Figure 4-2 shows a block diagram of the 82C557 SYSC.

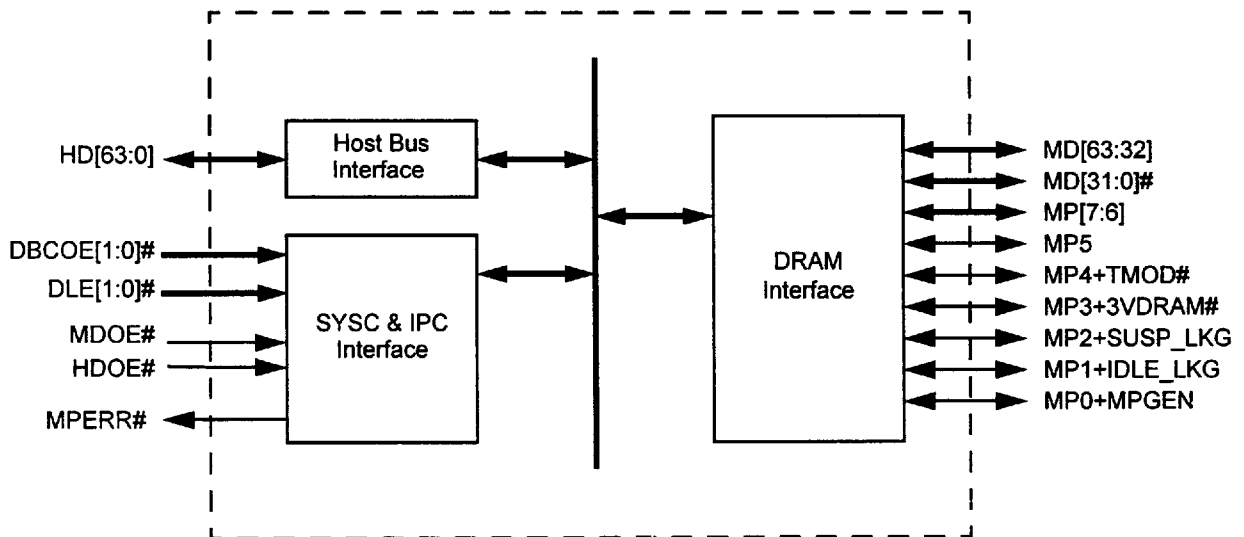
2.3 82C558N Integrated Peripherals Controller (IPC)

The 82C558N Integrated Peripherals Controller (IPC) contains the ISA bus controller and includes an 82C206, RTC interface, DMA controller, PCI arbitration logic, and a sophisticated system power management unit. It also includes buffers and steering control for the 32-bit PCI interface.

- ISA bus controller
- Integrated 82C206 IPC
- CPU thermal management functions
- System power management functions
- PCI local bus interface
- Keyboard emulation of A20M# and CPU warm reset
- Port B and Port 92h Register
- 208-pin PQFP or TQFP

Figure 4-3 shows a block diagram of the 82C558 IPC.

Figure 2-1 82C556 Block Diagram



82C556/82C557/82C558N

Figure 2-2 82C557 Block Diagram

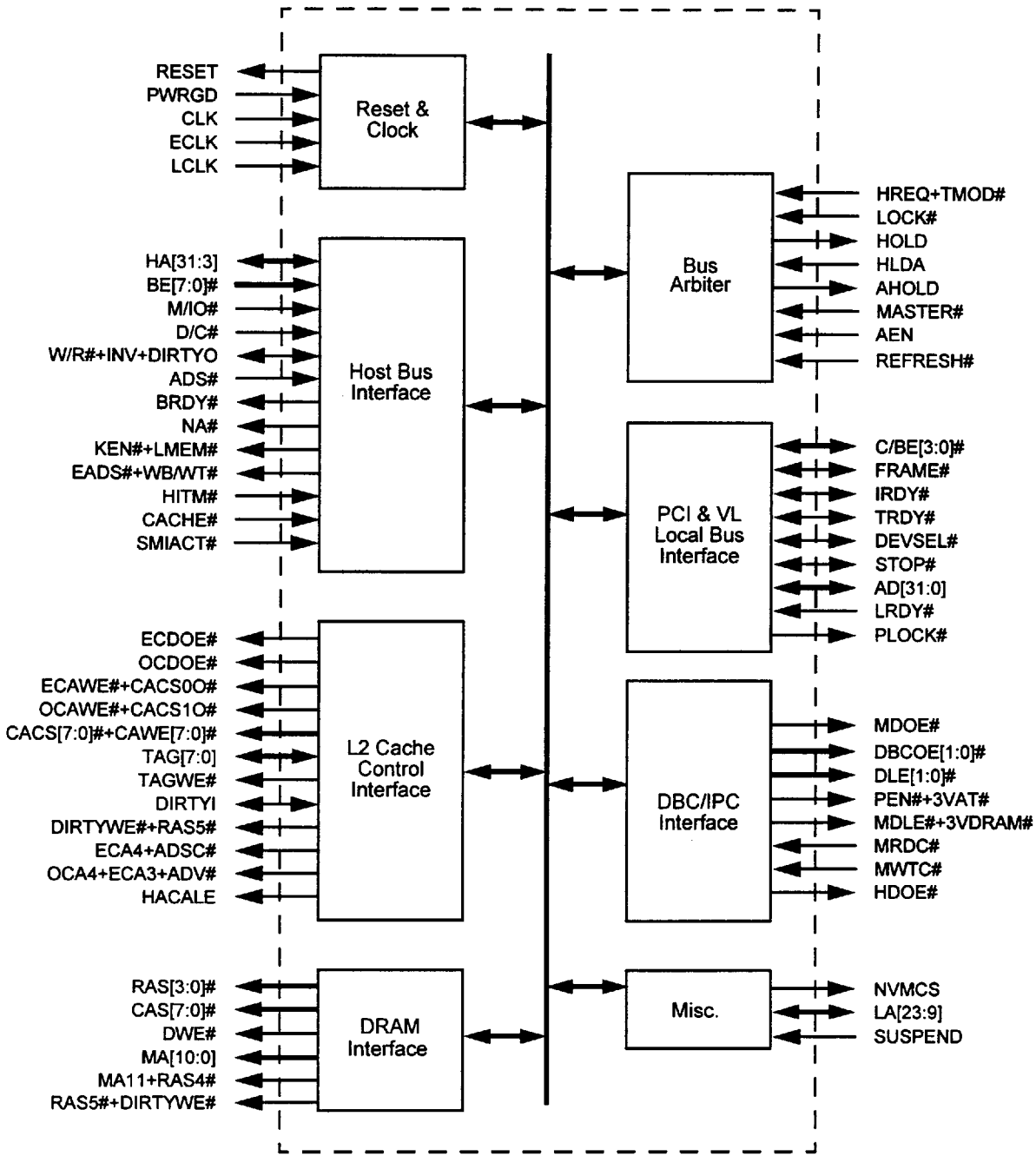
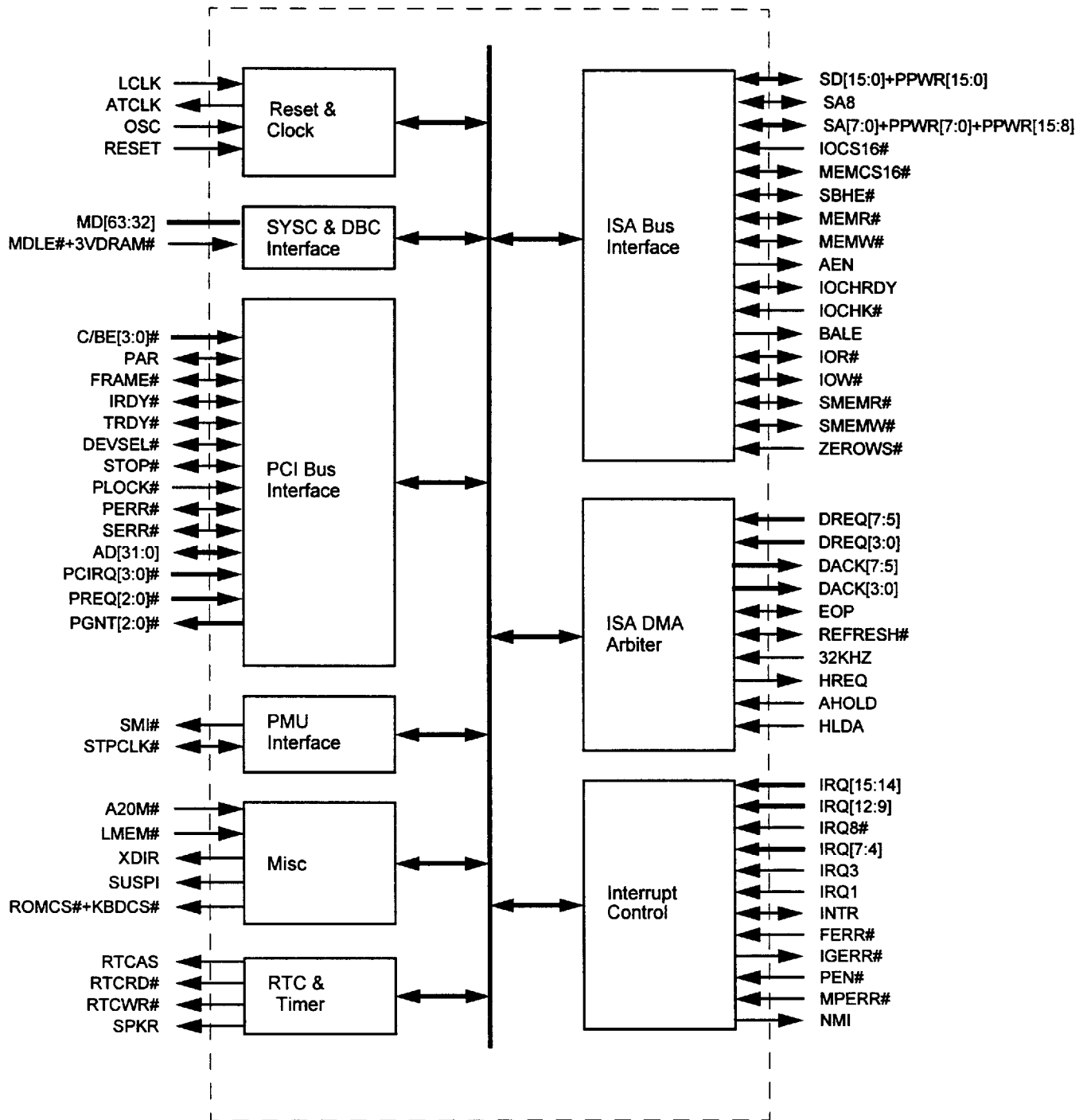


Figure 2-3 82C558N Block Diagram



3.0 Signal Definitions

3.1 Terminology/Nomenclature Conventions

The “#” symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When “#” is not present after the signal name, the signal is asserted when at the high voltage level.

The terms “assertion” and “negation” are used extensively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signals. The term “assert”, or “assertion” indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term “negate”, or “negation” indicates that a signal is inactive.

Some of the pin functions in the Viper-N Chipset are time-multiplexed, some have strap options, and some are selected

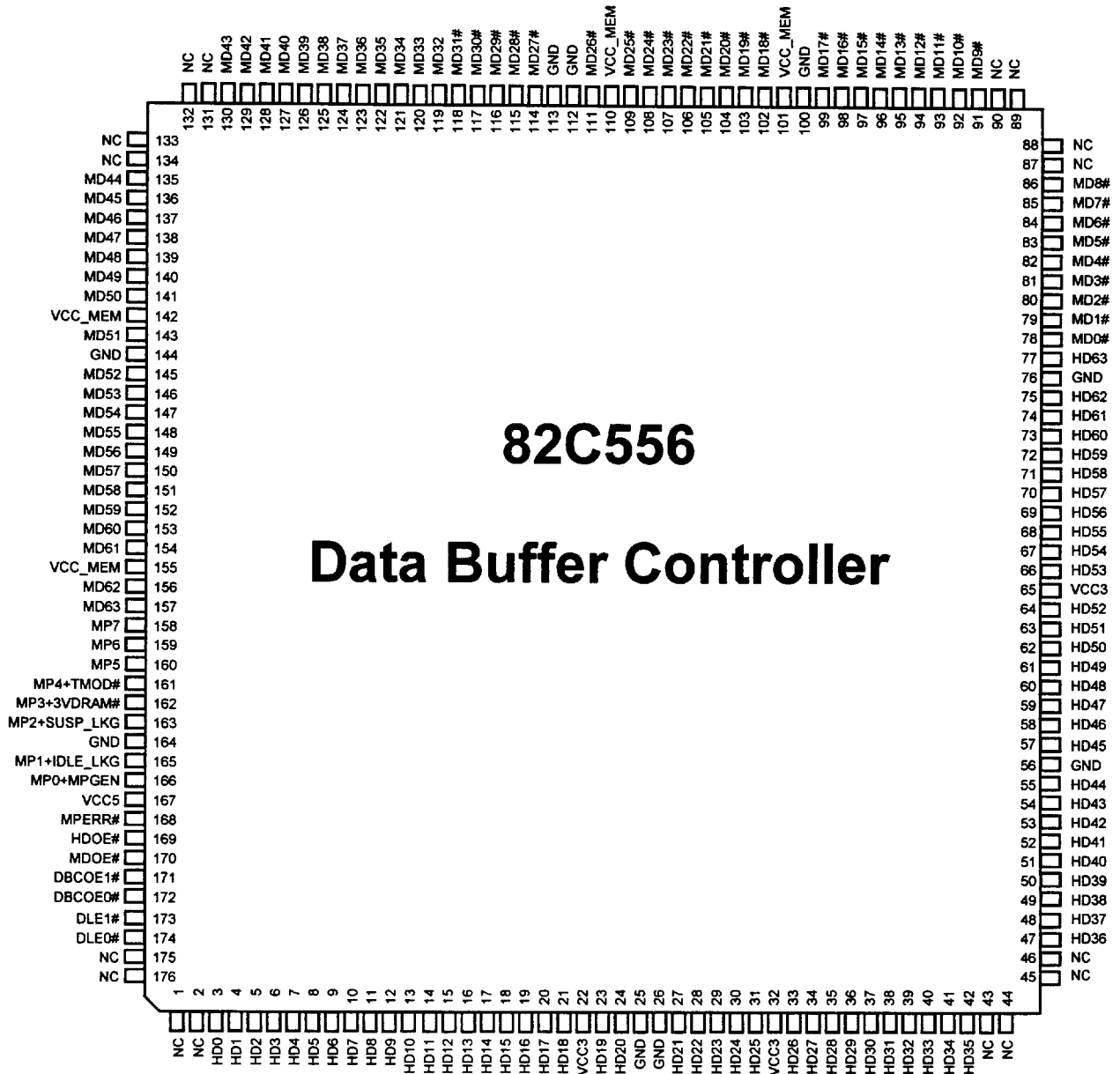
via register programming. Included in each device's signal description is a column titled “Selected By” which explains how to implement/invoke the various functions that a pin may have. The terms PCIDV0, PCIDV1, and SYSCFG relate to registers located in the PCI Configuration Register Spaces and System Configuration Register Space of the Viper-N Chipset. Refer to Section 5.0, “Register Descriptions” for more details regarding these register spaces and their access mechanisms.

The tables in this section use several common abbreviations. Table 3-1 lists the mnemonics and their meanings. Note that TTL/CMOS/Schmitt-trigger levels pertain to inputs only. Outputs are driven at CMOS levels.

Table 3-1 Signal Definitions Legend

Mnemonic	Description
CMOS	CMOS-level compatible
Ext	External
G	Ground
Int	Internal
I/O	Input/Output
OD	Open drain
P	Power
PD	Pull-down resistor
PU	Pull-up resistor
S	Schmitt-trigger
TTL	TTL-level compatible
VCC3	3.3V power plane only
VCC5	5.0V power plane only
VCC_AT	ISA bus power plane, 3.3V or 5.0V
VCC_MEM	Memory power plane, 3.3V or 5.0V

Figure 3-1 82C556 Pin Diagram (176-Pin TQFP)



82C556/82C557/82C558N

Table 3-2 82C556 Numerical Pin Cross-Reference List (176-Pin TQFP)

Pin No.	Pin Name	Signal Type	Drive (mA)	Power Plane
1	NC			
2	NC			
3	HD0	I/O-TTL	4	VCC3
4	HD1	I/O-TTL	4	VCC3
5	HD2	I/O-TTL	4	VCC3
6	HD3	I/O-TTL	4	VCC3
7	HD4	I/O-TTL	4	VCC3
8	HD5	I/O-TTL	4	VCC3
9	HD6	I/O-TTL	4	VCC3
10	HD7	I/O-TTL	4	VCC3
11	HD8	I/O-TTL	4	VCC3
12	HD9	I/O-TTL	4	VCC3
13	HD10	I/O-TTL	4	VCC3
14	HD11	I/O-TTL	4	VCC3
15	HD12	I/O-TTL	4	VCC3
16	HD13	I/O-TTL	4	VCC3
17	HD14	I/O-TTL	4	VCC3
18	HD15	I/O-TTL	4	VCC3
19	HD16	I/O-TTL	4	VCC3
20	HD17	I/O-TTL	4	VCC3
21	HD18	I/O-TTL	4	VCC3
22	VCC3	I-P		
23	HD19	I/O-TTL	4	VCC3
24	HD20	I/O-TTL	4	VCC3
25	GND	I-G		
26	GND	I-G		
27	HD21	I/O-TTL	4	VCC3
28	HD22	I/O-TTL	4	VCC3
29	HD23	I/O-TTL	4	VCC3
30	HD24	I/O-TTL	4	VCC3
31	HD25	I/O-TTL	4	VCC3
32	VCC3	I-P		
33	HD26	I/O-TTL	4	VCC3
34	HD27	I/O-TTL	4	VCC3
35	HD28	I/O-TTL	4	VCC3
36	HD29	I/O-TTL	4	VCC3
37	HD30	I/O-TTL	4	VCC3
38	HD31	I/O-TTL	4	VCC3
39	HD32	I/O-TTL	4	VCC3
40	HD33	I/O-TTL	4	VCC3
41	HD34	I/O-TTL	4	VCC3
42	HD35	I/O-TTL	4	VCC3
43	NC			
44	NC			
45	NC			
46	NC			
47	HD36	I/O-TTL	4	VCC3
48	HD37	I/O-TTL	4	VCC3
49	HD38	I/O-TTL	4	VCC3
50	HD39	I/O-TTL	4	VCC3
51	HD40	I/O-TTL	4	VCC3
52	HD41	I/O-TTL	4	VCC3
53	HD42	I/O-TTL	4	VCC3
54	HD43	I/O-TTL	4	VCC3
55	HD44	I/O-TTL	4	VCC3
56	GND	I-G		
57	HD45	I/O-TTL	4	VCC3
58	HD46	I/O-TTL	4	VCC3
59	HD47	I/O-TTL	4	VCC3
60	HD48	I/O-TTL	4	VCC3
61	HD49	I/O-TTL	4	VCC3
62	HD50	I/O-TTL	4	VCC3
63	HD51	I/O-TTL	4	VCC3
64	HD52	I/O-TTL	4	VCC3
65	VCC3	I-P		
66	HD53	I/O-TTL	4	VCC3
67	HD54	I/O-TTL	4	VCC3
68	HD55	I/O-TTL	4	VCC3
69	HD56	I/O-TTL	4	VCC3
70	HD57	I/O-TTL	4	VCC3
71	HD58	I/O-TTL	4	VCC3
72	HD59	I/O-TTL	4	VCC3
73	HD60	I/O-TTL	4	VCC3
74	HD61	I/O-TTL	4	VCC3
75	HD62	I/O-TTL	4	VCC3
76	GND	I-G		
77	HD63	I/O-TTL	4	VCC3
78	MD0#	I/O-CMOS	4	VCC_MEM
79	MD1#	I/O-CMOS	4	VCC_MEM
80	MD2#	I/O-CMOS	4	VCC_MEM
81	MD3#	I/O-CMOS	4	VCC_MEM
82	MD4#	I/O-CMOS	4	VCC_MEM
83	MD5#	I/O-CMOS	4	VCC_MEM
84	MD6#	I/O-CMOS	4	VCC_MEM
85	MD7#	I/O-CMOS	4	VCC_MEM
86	MD8#	I/O-CMOS	4	VCC_MEM
87	NC			
88	NC			
89	NC			
90	NC			
91	MD9#	I/O-CMOS	4	VCC_MEM
92	MD10#	I/O-CMOS	4	VCC_MEM
93	MD11#	I/O-CMOS	4	VCC_MEM
94	MD12#	I/O-CMOS	4	VCC_MEM
95	MD13#	I/O-CMOS	4	VCC_MEM
96	MD14#	I/O-CMOS	4	VCC_MEM
97	MD15#	I/O-CMOS	4	VCC_MEM
98	MD16#	I/O-CMOS	4	VCC_MEM
99	MD17#	I/O-CMOS	4	VCC_MEM
100	GND	I-G		
101	VCC_MEM	I-P		
102	MD18#	I/O-CMOS	4	VCC_MEM
103	MD19#	I/O-CMOS	4	VCC_MEM
104	MD20#	I/O-CMOS	4	VCC_MEM
105	MD21#	I/O-CMOS	4	VCC_MEM
106	MD22#	I/O-CMOS	4	VCC_MEM
107	MD23#	I/O-CMOS	4	VCC_MEM
108	MD24#	I/O-CMOS	4	VCC_MEM
109	MD25#	I/O-CMOS	4	VCC_MEM
110	VCC_MEM	I-P		
111	MD26#	I/O-CMOS	4	VCC_MEM
112	GND	I-G		
113	GND	I-G		
114	MD27#	I/O-CMOS	4	VCC_MEM
115	MD28#	I/O-CMOS	4	VCC_MEM
116	MD29#	I/O-CMOS	4	VCC_MEM
117	MD30#	I/O-CMOS	4	VCC_MEM
118	MD31#	I/O-CMOS	4	VCC_MEM
119	MD32	I/O-CMOS	4	VCC_MEM
120	MD33	I/O-CMOS	4	VCC_MEM
121	MD34	I/O-CMOS	4	VCC_MEM
122	MD35	I/O-CMOS	4	VCC_MEM
123	MD36	I/O-CMOS	4	VCC_MEM
124	MD37	I/O-CMOS	4	VCC_MEM
125	MD38	I/O-CMOS	4	VCC_MEM
126	MD39	I/O-CMOS	4	VCC_MEM
127	MD40	I/O-CMOS	4	VCC_MEM
128	MD41	I/O-CMOS	4	VCC_MEM
129	MD42	I/O-CMOS	4	VCC_MEM
130	MD43	I/O-CMOS	4	VCC_MEM
131	NC			
132	NC			
133	NC			
134	NC			
135	MD44	I/O-CMOS	4	VCC_MEM
136	MD45	I/O-CMOS	4	VCC_MEM
137	MD46	I/O-CMOS	4	VCC_MEM
138	MD47	I/O-CMOS	4	VCC_MEM
139	MD48	I/O-CMOS	4	VCC_MEM
140	MD49	I/O-CMOS	4	VCC_MEM
141	MD50	I/O-CMOS	4	VCC_MEM
142	VCC_MEM	I-P		
143	MD51	I/O-CMOS	4	VCC_MEM
144	GND	I-G		
145	MD52	I/O-CMOS	4	VCC_MEM
146	MD53	I/O-CMOS	4	VCC_MEM
147	MD54	I/O-CMOS	4	VCC_MEM
148	MD55	I/O-CMOS	4	VCC_MEM
149	MD56	I/O-CMOS	4	VCC_MEM
150	MD57	I/O-CMOS	4	VCC_MEM
151	MD58	I/O-CMOS	4	VCC_MEM
152	MD59	I/O-CMOS	4	VCC_MEM
153	MD60	I/O-CMOS	4	VCC_MEM
154	MD61	I/O-CMOS	4	VCC_MEM
155	VCC_MEM	I-P	4	
156	MD62	I/O-CMOS	4	VCC_MEM
157	MD63	I/O-CMOS	4	VCC_MEM
158	MP7	I/O-CMOS	4	VCC_MEM
159	MP6	I/O-CMOS	4	VCC_MEM
160	MP5	I/O-CMOS	4	VCC_MEM
161	MP4	I/O-CMOS	4	VCC_MEM
	TMOD#			
162	MP3	I/O-CMOS	4	VCC_MEM
	3VDRAM#			
163	MP2	I/O-CMOS	4	VCC_MEM
	SUSP_LKG			
164	GND	I-G		
165	MP1	I/O-CMOS	4	VCC_MEM
	IDLE_LKG			
166	MP0	I/O-CMOS	4	VCC_MEM
	MPGEN			
167	VCC5	I-P		
168	MPERR#	O	4	VCC5
169	HDOE#	I-TTL		VCC5
170	MDOE#	I-TTL		VCC5
171	DBC0E1#	I-TTL		VCC5
172	DBC0E0#	I-TTL		VCC5
173	DLE1#	I-TTL		VCC5
174	DLE0#	I-TTL		VCC5
175	NC			
176	NC			



Table 3-3 82C556 Alphabetical Pin Cross-Reference List (176-Pin TQFP)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
DBCOE0#	172	HD24	30	HD61	74	MD33	120	MP2	163
DBCOE1#	171	HD25	31	HD62	75	MD34	121	SUSP_LKG	
DLE0#	174	HD26	33	HD63	77	MD35	122	MP3	162
DLE1#	173	HD27	34	HDOE#	169	MD36	123	3VDRAM#	
GND	25	HD28	35	MD0#	78	MD37	124	MP4	161
GND	26	HD29	36	MD1#	79	MD38	125	TMOD#	
GND	56	HD30	37	MD2#	80	MD39	126	MP5	160
GND	76	HD31	38	MD3#	81	MD40	127	MP6	159
GND	100	HD32	39	MD4#	82	MD41	128	MP7	158
GND	112	HD33	40	MD5#	83	MD42	129	MPERR#	168
GND	113	HD34	41	MD6#	84	MD43	130	NC	1
GND	144	HD35	42	MD7#	85	MD44	135	NC	2
GND	164	HD36	47	MD8#	86	MD45	136	NC	43
HD0	3	HD37	48	MD9#	91	MD46	137	NC	44
HD1	4	HD38	49	MD10#	92	MD47	138	NC	45
HD2	5	HD39	50	MD11#	93	MD48	139	NC	46
HD3	6	HD40	51	MD12#	94	MD49	140	NC	87
HD4	7	HD41	52	MD13#	95	MD50	141	NC	88
HD5	8	HD42	53	MD14#	96	MD51	143	NC	89
HD6	9	HD43	54	MD15#	97	MD52	145	NC	90
HD7	10	HD44	55	MD16#	98	MD53	146	NC	131
HD8	11	HD45	57	MD17#	99	MD54	147	NC	132
HD9	12	HD46	58	MD18#	102	MD55	148	NC	133
HD10	13	HD47	59	MD19#	103	MD56	149	NC	134
HD11	14	HD48	60	MD20#	104	MD57	150	NC	175
HD12	15	HD49	61	MD21#	105	MD58	151	NC	176
HD13	16	HD50	62	MD22#	106	MD59	152	VCC3	22
HD14	17	HD51	63	MD23#	107	MD60	153	VCC3	32
HD15	18	HD52	64	MD24#	108	MD61	154	VCC3	65
HD16	19	HD53	66	MD25#	109	MD62	156	VCC5	167
HD17	20	HD54	67	MD26#	111	MD63	157	VCC_MEM	101
HD18	21	HD55	68	MD27#	114	MDOE#	170	VCC_MEM	110
HD19	23	HD56	69	MD28#	115	MP0	166	VCC_MEM	142
HD20	24	HD57	70	MD29#	116	MPGEN		VCC_MEM	155
HD21	27	HD58	71	MD30#	117	MP1	165		
HD22	28	HD59	72	MD31#	118	IDLE_LKG			
HD23	29	HD60	73	MD32	119				



82C556/82C557/82C558N

Figure 3-2 82C556 Pin Diagram (160-Pin PQFP)

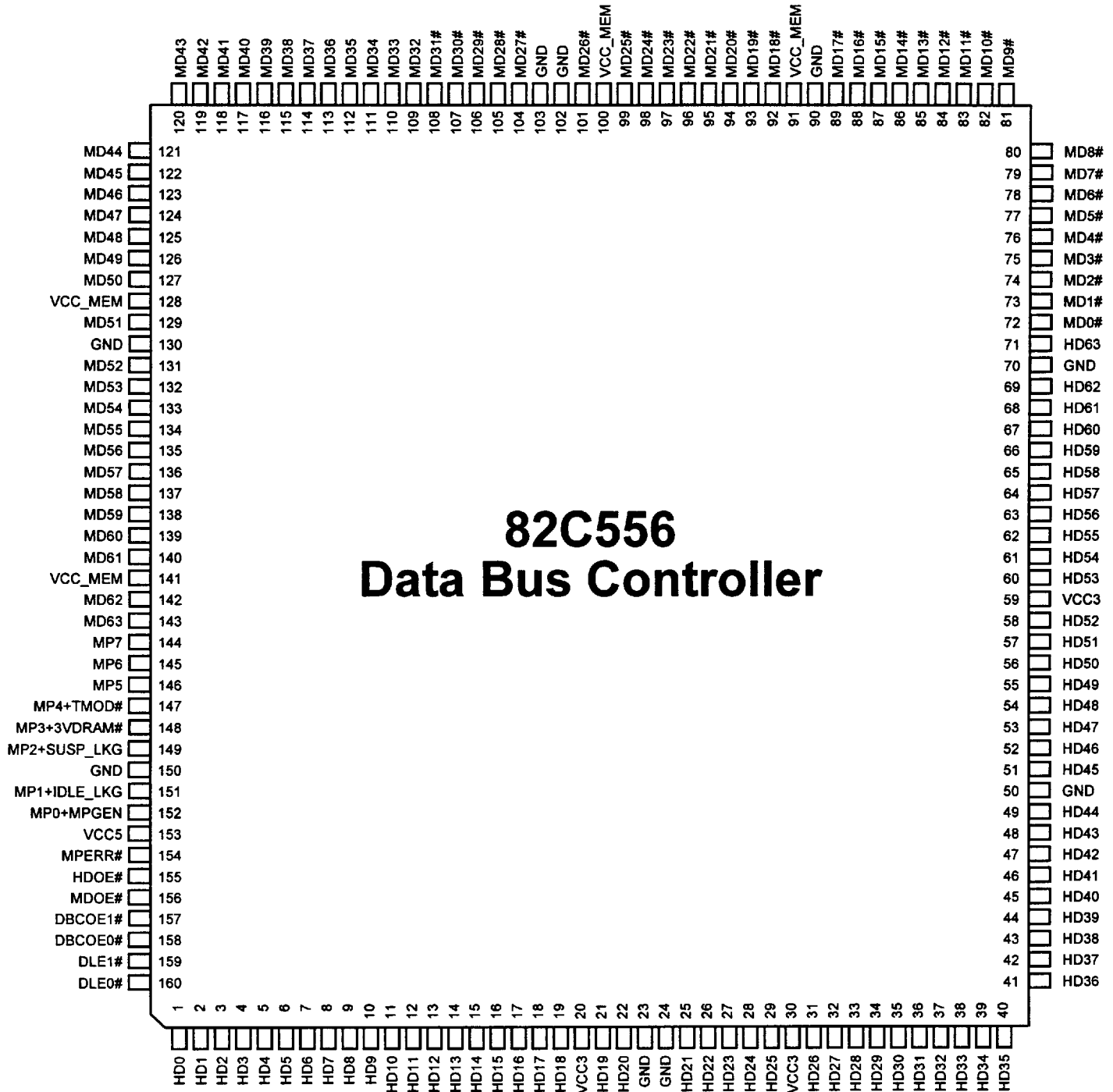


Table 3-4 82C556 Numerical Pin Cross-Reference List (160-Pin PQFP)

Pin No.	Pin Name	Signal Type	Drive (mA)	Power Plane
1	HD0	I/O-TTL	4	VCC3
2	HD1	I/O-TTL	4	VCC3
3	HD2	I/O-TTL	4	VCC3
4	HD3	I/O-TTL	4	VCC3
5	HD4	I/O-TTL	4	VCC3
6	HD5	I/O-TTL	4	VCC3
7	HD6	I/O-TTL	4	VCC3
8	HD7	I/O-TTL	4	VCC3
9	HD8	I/O-TTL	4	VCC3
10	HD9	I/O-TTL	4	VCC3
11	HD10	I/O-TTL	4	VCC3
12	HD11	I/O-TTL	4	VCC3
13	HD12	I/O-TTL	4	VCC3
14	HD13	I/O-TTL	4	VCC3
15	HD14	I/O-TTL	4	VCC3
16	HD15	I/O-TTL	4	VCC3
17	HD16	I/O-TTL	4	VCC3
18	HD17	I/O-TTL	4	VCC3
19	HD18	I/O-TTL	4	VCC3
20	VCC3	I-P		
21	HD19	I/O-TTL	4	VCC3
22	HD20	I/O-TTL	4	VCC3
23	GND	I-G		
24	GND	I-G		
25	HD21	I/O-TTL	4	VCC3
26	HD22	I/O-TTL	4	VCC3
27	HD23	I/O-TTL	4	VCC3
28	HD24	I/O-TTL	4	VCC3
29	HD25	I/O-TTL	4	VCC3
30	VCC3	I-P		
31	HD26	I/O-TTL	4	VCC3
32	HD27	I/O-TTL	4	VCC3
33	HD28	I/O-TTL	4	VCC3
34	HD29	I/O-TTL	4	VCC3
35	HD30	I/O-TTL	4	VCC3
36	HD31	I/O-TTL	4	VCC3
37	HD32	I/O-TTL	4	VCC3
38	HD33	I/O-TTL	4	VCC3
39	HD34	I/O-TTL	4	VCC3
40	HD35	I/O-TTL	4	VCC3
41	HD36	I/O-TTL	4	VCC3
42	HD37	I/O-TTL	4	VCC3
43	HD38	I/O-TTL	4	VCC3
44	HD39	I/O-TTL	4	VCC3
45	HD40	I/O-TTL	4	VCC3
46	HD41	I/O-TTL	4	VCC3
47	HD42	I/O-TTL	4	VCC3
48	HD43	I/O-TTL	4	VCC3
49	HD44	I/O-TTL	4	VCC3
50	GND	I-G		
51	HD45	I/O-TTL	4	VCC3
52	HD46	I/O-TTL	4	VCC3
53	HD47	I/O-TTL	4	VCC3
54	HD48	I/O-TTL	4	VCC3
55	HD49	I/O-TTL	4	VCC3

Pin No.	Pin Name	Signal Type	Drive (mA)	Power Plane
56	HD50	I/O-TTL	4	VCC3
57	HD51	I/O-TTL	4	VCC3
58	HD52	I/O-TTL	4	VCC3
59	VCC3	I-P		
60	HD53	I/O-TTL	4	VCC3
61	HD54	I/O-TTL	4	VCC3
62	HD55	I/O-TTL	4	VCC3
63	HD56	I/O-TTL	4	VCC3
64	HD57	I/O-TTL	4	VCC3
65	HD58	I/O-TTL	4	VCC3
66	HD59	I/O-TTL	4	VCC3
67	HD60	I/O-TTL	4	VCC3
68	HD61	I/O-TTL	4	VCC3
69	HD62	I/O-TTL	4	VCC3
70	GND	I-G		
71	HD63	I/O-TTL	4	VCC3
72	MD0#	I/O-CMOS	4	VCC_MEM
73	MD1#	I/O-CMOS	4	VCC_MEM
74	MD2#	I/O-CMOS	4	VCC_MEM
75	MD3#	I/O-CMOS	4	VCC_MEM
76	MD4#	I/O-CMOS	4	VCC_MEM
77	MD5#	I/O-CMOS	4	VCC_MEM
78	MD6#	I/O-CMOS	4	VCC_MEM
79	MD7#	I/O-CMOS	4	VCC_MEM
80	MD8#	I/O-CMOS	4	VCC_MEM
81	MD9#	I/O-CMOS	4	VCC_MEM
82	MD10#	I/O-CMOS	4	VCC_MEM
83	MD11#	I/O-CMOS	4	VCC_MEM
84	MD12#	I/O-CMOS	4	VCC_MEM
85	MD13#	I/O-CMOS	4	VCC_MEM
86	MD14#	I/O-CMOS	4	VCC_MEM
87	MD15#	I/O-CMOS	4	VCC_MEM
88	MD16#	I/O-CMOS	4	VCC_MEM
89	MD17#	I/O-CMOS	4	VCC_MEM
90	GND	I-G		
91	VCC_MEM	I-P		
92	MD18#	I/O-CMOS	4	VCC_MEM
93	MD19#	I/O-CMOS	4	VCC_MEM
94	MD20#	I/O-CMOS	4	VCC_MEM
95	MD21#	I/O-CMOS	4	VCC_MEM
96	MD22#	I/O-CMOS	4	VCC_MEM
97	MD23#	I/O-CMOS	4	VCC_MEM
98	MD24#	I/O-CMOS	4	VCC_MEM
99	MD25#	I/O-CMOS	4	VCC_MEM
100	VCC_MEM	I-P		
101	MD26#	I/O-CMOS	4	VCC_MEM
102	GND	I-G		
103	GND	I-G		
104	MD27#	I/O-CMOS	4	VCC_MEM
105	MD28#	I/O-CMOS	4	VCC_MEM
106	MD29#	I/O-CMOS	4	VCC_MEM
107	MD30#	I/O-CMOS	4	VCC_MEM
108	MD31#	I/O-CMOS	4	VCC_MEM
109	MD32	I/O-CMOS	4	VCC_MEM
110	MD33	I/O-CMOS	4	VCC_MEM

Pin No.	Pin Name	Signal Type	Drive (mA)	Power Plane
111	MD34	I/O-CMOS	4	VCC_MEM
112	MD35	I/O-CMOS	4	VCC_MEM
113	MD36	I/O-CMOS	4	VCC_MEM
114	MD37	I/O-CMOS	4	VCC_MEM
115	MD38	I/O-CMOS	4	VCC_MEM
116	MD39	I/O-CMOS	4	VCC_MEM
117	MD40	I/O-CMOS	4	VCC_MEM
118	MD41	I/O-CMOS	4	VCC_MEM
119	MD42	I/O-CMOS	4	VCC_MEM
120	MD43	I/O-CMOS	4	VCC_MEM
121	MD44	I/O-CMOS	4	VCC_MEM
122	MD45	I/O-CMOS	4	VCC_MEM
123	MD46	I/O-CMOS	4	VCC_MEM
124	MD47	I/O-CMOS	4	VCC_MEM
125	MD48	I/O-CMOS	4	VCC_MEM
126	MD49	I/O-CMOS	4	VCC_MEM
127	MD50	I/O-CMOS	4	VCC_MEM
128	VCC_MEM	I-P		
129	MD51	I/O-CMOS	4	VCC_MEM
130	GND	I-G		
131	MD52	I/O-CMOS	4	VCC_MEM
132	MD53	I/O-CMOS	4	VCC_MEM
133	MD54	I/O-CMOS	4	VCC_MEM
134	MD55	I/O-CMOS	4	VCC_MEM
135	MD56	I/O-CMOS	4	VCC_MEM
136	MD57	I/O-CMOS	4	VCC_MEM
137	MD58	I/O-CMOS	4	VCC_MEM
138	MD59	I/O-CMOS	4	VCC_MEM
139	MD60	I/O-CMOS	4	VCC_MEM
140	MD61	I/O-CMOS	4	VCC_MEM
141	VCC_MEM	I-P	4	
142	MD62	I/O-CMOS	4	VCC_MEM
143	MD63	I/O-CMOS	4	VCC_MEM
144	MP7	I/O-CMOS	4	VCC_MEM
145	MP6	I/O-CMOS	4	VCC_MEM
146	MP5	I/O-CMOS	4	VCC_MEM
147	MP4	I/O-CMOS	4	VCC_MEM
	TMOD#			
148	MP3	I/O-CMOS	4	VCC_MEM
	3VDRAM#			
149	MP2	I/O-CMOS	4	VCC_MEM
	SUSP_LKG			
150	GND	I-G		
151	MP1	I/O-CMOS	4	VCC_MEM
	IDLE_LKG			
152	MP0	I/O-CMOS	4	VCC_MEM
	MPGEN			
153	VCC5	I-P		
154	MPERR#	O	4	VCC5
155	HDOE#	I-TTL		VCC5
156	MDOE#	I-TTL		VCC5
157	DBCOE1#	I-TTL		VCC5
158	DBCOE0#	I-TTL		VCC5
159	DLE1#	I-TTL		VCC5
160	DLE0#	I-TTL		VCC5



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Table 3-5 82C556 Alphabetical Pin Cross-Reference List (160-Pin PQFP)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
DBC0E0#	158	HD20	22	HD53	60	MD21#	95	MD54	133
DBC0E1#	157	HD21	25	HD54	61	MD22#	96	MD55	134
DLE0#	160	HD22	26	HD55	62	MD23#	97	MD56	135
DLE1#	159	HD23	27	HD56	63	MD24#	98	MD57	136
GND	23	HD24	28	HD57	64	MD25#	99	MD58	137
GND	24	HD25	29	HD58	65	MD26#	101	MD59	138
GND	50	HD26	31	HD59	66	MD27#	104	MD60	139
GND	70	HD27	32	HD60	67	MD28#	105	MD61	140
GND	90	HD28	33	HD61	68	MD29#	106	MD62	142
GND	102	HD29	34	HD62	69	MD30#	107	MD63	143
GND	103	HD30	35	HD63	71	MD31#	108	MDOE#	156
GND	130	HD31	36	HDOE#	155	MD32	109	MP0	152
GND	150	HD32	37	MD0#	72	MD33	110	MPGEN	
HD0	1	HD33	38	MD1#	73	MD34	111	MP1	151
HD1	2	HD34	39	MD2#	74	MD35	112	IDLE_LKG	
HD2	3	HD35	40	MD3#	75	MD36	113	MP2	149
HD3	4	HD36	41	MD4#	76	MD37	114	SUSP_LKG	
HD4	5	HD37	42	MD5#	77	MD38	115	MP3	148
HD5	6	HD38	43	MD6#	78	MD39	116	3VDRAM#	
HD6	7	HD39	44	MD7#	79	MD40	117	MP4	147
HD7	8	HD40	45	MD8#	80	MD41	118	TMOD#	
HD8	9	HD41	46	MD9#	81	MD42	119	MP5	146
HD9	10	HD42	47	MD10#	82	MD43	120	MP6	145
HD10	11	HD43	48	MD11#	83	MD44	121	MP7	144
HD11	12	HD44	49	MD12#	84	MD45	122	MPERR#	154
HD12	13	HD45	51	MD13#	85	MD46	123	VCC3	20
HD13	14	HD46	52	MD14#	86	MD47	124	VCC3	30
HD14	15	HD47	53	MD15#	87	MD48	125	VCC3	59
HD15	16	HD48	54	MD16#	88	MD49	126	VCC5	153
HD16	17	HD49	55	MD17#	89	MD50	127	VCC_MEM	91
HD17	18	HD50	56	MD18#	92	MD51	129	VCC_MEM	100
HD18	19	HD51	57	MD19#	93	MD52	131	VCC_MEM	128
HD19	21	HD52	58	MD20#	94	MD53	132	VCC_MEM	141



3.2 82C556 Signal Descriptions

3.2.1 Host Bus Interface Signals

Signal Name	Pin No. 176 TQFP	Pin No. 160 PQFP	Signal Type (Drive)	Signal Description
HD[63:0]	77, 75:66, 64:57, 55:47, 42:33, 31:27, 24, 23, 21:3	71, 69:60, 58:51, 49:31, 29:25, 22, 21, 19:1	I/O-TTL (4mA)	Host Data Bus: These pins are bidirectional and connected directly to the CPU data bus and L2 cache data lines. There are internal pull-downs on these lines which can be engaged during the Suspend mode or if the HD/MD lines are idle, depending on the strap information sampled on the MP1 and MP2 lines during power-on reset.

3.2.2 82C557 Interface Signals

Signal Name	Pin No. 176 TQFP	Pin No. 160 PQFP	Signal Type (Drive)	Signal Description
DBC OE[1:0]#	171, 172	157, 158	I-TTL	DBC Output Enables: These input signals are connected to the DBC OE[1:0]# output signals of the 82C557. These signals, along with MDOE# and HDOE#, form the encoded command sent from the 82C557 to the 82C556. These commands indicate the type of cycle currently underway and enables the 82C556 to perform the appropriate data steering, latching and direction control. The encoded commands are defined in Table 3-6.
MDOE#	170	156	I-TTL	Memory Data Output Enable: This signal is used along with DBC OE[1:0]# and HDOE# to form the encoded commands that are sent out by the 82C557. When asserted, MDOE# enables data to be put out on the MD bus. MDOE# is asserted for writes to DRAM, CPU writes to PCI, PCI reads from cache/DRAM, L2 cache write-back cycles, and PCI writes to DRAM.
HDOE#	169	155	I-TTL	Host Data Output Enable: This signal is used along with DBC OE[1:0]# and MDOE# to form the encoded commands that are sent out by the 82C557. When asserted, HDOE# enables data to be put out on the HD bus. HDOE# is asserted for CPU reads from DRAM/PCI/VL bus, PCI writes to cache, CPU linefills, Suspend mode indication, and reset state indication.
DLE[1:0]#	173, 174	159, 160	I-TTL	Data Latch Enables: These input signals are connected to the DLE[1:0]# output signals of the 82C557 and used to latch the HD and MD data bus depending on which cycle is occurring.

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82C556 Signal Descriptions (cont.)

3.2.3 DRAM Interface Signals

Signal Name	Pin No. 176 TQFP	Pin No. 160 PQFP	Signal Type (Drive)	Signal Description
MP7	158	144	I/O-CMOS (4mA)	<p>Memory Parity: These pins (MP[7:0]) are connected directly to the system DRAM data bus. As outputs, these lines are only driven when DWE# is active.</p> <p>MP[7:4] can be configured as outputs for PCI master writes with the aid of the strap option on MP0. During power-up reset, MP[4:0] are used to provide strap functions. (See descriptions below.)</p> <p>MP[7:0] have internal pull-up resistors with a value approximately equal to 75Kohms which are enabled during reset. A stronger pull-down will be required to sample these pins low.</p>
MP6	159	145	I/O-CMOS (4mA)	<p>MP6: This pin must never be pulled low (default = 1). An external pull-up is recommended.</p>
MP5	160	146	I/O-CMOS (4mA)	<p>MP5: Test mode selection (default = 1).</p> <p>0 = Enter Test Mode 0 (Tristate all outputs and bidirectional pins.) 1 = Enter Test Mode 1 (Tristate all bidirectional pins and present the end of NAND chain output on the MPERR# output.)</p>
MP4+TMOD#	161	147	I/O-CMOS (4mA)	<p>MP4+TMOD#: Enable test mode (default = 1).</p> <p>0 = Enable (the test mode entered is dependent on the MP5 strap) 1 = Disable (Normal mode)</p>
MP3+3VDRAM#	162	148	I/O-CMOS (4mA)	<p>MP3+3VDRAM#: DRAM interface (default = 1).</p> <p>0 = 3.3V DRAM interface 1 = 5.0V DRAM interface</p>
MP2+SUSP_LKG	163	149	I/O-CMOS (4mA)	<p>MP2+SUSP_LKG: Engage internal pull-downs on the CPU data bus (HD[63:0]) and internal pull-ups on the memory data bus (MD[63:0]) during Suspend mode (default = 1).</p> <p>0 = Enable 1 = Disable</p> <p>No external pull-up/down needed. This strap is internally blocked if MP1 is sampled high during reset.</p>
MP1+IDLE_LKG	165	151	I/O-CMOS (4mA)	<p>MP1+IDLE_LKG: Engage internal pull-downs on the CPU data bus (HD[63:0]) and internal pull-ups on the memory data bus (MD[63:0]) if the data bus is Idle mode (default = 1).</p> <p>0 = Disable 1 = Enable</p> <p>Note that the bus Idle condition includes the Suspend condition also because the buses are not driven in Suspend. This implies that an external pull-down strap to engage leakage control during Suspend is not needed on MP2.</p>
MP0+MPGEN	166	152	I/O-CMOS (4mA)	<p>MP0+MPGEN: Generate MP[7:4] during non-CPU master writes to DRAM high bits. (Default = 1)</p> <p>0 = Disable (The 82C558N should be programmed to generate MP[7:4] on pins 115, 113, 112, and 52.) 1 = Enable</p>



82C556 Signal Descriptions (cont.)

Signal Name	Pin No. 176 TQFP	Pin No. 160 PQFP	Signal Type (Drive)	Signal Description
MD[63:32]	157, 156, 154:145, 143, 141:135, 130:119	143, 142, 140:131, 129, 127:109	I/O- CMOS (4mA)	Higher Order Memory Data Bus: These pins are connected directly to the higher order DRAM data bus and the 82C558N. This bus serves as a conduit for all high order reads/writes to and from system memory, CPU writes/reads to/from PCI/VL bus/ISA. These lines have internal pull-up resistors.
MD[31:0]#	118:114, 111, 109:102, 99:91, 86:78	108:104, 101, 99:92, 89:72	I/O- CMOS (4mA)	Lower Order Memory Data Bus: These pins are connected directly to the lower order DRAM data bus. During lower order CPU/PCI writes to DRAM, this bus carries the inverted version of the MD[31:0] bus or the MD[63:32] bus. These lines have internal pull-up resistors.
MPERR#	168	154	O- (4mA)	Memory Parity Error Indication: This pin is connected to the MPERR# input of the 82C558N. It indicates the detection of a parity error during a read from the system DRAM and is qualified within the 82C558N only when the PEN# output from the 82C557 is active.

3.2.4 Power, Ground, and NC Pins

Signal Name	Pin No. 176 TQFP	Pin No. 160 PQFP	Signal Type (Drive)	Signal Description
GND	25, 26, 56, 76, 100, 112, 113, 144, 164	23, 24, 50, 70, 90, 102, 103, 130, 150	I-G	Ground Connection
VCC3	22, 32, 65	20, 30, 59	I-P	Power Connection: 3.3V power plane
VCC5	167	153	I-P	Power Connection: 5.0V power plane
VCC_MEM	101, 110, 142, 155	91, 100, 128, 141	I-P	Power Connection: Memory power plane. Can be at 3.3V or 5.0V.
NC	1, 2, 43:46, 87:90, 131:134, 175, 176			No Connection: These pins should not be connected.

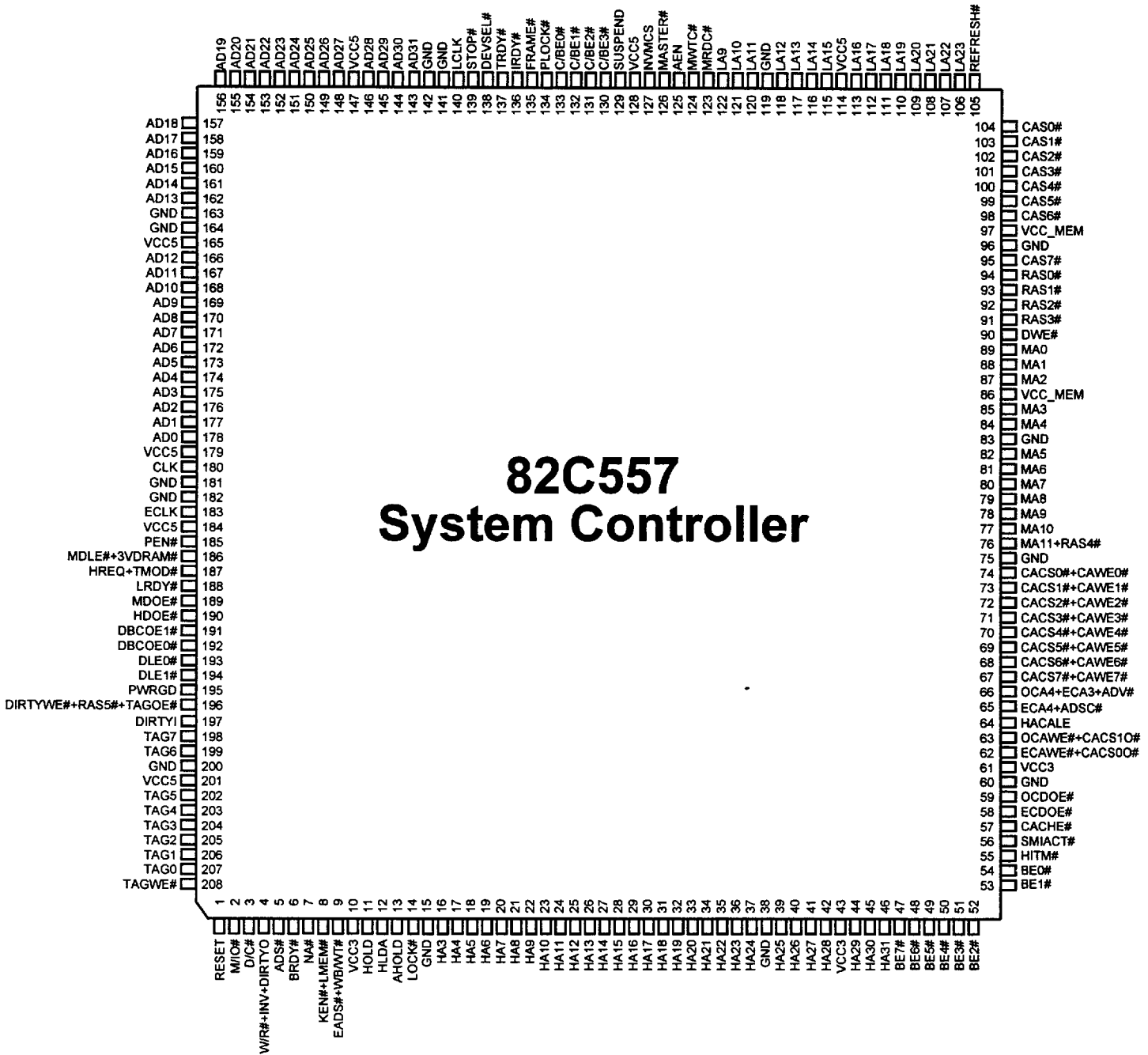
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Table 3-6 82C556 Encoded Commands

Parameter	Description
DBC0E[1:0]# = 01 MDOE# = 0 HDOE# = 1	This code indicates that one of the following cycles is underway: <ul style="list-style-type: none"> - CPU write low order data to PCI - PCI read low order data from cache The 82C556 then, along with the appropriate control signals from the 82C557, performs the required data bus steering, buffering and latching control.
DBC0E[1:0]# = 11 MDOE# = 0 HDOE# = 1	This code indicates that one of the following cycles is underway: <ul style="list-style-type: none"> - L2 cache write-back cycle - CPU write to cache/DRAM - CPU write high order data to PCI - PCI read high order data from cache The 82C556 then, along with the appropriate control signals from the 82C557, performs the required data bus steering, buffering and latching control.
DBC0E[1:0]# = 10 MDOE# = 0 HDOE# = 1	This code indicates that the following cycle is underway: <ul style="list-style-type: none"> - PCI read low order data from DRAM The 82C556 then, along with the appropriate control signals from the 82C557, performs the required data bus steering, buffering and latching control.
DBC0E[1:0]# = 10 MDOE# = 1 HDOE# = 0	This code indicates that currently the system is in the Suspend state and all the buffer outputs should be tristated.
DBC0E[1:0]# = 00 MDOE# = 1 HDOE# = 0	This code indicates that one of the following cycles is underway: <ul style="list-style-type: none"> - CPU read 64 bits of data from PCI/VLB - CPU read high order data from PCI/VLB - CPU read low order data from PCI/VLB The 82C556 then, along with the appropriate control signals from the 82C557, performs the required data bus steering, buffering and latching control.
DBC0E[1:0]# = 00 MDOE# = 0 HDOE# = 0	This code indicates that the following cycle is underway: <ul style="list-style-type: none"> - PCI write to cache/DRAM The 82C556 then, along with the appropriate control signals from the 82C557, performs the required data bus steering, buffering and latching control.
DBC0E[1:0]# = 11 MDOE# = 1 HDOE# = 0	This code indicates that one of the following cycles is underway: <ul style="list-style-type: none"> - CPU read from DRAM, and the cache line being replaced is not dirty - CPU linefill The 82C556 then, along with the appropriate control signals from the 82C557, performs the required data bus steering, buffering and latching control.
DBC0E[1:0]# = 11 MDOE# = 1 HDOE# = 1	This code indicates that one of the following cycles is underway: <ul style="list-style-type: none"> - PCI read from PCI - PCI write to PCI - CPU read/write cache hit - PCI read VLB - PCI write VLB - Idle The 82C556 then, along with the appropriate control signals from the 82C557, performs the required data bus steering, buffering and latching control.
DBC0E[1:0]# = 10 MDOE# = 1 HDOE# = 1	This code indicates that the following cycle is underway: <ul style="list-style-type: none"> - PCI read high order data from DRAM The 82C556 then, along with the appropriate control signals from the 82C557, performs the required data bus steering, buffering and latching control.
DBC0E[1:0]# = 01 MDOE# = 1 HDOE# = 0	This code indicates that the system is in the reset state.



Figure 3-3 82C557 Pin Diagram



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Table 3-7 82C557 Numerical Pin Cross-Reference List

Pin No.	Pin Name	Signal Type	Drive (mA)	Power Plane
1	RESET	O	8	VCC3
2	M/IO#	I-TTL		VCC3
3	D/C#	I-TTL		VCC3
4	W/R#	I/O-TTL	4	VCC3
	INV			
	DIRTYO			
5	ADS#	I-TTL		VCC3
6	BRDY#	O	8	VCC3
7	NA#	O	8	VCC3
8	KEN#	O	8	VCC3
	LMEM#			
9	EADS#	O	8	VCC3
	WB/WT#			
10	VCC3	I-P		
11	HOLD	O	8	VCC3
12	HLDA	I-TTL		VCC3
13	AHOLD	O	8	VCC3
14	LOCK#	I-TTL		VCC3
15	GND	I-G		
16	HA3	I/O-TTL	4	VCC3
17	HA4	I/O-TTL	4	VCC3
18	HA5	I/O-TTL	4	VCC3
19	HA6	I/O-TTL	4	VCC3
20	HA7	I/O-TTL	4	VCC3
21	HA8	I/O-TTL	4	VCC3
22	HA9	I/O-TTL	4	VCC3
23	HA10	I/O-TTL	4	VCC3
24	HA11	I/O-TTL	4	VCC3
25	HA12	I/O-TTL	4	VCC3
26	HA13	I/O-TTL	4	VCC3
27	HA14	I/O-TTL	4	VCC3
28	HA15	I/O-TTL	4	VCC3
29	HA16	I/O-TTL	4	VCC3
30	HA17	I/O-TTL	4	VCC3
31	HA18	I/O-TTL	4	VCC3
32	HA19	I/O-TTL	4	VCC3
33	HA20	I/O-TTL	4	VCC3
34	HA21	I/O-TTL	4	VCC3
35	HA22	I/O-TTL	4	VCC3
36	HA23	I/O-TTL	4	VCC3
37	HA24	I/O-TTL	4	VCC3
38	GND	I-G		
39	HA25	I/O-TTL	4	VCC3
40	HA26	I/O-TTL	4	VCC3
41	HA27	I/O-TTL	4	VCC3
42	HA28	I/O-TTL	4	VCC3
43	VCC3	I-P		

Pin No.	Pin Name	Signal Type	Drive (mA)	Power Plane
44	HA29	I/O-TTL	4	VCC3
45	HA30	I/O-TTL	4	VCC3
46	HA31	I/O-TTL	4	VCC3
47	BE7#	I-TTL		VCC3
48	BE6#	I-TTL		VCC3
49	BE5#	I-TTL		VCC3
50	BE4#	I-TTL		VCC3
51	BE3#	I-TTL		VCC3
52	BE2#	I-TTL		VCC3
53	BE1#	I-TTL		VCC3
54	BE0#	I-TTL		VCC3
55	HITM#	I-TTL		VCC3
56	SMIACK#	I-TTL		VCC3
57	CACHE#	I-TTL		VCC3
58	ECDOE#	O	8	VCC3
59	OCDOE#	O	8	VCC3
60	GND	I-G		
61	VCC3	I-P		
62	ECAWE#	O	8	VCC3
	CACS00#			
63	OCAWE#	O	8	VCC3
	CACS10#			
64	HACALE	O	8	VCC3
65	ECA4	O	8	VCC3
	ADSC#			
66	OCA4	O	8	VCC3
	ECA3			
	ADV#			
67	CACS7#	O	4	VCC3
	CAWE7#			
68	CACS6#	O	4	VCC3
	CAWE6#			
69	CACS5#	O	4	VCC3
	CAWE5#			
70	CACS4#	O	4	VCC3
	CAWE4#			
71	CACS3#	O	4	VCC3
	CAWE3#			
72	CACS2#	O	4	VCC3
	CAWE2#			
73	CACS1#	O	4	VCC3
	CAWE1#			
74	CACS0#	O	4	VCC3
	CAWE0#			
75	GND	I-G		
76	MA11	O	4*	VCC_MEM
	RAS4#			

Pin No.	Pin Name	Signal Type	Drive (mA)	Power Plane
77	MA10	O	4*	VCC_MEM
78	MA9	O	4*	VCC_MEM
79	MA8	O	4*	VCC_MEM
80	MA7	O	4*	VCC_MEM
81	MA6	O	4*	VCC_MEM
82	MA5	O	4*	VCC_MEM
83	GND	I-G		
84	MA4	O	4*	VCC_MEM
85	MA3	O	4*	VCC_MEM
86	VCC_MEM	I-P		
87	MA2	O	4*	VCC_MEM
88	MA1	O	4*	VCC_MEM
89	MA0	O	4*	VCC_MEM
90	DWE#	O	16	VCC_MEM
91	RAS3#	O	4*	VCC_MEM
92	RAS2#	O	4*	VCC_MEM
93	RAS1#	O	4*	VCC_MEM
94	RAS0#	O	4*	VCC_MEM
95	CAS7#	O	8	VCC_MEM
96	GND	I-G		
97	VCC_MEM	I-P		
98	CAS6#	O	8	VCC_MEM
99	CAS5#	O	8	VCC_MEM
100	CAS4#	O	8	VCC_MEM
101	CAS3#	O	8	VCC_MEM
102	CAS2#	O	8	VCC_MEM
103	CAS1#	O	8	VCC_MEM
104	CAS0#	O	8	VCC_MEM
105	REFRESH#	I-CMOS		VCC5
106	LA23	I/O-CMOS	8	VCC5
107	LA22	I/O-CMOS	8	VCC5
108	LA21	I/O-CMOS	8	VCC5
109	LA20	I/O-CMOS	8	VCC5
110	LA19	I/O-CMOS	8	VCC5
111	LA18	I/O-CMOS	8	VCC5
112	LA17	I/O-CMOS	8	VCC5
113	LA16	I/O-CMOS	8	VCC5
114	VCC5	I-P		
115	LA15	I/O-CMOS	8	VCC5
116	LA14	I/O-CMOS	8	VCC5
117	LA13	I/O-CMOS	8	VCC5
118	LA12	I/O-CMOS	8	VCC5
119	GND	I-G		
120	LA11	I/O-CMOS	8	VCC5
121	LA10	I/O-CMOS	8	VCC5
122	LA9	I/O-CMOS	8	VCC5
123	MRDC#	I-CMOS		VCC5



82C557 Numerical Pin Cross-Reference List (cont.)

Pin No.	Pin Name	Signal Type	Drive (mA)	Power Plane
124	MWTC#	I-CMOS		VCC5
125	AEN	I-CMOS		VCC5
126	MASTER#	I-CMOS		VCC5
127	NVMCS	O	4	VCC5
128	VCC5	I-P		
129	SUSPEND	I-TTL		VCC5
130	C/BE3#	I/O-TTL	PCI	VCC5
131	C/BE2#	I/O-TTL	PCI	VCC5
132	C/BE1#	I/O-TTL	PCI	VCC5
133	C/BE0#	I/O-TTL	PCI	VCC5
134	PLOCK#	O-TTL	PCI	VCC5
135	FRAME#	I/O-TTL	PCI	VCC5
136	IRDY#	I/O-TTL	PCI	VCC5
137	TRDY#	I/O-TTL	PCI	VCC5
138	DEVSEL#	I/O-TTL	PCI	VCC5
139	STOP#	I/O-TTL	PCI	VCC5
140	LCLK	I-TTL		VCC5
141	GND	I-G		
142	GND	I-G		
143	AD31	I/O-TTL	PCI	VCC5
144	AD30	I/O-TTL	PCI	VCC5
145	AD29	I/O-TTL	PCI	VCC5
146	AD28	I/O-TTL	PCI	VCC5
147	VCC5	I-P		
148	AD27	I/O-TTL	PCI	VCC5
149	AD26	I/O-TTL	PCI	VCC5
150	AD25	I/O-TTL	PCI	VCC5
151	AD24	I/O-TTL	PCI	VCC5
152	AD23	I/O-TTL	PCI	VCC5
153	AD22	I/O-TTL	PCI	VCC5

Pin No.	Pin Name	Signal Type	Drive (mA)	Power Plane
154	AD21	I/O-TTL	PCI	VCC5
155	AD20	I/O-TTL	PCI	VCC5
156	AD19	I/O-TTL	PCI	VCC5
157	AD18	I/O-TTL	PCI	VCC5
158	AD17	I/O-TTL	PCI	VCC5
159	AD16	I/O-TTL	PCI	VCC5
160	AD15	I/O-TTL	PCI	VCC5
161	AD14	I/O-TTL	PCI	VCC5
162	AD13	I/O-TTL	PCI	VCC5
163	GND	I-G		
164	GND	I-G		
165	VCC5	I-P		
166	AD12	I/O-TTL	PCI	VCC5
167	AD11	I/O-TTL	PCI	VCC5
168	AD10	I/O-TTL	PCI	VCC5
169	AD9	I/O-TTL	PCI	VCC5
170	AD8	I/O-TTL	PCI	VCC5
171	AD7	I/O-TTL	PCI	VCC5
172	AD6	I/O-TTL	PCI	VCC5
173	AD5	I/O-TTL	PCI	VCC5
174	AD4	I/O-TTL	PCI	VCC5
175	AD3	I/O-TTL	PCI	VCC5
176	AD2	I/O-TTL	PCI	VCC5
177	AD1	I/O-TTL	PCI	VCC5
178	AD0	I/O-TTL	PCI	VCC5
179	VCC5	I-P		
180	CLK	I-TTL		VCC5
181	GND	I-G		
182	GND	I-G		
183	ECLK	I-TTL		VCC5

Pin No.	Pin Name	Signal Type	Drive (mA)	Power Plane
184	VCC5	I-P		
185	PEN#	O	4	VCC5
186	MDLE#	O	4	VCC5
	3VDRAM#	I		
187	HREQ	I-TTL		VCC5
	TMOD#			
188	LRDY#	I		VCC5
189	MDOE#	O	4	VCC5
190	HDOE#	O	4	VCC5
191	DBC0E1#	O	4	VCC5
192	DBC0E0#	O	4	VCC5
193	DLE0#	O	4	VCC5
194	DLE1#	O	4	VCC5
195	PWRGD	I-S		VCC5
196	DIRTYWE#	O	8	VCC5
	RAS5#			
	TAG0E#			
197	DIRTYI	I/O-TTL		VCC5
198	TAG7	I/O-TTL	4	VCC5
199	TAG6	I/O-TTL	4	VCC5
200	GND	I-G		
201	VCC5	I-P		
202	TAG5	I/O-TTL	4	VCC5
203	TAG4	I/O-TTL	4	VCC5
204	TAG3	I/O-TTL	4	VCC5
205	TAG2	I/O-TTL	4	VCC5
206	TAG1	I/O-TTL	4	VCC5
207	TAG0	I/O-TTL	4	VCC5
208	TAGWE#	O	8	VCC5

*Default drive is 4mA. However, by setting SYSCFG 18h[4] = 1, the drive strength can be increased to 16mA.

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Table 3-8 82C557 Alphabetical Pin Cross-Reference List

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
AD0	178	C/BE2#	131	ECLK	183	HDOE#	190	MWTC#	124
AD1	177	C/BE3#	130	FRAME#	135	HITM#	55	NA#	7
AD2	176	CACHE#	57	GND	15	HLDA	12	NVMCS	127
AD3	175	CACS0#	74	GND	38	HOLD	11	OCA4	66
AD4	174	CAWE0#		GND	60	HREQ	187	ECA3	
AD5	173	CACS1#	73	GND	75	TMOD#		ADV#	
AD6	172	CAWE1#		GND	83	IRDY#	136	OCAWE#	63
AD7	171	CACS2#	72	GND	96	KEN#	8	CACS10#	
AD8	170	CAWE2#		GND	119	LMEM#		OCDOE#	59
AD9	169	CACS3#	71	GND	141	LA9	122	PEN#	185
AD10	168	CAWE3#		GND	142	LA10	121	PLOCK#	134
AD11	167	CACS4#	70	GND	163	LA11	120	PWRGD	195
AD12	166	CAWE4#		GND	164	LA12	118	RAS0#	94
AD13	162	CACS5#	69	GND	181	LA13	117	RAS1#	93
AD14	161	CAWE5#		GND	182	LA14	116	RAS2#	92
AD15	160	CACS6#	68	GND	200	LA15	115	RAS3#	91
AD16	159	CAWE6#		HA3	16	LA16	113	REFRESH#	105
AD17	158	CACS7#	67	HA4	17	LA17	112	RESET	1
AD18	157	CAWE7#		HA5	18	LA18	111	SMIACT#	56
AD19	156	CAS0#	104	HA6	19	LA19	110	STOP#	139
AD20	155	CAS1#	103	HA7	20	LA20	109	SUSPEND	129
AD21	154	CAS2#	102	HA8	21	LA21	108	TAG0	207
AD22	153	CAS3#	101	HA9	22	LA22	107	TAG1	206
AD23	152	CAS4#	100	HA10	23	LA23	106	TAG2	205
AD24	151	CAS5#	99	HA11	24	LCLK	140	TAG3	204
AD25	150	CAS6#	98	HA12	25	LOCK#	14	TAG4	203
AD26	149	CAS7#	95	HA13	26	LRDY#	188	TAG5	202
AD27	148	CLK	180	HA14	27	M/IO#	2	TAG6	199
AD28	146	D/C#	3	HA15	28	MA0	89	TAG7	198
AD29	145	DBCOE0#	192	HA16	29	MA1	88	TAGWE#	208
AD30	144	DBCOE1#	191	HA17	30	MA2	87	TRDY#	137
AD31	143	DEVSEL#	138	HA18	31	MA3	85	VCC3	10
ADS#	5	DIRTYI	197	HA19	32	MA4	84	VCC3	43
AEN	125	DIRTYWE#	196	HA20	33	MA5	82	VCC3	61
AHOLD	13	RAS5#		HA21	34	MA6	81	VCC5	114
BE0#	54	TAGOE#		HA22	35	MA7	80	VCC5	128
BE1#	53	DLE0#	193	HA23	36	MA8	79	VCC5	147
BE2#	52	DLE1#	194	HA24	37	MA9	78	VCC5	165
BE3#	51	DWE#	90	HA25	39	MA10	77	VCC5	179
BE4#	50	EADS#	9	HA26	40	MA11	76	VCC5	184
BE5#	49	WB/WT#		HA27	41	RAS4#		VCC5	201
BE6#	48	ECA4	65	HA28	42	MASTER#	126	VCC_MEM	86
BE7#	47	ADSC#		HA29	44	MDLE#	186	VCC_MEM	97
BRDY#	6	ECAWE#	62	HA30	45	3VDRAM#		W/R#	4
C/BE0#	133	CACS00#		HA31	46	MDOE#	189	INV	
C/BE1#	132	ECDOE#	58	HACALE	64	MRDC#	123	DIRTYO	



3.3 82C557 Signal Descriptions

3.3.1 Reset and Clock Signals

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
RESET	1	O (8mA)		System Reset: When asserted, this signal resets the CPU and the 82C558N. RESET is asserted in response to a PWRGD only and is guaranteed to be active for 1ms. The LCLK input must be stable to provide a 1ms reset pulse.
PWRGD	195	I-S		Power Good: This input reflects the "wired-OR" status of the external reset switch and the power good status from the power supply.
CLK	180	I-TTL		Clock: This input is used as the master single frequency clock. This signal has to be identical to the clock signal sent to the CPU.
ECLK	183	I-TTL		Early Clock: This input clock is required to be 3ns to 6ns earlier than CLK. This signal is used by the 82C557 to generate some critical signals for the host CPU and the cache controller logic.
LCLK	140	I-TTL		Local Bus Clock: This clock is used by the PCI and local bus state machine within the 82C557. The same clock or another identical signal is used by the local bus devices. For a synchronous PCI/VL implementation, the skew between this input and the CLK input should satisfy the following requirements: LCLK < CLK+2 period ahead in phase of CLK LCLK < 0.5ns behind in phase of CLK

3.3.2 CPU Bus Interface Signals

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
HA[31:3]	46:44, 42:39, 37:16	I/O-TTL (4mA)		Host Address Bus: HA[31:3] are the address lines of the CPU bus. HA[31:3] are connected to the CPU A[31:3] lines. Along with the byte enable signals, the HA[31:3] lines define the physical area of memory or I/O being accessed. During CPU cycles, the HA[31:3] lines are inputs to the 82C557. They are used for address decoding and second level cache tag lookup sequences. During inquire cycles, the HA[31:5] are outputs from the 82C557 to the CPU to snoop the first level cache tags. They also are outputs from the 82C557 to the L2 cache. HA[31:3] have internal pull-downs, however, external pull-ups are required on HA3 and HA4.



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82C557 Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
BE[7:0]#	47:54	I-TTL		<p>Byte Enable: The byte enables indicate which byte lanes on the CPU data bus are carrying valid data during the current bus cycle. During cacheable read cycles, all eight bytes of data are driven to the CPU, regardless of the state of the byte enables. The byte enable signals indicate the type of special cycle when M/IO# = D/C# = 0 and W/R# = 1.</p> <p>BE[7:0]# have internal pull-downs that are activated during Suspend or when HLDA is active.</p>
M/IO#	2	I-TTL		<p>Memory/Input-Output: M/IO# along with D/C# and W/R# define CPU bus cycles. Interrupt acknowledge cycles are forwarded to the PCI bus as PCI interrupt acknowledge cycles. All I/O cycles and any memory cycles that are not directed to memory controlled by the DRAM interface of the 82C557 are forwarded to PCI.</p>
D/C#	3	I-TTL		<p>Data/Control: D/C# along with M/IO# and W/R# define CPU bus cycles. (See M/IO# definition above.)</p>
W/R#	4	I/O-TTL (4mA)	Cycle Multiplexed	<p>Write/Read: W/R# along with M/IO# and D/C# define CPU bus cycles. (See M/IO# definition above.)</p>
INV				<p>Invalidate: Pin 4 also serves as an output signal and is used as INV for the L1 cache during an inquire cycle.</p>
DIRTYO				<p>Dirty Output: Pin 4 also serves as an output signal and is used as DIRTYO for the L2 cache during an inquire cycle.</p> <p>If a combined Tag/Dirty RAM implementation is being used, then the pin 4 will not serve as a DIRTYO pin.</p>
ADS#	5	I-TTL		<p>Address Strobe: The CPU asserts ADS# to indicate that a new bus cycle is beginning. ADS# is driven active in the same clock as the address, byte enables, and cycle definition signals. An external pull-up of 10K is recommended.</p>
BRDY#	6	O (8mA)		<p>Burst Ready: BRDY# indicates that the system has responded in one of three ways:</p> <ol style="list-style-type: none"> 1) Valid data has been placed on the CPU data bus in response to a read, 2) CPU write data has been accepted by the system, or 3) the system has responded to a special cycle.
NA#	7	O (8mA)		<p>Next Address: This signal is connected to the NA# pin of the CPU and is used to request pipelined addressing for local memory cycles. The 82C557 asserts NA# for one clock when the system is ready to accept a new address from the CPU, even if all data transfers for the current cycle have not completed.</p> <p>The 3.3V Pentium processor and the M1 processor support pipelined memory accesses, however, the K5 processor does not support this feature.</p>

82C557 Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
KEN#	8	O (8mA)	Cycle Multiplexed	Cache Enable: This pin is connected to the KEN# input of the CPU and is used to determine whether the current cycle is cacheable.
LMEM#				Local Memory Accessed: During CPU or master cycles to local memory, the 82C557 asserts this signal to inform the 82C558N that local system memory needs to be accessed. The 82C558N is then responsible for providing the data path to the corresponding master.
EADS#	9	O (8mA)	Cycle Multiplexed	External Address Strobe: This output indicates that a valid address has been driven onto the CPU address bus by an external device. This address will be used to perform an internal cache inquiry cycle when the CPU samples EADS# active.
WB/WT#				Write-Back/Write-Through: Pin 9 is also used to control write-back or write-through policy for the primary cache during CPU cycles on a line-by-line basis.
HITM#	55	I-TTL		Hit Modified: Indicates that the CPU has had a hit on a modified line in its internal cache during an inquire cycle. It is used to prepare for write-back.
CACHE#	57	I-TTL		Cacheability: This signal is connected to the CACHE# pin of the CPU. It goes active during a CPU initiated cycle to indicate when an internal cacheable read cycle or a burst write-back cycle occurs.
SMIACT#	56	I-TTL		System Management Interrupt Active: The CPU asserts SMIACT# in response to the SMI# signal to indicate that it is operating in System Management Mode (SMM).
HOLD	11	O (8mA)		CPU Hold Request: This output is connected to the HOLD input of the CPU. HOLD requests that the CPU allow another bus master complete control of its buses. In response to HOLD going active, the CPU will float most of its output and bidirectional pins and then assert HLDA.
HLDA	12	I-TTL		CPU Hold Acknowledge: This input is connected to the HLDA pin of the CPU. HLDA indicates, in response to a HOLD, when the CPU has relinquished bus control to another bus master.
AHOLD	13	O (8mA)		Address Hold: This signal is used to tristate the CPU address bus for internal cache snooping.
LOCK#	14	I-TTL		CPU Bus Lock: The processor asserts LOCK# to indicate the current bus cycle is locked. It is used to generate PLOCK# for the PCI bus. LOCK# has an internal pull-down resistor that is engaged when HLDA is active.

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82C557 Signal Descriptions (cont.)

3.3.3 Cache Control Interface Signals

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
ECDOE#	58	O (8mA)		Even Bank Cache Output Enable: This signal is connected to the output enables of the SRAMs in the even bank of the L2 cache to enable data read.
OCDOE#	59	O (8mA)		Odd Bank Cache Output Enable: This signal is connected to output enables of the SRAMs in the odd bank of the L2 cache to enable data read.
ECAWE#	62	O (8mA)	SYSCFG 11h[3] = 0	Even Bank Cache Write Enable: For asynchronous L2 cache operation, this pin becomes ECAWE# and is connected to the write enables of the SRAMs in the even bank of the L2 cache to enable data update.
CACS00#			SYSCFG 11h[3] = 1	Bank 0 Synchronous SRAM Chip Select: For synchronous L2 cache operation, this pin provides the chip select for the even bank (synchronous L2 cache is always non-interleaved).
OCAWE#	63	O (8mA)	SYSCFG 11h[3] = 0	Odd Bank Cache Write Enable: For asynchronous L2 cache operation, this pin becomes OCAWE# and is connected to the write enables of the SRAMs in the odd bank of the L2 cache to enable data update.
CACS10#			SYSCFG 11h[3] = 1	Bank 1 Synchronous SRAM Chip Select: For synchronous L2 cache operation, this pin provides the chip select for the odd bank (synchronous L2 cache is always non-interleaved).
CACS[7:0]#	67:74	O (4mA)	SYSCFG 11h[3] = 0	Cache Chip Selects 7-0: For asynchronous L2 cache operation, these pins become chip selects and are connected to the chip selects of the SRAMs in the L2 cache in both banks to enable data read/write operations.
CAWE[7:0]#			SYSCFG 11h[3] = 1	Cache Write Enables 7-0: For synchronous L2 cache operation, these pins become cache write enables for the SRAMs.
TAG[7:0]	198, 199, 202:207	I/O-TTL (4mA)	SYSCFG 16h[5]: 0 = 8-bit Tag 1 = 7-bit Tag	<p>Tag RAM Data Bits 7-0: These input signals become outputs whenever TAGWE# is activated to write new tags to the Tag RAM.</p> <p>If using the Sony cache module, then TAG1 and TAG2 are connected to the START# output from the module and TAG3 is connected to the BOFF# output from the module. The remaining TAG bits are unused.</p> <p>Dirty I/O (Pin 207): If using a 7-bit Tag in a combined Tag/Dirty RAM implementation, then TAG0 functions as the Dirty I/O bit. The DIRTY pin (pin 197) needs to be externally pulled up in this case.</p>
TAGWE#	208	O (8mA)	SYSCFG 08h[3] = 0	Tag RAM Write Enable: This control strobe is used to update the Tag RAM with the valid tag of the new cache line that replaces the current one during external cache read miss cycles.
			SYSCFG 08h[3] = 1	Tag and Dirty Write Enable: If using a combined Tag/Dirty RAM implementation, this signal functions as both the TAGWE# and DIRTYWE#.



82C557 Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
DIRTYI	197	I/O-TTL	SYSCFG 16h[7]: 0 = Input only 1 = I/O (for combined Tag/Dirty SRAM)	Dirty Bit: This input signal represents the dirty bit of the Tag RAM and is used to indicate whether a corresponding cache line has been overwritten. If using a combined Tag/Dirty implementation, this pin becomes bidirectional. If using a 7-bit Tag in a combined Tag/Dirty RAM implementation, then this pin is not used and must be pulled up externally.
DIRTYWE#	196	O (8mA)	SYSCFG 19h[7] = 0 and 08h[3] = 0.	Dirty RAM Write Enable: This control strobe is used to update the dirty bit RAM when a cache write hit occurs. A cache write hit will set the dirty bit for the currently accessed cache line.
RAS5#			SYSCFG 19h[7] = 1	Row Address Strobe bit 5: Each RAS# signal corresponds to a unique DRAM bank. Depending on the kind of DRAM modules being used, this signal may or may not need to be buffered externally. This signal, however, should be connected to the corresponding DRAM RAS# line through a damping resistor.
TAGOE#			SYSCFG 08h[3] = 1	Tag Output Enable: This pin becomes TAGOE# when a combined Tag/Dirty implementation is being used. If a combined Tag/Dirty implementation is being used, then this signal is not used to update the Dirty RAM.
ECA4	65	O (8mA)	SYSCFG 11h[3] = 0	Even Cache Address 4: For asynchronous L2 cache operation in a single bank configuration, this pin is mapped from HA4 and connected to the second LSB of the cache SRAMs' address inputs. For asynchronous L2 cache operation in a double bank configuration, this pin is connected to the LSB of the cache SRAMs' address input in the even bank.
ADSC#			SYSCFG 11h[3] = 1	Controller Address Strobe: For a synchronous L2 cache operation, this pin is connected to the ADSC# input of the synchronous SRAMs.
ECA3	66	O (8mA)	SYSCFG 11h[3] = 0 and SYSCFG 08h[7] = 1 (single bank, non-interleaved)	Even Cache Address 3: For asynchronous L2 cache operation in a single bank configuration, this pin takes on the functionality of ECA3 and is mapped from HA3 and connected to the cache SRAMs LSB address input.
OCA4			SYSCFG 11h[3] = 0 and SYSCFG 08h[7] = 0 (double bank, interleaved)	Odd Cache Address 4: For asynchronous L2 cache operation in a double bank configuration, this pin takes on the functionality of OCA4 and is mapped from HA4 and connected to the LSB address input of the SRAMs in the odd bank.
ADV#			SYSCFG 11h[3] = 1	Advance Output: For synchronous cache L2 operation, this pin becomes the advance output and is connected to the ADV# input of the synchronous SRAMs.

82C557 Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
HACALE	64	O (8mA)		Cache Address Latch Enable: It is used to latch the CPU address and generate latched cache addresses for the asynchronous L2 cache. This pin is a "no connect" for synchronous cache.

3.3.4 DRAM Interface Signals

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
RAS[3:0]#	91:94	O (4mA)		Row Address Strobe bits 3-0: Each RAS# signal corresponds to a unique DRAM bank. Depending on the kind of DRAM modules being used, these signals may or may not need to be buffered externally. These signals, however, should be connected to the corresponding DRAM RAS# lines through a damping resistor. The default drive current on these lines is 4mA, however, by setting SYSCFG 18h[4] = 1, it can be increased to 16mA. RAS4# is pin-wise programmable with MA11 and RAS5# is pin-wise programmable with DIRTYWE#.
CAS[7:0]#	95, 98:104	O (8mA)		Column Address Strobe bits 7-0: The CAS[7:0]# outputs correspond to the eight bytes for each DRAM bank. Each DRAM bank has a 64-bit data bus. These signals are typically connected directly to the DRAM's CAS# inputs through a damping resistor.
DWE#	90	O (16mA)		DRAM Write Enable: This signal is typically buffered externally before connection to the WE# input of the DRAMs. The default drive current on this line is 4mA, however, by setting SYSCFG 18h[4] = 1, it can be increased to 16mA.
MA11	76	O (4mA)	SYSCFG 19h[3] = 0	Memory Address bit 11: A part of the multiplexed row/column address lines to the DRAMs. Depending on the kind of DRAM modules being used, this signal may or may not need to be buffered externally. The default drive current on the MA[11:0] lines is 4mA, however, by setting SYSCFG 18h[4] = 1, it can be increased to 16mA. As MA11, 8Mx36 and 16Mx36 SIMMs will be supported.
RAS4#			SYSCFG 19h[3] = 1	Row Address Strobe bit 4: Each RAS# signal corresponds to a unique DRAM bank. Depending on the kind of DRAM modules being used, this signal may or may not need to be buffered externally. This signal, however, should be connected to the corresponding DRAM RAS# line through a damping resistor. As RAS4#, SIMM sizes above 4Mx36 will not be supported and a maximum of 192MB of DRAM will be supported.

82C557 Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
MA[10:0]	77:82, 84, 85, 87:89	O (4mA)		<p>Memory Address Bus: Multiplexed row/column address lines to the DRAMs. Depending on the kind of DRAM modules being used, these signals may or may not need to be buffered externally.</p> <p>The default drive current on the MA[11:0] lines is 4mA, however, by setting SYSCFG 18h[4] = 1, it can be increased to 16mA.</p>
REFRESH#	105	I-CMOS		<p>Refresh: During normal system operation this signal is generated once every 15μs by the 82C558N. During Suspend, if the CLK input to the 82C557 is stopped, the DRAM controller can be programmed to generate DRAM refresh based on the toggles on this input.</p>

3.3.5 Local Bus Interface Signals

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
C/BE[3:0]#	130:133	I/O-TTL (PCI)		<p>PCI Bus Command and Byte Enables 3-0: C/BE[3:0]# are driven by the current bus master (CPU or PCI) during the address phase of a PCI cycle to define the PCI command, and during the data phase as the PCI byte enables. The PCI commands indicate the current cycle type and the PCI byte enables indicate which byte lanes carry meaningful data.</p> <p>C/BE[3:0]# are outputs from the 82C557 during CPU cycles that are directed to the PCI bus. They are inputs during PCI master cycles.</p>
FRAME#	135	I/O-TTL (PCI)		<p>Cycle Frame: Every CPU cycle is translated by the 82C557 to a PCI cycle if it is not a local memory cycle. FRAME# is asserted by the bus master, 82C557 (CPU) or PCI to indicate the beginning and the duration of an access.</p> <p>FRAME# is an input when the 82C557 acts as a slave.</p>
IRDY#	136	I/O-TTL (PCI)		<p>Initiator Ready: The assertion of IRDY# indicates the current bus master's ability to complete the current data phase. IRDY# works in conjunction with TRDY# to indicate when data has been transferred. A data phase is completed on each clock that TRDY# and IRDY# are both sampled asserted. Wait states are inserted until both IRDY# and TRDY# are asserted together.</p> <p>IRDY# is an output from the 82C557 during CPU cycles to the PCI bus and is an input when the 82C557 acts as a slave.</p>

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82C557 Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
TRDY#	137	I/O-TTL (PCI)		<p>Target Ready: TRDY# indicates the target device's ability to complete the current data phase of the transaction. It is used in conjunction with IRDY#. A data phase is completed on each clock that TRDY# and IRDY# are both sampled asserted. Wait states are inserted on the bus until both IRDY# and TRDY# are asserted together.</p> <p>TRDY# is an output from the 82C557 when the 82C557 is the PCI slave and is an input when the 82C557 is a master.</p>
DEVSEL#	138	I/O-TTL (PCI)		<p>Device Select: When asserted, DEVSEL# indicates that the driving device has decoded its address as the target of the current access. DEVSEL# is an output of the 82C557 when 82C557 is a PCI slave. During CPU-to-PCI cycles, DEVSEL# is an input. It is used to determine if any device has responded to the current bus cycle, and to detect a target abort cycle. Master abort termination results if no decode agent exists in the system, and DEVSEL# is not asserted within a fixed number of clocks.</p>
STOP#	139	I/O-TTL (PCI)		<p>Stop: STOP# indicates that the current target is requesting the master to stop the current transaction. This signal is used in conjunction with DEVSEL# to indicate disconnect, target abort, and retry cycles.</p> <p>When the 82C557 is acting as a master on the PCI bus, if STOP# is sampled active on a rising edge of LCLK, FRAME# is negated within a maximum of three clock cycles. STOP# may be asserted by the 82C557. Once asserted, STOP# remains asserted until FRAME# is negated.</p>
AD[31:0]	143:146, 148:162, 166:178	I/O-TTL (PCI)		<p>PCI Address and Data: AD[31:0] are bidirectional address and data lines of the PCI bus. The AD[31:0] signals sample or drive the address and data on the PCI bus. During power-on reset, the 82C557 will drive the AD lines by default.</p> <p>This bus also serves as a conduit for receiving address information during ISA master cycles. The 82C558N conveys the SA[8:0] information to the 82C557 on the AD lines.</p>
PLOCK#	134	O-TTL (PCI)		<p>PCI Lock: PLOCK# is used to indicate an atomic operation that may require multiple transactions to complete. When PLOCK# is asserted, nonexclusive transactions may proceed to an address that is not currently locked.</p>
LRDY#	188	I		<p>Local Ready: The VL bus cycle will be terminated by asserting LRDY#. The 82C558N terminates VL memory requests by asserting LRDY# when other masters own the bus.</p> <p>This signal should be pulled up externally.</p>

82C557 Signal Descriptions (cont.)

3.3.6 82C556/82C558N Interface Signals

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
HREQ	187	I-TTL	During reset if: Pin 187 = 1, normal operation	Hold Request: Master or DMA cycle request from the 82C558N. An external pull-up is required for normal operation.
TMOD#			During reset if: Pin 187 = 0, test mode is entered	<p>Strap Signal for Test Mode Operation (shared with 82C558N): During power-on reset, this is the strap pin to enter the test mode operation.</p> <p>Enable Test Mode: An external pull-down is required on HREQ. If a test mode is to be entered, external pull-ups or pull-downs will also be required on MASTER#, AEN, and REFRESH# as defined below.</p> <p>Test Mode 0: During reset, when HREQ = 0, MASTER# = 0, AEN = 0, and REFRESH# = 1, tristate all outputs and bidirectional pins.</p> <p>Test Mode 1: During reset, when HREQ = 0, MASTER# = 0, AEN = 1, and REFRESH# = 1, tristate all bidirectional pins, and present the output of the NAND chain on the NVMCS output.</p> <p>Test Mode 2: During reset, when HREQ = 0, MASTER# = 1, AEN = 0, and REFRESH# = 1, force all even numbered pins high and odd numbered pins low.</p> <p>Test Mode 3: During reset, when HREQ = 0, MASTER# = 1, AEN = 1, and REFRESH# = 1, force all odd numbered pins high and even numbered pins low.</p>
DBCOE[1:0]#	191, 192	O (4mA)		DBC Output Enables 1 and 0: These two signals along with MDOE# and the HDOE# form the encoded commands that are sent out to the 82C556. These commands inform the 82C556 about the current cycle type and enable it to perform the appropriate data steering, latching and direction controls. The encoded commands are defined in Table 3-6.
MDOE#	189	O (4mA)		Memory Data Output Enable: This signal is used along with DBCOE[1:0]# and HDOE# form the encoded commands that are sent out to the 82C556. When asserted, MDOE# enables data to be put out on the MD bus. MDOE# is asserted for CPU writes to cache/DRAM, CPU writes to PCI, PCI reads from cache/DRAM, L2 cache write-back cycles, and PCI writes to DRAM.
HDOE#	190	O (4mA)		Host Data Output Enable: This signal is used along with DBCOE[1:0]# and MDOE# to form the encoded commands that are sent out to the 82C556. When asserted, HDOE# enables data to be put out on the HD bus. HDOE# is asserted for CPU reads from DRAM/PCI/VL bus, PCI writes to cache, CPU linefills, Suspend mode indication, and reset state indication.



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82C557 Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
DLE[1:0]#	194, 193	O (4mA)		Data Latch Enables: These lines are connected to the DLE[1:0]# pins of the 82C556. They are used to latch the HD and MD data bus depending on which cycle is occurring.
PEN#	185	O (4mA)		Parity Enable: This signal is connected to the PEN# pin of the 82C558N and controls the qualification of the memory parity error (MPERR#) signal.
MDLE#	186	O (4mA)		Memory Data Latch Enable: This signal is connected to the MDLE# pin of the 82C558N. It controls the data flow from the PCI AD[31:0] bus to the high 32-bit memory data bus, MD[63:32], and vice versa. MDLE# is used to latch the data during CPU writes to PCI and PCI writes to DRAM and L2 cache.
3VDRAM#		I	During reset if: Pin 186 = 0, 3.3V Pin 186 = 1, 5.0V	Strap Option for 3.3V DRAM (shared with 82C558N): At power-on reset, this pin functions as a strapping option for 3.3V or 5.0V DRAM operation. If 3.3V DRAM operation, an external pull-down is required. If 5.0V DRAM operation, an external pull-up is required.
MRDC#	123	I-CMOS		Memory Read Command: This input is connected to the MEMR# pin of the 82C558N and monitors ISA memory read operations.
MWTC#	124	I-CMOS		Memory Write Command: This input is connected to the MEMW# pin of the 82C558N and monitors ISA memory write operations.

3.3.7 ISA Bus Interface Signals

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
NVMCS	127	O (4mA)		NVRAM Chip Select: If the current cycle has been decoded as an access to NVRAM, then this pin is used to issue the chip select signal. NVRAM is used for storing the system configuration information and is required for "plug and play" support. The NVRAM must sit on the XD bus.
LA[23:9]	106:113, 115:118, 120:122	I/O- CMOS (8mA)		System Address Bus: LA[23:9] and SA[8:0] on the 82C558N provide the memory and I/O access on the ISA bus and VL bus. The addresses are outputs when the 82C557 owns the ISA bus and are inputs when an external ISA master owns the bus. These signals are internally latched and do not require an external latch. LA[23:9] have internal pull-ups which are disabled when in the Suspend mode.
MASTER#	126	I-CMOS		Master: An ISA bus master asserts MASTER# to indicate that it has control of the ISA bus. Before the ISA master can assert MASTER#, it must first sample DACK# active. Once MASTER# is asserted, the ISA master has control of the ISA bus until it negates MASTER#.



82C557 Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
AEN	125	I-CMOS		Address Enable: This signal is connected to the AEN pin of the 82C558N and monitors ISA bus activity. During power-on reset, if TMOD# is sample low, the AEN pin will be floated. This pin requires an external pull-up.
SUSPEND	129	I-TTL		Suspend: This signal is used to inform the 82C557 about getting into the Suspend mode. SUSPEND needs to be pulled low to resume normal operation.

3.3.8 Power and Ground Pins

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
GND	15, 38, 60, 75, 83, 96, 119, 141, 142, 163, 164, 181, 182, 200	I-G		Ground Connection
VCC3	10, 43, 61	I-P		Power Connection: 3.3V power plane
VCC5	114, 128, 147, 165, 179, 184, 201	I-P		Power Connection: 5.0V power plane
VCC_MEM	86, 97	I-P		Power Connection: 3.3V/5.0V power plane

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3.4 82C557 Suspend Mode Support

Tables 3-9 lists the pin status of the 82C557 during Suspend (refer to Table 3-19 for pin status of the 82C558 during Suspend). The table also list pull-ups/-downs that are engaged internally and external pull-ups that may be required. The 82C556 has a strap option that will enable it to engage inter-

nal pull-downs on the HD bus and pull-ups on the MD bus during Suspend. Please refer to the 82C556 Signal Descriptions for details.

Note: Pins not listed in the table are always driven during Suspend.

Table 3-9 82C557 Pin Status During Suspend

Pin No./Name	When Tristated	Pull-down Engaged	Pull-up Dis-Engaged
2 M/IO#		Suspend	Ext PU
3 D/C#		Suspend or Hold	
4 W/R#+INV+DIRTYO	Suspend	Suspend/18h[3]	
5 ADS#			(Ext PU recommended) Suspend/18h[3]
6 BRDY#	Suspend/18h[3]		
7 NA#	Suspend/18h[3]		
8 KEN#/LEMEM#	Suspend/18h[3]		
9 EADS#+WB/WT	Suspend/18h[3]		
12 HLDA		Suspend/18h[3]	
14 LOCK#		Hold, Suspend/18h[3]	
16 HA3	Suspend	Suspend/18h[3]	Ext PU
17 HA4	Suspend	Suspend/18h[3]	Ext PU
18 HA5	Suspend	Suspend/18h[3]	
19 HA6	Suspend	Suspend/18h[3]	
20 HA7	Suspend	Suspend/18h[3]	
21 HA8	Suspend	Suspend/18h[3]	
22 HA9	Suspend	Suspend/18h[3]	
23 HA10	Suspend	Suspend/18h[3]	
24 HA11	Suspend	Suspend/18h[3]	
25 HA12	Suspend	Suspend/18h[3]	
26 HA13	Suspend	Suspend/18h[3]	
27 HA14	Suspend	Suspend/18h[3]	
28 HA15	Suspend	Suspend/18h[3]	
29 HA16	Suspend	Suspend/18h[3]	
30 HA17	Suspend	Suspend/18h[3]	
31 HA18	Suspend	Suspend/18h[3]	
32 HA19	Suspend	Suspend/18h[3]	
33 HA20	Suspend	Suspend/18h[3]	
34 HA21	Suspend	Suspend/18h[3]	
35 HA22	Suspend	Suspend/18h[3]	
36 HA23	Suspend	Suspend/18h[3]	
37 HA24	Suspend	Suspend/18h[3]	
39 HA25	Suspend	Suspend/18h[3]	

Pin No./Name	When Tristated	Pull-down Engaged	Pull-up Dis-Engaged
40 HA26	Suspend	Suspend/18h[3]	
41 HA27	Suspend	Suspend/18h[3]	
42 HA28	Suspend	Suspend/18h[3]	
44 HA29	Suspend	Suspend/18h[3]	
45 HA30	Suspend	Suspend/18h[3]	
46 HA31	Suspend	Suspend/18h[3]	
47 BE7#		Hold, Suspend/18h[3]	
48 BE6#		Hold, Suspend/18h[3]	
49 BE5#		Hold, Suspend/18h[3]	
50 BE4#		Hold, Suspend/18h[3]	
51 BE3#		Hold, Suspend/18h[3]	
52 BE2#		Hold, Suspend/18h[3]	
53 BE1#		Hold, Suspend/18h[3]	
54 BE0#		Hold, Suspend/18h[3]	
55 HITM#		Suspend/18h[3]	
56 SMIACT#		Suspend/18h[3]	
57 CACHE#		Hold, Suspend/18h[3]	
58 ECDOE#	Suspend/18h[1]		
59 OCDOE#	Suspend/18h[1]		
62 ECAWE#	Suspend/18h[1]		
63 OCAWE#	Suspend/18h[1]		
64 HACALED	Suspend/18h[1]		
65 ECA4	Suspend/18h[1]		
66 OCA4+ECA3	Suspend/18h[1]		
67 CACS7#	Suspend/18h[1]		
68 CACS6#	Suspend/18h[1]		
69 CACS5#	Suspend/18h[1]		
70 CACS4#	Suspend/18h[1]		
71 CACS3#	Suspend/18h[1]		
72 CACS2#	Suspend/18h[1]		
73 CACS1#	Suspend/18h[1]		
74 CACS0#	Suspend/18h[1]		
106 LA23	Suspend		Suspend



82C557 Pin Status During Suspend (cont.)

Pin No./Name	When Tristated	Pull-down Engaged	Pull-up Dis-Engaged
107 LA22	Suspend		Suspend
108 LA21	Suspend		Suspend
109 LA20	Suspend		Suspend
110 LA19	Suspend		Suspend
111 LA18	Suspend		Suspend
112 LA17	Suspend		Suspend
113 LA16	Suspend		Suspend
115 LA15	Suspend		Suspend
116 LA14	Suspend		Suspend
117 LA13	Suspend		Suspend
118 LA12	Suspend		Suspend
120 LA11	Suspend		Suspend
121 LA10	Suspend		Suspend
122 LA9	Suspend		Suspend
127 NVMCS	Suspend		Ext PU to VCC_AT
130 C/BE3#	Suspend/18h[2]		Ext PU to VCC_PCI
131 C/BE2#	Suspend/18h[2]		Ext PU to VCC_PCI
132 C/BE1#	Suspend/18h[2]		Ext PU to VCC_PCI
133 C/BE0#	Suspend/18h[2]		Ext PU VCC_PCI
134 PLOCK#	Suspend/18h[2]		Ext PU to VCC_PCI
135 FRAME#	Suspend/18h[2]		Ext PU to VCC_PCI
136 IRDY#	Suspend/18h[2]		Ext PU to VCC_PCI
137 TRDY#	Suspend/18h[2]		Ext PU to VCC_PCI
138 DEVSEL#	Suspend/18h[2]		Ext PU to VCC_PCI
139 STOP#	Suspend/18h[2]		Ext PU to VCC_PCI
143 AD31	Suspend/18h[2]		
144 AD30	Suspend/18h[2]		
145 AD29	Suspend/18h[2]		
146 AD28	Suspend/18h[2]		
148 AD27	Suspend/18h[2]		
149 AD26	Suspend/18h[2]		
150 AD25	Suspend/18h[2]		
151 AD24	Suspend/18h[2]		
152 AD23	Suspend/18h[2]		
153 AD22	Suspend/18h[2]		
154 AD21	Suspend/18h[2]		
155 AD20	Suspend/18h[2]		
156 AD19	Suspend/18h[2]		
157 AD18	Suspend/18h[2]		
158 AD17	Suspend/18h[2]		

Pin No./Name	When Tristated	Pull-down Engaged	Pull-up Dis-Engaged
159 AD16	Suspend/18h[2]		
160 AD15	Suspend/18h[2]		
161 AD14	Suspend/18h[2]		
162 AD13	Suspend/18h[2]		
166 AD12	Suspend/18h[2]		
167 AD11	Suspend/18h[2]		
168 AD10	Suspend/18h[2]		
169 AD9	Suspend/18h[2]		
170 AD8	Suspend/18h[2]		
171 AD7	Suspend/18h[2]		
172 AD6	Suspend/18h[2]		
173 AD5	Suspend/18h[2]		
174 AD4	Suspend/18h[2]		
175 AD3	Suspend/18h[2]		
176 AD2	Suspend/18h[2]		
177 AD1	Suspend/18h[2]		
178 AD0	Suspend/18h[2]		
185 PEN#			PU Int
186 MDLE#			PU Int
187 HREQ+ TMOD#			Ext PU
188 LRDY#			Ext PU
196 DIRTYWE#	Suspend/18h[1]		
197 DIRTYI	Suspend/18h[1]	Suspend/18h[1]	
198 TAG7	Suspend/18h[1]	Suspend/18h[1]	
199 TAG6	Suspend/18h[1]	Suspend/18h[1]	
202 TAG5	Suspend/18h[1]	Suspend/18h[1]	
203 TAG4	Suspend/18h[1]	Suspend/18h[1]	
204 TAG3	Suspend/18h[1]	Suspend/18h[1]	
205 TAG2	Suspend/18h[1]	Suspend/18h[1]	
206 TAG1	Suspend/18h[1]	Suspend/18h[1]	
207 TAG0	Suspend/18h[1]	Suspend/18h[1]	
208 TAGWE#	Suspend/18h[1]		

Table Abbreviations:

Hold or Suspend: During Hold or during Suspend Mode
 Suspend: During Suspend mode
 Suspend/18h[1]: During Suspend if SYSCFG 18h[1] = 1
 Suspend/18h[2]: During Suspend if SYSCFG 18h[2] = 1
 Suspend/18h[3]: During Suspend if SYSCFG 18h[3] = 1
 Hold, Suspend/18h[3]: During Hold, or during Suspend if SYSCFG 18h[3] = 1
 Ext PU: External pull-up required
 Ext PU to VCC_PCI: External pull-up to VCC_PCI required
 PU Int: Always pulled up internally
Note: SYSCFG 18h[0] must be set to 1 for the controls listed in the above table to be effective.



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Figure 3-4 82C558N Pin Diagram

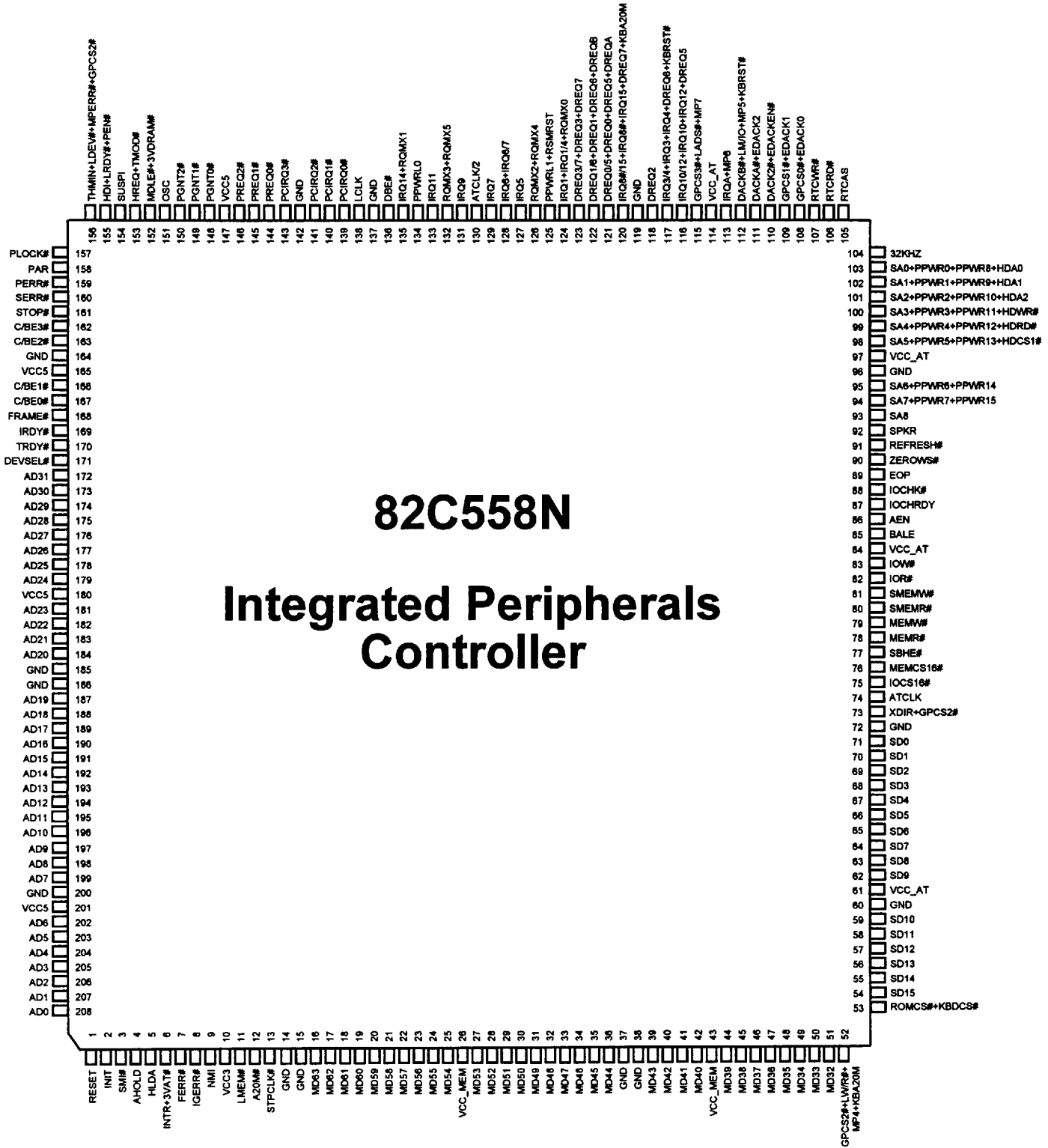


Table 3-10 82C558N Numerical Pin Cross-Reference List

Pin No.	Pin Name	Signal Type	Drive (mA)	Power Plane
1	RESET	I-S-TTL		VCC3
2	INIT	O	4	VCC3
3	SMI#	O	4	VCC3
4	AHOLD	I-TTL		VCC3
5	HLDA	I-TTL		VCC3
6	INTR	O	4	VCC3
	3VAT#	I-TTL		
7	FERR#	I-TTL		VCC3
8	IGERR#	O	4	VCC3
9	NMI	O	4	VCC3
10	VCC3	I-P		
11	LMEM#	I-TTL		VCC3
12	A20M#	O	4	VCC3
13	STPCLK#	O	4	VCC3
14	GND	I-G		
15	GND	I-G		
16	MD63	I/O-TTL	4	VCC_MEM
17	MD62	I/O-TTL	4	VCC_MEM
18	MD61	I/O-TTL	4	VCC_MEM
19	MD60	I/O-TTL	4	VCC_MEM
20	MD59	I/O-TTL	4	VCC_MEM
21	MD58	I/O-TTL	4	VCC_MEM
22	MD57	I/O-TTL	4	VCC_MEM
23	MD56	I/O-TTL	4	VCC_MEM
24	MD55	I/O-TTL	4	VCC_MEM
25	MD54	I/O-TTL	4	VCC_MEM
26	VCC_MEM	I-P		
27	MD53	I/O-TTL	4	VCC_MEM
28	MD52	I/O-TTL	4	VCC_MEM
29	MD51	I/O-TTL	4	VCC_MEM
30	MD50	I/O-TTL	4	VCC_MEM
31	MD49	I/O-TTL	4	VCC_MEM
32	MD48	I/O-TTL	4	VCC_MEM
33	MD47	I/O-TTL	4	VCC_MEM
34	MD46	I/O-TTL	4	VCC_MEM
35	MD45	I/O-TTL	4	VCC_MEM
36	MD44	I/O-TTL	4	VCC_MEM
37	GND	I-G		
38	GND	I-G		
39	MD43	I/O-TTL	4	VCC_MEM
40	MD42	I/O-TTL	4	VCC_MEM
41	MD41	I/O-TTL	4	VCC_MEM
42	MD40	I/O-TTL	4	VCC_MEM
43	VCC_MEM	I-P		
44	MD39	I/O-TTL	4	VCC_MEM
45	MD38	I/O-TTL	4	VCC_MEM
46	MD37	I/O-TTL	4	VCC_MEM

Pin No.	Pin Name	Signal Type	Drive (mA)	Power Plane
47	MD36	I/O-TTL	4	VCC_MEM
48	MD35	I/O-TTL	4	VCC_MEM
49	MD34	I/O-TTL	4	VCC_MEM
50	MD33	I/O-TTL	4	VCC_MEM
51	MD32	I/O-TTL	4	VCC_MEM
52	GPCS2#	O	4	VCC_AT
	LW/R#	O		
	MP4	O		
	KBA20M	I-TTL		
53	ROMCS#	O	4	VCC_AT
	KBDCS#			
54	SD15	I/O-TTL	8	VCC_AT
55	SD14	I/O-TTL	8	VCC_AT
56	SD13	I/O-TTL	8	VCC_AT
57	SD12	I/O-TTL	8	VCC_AT
58	SD11	I/O-TTL	8	VCC_AT
59	SD10	I/O-TTL	8	VCC_AT
60	GND	I-G		
61	VCC_AT	I-P		
62	SD9	I/O-TTL	8	VCC_AT
63	SD8	I/O-TTL	8	VCC_AT
64	SD7	I/O-TTL	8	VCC_AT
65	SD6	I/O-TTL	8	VCC_AT
66	SD5	I/O-TTL	8	VCC_AT
67	SD4	I/O-TTL	8	VCC_AT
68	SD3	I/O-TTL	8	VCC_AT
69	SD2	I/O-TTL	8	VCC_AT
70	SD1	I/O-TTL	8	VCC_AT
71	SD0	I/O-TTL	8	VCC_AT
72	GND	I-G		
73	XDIR	O	4	VCC_AT
	GPCS2#			
74	ATCLK	O	8	VCC_AT
75	IOCS16#	I-TTL		VCC_AT
76	MEMCS16#	I/O-TTL	8	VCC_AT
77	SBHE#	I/O-TTL	8	VCC_AT
78	MEMR#	I/O-TTL	8	VCC_AT
79	MEMW#	I/O-TTL	8	VCC_AT
80	SMEMR#	I/O-TTL	8	VCC_AT
81	SMEMW#	I/O-TTL	8	VCC_AT
82	IOR#	I/O-S-TTL	8	VCC_AT
83	IOW#	I/O-S-TTL	8	VCC_AT
84	VCC_AT	I-P		
85	BALE	O	8	VCC_AT
86	AEN	O	8	VCC_AT
87	IOCHRDY	I/O-TTL	8	VCC_AT
88	IOCHK#	I-TTL		VCC_AT

Pin No.	Pin Name	Signal Type	Drive (mA)	Power Plane
89	EOP	I/O-TTL	8	VCC_AT
90	ZEROWS#	I-TTL		VCC_AT
91	REFRESH#	I/O-TTL	8	VCC_AT
92	SPKR	O	8	VCC_AT
93	SA8	I/O-TTL	8	VCC_AT
94	SA7	I/O-TTL	8	VCC_AT
	PPWR7			
	PPWR15			
95	SA6	I/O-TTL	8	VCC_AT
	PPWR6			
	PPWR14			
96	GND	I-G		
97	VCC_AT	I-P		
98	SA5	I/O-TTL	8	VCC_AT
	PPWR5			
	PPWR13			
	HDCS1#			
99	SA4	I/O-TTL		VCC_AT
	PPWR4			
	PPWR12			
	HDRD#			
100	SA3	I/O-TTL		VCC_AT
	PPWR3			
	PPWR11			
	HDWR#			
101	SA2	I/O-TTL		VCC_AT
	PPWR2			
	PPWR10			
	HDA2			
102	SA1	I/O-TTL		VCC_AT
	PPWR1			
	PPWR9			
	HDA1			
103	SA0	I/O-TTL	8	VCC_AT
	PPWR0			
	PPWR8			
	HDA0			
104	32KHZ	I-S		VCC_AT
105	RTCAS	O	4	VCC_AT
106	RTC RD#	O	4	VCC_AT
107	RTCWR#	O	4	VCC_AT
108	GPCS0#	O	4	VCC_AT
	EDACK0			
109	GPCS1#	O	4	VCC_AT
	EDACK1			
110	DACK2#	O	4	VCC_AT
	EDACKEN#			



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82C558N Numerical Pin Cross-Reference List (cont.)

Pin No.	Pin Name	Signal Type	Drive (mA)	Power Plane
111	DACKA#	O	4	VCC_AT
	EDACK2			
112	DACKB#	I/O-TTL	4	VCC_AT
	LM/IO#			
	MP5			
	KBRST#			
113	IRQA	I-TTL		VCC_AT
	MP6	O	4	
114	VCC_AT	I-P		
115	GPCS3#	O	4	VCC_AT
	LADS#			
	MP7			
116	IRQ10/12	I-TTL		VCC_AT
	IRQ10			
	IRQ12			
	DREQ5			
117	IRQ3/4	I-TTL		VCC_AT
	IRQ3			
	IRQ4			
	DREQ6			
	KBRST#			
118	DREQ2	I-TTL		VCC_AT
119	GND	I-G		
120	IRQ8#/15	I-TTL		VCC_AT
	IRQ8#			
	IRQ15			
	DREQ7			
	KBA20M			
121	DREQ0/5	I-TTL		VCC_AT
	DREQ0			
	DREQ5			
	DREQA			
122	DREQ1/6	I-TTL		VCC_AT
	DREQ1			
	DREQ6			
	DREQB			
123	DREQ3/7	I-TTL		VCC_AT
	DREQ3			
	DREQ7			
124	IRQ1	I-TTL		VCC_AT
	IRQ1/4			
	RQMX0			
125	PPWRL1	O	4	VCC_AT
	RSMRST			
126	RQMX2	I-TTL		VCC_AT
	RQMX4			

Pin No.	Pin Name	Signal Type	Drive (mA)	Power Plane
127	IRQ5	I-TTL		VCC_AT
128	IRQ6	I-TTL		VCC_AT
	IRQ6/7			
129	IRQ7	I-TTL		VCC_AT
130	ATCLK/2	O	4	VCC_AT
131	IRQ9	I-TTL		VCC_AT
132	RQMX3	I-TTL		VCC_AT
	RQMX5			
133	IRQ11	I-TTL		VCC_AT
134	PPWRL0	O	4	VCC_AT
135	IRQ14	I-TTL		VCC_AT
	RQMX1			
136	DBE#	O	4	VCC_AT
137	GND	I-G		
138	LCLK	I-TTL		VCC
139	PCIRQ0#	I-TTL		VCC
140	PCIRQ1#	I-TTL		VCC
141	PCIRQ2#	I-TTL		VCC
142	GND	I-G		
143	PCIRQ3#	I-TTL		VCC
144	PREQ0#	I-TTL		VCC
145	PREQ1#	I-TTL		VCC
146	PREQ2#	I-TTL		VCC
147	VCC5	I-P		
148	PGNT0#	O	PCI	VCC
149	PGNT1#	O	PCI	VCC
150	PGNT2#	O	PCI	VCC
151	OSC	I-TTL		VCC
152	MDLE#	I-TTL		VCC
	3VDRAM#			
153	HREQ	O	4	VCC
	TMOD#			
154	SUSPI	O	4	VCC
155	HDI	I-TTL		VCC
	LRDY#			
	PEN#			
156	THMIN	I/O-TTL	4	VCC
	LDEV#			
	MPERR#			
	GPCS2#			
157	PLOCK#	I-TTL		VCC
158	PAR	I/O-TTL	PCI	VCC
159	PERR#	I/O-TTL	PCI	VCC
160	SERR#	I/O-TTL	PCI	VCC
161	STOP#	I/O-TTL	PCI	VCC
162	C/BE3#	I/O-TTL	PCI	VCC

Pin No.	Pin Name	Signal Type	Drive (mA)	Power Plane
163	C/BE2#	I/O-TTL	PCI	VCC
164	GND	I-G		
165	VCC	I-P		
166	C/BE1#	I/O-TTL	PCI	VCC
167	C/BE0#	I/O-TTL	PCI	VCC
168	FRAME#	I/O-TTL	PCI	VCC
169	IRDY#	I/O-TTL	PCI	VCC
170	TRDY#	I/O-TTL	PCI	VCC
171	DEVSEL#	I/O-TTL	PCI	VCC
172	AD31	I/O-TTL	PCI	VCC
173	AD30	I/O-TTL	PCI	VCC
174	AD29	I/O-TTL	PCI	VCC
175	AD28	I/O-TTL	PCI	VCC
176	AD27	I/O-TTL	PCI	VCC
177	AD26	I/O-TTL	PCI	VCC
178	AD25	I/O-TTL	PCI	VCC
179	AD24	I/O-TTL	PCI	VCC
180	VCC5	I-P		
181	AD23	I/O-TTL	PCI	VCC
182	AD22	I/O-TTL	PCI	VCC
183	AD21	I/O-TTL	PCI	VCC
184	AD20	I/O-TTL	PCI	VCC
185	GND	I-G		
186	GND	I-G		
187	AD19	I/O-TTL	PCI	VCC
188	AD18	I/O-TTL	PCI	VCC
189	AD17	I/O-TTL	PCI	VCC
190	AD16	I/O-TTL	PCI	VCC
191	AD15	I/O-TTL	PCI	VCC
192	AD14	I/O-TTL	PCI	VCC
193	AD13	I/O-TTL	PCI	VCC
194	AD12	I/O-TTL	PCI	VCC
195	AD11	I/O-TTL	PCI	VCC
196	AD10	I/O-TTL	PCI	VCC
197	AD9	I/O-TTL	PCI	VCC
198	AD8	I/O-TTL	PCI	VCC
199	AD7	I/O-TTL	PCI	VCC
200	GND	I-G		
201	VCC5	I-P		
202	AD6	I/O-TTL	PCI	VCC
203	AD5	I/O-TTL	PCI	VCC
204	AD4	I/O-TTL	PCI	VCC
205	AD3	I/O-TTL	PCI	VCC
206	AD2	I/O-TTL	PCI	VCC
207	AD1	I/O-TTL	PCI	VCC
208	AD0	I/O-TTL	PCI	VCC



Table 3-11 82C558N Alphabetical Pin Cross-Reference List

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
32KHZ	104	DREQ1/6	122	IRQ3/4	117	MDLE#	152	SA5	98
A20M#	12	DREQ1		IRQ3		3VDRAM#		PPWR5	
AD0	208	DREQ6		IRQ4		MEMCS16#	76	PPWR13	
AD1	207	DREQB		DREQ6		MEMR#	78	HDCS1#	
AD2	206	DREQ2	118	KBRST#		MEMW#	79	SA6	95
AD3	205	DREQ3/7	123	IRQ5	127	NMI	9	PPWR6	
AD4	204	DREQ3		IRQ6/7	128	OSC	151	PPWR14	
AD5	203	DREQ7		IRQ6		PAR	158	SA7	94
AD6	202	EOP	89	IRQ7	129	PCIRQ0#	139	PPWR7	
AD7	199	FERR#	7	IRQ8#/15	120	PCIRQ1#	140	PPWR15	
AD8	198	FRAME#	168	IRQ8#		PCIRQ2#	141	SA8	93
AD9	197	GND	14	IRQ15		PCIRQ3#	143	SBHE#	77
AD10	196	GND	15	DREQ7		PERR#	159	SD0	71
AD11	195	GND	37	KBA20M		PGNT0#	148	SD1	70
AD12	194	GND	38	IRQ9	131	PGNT1#	149	SD2	69
AD13	193	GND	60	IRQ10/12	116	PGNT2#	150	SD3	68
AD14	192	GND	72	IRQ10		PLOCK#	157	SD4	67
AD15	191	GND	96	IRQ12		PPWRL0	134	SD5	66
AD16	190	GND	119	DREQ5		PPWRL1	125	SD6	65
AD17	189	GND	137	IRQ11	133	RSMRST		SD7	64
AD18	188	GND	142	IRQ14	135	PREQ0#	144	SD8	63
AD19	187	GND	164	RQXM1		PREQ1#	145	SD9	62
AD20	184	GND	185	LCLK	138	PREQ2#	146	SD10	59
AD21	183	GND	186	LMEM#	11	REFRESH#	91	SD11	58
AD22	182	GND	200	MD32	51	RESET	1	SD12	57
AD23	181	GPCS0#	108	MD33	50	ROMCS#	53	SD13	56
AD24	179	EDACK0		MD34	49	KBDCS#		SD14	55
AD25	178	GPCS1#	109	MD35	48	RQMX2	126	SD15	54
AD26	177	EDACK1		MD36	47	RQMX4		SERR#	160
AD27	176	GPCS2#	52	MD37	46	RQMX3	132	SMEMR#	80
AD28	175	LWR#		MD38	45	RQMX5		SMEMW#	81
AD29	174	MP4		MD39	44	RTCAS	105	SMi#	3
AD30	173	KBA20M		MD40	42	RTCRD#	106	SPKR	92
AD31	172	GPCS3#	115	MD41	41	RTCWR#	107	STOP#	161
AEN	86	LADS#		MD42	40	SA0	103	STPCLK#	13
AHOLD	4	MP7		MD43	39	PPWR0		SUSPI	154
ATCLK	74	HDI	155	MD44	36	PPWR8		THMIN	156
ATCLK/2	130	LRDY#		MD45	35	HDA0		LDEV#	
BALE	85	PEN#		MD46	34	SA1	102	MPERR#	
C/BE0#	167	HLDA	5	MD47	33	PPWR1		GPCS2#	
C/BE1#	166	HREQ	153	MD48	32	PPWR9		TRDY#	170
C/BE2#	163	IGERR#	8	MD49	31	HDA1		VCC3	10
C/BE3#	162	INIT	2	MD50	30	SA2	101	VCC5	147
DACK2#	110	INTR	6	MD51	29	PPWR2		VCC5	165
EDACKEN#		3VAT#		MD52	28	PPWR10		VCC5	180
DACKA#	111	IOCHRDY	87	MD53	27	HDA2		VCC5	201
EDACK2		IOCHK#	88	MD54	25	SA3	100	VCC_AT	61
DACKB#	112	IOCS16#	75	MD55	24	PPWR3		VCC_AT	84
LMIO#		IOR#	82	MD56	23	PPWR11		VCC_AT	97
MP5		IOW#	83	MD57	22	HDIR#		VCC_AT	114
KBRST#		IRDY#	169	MD58	21	SA4	99	VCC_MEM	26
DBE#	136	IRQA	113	MD59	20	PPWR4		VCC_MEM	43
DEVSEL#	171	MP6		MD60	19	PPWR12		XDIR	73
DREQ0/5	121	IRQ1	124	MD61	18	HDRD#		GPCS2#	
DREQ0		IRQ1/4		MD62	17			ZEROWS#	90
DREQ5		RQMX0		MD63	16				
DREQA									



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3.5 82C558N Signal Descriptions

3.5.1 Reset and Clock Signals

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
LCLK	138	I-TTL		Local Bus Clock: This input clock is the same clock that is used by local bus devices. It can also be divided internally to provide the AT clock signal. This input may also be used to provide timing information to the integrated IDE interface state machine.
ATCLK	74	O (8mA)		AT Bus Clock: This signal is derived from an internal division of LCLK. It is used to sample and drive all ISA synchronous signals. PCIDV1 47h[5:4] sets the ATCLK: 00 = LCLK+4 10 = LCLK+2 01 = LCLK+3 11 = LCLK. The ATCLK is also used to demultiplex and sample externally multiplexed inputs. During Suspend, it is possible to output 32KHz on this pin.
ATCLK/2	130	O (4mA)		AT Bus Clock Divide by 2: This signal is simply ATCLK divided by 2 and it is used for multiplexed signal sampling.
OSC	151	I-TTL		Timer Oscillator Clock: This is the main clock used by the internal 8254 timers. It is connected to the 14.31818MHz oscillator. This input may also be used to provide timing information to the integrated IDE interface state machine.
INIT	2	O (4mA)		CPU Initialize: Emulated keyboard reset, I/O Port 092h bit 0 low-to-high transition or a shutdown cycle will trigger INIT. INIT will be valid for a minimum of 16 clocks when asserted.
RESET	1	I-S-TTL		CPU Reset: An output from the 82C557 in response to a PWRGD input.

3.5.2 82C557 and 82C556 Interface Signals

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
MD[63:32]	16:25, 27:36, 39:42, 44:51	I/O-TTL (4mA)		High 32-Bit Memory Data Bus: These pins are connected directly to the high 32 bits of the system MD bus. All PCI, VL, and ISA data accesses to the system are conducted via these pins.



82C558N Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
MDLE#	152	I-TTL		Memory Data Latch Enable: This signal is connected to the MDLE# pin of the 82C557 and controls the data flow from the PCI AD[31:0] bus to the high 32-bit memory bus and vice versa. It is used to latch the data during CPU write to PCI and PCI write to DRAM and L2 cache.
3VDRAM#			During reset if: Pin 152 = 0, 3.3V Pin 152 = 1, 5.0V	Strap Option for 3.3V DRAM (shared with 82C557): At power-on reset, this pin functions as a strapping option for 3.3V or 5.0V DRAM operation. The strap information is also passed to the 82C557 through AD0 during power-on reset. 3.3V DRAM Interface - An external pull-down is required. 5.0V DRAM Interface - An external pull-up is required.

3.5.3 PCI Bus Interface Signals

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
C/BE[3:0]#	162, 163, 166, 167	I/O-TTL (PCI)		PCI Bus Command and Byte Enables: During the address phase of a transaction, C/BE[3:0]# define the PCI command. During the data phase, C/BE[3:0]# are used as the PCI byte enables. The PCI commands indicate the current cycle type, and the PCI byte enables indicate which byte lanes carry meaningful data. The 82C558N drives C/BE[3:0]# as an initiator of a PCI bus cycle and monitors C/BE[3:0]# as a target.
PAR	158	I/O-TTL (PCI)		Calculated Parity Signal: PAR is "even" parity and is calculated on 36 bits AD[31:0] plus C/BE[3:0]#. PAR is generated for address and data phases and is only guaranteed to be valid on the PCI clock after the corresponding address or data phase.
FRAME#	168	I/O-TTL (PCI)		Cycle Frame: FRAME# is driven by the current bus master to indicate the beginning and duration of an access. FRAME# is asserted to indicate that a bus transaction is beginning. FRAME# is an input to the 82C558N when the 82C558N is the target. FRAME# is an output when it is the initiator.
IRDY#	169	I/O-TTL (PCI)		Initiator Ready: IRDY# indicates the 82C558N's ability, as an initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on each clock that both IRDY# and TRDY# are sampled asserted. IRDY# is an input to the 82C558N when the 82C558N is the target and an output when it is the initiator.
TRDY#	170	I/O-TTL (PCI)		Target Ready: TRDY# indicates the 82C558N's ability to complete the current data phase of the transaction. It is used in conjunction with IRDY#. A data phase is completed on each clock that TRDY# and IRDY# are both sampled asserted. TRDY# is an input to the 82C558N when the 82C558N is the initiator and an output when it is the target.



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82C558N Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
DEVSEL#	171	I/O-TTL (PCI)		Device Select: The 82C558N asserts DEVSEL# to claim a PCI transaction. As an output, the 82C558N asserts DEVSEL# when it samples configuration cycles to the 82C558N's configuration registers. The 82C558N also asserts DEVSEL# when an internal IPC address is decoded. As an input, DEVSEL# indicates the response to a transaction. If no slave claims the cycle, the 82C558N will assert DEVSEL# to terminate the cycle.
STOP#	161	I/O-TTL (PCI)		STOP: STOP# indicates that the 82C558N, as a target, is requesting a master to stop the current transaction. As a master, STOP# causes the 82C558N to stop the current transaction. STOP# is an output when the 82C558N is a target and an input when it is the initiator.
PLOCK#	157	I-TTL		PCI Lock: PLOCK# is used to indicate an atomic operation that may require multiple transactions to complete. When PLOCK# is asserted, nonexclusive transactions may proceed to an address that is not currently locked. Control of PLOCK# is obtained under its own protocol in conjunction with PGNT#.
PERR#	159	I/O-TTL (PCI)		Parity Error: PERR# may be pulsed by any agent that detects a parity error during an address phase, or by the master, or by the selected target during any data phase in which the AD[31:0] lines are inputs. Upon sampling PERR# active, the 82C558N generates a non-maskable interrupt (NMI) to the 3.3V Pentium CPU.
SERR#	160	I/O-TTL (PCI)		System Error: SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the 82C558N generates a non-maskable interrupt (NMI) to the 3.3V Pentium CPU.
AD[31:0]	172:179, 181:184, 187:199, 202:208	I/O-TTL (PCI)		PCI Address and Data: AD[31:0] are bidirectional address and data lines for the PCI bus. The AD[31:0] signals sample or drive the address and data on the PCI bus. During power-on reset, the AD0 line is driven by the 82C558N to reflect the 3.3V/5.0V DRAM strap option.
PCIRQ[3:0]#	143, 141:139	I-TTL		PCI Interrupt Requests 3-0: An active low assertion indicates that the respective interrupt is active.
PREQ[2:0]#	146:144	I-TTL		PCI Requests 2-0: An active low assertion indicates that one of the initiators desires the use of the PCI bus.
PGNT[2:0]#	150:148	O (PCI)		PCI Grants 2-0: An active low signal on one of these pins indicates that one of the initiators has been granted use of the PCI bus. Note that only one of these signals may be active at any time.



82C558N Signal Descriptions (cont.)

3.5.4 PMU Interface Signals

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
SMI#	3	O (4mA)		System Management Interrupt: This signal is used to request System Management Mode (SMM) operation from the 3.3V Pentium CPU.
STPCLK#	13	O (4mA)		Stop Clock: The 82C558N asserts STPCLK# to request a CPU transition to a low power mode. The CPU responds with a Stop Grant cycle before going to the low power mode. This signal is always asserted during Suspend.
PPWRL1	125	O (4mA)	PCIDV1 4Dh[4] = 0	Power Control Latch 1: This signal latches the values on an external '373 latch from SA[7:0] to control external peripheral devices. Regardless of what signal this pin is programmed to be, the pin will behave like PPWRL1 during RESET. It will be high for the duration of the RESET input to the 82C558N, will drop low with RESET, and remain so until it is programmed to be anything else.
RSMRST			PCIDV1 4Dh[4] = 1	Resume Reset: Generates a hard reset to the CPU on resuming from Suspend mode.
PPWRL0	134	O (4mA)		Power Control Latch 0: This signal latches the values on an external '373 latch from SA[7:0] to control external peripheral devices.
RQMX2	126	I-TTL	PCIDV1 45h[6] = 0	Request Mux 2: A time multiplexed input for RINGI, EPMI2#, EPMI3#, and LOBAT.
RQMX4			PCIDV1 45h[6] = 1	Request Mux 4: A time multiplexed input for RINGI, EPMI2#, KBRST#, and LOBAT.
RQMX3	132	I-TTL	PCIDV1 45h[6] = 0	Request Mux 3: A time multiplexed input for SUS/RES#, EPMI0#, EPMI1#, and LLOBAT.
RQMX5			PCIDV1 45h[6] = 1	Request Mux 5: A time multiplexed input for SUS/RES#, EPMI0#, EPMI1#, and KBA20.
SUSPI	154	O (4mA)		The 82C558N activates this output to put the 82C557 in the Suspend mode. SUSPI is also activated by the 82C558N during "hot docking" without actually engaging Suspend, to indicate to the 82C557 that it should tristate its buses based upon register values in SYSCFG 18h.
HDI	155	I-TTL	PCIDV1 45h[4:3] = 00 or 11	Hot Docking Indication: An external pull-down is recommended if this feature is not used.
LRDY#			PCIDV1 45h[4:3] = 01	Local Bus Ready Indication: The VL bus cycle will be terminated by asserting LRDY#. The 82C558N terminates VL memory requests by asserting LRDY# when other masters own the bus. An external pull-up is required.
PEN#			PCIDV1 45h[4:3] = 10	Parity Enable Indication: This signal controls the qualification of the memory parity error (MPERR#) signal from the 82C556.



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82C558N Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
THMIN	156	I/O-TTL	PCIDV1 45h[4:3] = 00	Thermal Management Input
LDEV#			PCIDV1 45h[4:3] = 01	Local Bus Device
MPERR#			PCIDV1 45h[4:3] = 10	Memory Parity Error Indication
GPCS2#			PCIDV1 45h[4:3] = 11	General Purpose Chip Select 2

3.5.5 ISA Bus Interface Signals

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
SD[15:0]	54:59, 62:71	I/O-TTL (8mA)		System Data Bus: SD[15:0] provides the 16-bit data path for devices residing on the ISA bus.
SA8	93	I/O-TTL (8mA)		System Address Bus Line 8: SA[8:0] and LA[23:9] on the 82C557 provide the memory and I/O access on the ISA bus. The addresses are outputs when the 82C558N owns the ISA bus. The addresses are inputs when an external ISA master owns the ISA bus.
SA7	94	I/O-TTL (8mA)	Cycle Multiplexed	System Address Bus Line 7
PPWR7				Peripheral Power Control Line 7
PPWR15				Peripheral Power Control Line 7
SA6	95	I/O-TTL (8mA)	Cycle Multiplexed	System Address Bus Line 6
PPWR6				Peripheral Power Control Line 6
PPWR14				Peripheral Power Control Line 14
SA5	98	I/O-TTL (8mA)	Cycle Multiplexed	System Address Bus Line 5
PPWR5				Peripheral Power Control Line 5
PPWR13				Peripheral Power Control Line 13
HDCS1#				Drive Chip Select 1: Provides a stable version of SA9 for decoding.
SA4	99	I/O-TTL (8mA)	Cycle Multiplexed	System Address Bus Line 4
PPWR4				Peripheral Power Control Line 4
PPWR12				Peripheral Power Control Line 12
HDRD#				Drive Read Strobe: Provides the read strobe signal for the IDE drive; also switches the data buffer direction toward the SD bus during read cycles.
SA3	100	I/O-TTL (8mA)	Cycle Multiplexed	System Address Bus Line 3
PPWR3				Peripheral Power Control Line 3
PPWR11				Peripheral Power Control Line 11
HDWR#				Drive Write Strobe: Provides the write strobe signal for the IDE drive.



82C558N Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
SA2	101	I/O-TTL (8mA)	Cycle Multiplexed	System Address Bus Line 2
PPWR2				Peripheral Power Control Line 2
PPWR10				Peripheral Power Control Line 10
HDA2				Drive Address Line 2
SA1	102	I/O-TTL (8mA)	Cycle Multiplexed	System Address Bus Line 1
PPWR1				Peripheral Power Control Line 1
PPWR9				Peripheral Power Control Line 9
HDA1				Drive Address Line 1
SA0	103	I/O-TTL (8mA)	Cycle Multiplexed	System Address Bus Line 0
PPWR0				Peripheral Power Control Line 2
PPWR8				Peripheral Power Control Line 8
HDA0				Drive Address Line 0
IOCS16#	75	I-TTL		16-Bit I/O Chip Select: This signal is driven by I/O devices on the ISA bus to indicate that they support 16-bit I/O bus cycles.
MEMCS16#	76	I/O-TTL (8mA)		16-Bit Memory Chip Select: ISA slaves that are 16-bit memory devices drive this signal low. MEMCS16# is an input when the 82C558N owns the ISA bus. The 82C558N drives this signal low during ISA master to PCI memory cycles.
SBHE#	77	I/O-TTL (8mA)		System Byte High Enable: When asserted, SBHE# indicates that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is negated during refresh cycles. SBHE# is an output when the 82C558N owns the ISA bus.
DBE#	136	O (4mA)		Data Buffer Enable: The IDE controller multiplexes its control and address signals on the SA lines. DBE# goes active when the SA lines are generating an IDE cycle.
MEMR#	78	I/O-TTL (8mA)		Memory Read: MEMR# is the command to a memory slave that it may drive data onto the ISA data bus. MEMR# is an output when the 82C558N is a master on the ISA bus. MEMR# is an input when an ISA master, other than 82C558N, owns the ISA bus.
MEMW#	79	I/O-TTL (8mA)		Memory Write: MEMW# is the command to a memory slave that it may latch data from the ISA data bus. MEMW# is an output when the 82C558N owns the ISA bus. MEMW# is an input when an ISA master, other than 82C558N, owns the ISA bus.
AEN	86	O (8mA)		Address Enable: AEN is asserted during DMA cycles to prevent I/O slaves from misinterpreting DMA cycles as valid I/O cycles. When asserted, AEN indicates to an I/O resource on the ISA bus that a DMA transfer is occurring. This signal is asserted also during refresh cycles. AEN is driven low upon reset.

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82C558N Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
IOCHRDY	87	I/O-TTL (8mA)		I/O Channel Ready: Resources on the ISA bus deassert IOCHRDY to indicate that wait states are required to complete the cycle. IOCHRDY is an input when the 82C558N owns the ISA bus. IOCHRDY is an output when an external ISA bus master owns the ISA bus.
IOCHK#	88	I-TTL		I/O Channel Check: When asserted, it indicates that a parity or a non-correctable error has occurred for a device or memory on the ISA bus. A NMI will be generated to the 3.3V Pentium CPU.
BALE	85	O (8mA)		Bus Address Latch Enable: BALE is an active high signal asserted by the 82C558N to indicate that the address, AEN, and SBHE# signal lines are valid. BALE remains asserted throughout ISA master and DMA cycles.
IOR#	82	I/O-S-TTL (8mA)		I/O Read: IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus (SD[15:0]). The I/O slave device must hold the data valid until after IOR# is negated. IOR# is an output when the IPC owns the ISA bus. IOR# is an input when an external ISA master owns the ISA bus.
IOW#	83	I/O-S-TTL (8mA)		I/O Write: IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus (SD[15:0]). IOW# is an output when the 82C558N owns the ISA bus. IOW# is an input when an external ISA master owns the ISA bus.
SMEMR#	80	I/O-TTL (8mA)		System Memory Read: The 82C558N asserts SMEMR# to request a memory slave to provide data. If the access is below the 1MB range (00000000h-000FFFFh) during DMA compatible, IPC master, or ISA master cycles, the 82C558N asserts SMEMR#.
SMEMW#	81	I/O-TTL (8mA)		System Memory Write: The 82C558N asserts SMEMW# to request a memory slave to accept data from the data lines. If the access is below the 1MB range (00000000h-000FFFFh) during DMA compatible, IPC master, or ISA master cycles, the 82C558N asserts SMEMW#.
ZEROWS#	90	I-TTL		Zero Wait States: An ISA slave asserts ZEROWS# after its address and command signals have been decoded to indicate that the current cycle does not require any wait states.

82C558N Signal Descriptions (cont.)

3.5.6 ISA DMA Arbiter Signals

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
DREQ0/5	121	I-TTL	Non-602A Mode: PCIDV1 49h[1:0] = 00	Multiplexed DMA Request 0/5: The DREQ is used to request DMA service from the DMA controller within the 82C558N or for a 16-bit master to gain control of the expansion bus.
DREQ0			602A Mode: PCIDV1 49h[1:0] = 01	DMA Request 0
DREQ5			Non-602A Mode: PCIDV1 49h[1:0] = 10	DMA Request 5
DREQA			602A Mode: PCIDV1 49h[1:0] = 11	DMA Request A: The DMA request on this input may be mapped to any internal DMA channel (DREQ[7:5] or DREQ[3:0]) by programming PCIDV1 4Ch[7] and 4Dh[1:0]. If pin 121 has been selected to be DREQA, then the DREQ[x] to which DREQA is internally mapped to will also be recognized through other pins that may also be programmed to accept DREQ[x].
DREQ1/6	122	I-TTL	Non-602A Mode: PCIDV1 48h[7:6] = 00	Multiplexed DMA Request 1/6: The DREQ is used to request DMA service from the DMA controller within the 82C558N, or for a 16-bit master to gain control of the expansion bus.
DREQ1			602A Mode: PCIDV1 48h[7:6] = 01	DMA Request 1
DREQ6			Non-602A Mode: PCIDV1 48h[7:6] = 10	DMA Request 6
DREQB			602A Mode: PCIDV1 48h[7:6] = 11	DMA Request B: The DMA request on this input may be mapped to any internal DMA channel (DREQ[7:5] or DREQ[3:0]) by programming PCIDV1 4Ch[6:4]. If pin 122 has been selected to be DREQB, then the DREQ[x] to which DREQB is internally mapped to will also be recognized through other pins that may also be programmed to accept DREQ[x].
DREQ2	118	I-TTL		DMA Request 2: The DREQ2 is used to request DMA service from the DMA controller within the 82C558N or for a 16-bit master to gain control of the expansion bus.

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82C558N Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
DREQ3/7	123	I-TTL	Non-602A Mode: PCIDV1 48h[5:4] = 00	Multiplexed DMA Request 3/7: The DREQ is used to request DMA service from the DMA controller within the 82C558N or for a 16-bit master to gain control of the expansion bus.
DREQ3			602A Mode: PCIDV1 48h[5:4] = 01	DMA Request 3
DREQ7			Non-602A Mode: PCIDV1 48h[5:4] = 10	DMA Request 7
DACK2#	110	O (4mA)	PCIDV1 45h[1] = 0	DMA Acknowledge 2
EDACKEN#			PCIDV1 45h[1] = 1	Encoded DACK# Enable: Enables DACK decoder output.
DACKA#	111	O (4mA)	PCIDV1 45h[1] = 0	General Purpose DMA Acknowledge: If pin 111 is selected to be DACKA#, the DACK[x]# that is generated on this pin depends upon the settings in PCIDV1 4Ch[7] and 4Dh[1:0]. Regardless of whether the corresponding DREQ[x] was generated via DREQA, or any other pin that may directly programmed to accept DREQ[x]. If PCIDV1 4Ch[7] and 4Dh[1:0] are set to 010b, then DACK2# is generated on this pin. DACK2# will not be generated on pin 110.
EDACK2			PCIDV1 45h[1] = 1	Encoded DACK Mux 2: EDACK[2:0] encode the currently active DACK# line.
DACKB#	112	I/O-TTL (4mA)	PCIDV1 45h[4:3] = 00	General Purpose DMA Acknowledge: If pin 112 is selected to be DACKB#, the DACK[x]# that is generated on this pin depends upon the settings in PCIDV1 4Ch[6:4]. Regardless of whether the corresponding DREQ[x] was generated via DREQB, or any other pin that may directly programmed to accept DREQ[x]. If PCIDV1 4Ch[6:4] are set to 010b, then DACK2# is generated on this pin. DACK2# will not be generated on pin 110.
LM/IO#			PCIDV1 45h[4:3] = 01	Local Bus Memory I/O
MP5			PCIDV1 45h[4:3] = 10	Memory Parity 5
KBRST#			PCIDV1 45h[4:3] = 11	Keyboard Reset: From keyboard controller if internal keyboard emulation is disabled by setting PCIDV1 41h[4].
EOP	89	I/O-TTL (8mA)		End of Process: EOP is bidirectional, acting in one of two modes, and is directly connected to the TC line of the ISA bus. DMA slaves assert EOP to the 82C558N to terminate DMA cycles. The 82C558N asserts EOP to DMA slaves as a terminal count indicator.



82C558N Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
REFRESH#	91	I/O-TTL (8mA)		<p>Refresh: As an output, this signal is used to inform the 82C557 to refresh the local DRAM.</p> <p>During normal operation, a low pulse is generated every 15μs to indicate to the 82C557 that the DRAM is to be refreshed.</p> <p>During Suspend, if normal DRAM is used, the 32KHZ input to the 82C558N is routed out on this pin so that the 82C557 may perform DRAM refresh.</p> <p>An option to continuously drive this signal low during Suspend is also provided. The internal pull-up on this pin is disengaged in Suspend.</p>
32KHZ	104	I-S		<p>32KHz Clock: This signal is used as a 32KHz clock input. This signal is used for power management, and is usually the only active clock when the system is in Suspend mode.</p>
HREQ	153	O (4mA)		<p>Hold Request: This signal is connected to the HREQ pin of the 82C557 to indicate that a master or DMA cycle has requested control of the bus.</p> <p>An external pull-up is required for normal operation.</p>
TMOD#		I-TTL	<p>During reset if: Pin 153 = 1, normal operation Pin 153 = 0, test mode is entered</p>	<p>Strap Signal for Test Mode Operation (shared with 82C557): During power-on reset, this is the strap pin to enter the test mode operation.</p> <p>Enable Test Mode: An external pull-down is required. If a test mode is to be entered, appropriate pull-ups or pull-downs on IRQ9 and IRQ11 will also be required for the straps shown below.</p> <p>Test Mode 0: During reset, when HRQ = 0, IRQ11 = 0, and IRQ9 = 0, float all outputs and bidirectional pins.</p> <p>Test Mode 1: During reset, when HRQ = 0, IRQ11 = 0, and IRQ9 = 1, configure all bidirectional pins as inputs and present the output of the NAND chain on the SPKR output.</p> <p>Test Mode 2: During reset, when HRQ = 0, IRQ11 = 1, and IRQ9 = 0, drive all even numbered pins high and all odd numbered pins low.</p> <p>Test Mode 3: During reset, when HRQ = 0, IRQ11 = 1, and IRQ9 = 1, drive all odd numbered pins high and all even numbered pins low.</p>
AHOLD	4	I-TTL		<p>Address Hold: This signal is connected to the AHOLD pin of the 82C557 and is used to monitor the bus arbitration.</p>
HLDA	5	I-TTL		<p>CPU Hold Acknowledge: This input is connected to the HLDA line of the 3.3V Pentium CPU. This signal indicates that the CPU has relinquished bus control to a bus master.</p>

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82C558N Signal Descriptions (cont.)

3.5.7 Interrupt Control Signals

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
IRQA	113	I-TTL	PCIDV1 45h[5:4]	Interrupt Request A: A general purpose interrupt that may be mapped internally to any IRQ by programming PCIDV1 4Ch[3:0]. The IRQ[x] that IRQA is internally mapped to will still be recognized through other pins that may be programmed to accept that interrupt (by itself or when muxed with other interrupts). If it is necessary to block other sources for IRQ[x] and have IRQA as the sole source, PCIDV1 45h[0] has to be set.
MP6		O (4mA)	PCIDV1 45h[4:3] = 10	Memory Parity 6
IRQ1	124	I-TTL	Non-602A Mode: PCIDV1 48h[3] = 0	Interrupt Request 1
IRQ1/4			Non-602A Mode: PCIDV1 48h[3] = 1	Multiplexed Interrupt Request 1/4: A time multiplexed input for IRQ1 and IRQ4.
RQMX0			602A Mode: PCIDV1 48h[3] = 0	Request Mux 0: A time multiplexed input for IRQ1, IRQ3, IRQ10, and IRQ12.
IRQ3/4	117	I-TTL	Non-602A Mode: PCIDV1 49h[5:4] = 00	Interrupt Request 3/4: A time multiplexed input for IRQ3 and IRQ4.
IRQ3			Non-602A Mode: PCIDV1 49h[5:4] = 01	Interrupt Request 3
IRQ4			Non-602A Mode: PCIDV1 49h[5:4] = 10	Interrupt Request 4
DREQ6			602A Mode: PCIDV1 49h[5:4] = 00	DMA Request 6
KBRST#			602A Mode: PCIDV1 49h[5:4] = 01	Keyboard Reset: An input from the keyboard controller if internal keyboard emulation is disabled.
IRQ5	127	I-TTL		Interrupt Request 5
IRQ6	128	I-TTL	Non-602A Mode: PCIDV1 48h[1] = 0	Interrupt Request 6
IRQ6/7			602A Mode: PCIDV1 48h[1] = 0	Multiplexed Interrupt Request 6/7: A time multiplexed input for IRQ6 and IRQ7.
IRQ7	129	I-TTL	Non-602A Mode: PCIDV1 48h[0] = 0 602A Mode: PCIDV1 48h[0] = 0	Interrupt Request 7
IRQ9	131	I-TTL		Interrupt Request 9 (Also refer to the signal description for HREQ.)

82C558N Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
IRQ11	133	I-TTL		Interrupt Request 11 (Also refer to the signal description for HREQ.)
IRQ14	135	I-TTL	Non-602A Mode: PCIDV1 48h[2] = 0	Interrupt Request 14
RQMX1			602A Mode: PCIDV1 48h[2] = 0	Request Mux 1: A time multiplexed input for IRQ8#, IRQ4, IRQ14, and IRQ15.
IRQ8#/15	120	I-TTL	Non-602A Mode: PCIDV1 49h[3:2] = 00	Multiplexed Interrupt Request 8#/15: A time multiplexed input for IRQ8# and IRQ15.
IRQ8#			Non-602A Mode: PCIDV1 49h[3:2] = 01	Interrupt Request 8#
IRQ15			Non-602A Mode: PCIDV1 49h[3:2] = 10	Interrupt Request 15
DREQ7			602A Mode: PCIDV1 49h[3:2] = 00	DMA Request 7
KBA20M			602A Mode: PCIDV1 49h[3:2] = 01	Keyboard Address Bit 20 Mask: An input from the keyboard controller if internal keyboard emulation is disabled.
IRQ10/12			116	I-TTL
IRQ10	Non-602A Mode: PCIDV1 49h[7:6] = 01	Interrupt Request 10		
IRQ12	Non-602A Mode: PCIDV1 49h[7:6] = 10	Interrupt Request 12		
DREQ5	602A Mode: PCIDV1 49h[7:6] = 00	DMA Request 5		
INTR	6	O (4mA)		Interrupt Request: INTR is driven by the 82C558N to signal the 3.3V Pentium CPU that an interrupt request is pending and needs to be serviced. The interrupt controller must be programmed following a reset to ensure that INTR is at a known state.
3VAT#		I-TTL	During reset if: Pin 6 = 0, 3.3V Pin 6 = 1, 5.0V	Strap Option for 3.3V ISA Bus: At power-on reset, this pin functions as a strapping option for 3.3V or 5.0V ISA bus operation. An internal pull-up is enabled during reset. 3.3V ISA bus operation - An external pull-down is required. 5.0V ISA bus operation - Default.
FERR#	7	I-TTL		Floating Point Coprocessor Error: This input causes two operations to occur. IRQ13 is triggered and IGERR# is enabled. An I/O write to Port 0F0h will set IGERR# low when FERR# is low.
IGERR#	8	O (4mA)		Ignore Coprocessor Error: IGERR# will go low after FERR# goes low and I/O write to Port 0F0h occurs. When FERR# goes high, IGERR# is driven high. This pin is normally high.



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82C558N Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
NMI	9	O (4mA)		Non-Maskable Interrupt: This signal is activated when a parity error from a local memory read is detected or when the IOCHK# signal from the ISA bus is asserted and the corresponding control bit in Port B is also enabled. The 82C558N also generates an NMI when either PERR# or SERR# is asserted.

3.5.7.1 RTC and Timer Signals

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
RTCAS	105	O (4mA)		RTC Address Strobe: This signal is connected to the real-time clock's address strobe.
RTCRD#	106	O (4mA)		RTC Read: This pin is used to drive the read signal of the real-time clock.
RTCWR#	107	O (4mA)		RTC Write: This pin is used to drive the write signal of the real-time clock.
SPKR	92	O (8mA)		Speaker Data: This pin is used to drive the system board speaker. This signal is a function of the Timer-0 Counter-2 and Port 061h bit 1.

3.5.7.2 Miscellaneous Signals

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
LMEM#	11	I-TTL		Local Memory Accessed Indication: During local bus master accesses to local DRAM memory, this signal is driven by the 82C557. This information is used by the 82C558N to decide if the cycle is to be passed on to the local bus.
GPCS3#	115	O (4mA)	PCIDV1 45h[4:3] = 00	General Purpose Chip Select 3
LADS#			PCIDV1 45h[4:3] = 01	Local ADS#
MP7			PCIDV1 45h[4:3] = 10	Memory Parity Bit 7
GPCS2#	52	O (4mA)	PCIDV1 45h[4:3] = 00	General Purpose Chip Select 2
LW/R#			PCIDV1 45h[4:3] = 01	Local Write/Read
MP4			PCIDV1 45h[4:3] = 10	Memory Parity Bit 4
KBA20M			I-TTL	PCIDV1 45h[4:3] = 11



82C558N Signal Descriptions (cont.)

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
GPCS1#	109	O (4mA)	PCIDV1 45h[1] = 0	General Purpose Chip Select 1
EDACK1			PCIDV1 45h[1] = 1	Encoded DACK 1
GPCS0#	108	O (4mA)	PCIDV1 45h[1] = 0	General Purpose Chip Select 0
EDACK0			PCIDV1 45h[1] = 1	Encoded DACK 0
XDIR	73	O (4mA)	PCIDV1 4Dh[6] = 0	X Bus Direction: This signal is connected directly to the direction control of a 74F245 that buffers the utility data bus.
GPCS2#			PCIDV1 4Dh[6] = 1	General Purpose Chip Select 2
A20M#	12	O (4mA)		<p>Address Bit 20 Mask: This pin is an output and generates the A20M# output by trapping GATEA20 commands to the keyboard or to Port 092h. The INIT signal to the CPU is generated whenever it senses reset commands to Port 060h/064h, or a Port 092h write command with bit 0 set high.</p> <p>When keyboard emulation is disabled, the 82C558N traps only Port 092h GATEA20 commands and accepts the GATEA20 input from the keyboard controller, which is sent out as A20M# to the CPU.</p>
ROMCS#	53	O (4mA)		BIOS ROM Chip Select: This output goes active on both reads and writes to the ROM area to support flash ROM. For flash ROM support, writes to ROM can be supported by appropriately setting PCIDV1 47h[7].
KBDCS#				Keyboard Chip Select: It is also used to decode accesses to the keyboard controller.



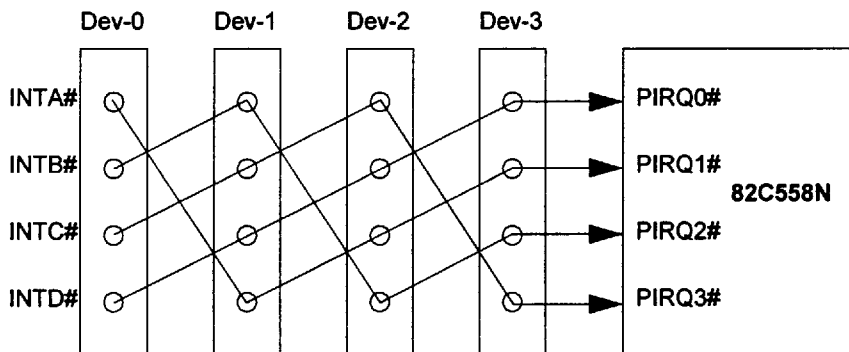
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82C558N Signal Descriptions (cont.)

3.5.7.3 Power and Ground Signals

Signal Name	Pin No.	Signal Type	Selected By	Signal Description
GND	14, 15, 37, 38, 60, 72, 96, 119, 137, 142, 164, 185, 186, 200	I-G		Ground Connection
VCC3	10	I-P		Power Connection: 3.3V plane
VCC5	147, 165, 180, 201	I-P		Power Connection: 5.0V plane
VCC_AT	61, 84, 97, 114,	I-P		Power Connection: ISA bus power plane
VCC_MEM	26, 43	I-P		Power Connection: Memory power plane

Figure 3-5 PCI Interrupts Mapping Matrix



3.6 82C558N Programmable Pin Information

Table 3-12 82C558N Group-Wise Programmable Pins - Group 1

Pin No.	Selection 0	Selection 1
108	GPCS0#	EDACK0
109	GPCS1#	EDACK1
110	DACK2#	EDACKEN#
111	DACKA#	EDACK2

Table 3-13 82C558N Group-Wise Programmable Pins - Group 2

Pin No.	Selection 00	Selection 01	Selection 10	Selection 11
52	GPCS2#	LWR#	MP4	KBA20M
112	DACKB#	LMIO#	MP5	KBRST#
113	IRQA	IRQA	MP6	Reserved
115	GPCS3#	LADS#	MP7	Reserved
155	HDI	LRDY#	PEN#	HDI
156	THMIN	LDEV#	MPERR#	GPCS2#

Table 3-14 82C558N Group-Wise Programmable Pins - Group 3

Pin No.	Selection 0	Selection 1
126	RQMX2: RINGI+EPMI2#+EPMI3#+LOBAT	RQMX4: RINGI+EPMI2#+KBRST#+LOBAT
132	RQMX3: SUS/RES#+EPMI0#+EPMI1#+LLOBAT	RQMX5: SUS/RES#+ EPMI0#+EPMI1#+KBA20M

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Table 3-15 lists those pins that may be group-wise programmed to be signals listed under "Selection 0" or "Selection 1". This group of pins must be programmed to "Selection 0" if the 82C602A is not used, and must be programmed to "Selection 1" if the 82C602A is used.

Table 3-15 Group-Wise Programmable Pins - Group 4

Pin No.	Selection 0 (Non-602A Mode)	Selection 1 (602A-Mode)
116	IRQ10/12+ IRQ10+IRQ12	DREQ5+Reserved
117	IRQ3/4+IRQ3+IRQ4	DREQ6+KBRST#+Reserved+Reserved
120	IRQ8#/15+IRQ8#+IRQ15	DREQ7+KBA20M+Reserved+Reserved
121	DREQ0/5+DREQ0+DREQ5	DREQ0+DREQ0/5+DREQ5+DREQA
122	DREQ1/6+DREQ1+DREQ6	DREQ1+DREQ1/6+DREQ6+DREQB
123	DREQ3/7+DREQ3+DREQ7	DREQ3+DREQ3/7+DREQ7+Reserved
124	IRQ1+IRQ1/4	RQMX0 (IRQ1/3/10/12)
128	IRQ6+IRQ6/7	IRQ6
129	IRQ7+Reserved	IRQ7
135	IRQ14+Reserved	RQMX1 (IRQ8#/4/14/15)

Table 3-16 82C558N Pin-Wise Programmable Pin #1

Pin No.	Selection 0	Selection 1
73	XDIR	GPCS2#

Table 3-17 82C558N Pin-Wise Programmable Pin #2

Pin No.	Selection 0	Selection 1
125	PPWRL1	RSMRST

Table 3-18 IDE Support Signals

Pin No.	IDE Support Signal Name	Multiplexed on 82C558N Signal
103	HDA0	SA0
102	HDA1	SA1
101	HDA2	SA2
99	HDRD#	SA4
100	HDWR#	SA3
98	HDCS1#	SA5
136	DBE#	DBE#



3.7 82C558N Suspend Mode Support

Table 3-19 list the status of the pins on the 82C558N during Suspend (refer to Table 3-9 for the pin status of the 82C557 during Suspend). The table also list pull-ups/-downs that are engaged internally and external pull-ups that may be required. The 82C556 has a strap option that will enable it to engage internal pull-downs on the HD bus and pull-ups on

the MD bus during Suspend. Please refer to the 82C556 Signal Descriptions for details.

Note: Pins not listed in the table are always driven during Suspend.

Table 3-19 82C558N Pin Status During Suspend

Pin No./Name	Hold/Suspend Level	PU/PD, Where
3 SMI#	TS CPU0V	
6 INTR	TS on Reset, Driven in Suspend	Int PU on Reset
7 FERR#		PD on CPU0V
8 IGERR#	TS CPU0V	
11 LMEM#		PD during CPU0V
12 A20M#	TS CPU0V	
13 STPCLK#	TS CPU0V	
16 MD63	TS Suspend	
17 MD62	TS Suspend	
18 MD61	TS Suspend	
19 MD60	TS Suspend	
20 MD59	TS Suspend	
21 MD58	TS Suspend	
22 MD57	TS Suspend	
23 MD56	TS Suspend	
24 MD55	TS Suspend	
25 MD54	TS Suspend	
27 MD53	TS Suspend	
28 MD52	TS Suspend	
29 MD51	TS Suspend	
30 MD50	TS Suspend	
31 MD49	TS Suspend	
32 MD48	TS Suspend	
33 MD47	TS Suspend	
34 MD46	TS Suspend	
35 MD45	TS Suspend	
36 MD44	TS Suspend	
39 MD43	TS Suspend	
40 MD42	TS Suspend	
41 MD41	TS Suspend	
42 MD40	TS Suspend	
44 MD39	TS Suspend	
45 MD38	TS Suspend	
46 MD37	TS Suspend	
47 MD36	TS Suspend	
48 MD35	TS Suspend	
49 MD34	TS Suspend	
50 MD33	TS Suspend	
51 MD32	TS Suspend	

Pin No./Name	Hold/Suspend Level	PU/PD, Where
52 GPCS2#	TS Suspend	Ext PU for GPCS2#, LWR#
53 ROMCS#+ KBDCS#	TS Suspend	Ext PU
54 SD15	TS Suspend	Ext PU/Int PU disengaged in Suspend
55 SD14	TS Suspend	Ext PU/Int PU disengaged in Suspend
56 SD13	TS Suspend	Ext PU/Int PU disengaged in Suspend
57 SD12	TS Suspend	Ext PU/Int PU disengaged in Suspend
58 SD11	TS Suspend	Ext PU/Int PU disengaged in Suspend
59 SD10	TS Suspend	Ext PU/Int PU disengaged in Suspend
62 SD9	TS Suspend	Ext PU/Int PU disengaged in Suspend
63 SD8	TS Suspend	Ext PU/Int PU disengaged in Suspend
64 SD7	TS Suspend	Ext PU/Int PU disengaged in Suspend
65 SD6	TS Suspend	Ext PU/Int PU disengaged in Suspend
66 SD5	TS Suspend	Ext PU/Int PU disengaged in Suspend
67 SD4	TS Suspend	Ext PU/Int PU disengaged in Suspend
68 SD3	TS Suspend	Ext PU/Int PU disengaged in Suspend
69 SD2	TS Suspend	Ext PU/Int PU disengaged in Suspend
70 SD1	TS Suspend	Ext PU/Int PU disengaged in Suspend
71 SD0	TS Suspend	Ext PU/Int PU disengaged in Suspend
73 XDIR+GPCS2#	TS Suspend	Ext PU for XDIR+GPCS2#
74 ATCLK	D/DL Suspend	
76 MEMCS16#	TS Suspend	
77 SBHE#	TS Suspend	
78 MEMR#	TS Suspend	



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82C558N Pin Status During Suspend (cont.)

Pin No./Name	Hold/Suspend Level	PU/PD, Where
79 MEMW#	TS Suspend	
80 SMEMR#	TS Suspend	
81 SMEMW#	TS Suspend	
82 IOR#	TS Suspend	
83 IOW#	TS Suspend	
85 BALE	DL	
86 AEN	DL	
87 IOCHRDY	TS Suspend	
89 EOP	DL	
92 SPKR	TS Suspend	
91 REFRESH#	D/DL	Int PU disengaged during Suspend
105 RTCAS	DL	
106 RTCRD#	TS Suspend	Ext 20K PU
107 RTCWR#	TS Suspend	Ext 20K PU
108 GPCS0#	TS for GPCS0#, D/TS for EDACK0 (SYSCFG D5h[7:6])	
109 GPCS1#	TS for GPCS1#, D/TS for EDACK1 (SYSCFG D5h[7:6])	
110 DACK2#	TS for DACK2#/ DL for EDACKEN#	Ext PU for DACK2#
111 DACKA#	TS for DACKA#, D/TS for EDACK2 (SYSCFG D5h[7:6])	
112 DACKB#	TS Suspend	Ext PU
113 IRQA	TS Suspend	
115 GPCS3#	TS Suspend	External PU
130 ATCLK/2	D/DL	
136 DBE#	DH	
148 PGNT0#	TS Suspend	Ext PU
149 PGNT1#	TS Suspend	Ext PU
150 PGNT2#	TS Suspend	Ext PU
153 HREQ	DH/DL	
154 SUSPI	D	Open Drain Output, Ext PU
156 THMIN	TS Suspend	Ext PU for GPCS2#
158 PAR	TS Suspend	
159 PERR#	TS Suspend	
160 SERR#	TS Suspend	
161 STOP#	TS Suspend	
162 C/BE3#	TS Suspend	
163 C/BE2#	TS Suspend	
166 C/BE1#	TS Suspend	
167 C/BE0#	TS Suspend	
168 FRAME#	TS Suspend	
169 IRDY#	TS Suspend	
170 TRDY#	TS Suspend	
171 DEVSEL#	TS Suspend	
172 AD31	TS Suspend	

Pin No./Name	Hold/Suspend Level	PU/PD, Where
173 AD30	TS Suspend	
174 AD29	TS Suspend	
175 AD28	TS Suspend	
176 AD27	TS Suspend	
177 AD26	TS Suspend	
178 AD25	TS Suspend	
179 AD24	TS Suspend	
181 AD23	TS Suspend	
182 AD22	TS Suspend	
183 AD21	TS Suspend	
184 AD20	TS Suspend	
187 AD19	TS Suspend	
188 AD18	TS Suspend	
189 AD17	TS Suspend	
190 AD16	TS Suspend	
191 AD15	TS Suspend	
192 AD14	TS Suspend	
193 AD13	TS Suspend	
194 AD12	TS Suspend	
195 AD11	TS Suspend	
196 AD10	TS Suspend	
197 AD9	TS Suspend	
198 AD8	TS Suspend	
199 AD7	TS Suspend	
202 AD6	TS Suspend	
203 AD5	TS Suspend	
204 AD4	TS Suspend	
205 AD3	TS Suspend	
206 AD2	TS Suspend	
207 AD1	TS Suspend	
208 AD0	TS Suspend	

Table Abbreviations:

TS: Tristate
 TS Suspend: Tristate during Suspend
 TS CPU0V: Tristate during CPU0V (SYSCFG ADh[5] = 1)
 D: Driven
 DL: Driven low
 DH: Driven high
 Ext PU: External pull-up required
 Int PU: Internal pull-up

Note: For the internal pull-ups/-downs to be active, SYSCFG A0h[6] = 1.



4.0 Functional Description

4.1 Reset Logic

The PWRGD input to the 82C557 is used to generate the CPU and the system reset (CPURST). PWRGD is a "cold reset" which is generated when either PWRGD goes low (from the power supply, indicating a low power condition) or the system reset button is activated. When PWRGD makes a low-to-high transition, CPURST will go active and will remain active for at least 1ms after PWRGD goes high.

The INIT signal is used to initialize the 3.3V CPU during warm resets. INIT is generated for the following cases:

- When a shutdown condition is decoded from the CPU bus definition signals, the 82C558N will assert INIT for 15 T-states.
- Keyboard reset to I/O Port 064h.
- Fast reset to I/O Port 092h.

4.2 System Clocks

4.2.1 CPU and 82C557 Clocks

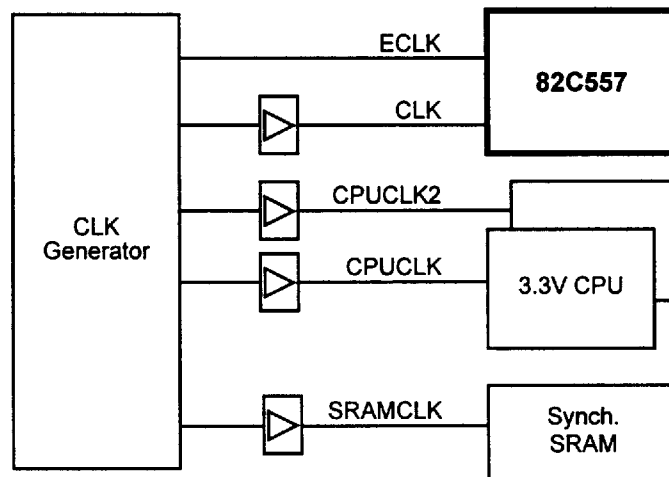
The 82C557 uses two high frequency clock inputs, CLK and ECLK.

The clock signals that go to the CPU and the 82C557's CLK inputs are required to be in the same phase and have minimum skew between them. The skew between the CLK input to the 82C557 and the CLK input to the CPU should not exceed 1ns. The 82C557's CLK is a single phase clock which is used to sample all host CPU synchronous signals and for clocking the 82C557's internal state machines.

ECLK literally means "Early Clock". ECLK is used for generating some critical signals for the host CPU and the cache controller logic. Its main use is to clock signals out earlier so that the signals are guaranteed to meet setup times of the CPU and cache. ECLK is required to be in the same phase as CLK but ahead of CLK. The delay from ECLK to CLK must meet the delay timing of a minimum of 2ns and a maximum of 4ns.

Figure 4-1 shows the relationship between CPUCLK, CLK, and ECLK and the typical CPU and 82C557's clock distribution circuit.

Figure 4-1 CPU and 82C557 Clock Distribution



82C556/82C557/82C558N

4.2.2 PCI and VL Bus Clocks

The 82C557 and the 82C558N require LCLK for the PCI and VL bus interface. The phase and frequency of the LCLK input to the 82C557, 82C558N, PCI bus, and VL bus is required to be the same and the maximum skew should not exceed 2ns. Figure 4-2 and Figure 4-3 show possible clock generation and distribution schemes for LCLK. The local bus can be asynchronous/synchronous to the CPU bus, but must be synchronous to the PCI bus.

4.2.3 ISA Bus Clocks

The 82C558N generates the ISA bus clock (ATCLK) from an internal division of LCLK. The ATCLK frequency is programmable and can be set to any of the four clock division options: LCLK/1, LCLK/2, LCLK/3, LCLK/4. This allows the system designer to tailor the ISA bus clock frequency to support a wide range of system designs and performance platforms.

Figure 4-2 Clock Distribution Method for VL Bus and PCI Connectors (Async. PCI and VL Bus)

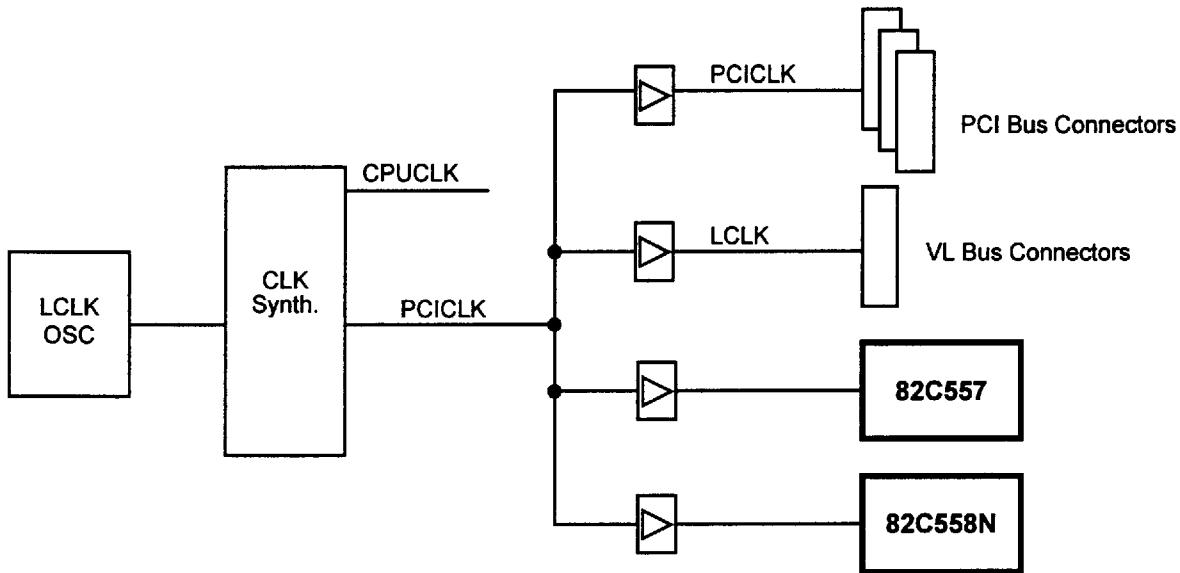
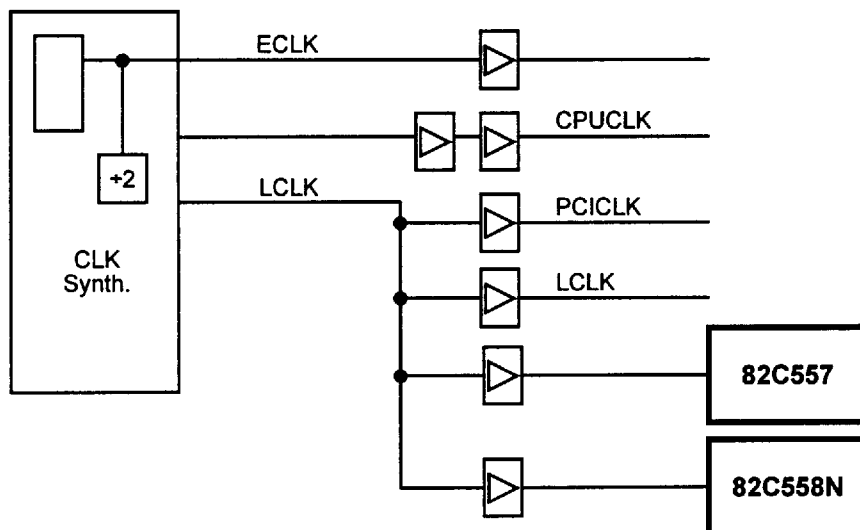


Figure 4-3 Clock Distribution Method for VL Bus and PCI Connectors (Sync. PCI and VL Bus)



4.3 Cache Subsystem

The integrated cache controller, which uses a direct-mapped, bank-interleaved scheme (for an asynchronous SRAM implementation) dramatically boosts the overall performance of the local memory subsystem by caching writes as well as reads (write-back mode). Cache memory can be configured as one or two banks of asynchronous SRAMs and sizes of 64KB, 128KB, 256KB, 512KB, 1MB, and 2MB are supported. In addition, the cache controller also supports 256KB, 512KB, 1MB, and 2MB of synchronous SRAM in a single/double bank configuration. Two programmable non-cacheable regions are provided. The cache controller operates in a non-pipelined or a pipelined mode, with a fixed 32-byte line size (optimized to match a CPU burst linefill) in order to simplify the motherboard design without increasing cost or degrading system performance. The secondary cache operates independently and in addition to the CPU's internal cache.

The cache controller of the 82C557 has a built-in tag comparator which improves system performance while reducing component count on the system board. The controller features a 64-bit wide data bus with 32-byte CPU burst support. The cache controller supports both write-back, adaptive write-back, and write-through schemes.

The cache controller uses a 32-byte secondary cache line size. It supports read and write bursting in 3-2-2-2 bursts for the asynchronous SRAM and 3-1-1-1 burst read/write for synchronous SRAMs. 2-1-1-1 burst read/write cycles are supported for synchronous SRAMs at 50MHz. In this case, the ADSC# output of the processor needs to be connected to the ADSC# input of the synchronous SRAM. The 8-bit tag has a "dirty" bit option for the write-back cache. The cache controller uses standard single bank SRAMs or dual bank SRAMs with interleaving (only in the case for asynchronous SRAM) for optimum cache performance.

4.3.1 CPU Burst Mode Control

The Viper-N Chipset fully supports the 64-bit wide data path for the CPU burst read and burst write cycles. The cache and DRAM controllers in the 82C557 ensure that data is burst into the CPU whenever the CPU requests a burst linefill or a burst write to the system memory.

The 82C557 contains separate burst counters to support DRAM and external cache burst cycles. The DRAM controller performs a burst for the L2 cache read miss linefill cycle (DRAM to L2 cache and CPU) and the cache controller burst supports the CPU burst linefill (3.3V Pentium and K5 burst linefill and the Cyrix M1 linear burst linefill) for the L2 cache hit cycle (L2 cache to the 3.3V Pentium CPU). Depending on the kind of processor being used, either the 3.3V Pentium quad word burst address sequencing or the Cyrix M1 quad word linear burst address sequencing is used for all system memory burst cycles.

4.3.1.1 Cyrix Linear Burst Mode Support

The Viper-N Chipset supports the Cyrix linear burst mode. SYSCFG 17h[0] in the 82C557 determines which burst mode is to be implemented, the Intel 3.3V Pentium CPU burst mode or the Cyrix linear burst mode (see Table 4-1). No additional hardware is required for supporting either of these modes.

When using a synchronous SRAM solution, care must be taken that the synchronous SRAM burst protocol complements the processor's burst protocol. Table 4-2 shows the burst mode sequence for both of these processors.

Table 4-1 Burst Type Select Register Bit

7	6	5	4	3	2	1	0
SYSCFG 17h			Miscellaneous Control Register 2				Default = 00h
Generate NA# for PCI slave access in sync LCLK mode: 0 = No 1 = Yes	NA# generation for PCI slave access: 0 = Do not generate NA# 1 = Generate NA# for async LCLK mode	Sync two bank select: 0 = Rsvd 1 = Set this bit to 1 when two banks of sync SRAM are installed	BRDY# control for PCI cycles: 0 = Normal BRDY# 1 = Fast BRDY#	Fast FRAME# generation for PCI cycles: 0 = Disable 1 = Enable	Pipelining during byte merge: 0 = Disabled 1 = Enabled	Sync SRAM type: 0 = Standard 1 = Pipelined	Burst type: 0 = Intel burst protocol 1 = Linear burst protocol



Table 4-2 Burst Modes

1st Address	2nd Address	3rd Address	4th Address
Cyrix Linear Burst Mode			
0	8	10	18
8	10	18	0
10	18	0	8
18	0	8	10
Intel Burst Mode			
0	8	10	18
8	0	18	10
10	18	0	8
18	10	8	0

4.3.2 Cache Cycle Types

Some cache terminology and cycle definitions that are chipset specific:

The cache hit/miss status is generated by comparing the high-order address bits (for the memory cycle in progress) with the stored tag bits from previous cache entries. When a match is detected and the location is cacheable, a cache hit cycle takes place. If the comparator does not detect a match or a non-cacheable location is accessed (based on the internal non-cacheable region registers), then the current cycle is a cache miss.

A cache hit/miss decision is always made at the end of the first T2 for a non-pipeline cycle and at the end of the first T2P for a pipeline cycle, so the SRAM read/write cycle will begin after the first T2 or T2P. The cacheable decision is based on the DRAM bank decodes and the chipset's configuration registers for non-system memory areas and non-cacheable area definitions. If the access falls outside the system memory area, it is always non-cacheable.

The dirty bit is a mechanism for monitoring coherency between the cache and system memory. Each tag entry has a corresponding dirty bit to indicate whether the data in the represented cache line has been modified since it was loaded from system memory. This allows the 82C557 to determine whether the data in the system memory is "stale" and needs to be updated before a new memory location is

allowed to overwrite the currently indexed cache entry. The Viper-N supports several Tag/Dirty schemes and those are described in Section 4.3.4.7 on page 76.

A linefill cycle occurs for a cache read miss cycle. It is a data read of the new address location from the system memory and a corresponding write to the cache. The tag data will also be updated with the new address.

A castout cycle occurs for a cache read miss cycle, but only if the cache line that is being replaced is "dirty". In this cycle, the dirty cache line is read from the cache and written to the system memory. The upper address bits for this cycle are provided by the tag data bits.

A write-back cycle consists of performing a castout cycle followed by a linefill cycle. The write-back cycle causes an entire cache line (32 bytes) to be written back to memory followed by a line burst from the new memory location into the cache and to the CPU simultaneously. The advantages of performing fast write cycles to the cache (for a write hit) typically outweigh the cycle overhead incurred by the write-back scheme.

4.3.3 Single and Double Bank Support

The 82C557 supports one or two banks of SRAM. SYSCFG 08h[7] controls this feature (as shown in Table 4-3).

Table 4-3 SRAM Bank Support Register Bit

7	6	5	4	3	2	1	0
SYSCFG 08h							
CPU Cache Control Register 1							
Default = 00h							
L2 cache bank select: 0 = Double bank (inter-leaved) ⁽¹⁾ 1 = Single bank (non-inter-leaved)	Line comparator for bus masters: ⁽²⁾ 0 = Disable 1 = Enable	CPU HITM# pin sample timing: 0 = Delay 1 more clock 1 = No delay	DRAM parity check: 0 = Disable 1 = Enable	Combined Tag/Dirty control: 0 = Tag and Dirty on different chips 1 = Tag and Dirty are on the same chip	CPU address pipelining: ⁽³⁾ 0 = Disable 1 = Enable	L1 cache write-back/write-through mode setting: 0 = Write-through only 1 = Write-back enabled	BIOS area cacheability in L1 cache: 0 = Cacheable 1 = Non-cacheable
(1) Interleaved on A3 for async SRAMs, interleaved on A17 for sync SRAMs. Note that for 2-1-1-1 sync SRAM operation, dual non-interleaved banks are not supported. Only single bank is supported. (2) For a master request if the subsequent read/write is within the same cache line, CPU 'Inquire' cycles are not done until there is a cache line miss. (3) Turn on for standard sync SRAMs in 3-1-1-1 RW or for async SRAMs. This bit must be off for standard sync SRAMs in 2-1-1-1 RW. Also refer to SYSCFG 11h[4]. At any time, either SYSCFG 08h[2] or 11h[4] can be active, but not both at the same time.							

4.3.4 Cache Operation

The following discussion pertains to asynchronous SRAMs, but is valid for the synchronous SRAM as well, except that the synchronous SRAM supports 3-1-1-1 cycles and 2-1-1-1 cycles at 50MHz instead of 3-2-2-2 cycles.

4.3.4.1 L2 Cache Read Hit

On an L1 read miss and an L2 read hit, the secondary cache provides data to the CPU. The 82C557 follows either the 3.3V Pentium CPU's burst protocol or the M1's linear burst mode protocol to fill the processor's internal cache line.

The cache controller will sample CACHE# from the CPU at the end of T1 and perform a burst read if CACHE# is sampled active. The first cache read hit for a cycle is always one wait state. If a read cycle can be converted to a burst, the read cycle is extended for the additional three words continuing at one wait state per cycle. To achieve the burst at this rate, the hit or miss decision must be made before BRDY# is returned to the CPU at the end of the second T2. The cache hit comparator in the 82C557 compares the data from the tag RAM with the higher address bits from the CPU bus. The output of this comparator generates the BRDY# signal to the 3.3V

Pentium CPU. The tag comparator's output is sampled at the end of the first T2, and BRDY# is generated one clock later for cache hits, resulting in a leadoff of three cycles. BRDY# will go inactive to add wait states depending on the wait states programmed. Refer to Table 4-5 for the tag compare table.

If two SRAM banks are used, address bit A4 from the CPU will be the least significant address bit that goes to the data SRAMs. The data output for each SRAM bank is controlled by a separate output enable for each SRAM bank (OCDOE# and ECDOE#). The OCDOE#/ECDOE# generation for the leadoff cycle is based on address bit A3 from the CPU. The two signals OCDOE# and ECDOE# will interleave the data read from the two cache banks in a burst cycle. If one SRAM bank is used, address bit A3 from the CPU will be the least significant address bit that goes to the SRAMs and the output enable ECDOE# will be active for the complete cycle.

Figures 4-4 through 4-6 show various L2 cache read hit cycles.



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Figure 4-4 L2 Cache Read Hit Cycle - Async. SRAMs (Double Bank)

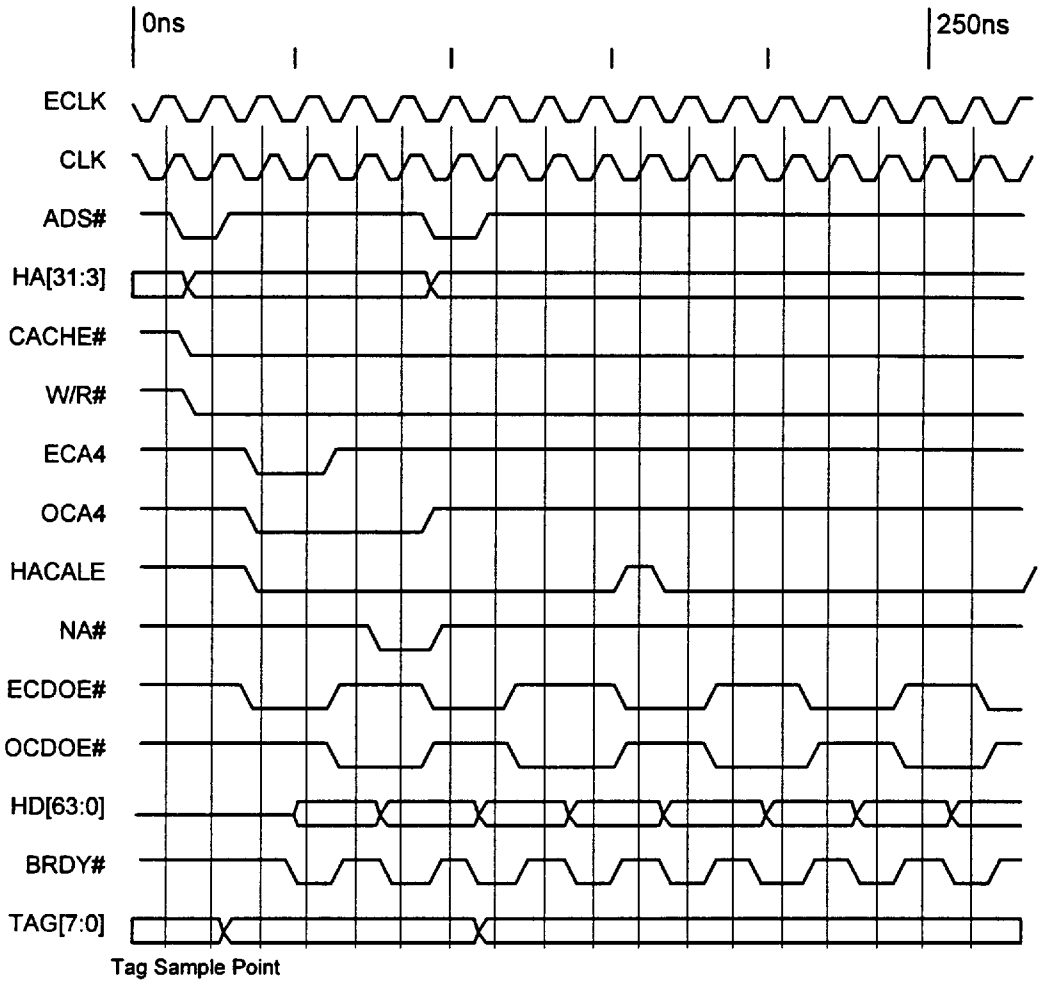
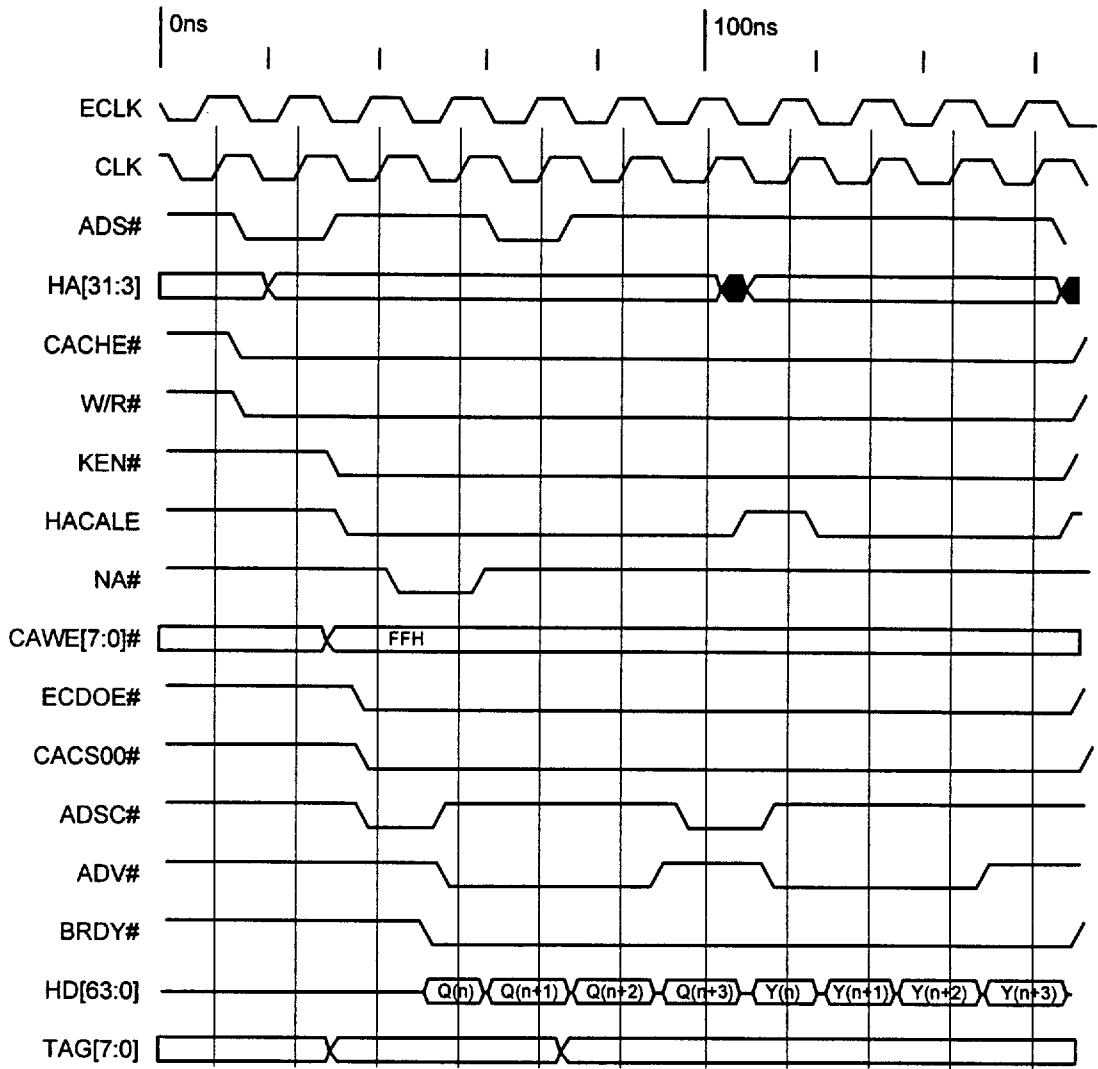
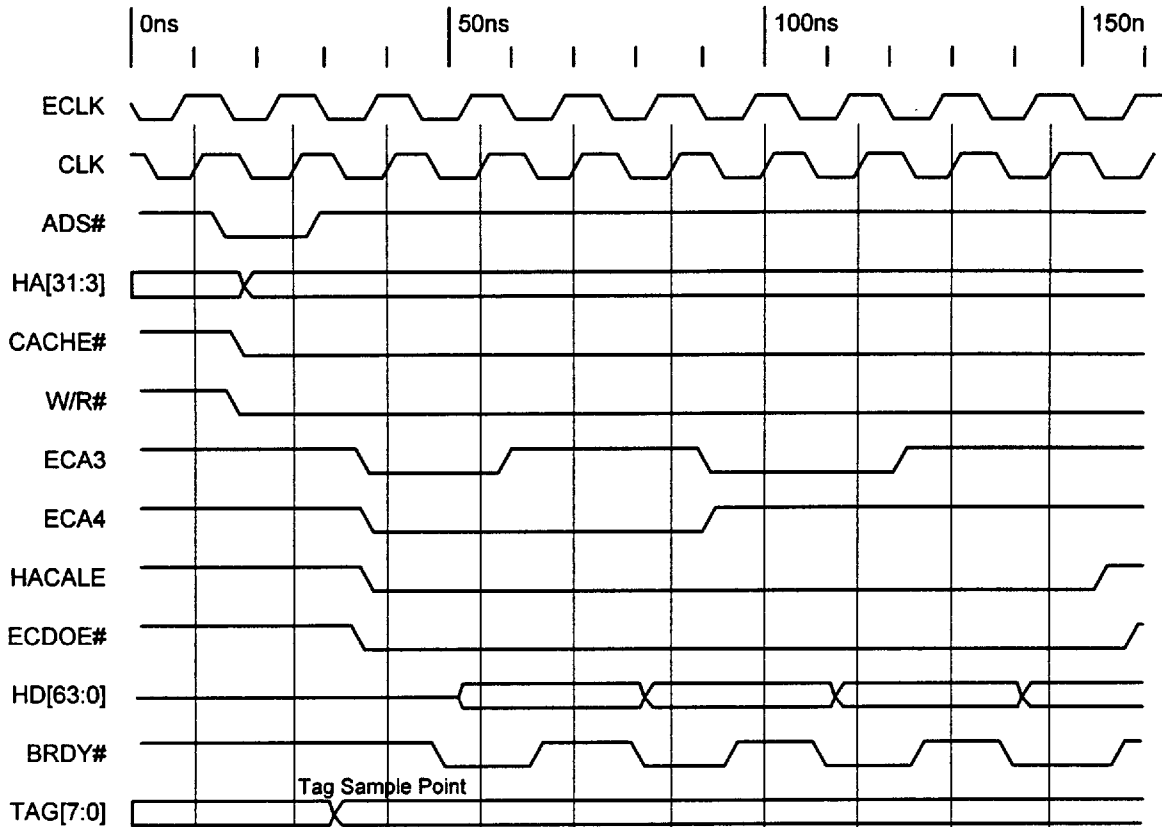


Figure 4-5 L2 Cache Read Hit Cycle - Sync. SRAMs



82C556/82C557/82C558N

Figure 4-6 L2 Cache Read Hit Cycle Async. SRAMs (Single Bank)



4.3.4.2 L2 Cache Write Hit Cycle

Write-through Mode: In this mode, data is always written to the L2 cache and to the system memory. The dirty bit is not used. When the write to the system memory is completed, BRDY# is returned to the CPU.

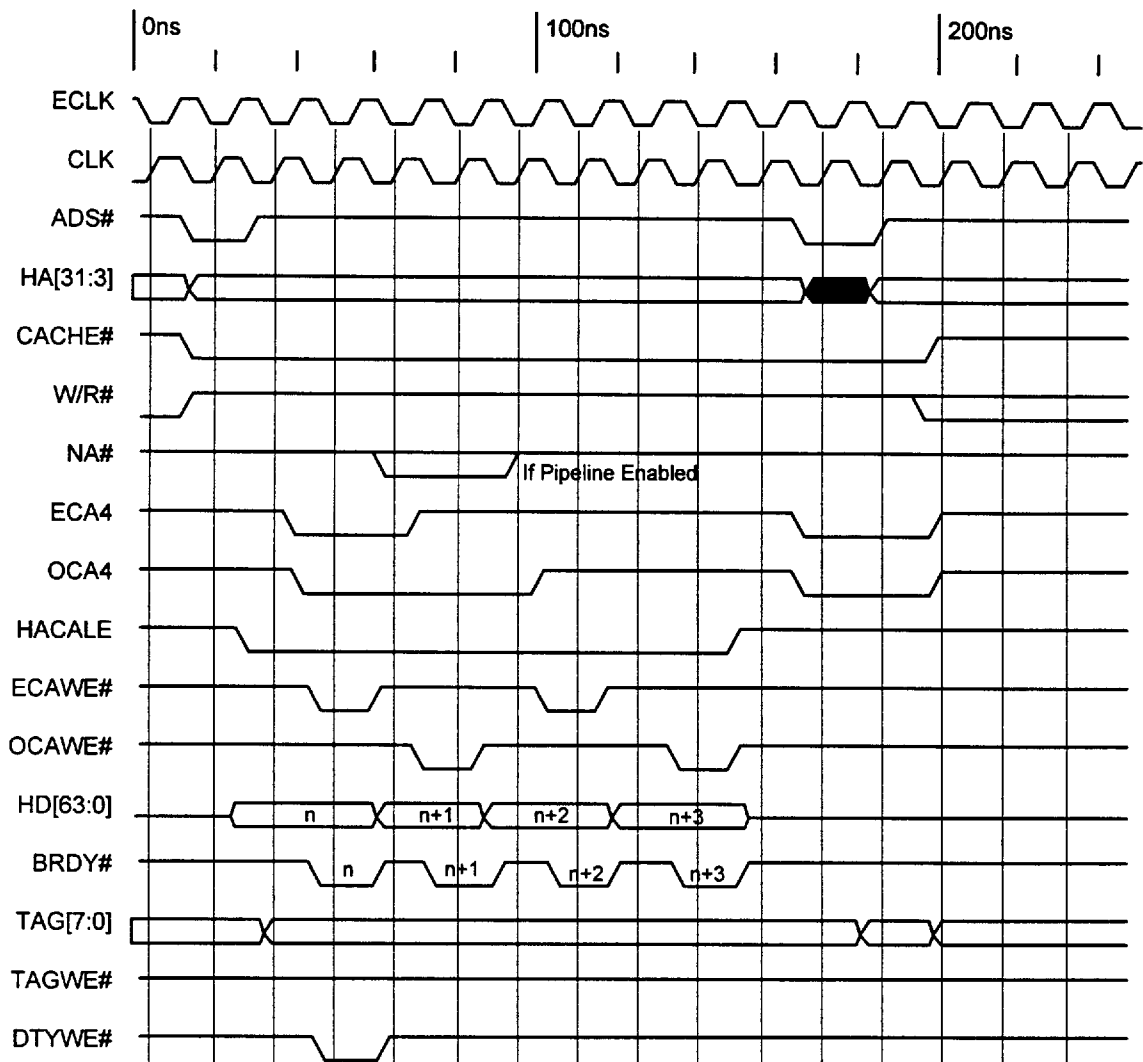
Write-back Mode: For a write hit case, the data is written only to the L2 cache (the system memory is not updated) and the dirty bit is always made dirty. The cache controller will sample CACHE# from the CPU at the end of T1 and execute a burst write if CACHE# is sampled active, otherwise the cycle will end in a single write. In this mode, the write cycle is

completed in a 3-2-2-2 burst. For synchronous SRAMs, the cycle can be completed in a 2-1-1-1 burst if operating at 50MHz. The write enable signals OCAWE# and ECAWE# to the SRAM odd and even banks respectively, are based on address bit A3 from the CPU and will interleave writes to the two banks.

For writes, only the byte requested by the CPU can be written to the cache. This is done by using the BEx# from the CPU to control the SRAM chip selects.

Refer to Figures 4-7 through 4-9 show various write hit burst cycles.

Figure 4-7 Write Hit Burst Cycle for Write-Back Mode - Async. SRAM (Double Bank)



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Figure 4-8 Write Hit Burst Cycle for Write-Back Mode (Single Bank) - Async. SRAM

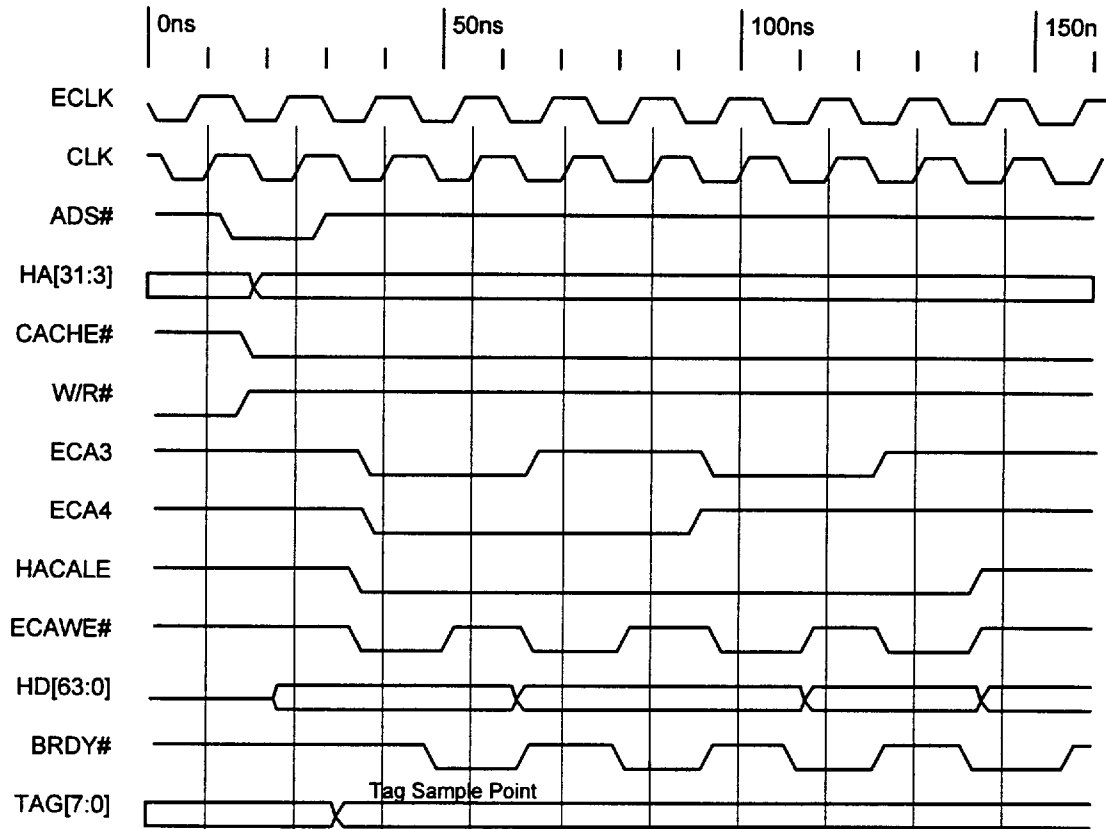
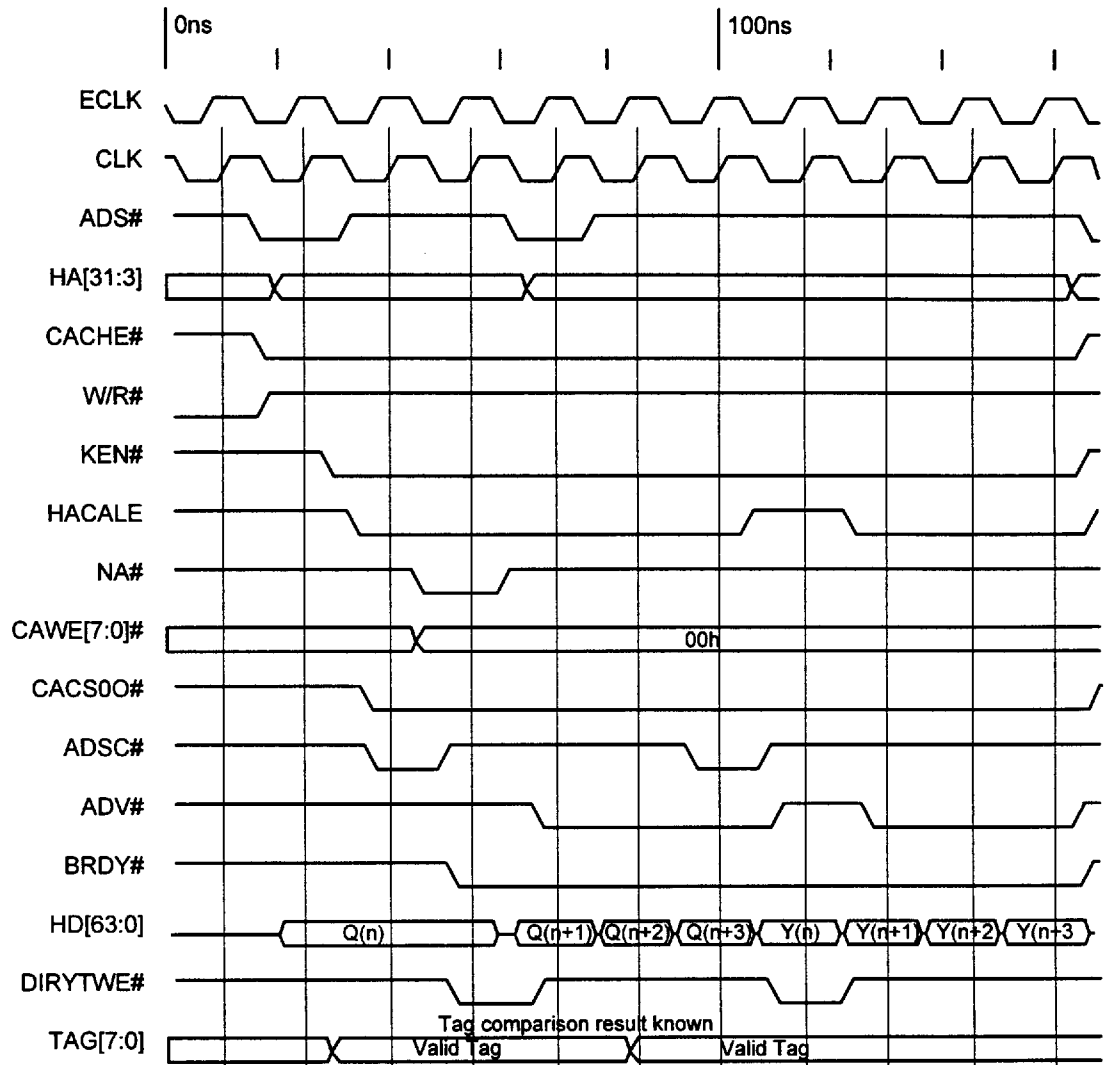


Figure 4-9 Write Hit Burst Cycle for Write-Back Mode - Sync. SRAM



4.3.4.3 L2 Cache Read Miss

Write-back Mode: There are two cache read miss cases depending on the status of the dirty bit.

CASE 1: Read miss of a "clean" cache line.

In this case, only a linefill cycle is executed. The L2 cache line that is to be replaced with a new line from the DRAM will just be overwritten. The linefill cycle is done by reading the new data from the system memory first and then the data is simultaneously written to both the CPU and the secondary cache.

The sequence for CASE 1 linefill is: System memory read ⇒ write to the L2 cache + CPU read.

The cache controller will update the tag data bits and the dirty bit in the background during the linefill cycle. At the end of T1, if the CACHE# signal from the CPU is negated, a linefill cycle will not be executed. Instead, only the eight bytes requested by the CPU will be read from the system memory. The tag and the dirty bit will not be updated.

CASE 2: Read miss with cache line dirty.

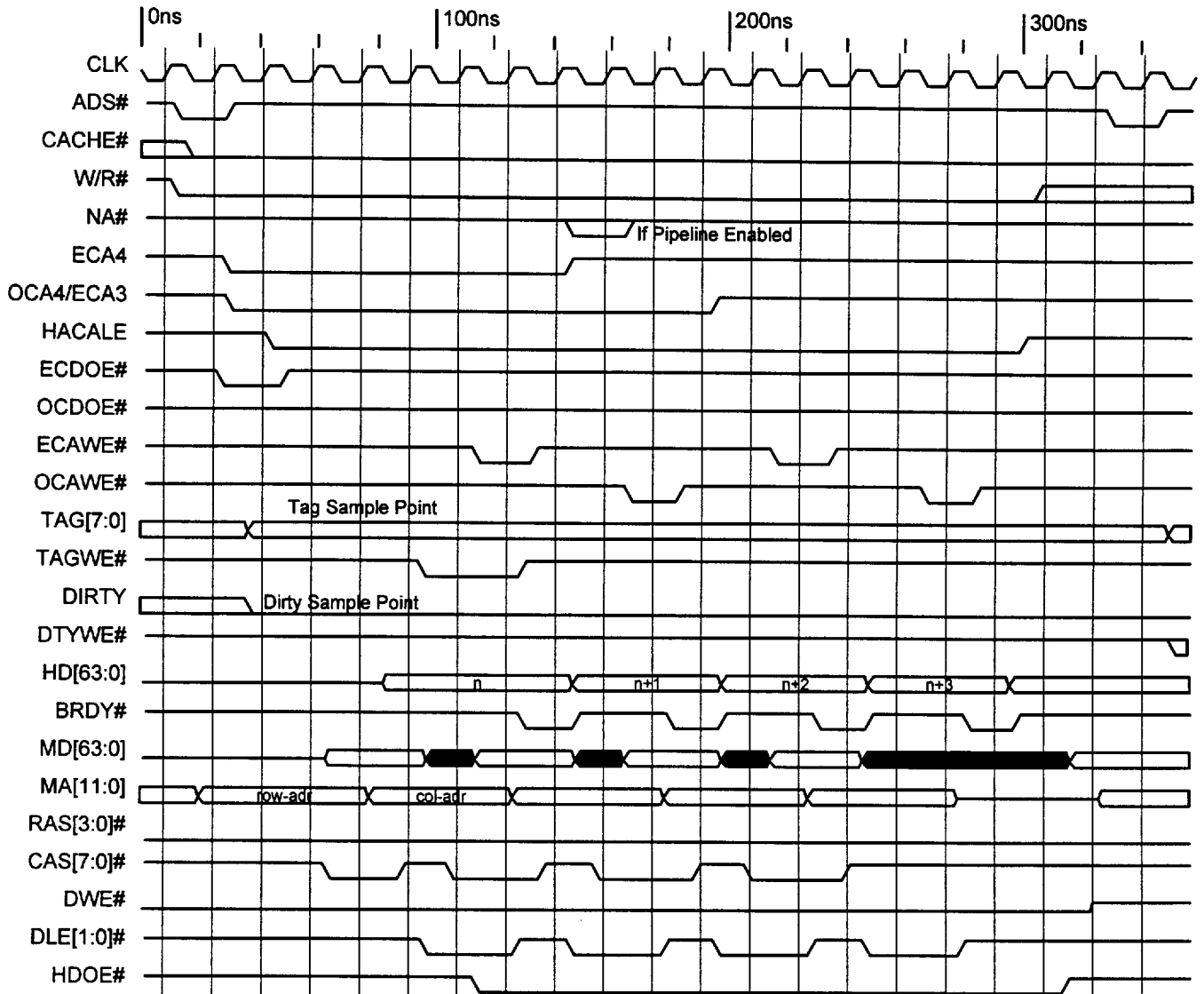
The cache line for this case has been modified and only the L1 and L2 cache have the updated copy of the data. Before this line is overwritten in the cache, the modified line must first be written to the system memory by performing a castout cycle. After the completion of the castout cycle, a linefill cycle is executed. The linefill cycle is performed by reading the new data from the system memory and then simultaneously writing this data to the CPU and the secondary cache.

The sequence for CASE 2 is: Read the dirty line from L2 cache ⇒ write to the system memory ⇒ new line read from system memory ⇒ write to the L2 cache + CPU read.

The cache controller will update the tag data bits and the dirty bit in the background during the castout cycle. If the CACHE# signal from the CPU is inactive, then the eight bytes requested by the CPU will be read from the system memory. The tag and the dirty bit are not updated.

Figures 4-10 through 4-12 show various L2 cache read miss cycles.

Figure 4-10 L2 Cache Read Miss Clean Burst of 8-3-3-3 (Linefill Cycle) - Async. SRAMs



Note: This diagram is also for "DRAM Read Page Hit Cycle".

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Figure 4-11 L2 Cache Read Miss Clean Burst of 8-3-3-3 (Linefill Cycle) - Sync. SRAMs

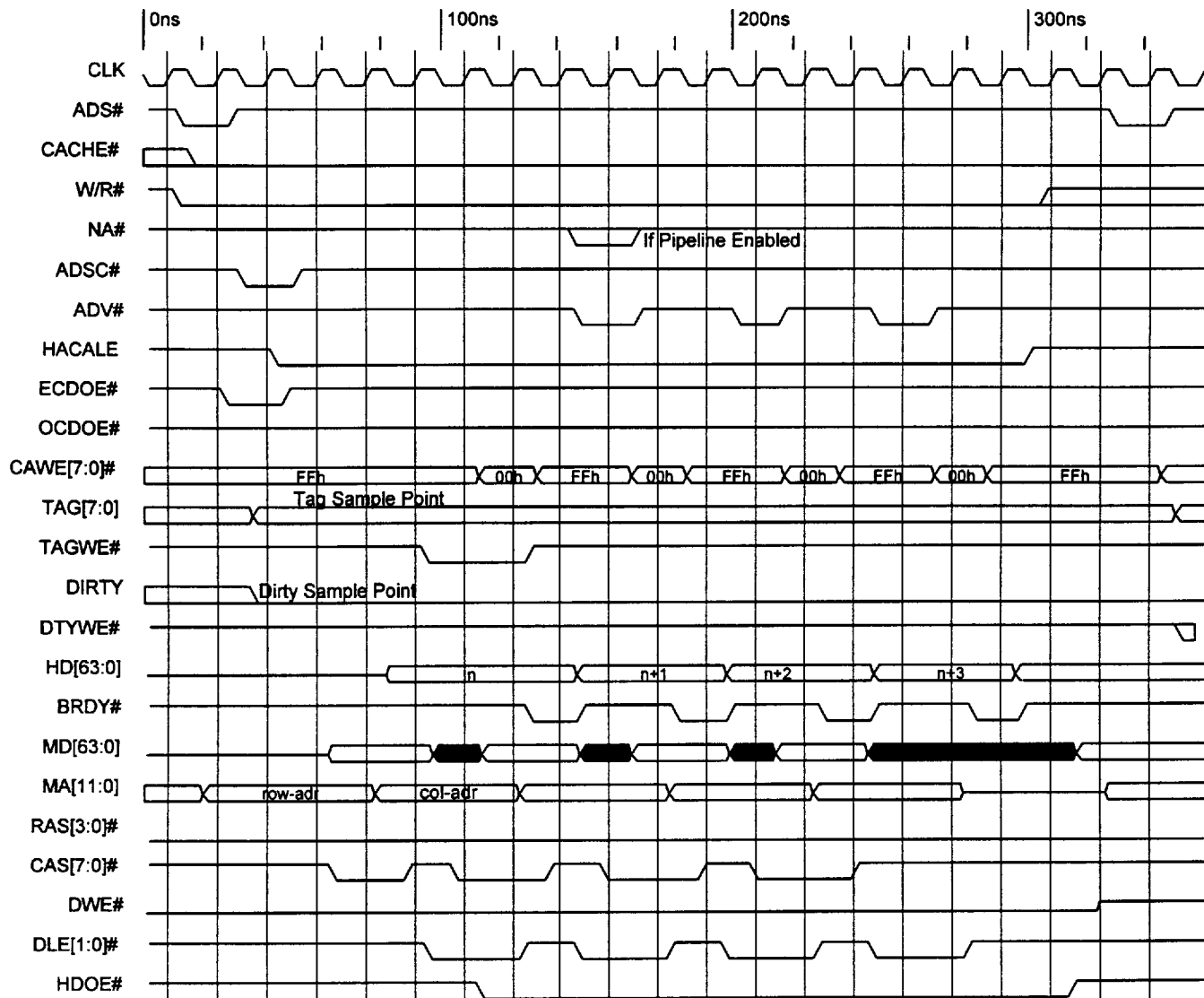


Figure 4-12 L2 Cache Read Miss Dirty Cycle - Async. SRAMs



82C556/82C557/82C558N

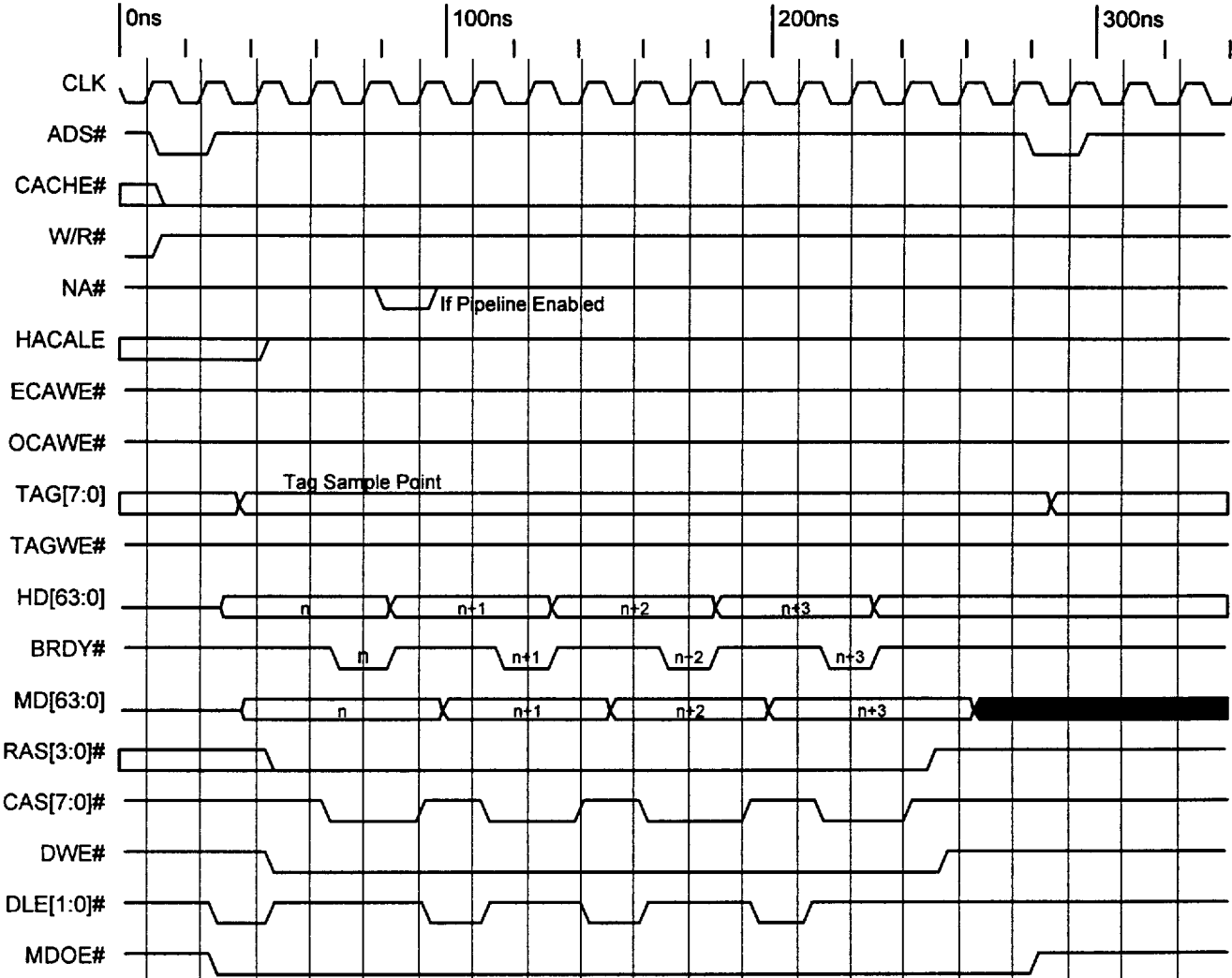
4.3.4.4 L2 Cache Write Miss

Write-back or Write-through Cases: The data is not written to the SRAM and the tag data remains unchanged. The data is written only to the system memory.

If the write buffer and DRAM posted write is enabled then is available, it is stored there and the cycles are posted writes to the DRAM. If the target is on the PCI bus, VL bus, or ISA bus the cache controller will not be active.

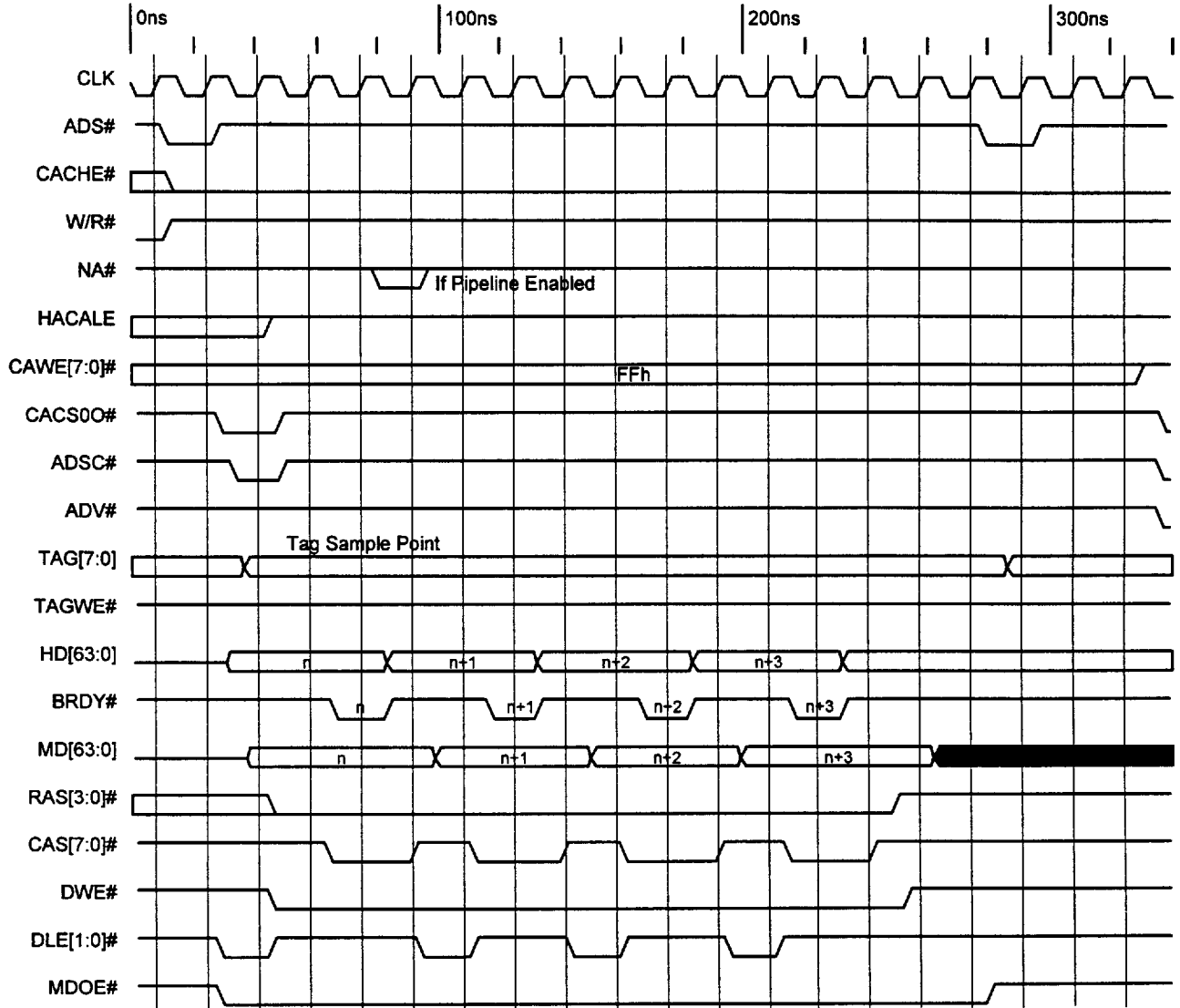
Figures 4-13 and 4-14 show L2 cache write miss cycles.

Figure 4-13 L2 Cache Write Miss Burst Cycle (4-3-3-3) - Async. SRAMs



Note: This diagram is also for "DRAM Write Page Hit Cycle".

Figure 4-14 L2 Cache Write Miss Burst Cycle - Sync. SRAMs



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4.3.4.5 Adaptive Write-Back Policy

Any of the following three write policies supported by the Viper Notebook Chipset can be chosen: write-back, write-through, and adaptive write-back, by programming SYSCFG 02h[5:4] and SYSCFG 08h[1] (as shown in Table 4-4).

Depending on the state of these bits and the type of DRAM cycle that would be required to complete the write hit cycle, the cache controller decides whether to update the DRAM memory, however, the cache is always updated. The adaptive write-back policy tries to reduce the disadvantages of

both the write-through and the write-back schemes to a minimum. The best case cache write burst timing (for an asynchronous cache) is 3-2-2-2, and the best case DRAM page hit write burst timing is 4-3-3-3. The adaptive write-back scheme converts a write hit cycle to a write through cycle only if the address location being written to corresponds to a page hit. In this manner, this scheme incurs a four CLK penalty for a burst write cycle but it saves a 13 CLK penalty (for a castout cycle) that would have occurred later due to a read miss access. There are two adaptive write-back modes.

Table 4-4 Register Bits Associated with Write Policies

7	6	5	4	3	2	1	0
SYSCFG 02h L2 Cache Control Register 1 Default = 00h							
Cache size selection: If SYSCFG 0Fh[0] = 0 00 = 64KB 01 = 128KB 10 = 256KB 11 = 512KB		Cache write policy: 00 = L2 cache write-through 01 = Adaptive Write-back Mode 1 10 = Adaptive Write-back Mode 2 11 = L2 cache write-back		Cache mode select: 00 = Disable L2 cache 01 = Test Mode 1 ⁽¹⁾ 10 = Test Mode 2 ⁽²⁾ 11 = Enable L2 cache		DRAM post write: 0 = Disable 1 = Enable	CAS precharge in CLKs: 0 = 2 CLKs 1 = 1 CLK
(1) Test Mode 1; External tag write (tag data write-through SYSCFG 07h) (2) Test Mode 2; External tag read (tag data read from SYSCFG 07h)							
SYSCFG 08h CPU Cache Control Register 1 Default = 00h							
L2 cache bank select: 0 = Double bank (inter-leaved) ⁽¹⁾ 1 = Single bank (non-inter-leaved)	Line comparator for bus masters: ⁽²⁾ 0 = Disable 1 = Enable	CPU HITM# pin sample timing: 0 = Delay 1 more clock 1 = No delay	DRAM parity check: 0 = Disable 1 = Enable	Combined Tag/Dirty control: 0 = Tag and Dirty on different chips 1 = Tag and Dirty are on the same chip	CPU address pipelining: ⁽³⁾ 0 = Disable 1 = Enable	L1 cache write-back/write-through mode setting: 0 = Write-through only 1 = Write-back enabled	BIOS area cacheability in L1 cache: 0 = Cacheable 1 = Non-cacheable
(1) Interleaved on A3 for async SRAMs, interleaved on A17 for sync SRAMs. Note that for 2-1-1-1 sync SRAM operation, dual non-inter-leaved banks are not supported. Only single bank is supported. (2) For a master request if the subsequent read/write is within the same cache line, CPU 'Inquire' cycles are not done until there is a cache line miss. (3) Turn on for standard sync SRAMs in 3-1-1-1 R/W or for async SRAMs. This bit must be off for standard sync SRAMs in 2-1-1-1 R/W. Also refer to SYSCFG 11h[4]. At any time, either SYSCFG 08h[2] or 11h[4] can be active, but not both at the same time.							

4.3.4.5.1 Write-Through on Page Hit and RAS# Active (AWB Mode 1)

In this mode, the data is written through to the DRAM on a write hit if the address being written to causes a page hit and the corresponding RAS# signal is active. The data will not be written through if, either the RAS# is inactive or if it is a page miss. In this case, the write hit cycle completes in the same manner as in a write-back scheme.

4.3.4.5.2 Write-Through on Page Hit (AWB Mode 2)

In this mode, data is written through to the DRAM on a write hit if the address being written to causes a page hit. RAS#

being active/inactive does not come into consideration when making this decision.

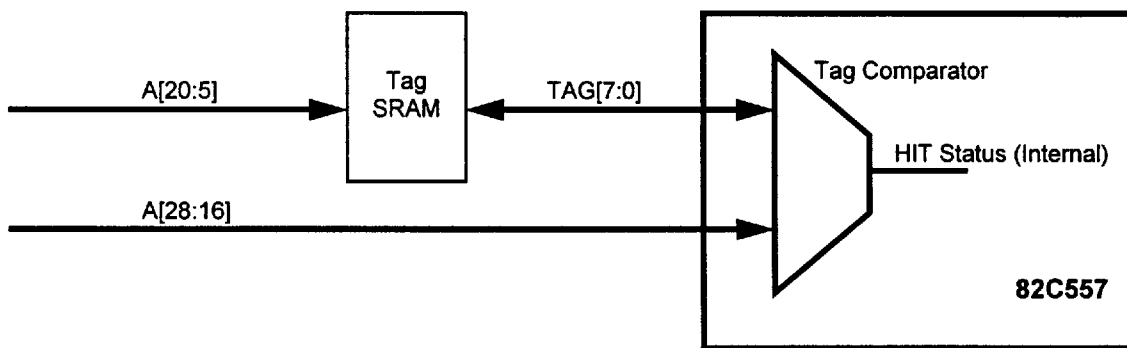
4.3.4.6 Tag Compare Table

The upper address bits used to compare for a L2 cache hit status will depend on the total L2 cache size. Table 4-5 shows the address bits from the CPU bus and the tag data bit used in the tag comparator of the 82C557. Figure 4-15 shows the block diagram of the L2 cache tag structure.

Table 4-5 Tag Compare Table

Tag Data	L2 Cache Size					
	64KB	128KB	256KB	512KB	1MB	2MB
TAG0	A16	A24	A24	A24	A24	A24
TAG1	A17	A17	A25	A25	A25	A25
TAG2	A18	A18	A18	A26	A26	A26
TAG3	A19	A19	A19	A19	A27	A27
TAG4	A20	A20	A20	A20	A20	A28
TAG5	A21	A21	A21	A21	A21	A21
TAG6	A22	A22	A22	A22	A22	A22
TAG7	A23	A23	A23	A23	A23	A23
Dirty Bit	Dirty	Dirty	Dirty	Dirty	Dirty	Dirty

Figure 4-15 82C557 Internal Tag Comparator Block Diagram



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4.3.4.7 Tag and Dirty RAM implementations

There are various tag/dirty RAM implementations supported by the Viper-N Chipset.

4.3.4.7.1 Separate Tag/Dirty RAM Implementation

If a 32Kx1 part is used for the dirty RAM, there has to be a separate dirty input bit and a separate dirty output bit. In this implementation, the TAGWE# signal from the 82C557 is used to update the tag RAM and the DIRYTWE# signal from the 82C557 is used to update the dirty RAM.

4.3.4.7.2 Combined Tag/Dirty RAM Implementation

There are various ways of achieving a combined tag/dirty RAM implementation. In all these implementations, the best write burst performance obtainable is a 4-2-2-2/5-2-2-2 cycle.

A 32Kx9 SRAM can be used to implement eight tag bits and one dirty bit. In this case, the TAGWE# signal from the 82C557 is used to update both the tag and dirty information.

The OE# signal of the 32Kx9 SRAM can be connected to the DIRYTWE# signal from the 82C557 or it can be tied to GND. The DIRYTI signal of the 82C557 becomes a bidirectional signal and it now serves as the dirty I/O bit. This scheme is shown in Figure 4-17 .

A 32Kx8 SRAM can be used, wherein seven bits are used for the tag RAM and one bit is used for the dirty RAM. In this case, the TAGWE# signal from the 82C557 is used to update both the tag and dirty information. The OE# of the 32Kx8 SRAM can be connected to the DIRYTWE# signal from the 82C557 or it can be tied to GND. TAG[7:1] convey the tag information and TAG0 becomes the dirty I/O bit. In this scheme, the amount of main memory that can be cached reduces by half as compared to an 8-bit tag implementation. This scheme is shown in Figure 4-18 .

A 32Kx8 SRAM can be used to implement the eight tag bits and another 32Kx8 SRAM used to implement the single dirty I/O bit. This scheme is identical to the 32Kx9 implementation and is shown in Figure 4-19 .

Table 4-6 Tag/Dirty RAM Control Register Bits

7	6	5	4	3	2	1	0
SYSCFG 16h L2 Cache Control Register 4 Default = 00h							
DIRTY pin control: 0 = Input only 1 = I/O (for a combined Tag/Dirty SRAM)	Reserved	Tag size: 0 = 8-bit tag 1 = 7-bit tag	Single write hit leadoff cycle: ⁽¹⁾ 0 = 5 cycles for combined Tag/Dirty 1 = 4 cycles	Pre-snoop control: 0 = Pre-snoop only for starting address of 0. 1 = Pre-snoop for all addresses except for line boundary.	Reserved	Assert DLE# one-half an LCLK cycle earlier during CPU read access from VL bus: 0 = No 1 = Yes	HDOE# ends one clock before the end of the cycle: 0 = No 1 = Yes

(1) This bit must be set only when the DIRTY bit is on a *1 part which has separate input and output.

SYSCFG 08h CPU Cache Control Register 1 Default = 00h							
L2 cache bank select: 0 = Double bank (interleaved) ⁽¹⁾ 1 = Single bank (non-interleaved)	Line comparator for bus masters: ⁽²⁾ 0 = Disable 1 = Enable	CPU HITM# pin sample timing: 0 = Delay 1 more clock 1 = No delay	DRAM parity check: 0 = Disable 1 = Enable	Combined Tag/Dirty control: 0 = Tag and Dirty on different chips 1 = Tag and Dirty are on the same chip	CPU address pipelining: ⁽³⁾ 0 = Disable 1 = Enable	L1 cache write-back/write-through mode setting: 0 = Write-through only 1 = Write-back enabled	BIOS area cacheability in L1 cache: 0 = Cacheable 1 = Non-cacheable

(1) Interleaved on A3 for async SRAMs, interleaved on A17 for sync SRAMs. Note that for 2-1-1-1 sync SRAM operation, dual non-interleaved banks are not supported. Only single bank is supported.

(2) For a master request if the subsequent read/write is within the same cache line, CPU 'Inquire' cycles are not done until there is a cache line miss.

(3) Turn on for standard sync SRAMs in 3-1-1-1 R/W or for async SRAMs. This bit must be off for standard sync SRAMs in 2-1-1-1 R/W. Also refer to SYSCFG 11h[4]. At any time, either SYSCFG 08h[2] or 11h[4] can be active, but not both at the same time.



Figure 4-16 32Kx8 and 32Kx1 Split Tag/Dirty RAM Implementation

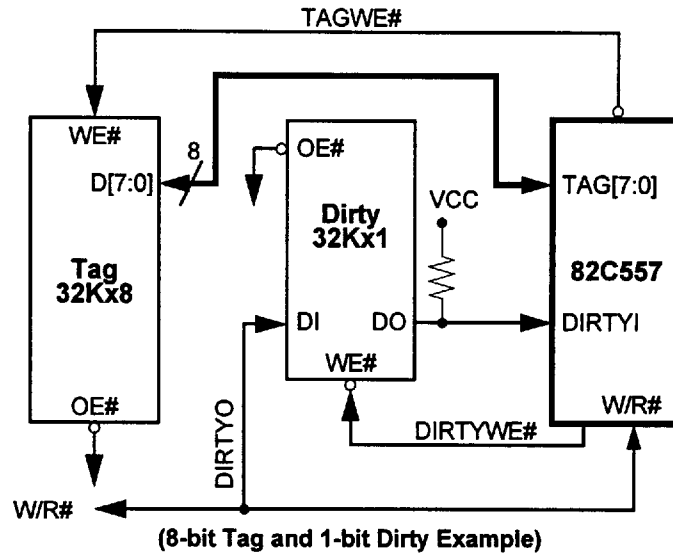


Figure 4-17 32Kx9 Combined Tag/Dirty RAM Implementation

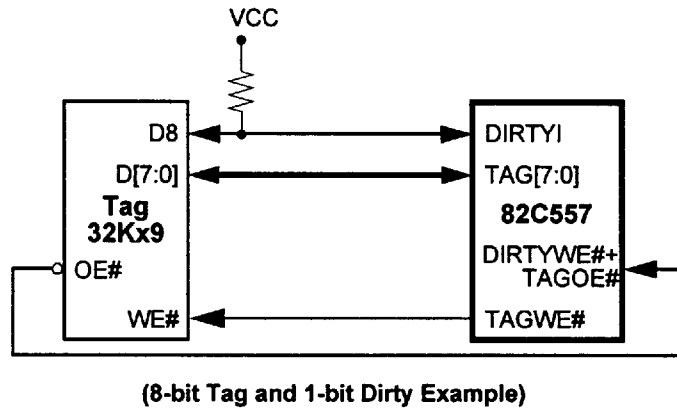
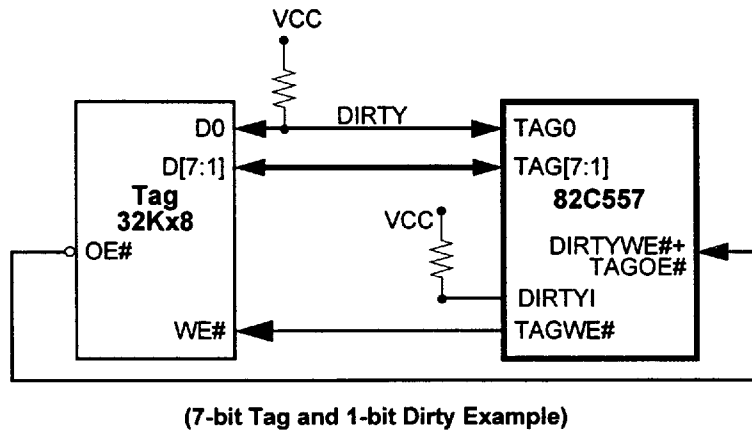
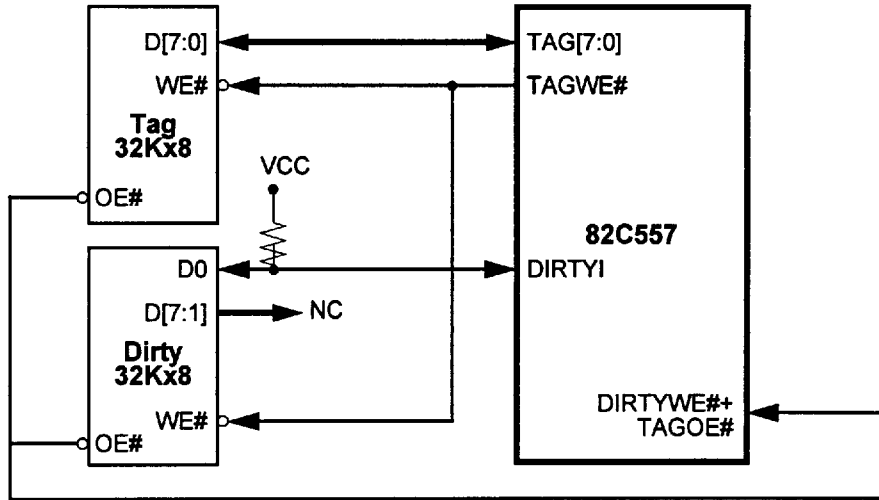


Figure 4-18 32Kx8 Combined Tag/Dirty RAM Implementation



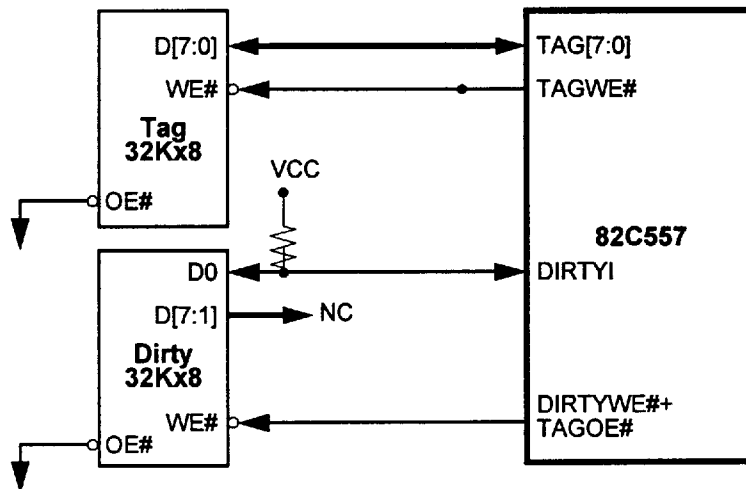
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Figure 4-19 32Kx8 and 32Kx8 Combined Tag/Dirty RAM Implementation



(8-bit Tag and 1-bit Dirty Example)

Figure 4-20 32Kx8 and 32Kx8 Combined Tag/Dirty RAM Implementation (Separate Devices)



(8-bit Tag and 1-bit Dirty Example)

4.3.4.8 Cache Initialization

On power-up, the tag RAM will contain random data and the L2 cache will contain no valid data. Therefore, the cache must be initialized before it is enabled.

Initializing Procedure 1: The cache is initialized by configuring the cache controller to the write-through mode. This will cause all the cache read miss cycles to fill the cache with valid data. This can be done by reading a block of system memory that is greater than or equal to the size of the cache. Once the cache is initialized, it is always valid. After this is done, the L2 cache can be set up for write-back operation by initializing the dirty bits. This is done by first enabling the cache controller to the write-back mode. Then, by reading a block of system memory that is greater than or equal to *twice* the size of the cache, the dirty bits will be cleared and the L2 cache will be valid.

Initializing Procedure 2: This procedure uses the cache controller in Test Mode 1 and Test Mode 2 as defined in SYSCFG 02h[3:2] and 07h[7:0]. (Refer to Table 4-1.)

The upper bits of an address is written to SYSCFG 07h. The cache controller is now set to Test Mode 2. Writing a block equal to the size of the cache to the system memory will write the contents of SYSCFG 07h to the tag. The cache controller is now configured in the write-through mode and reading a block of system memory equal to the size of the cache will make the data in the cache valid. Next, by reading a block of system memory which is greater than or equal to twice the size of the cache, the dirty bits will be cleared and the L2 cache will be valid.

Disabling the Cache: Disabling of a write-back cache cannot be done by just turning off the cache enable register bit in

the 82C557. There may still be valid data in the cache that has not been written to the system memory. Disabling write-back cache without flushing this valid data usually causes a system crash.

This situation can be avoided by first reading a cacheable memory block *twice* the size of the cache. "Twice the size" of the cache is required to make sure every location gets a read miss, which will cause a castout cycle if the cache line is dirty. The cache can then be disabled. **Note: No writes should occur during this process.**

4.3.4.9 Write Back Cache with DMA/ISA Master/PCI Master Operation

The L1 and the L2 cache contain the only valid copy (modified) of the data. The 82C557 will execute an inquire cycle to the L1 cache for all master accesses to the system memory area. This will increase the bus master cycle time for every access to the system memory which will also decrease the bus master performance. The Viper Notebook Chipset provides the option of a snoop-line comparator (snoop filtering) to increase the performance of a bus master with the L1 cache.

L1 Cache Inquire Cycle: This cycle begins with the CPU relinquishing the bus with the assertion of HLDA. On sampling HLDA active, the 82C557 will assert AHOLD. The address will flow from the master to the CPU bus and the 82C557 will assert EADS# for one CPU clock. If the CPU does not respond with the assertion of HITM#, the 82C557 will complete the cycle from the L2 cache or the system memory. If HITM# was asserted, the 82C557 will expect a castout cycle from the L1 cache and in response AHOLD is negated until the end of the castout cycle.

Table 4-7 Test Mode Selection/Control Bits

7	6	5	4	3	2	1	0
SYSCFG 02h L2 Cache Control Register 1 Default = 00h							
Cache size selection: If SYSCFG 0Fh[0] = 0 00 = 64KB 01 = 128KB 10 = 256KB 11 = 512KB		Cache write policy: 00 = L2 cache write-through 01 = Adaptive Write-back Mode 1 10 = Adaptive Write-back Mode 2 11 = L2 cache write-back		Cache mode select: 00 = Disable L2 cache 01 = Test Mode 1 ⁽¹⁾ 10 = Test Mode 2 ⁽²⁾ 11 = Enable L2 cache		DRAM post write: 0 = Disable 1 = Enable	CAS precharge in CLKs: 0 = 2 CLKs 1 = 1 CLK
(1) Test Mode 1; External tag write (tag data write-through SYSCFG 07h) (2) Test Mode 2; External tag read (tag data read from SYSCFG 07h)							
SYSCFG 07h Tag Test Register Default = 00h							
If in Test Mode 1, data from this register is written to the tag. If in Test Mode 2, data from the tag is read into this register. (Refer to SYSCFG 02h.)							



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DMA/Master Read Cycle: Table 4-8 shows the action taken by the 82C557 based on the L1 and L2 cache status for bus master reads from the system memory area. The L1 cache castout cycle will be completed in the burst order provided by the CPU and will be written to the L2 cache or the system memory based on the L2 cache status. The required bytes are then read back for the completion of the master read cycle. A read hit in the L1 cache will always invalidate the L1 cache line. Refer to Figures 4-21 and 4-22.

DMA/Master Write Cycle: Table 4-9 shows the action taken by the 82C557 based on the L1 and L2 cache status for bus master writes to the system memory area. A master write to the L2 cache will always be in the write-through mode. The L1 cache castout cycle will be completed in the CPU burst sequence and the data will be written to the L2 cache or to the system memory based on the L2 cache status. Data from the master is always written to the system DRAM memory and is written to the L2 cache only if it is a L2 cache hit. Refer to Figure 4-23.

Table 4-8 DMA/Master Read Cycle Summary

DMA/Master Read Cycle		Data Source	Type of Cycle for L1 Cache	Type of Cycle for L2 Cache	Type of Cycle for DRAM
L1 Cache	L2 Cache				
Hit	Hit	L2 Cache	Invalidate	Read the Bytes Requested	No Change
hitM	Hit	L1 Cache	Castout, invalidate	Write CPU Data, Read Back the Bytes Requested	No Change
Hit	Miss	DRAM	Invalidate	No Change	Read the Bytes Requested
hitM	Miss	L1 Cache	Castout, invalidate	No Change	Write CPU Data, Read Back the Bytes Requested
Miss	Hit	L2 Cache	No Change	Read the Bytes Requested	No Change
Miss	Miss	DRAM	No Change	No Change	Read

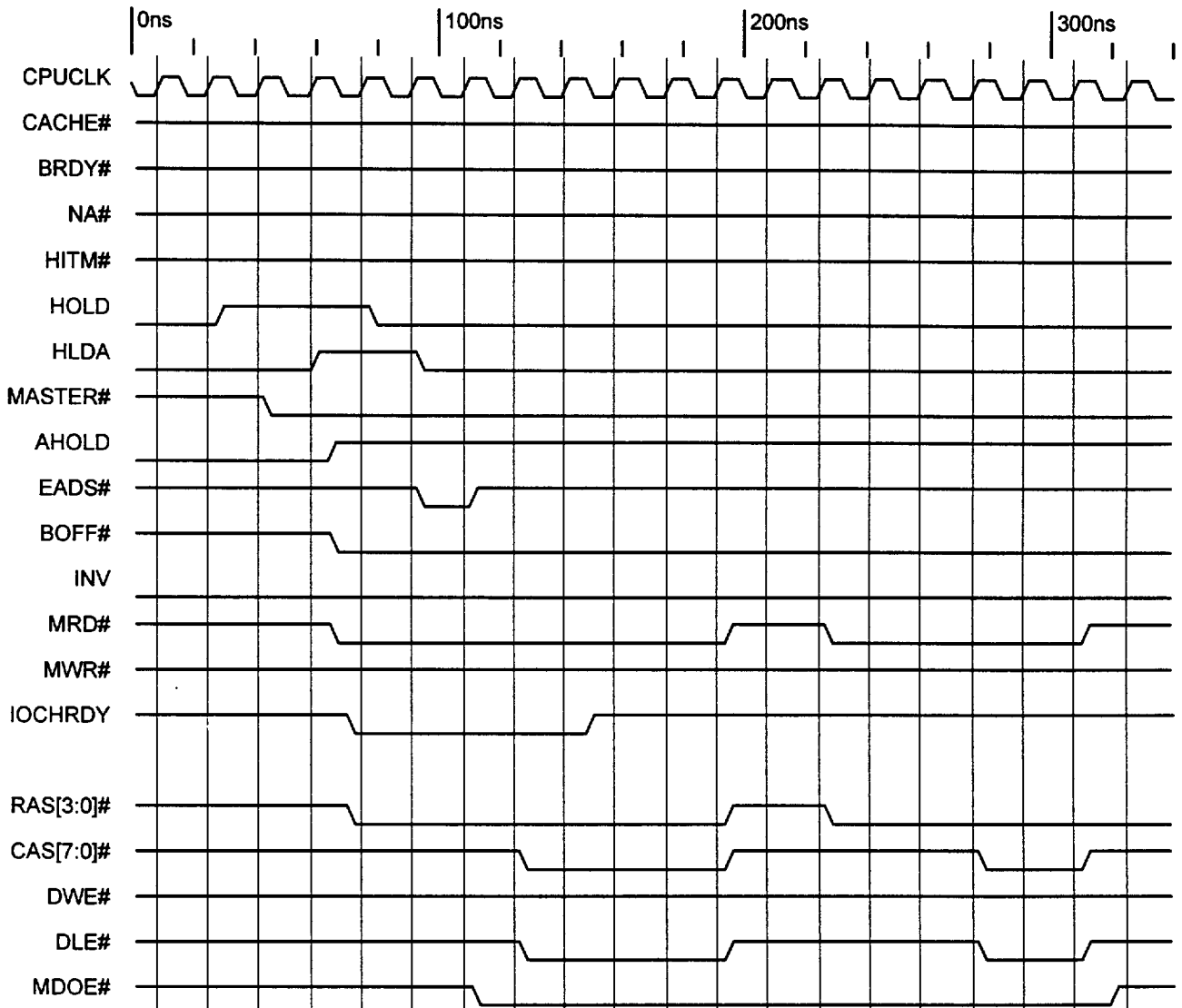
Note: hitM - L1 cache modified

Table 4-9 DMA/Master Write Cycle Summary

DMA/Master Read Cycle		Data Destination	Type of Cycle for L1 Cache	Type of Cycle for L2 Cache	Type of Cycle for DRAM
L1 Cache	L2 Cache				
Hit	Hit	DRAM, sec	Invalidate	Write Master Data	Write Master Data
hitM	Hit	DRAM, sec	Castout, Invalidate	Write CPU Data, Write Master Data	Write Master Data
Hit	Miss	DRAM	Invalidate	No Change	Write Master Data
hitM	Miss	DRAM	Castout, Invalidate	No Change	Write CPU Data, Write Master Data
Miss	Hit	DRAM, sec	No Change	Write Master Data	Write Master Data
Miss	Miss	DRAM	No Change	No Change	Write Master Data



Figure 4-21 ISA DMA/Master Read (L1 cache with non-modified line)



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Figure 4-22 ISA DMA/Master Read (L1 cache with modified line)

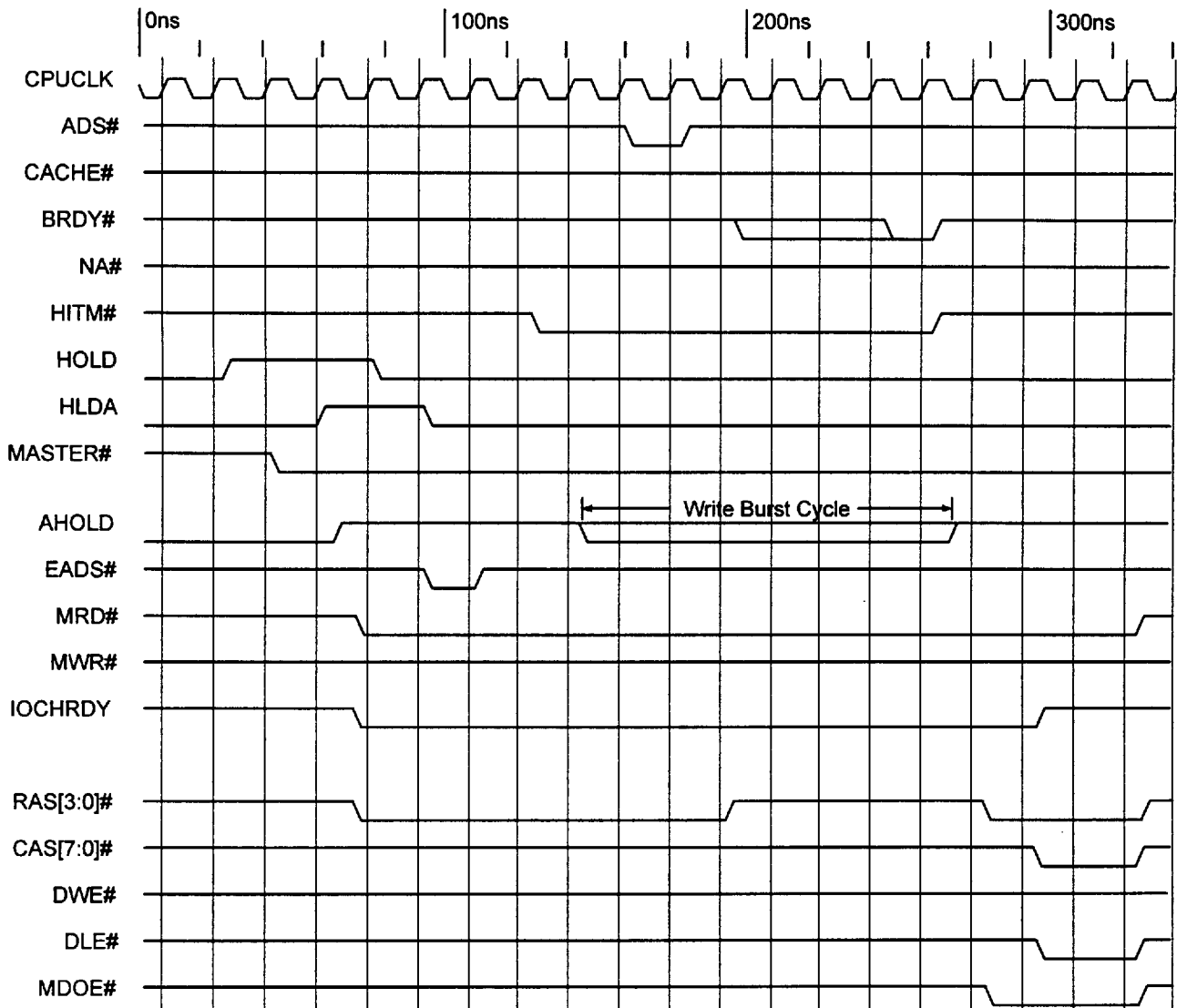
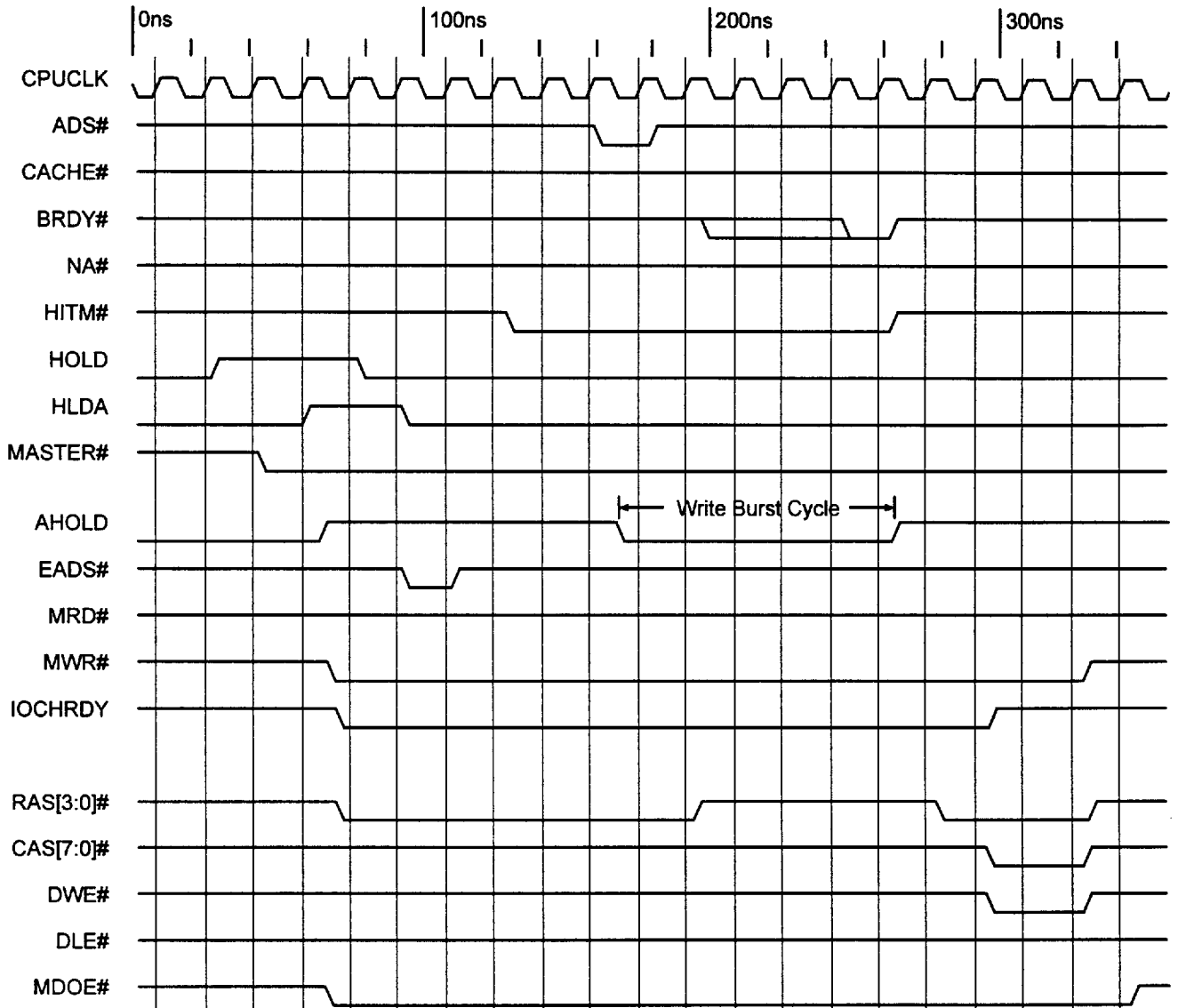


Figure 4-23 ISA DMA/Master Write (L1 cache with modified line)



4.3.5 Shadow ROM and BIOS Cacheability

When using the Viper-N Chipset, the procedures listed below should be followed for proper setup and configuration of shadow RAM utilities.

1. Enable ROMCS# generation for the segment to be shadowed. Although the F0000h-FFFFFh segment defaults to ROMCS# generation, the C, D, and E0000h ROM segments must have ROMCS# generation enabled by setting the appropriate bits in PCIDV1 4Ah and 4Bh.
2. Enable ROM contents to be copied into DRAM. To do this, the appropriate bits in SYSCFG 04h, 05h, and 06h should be set. These bits must be set so that reads from these segments will be executed out of ROM but will be written to DRAM.
3. Enable shadow RAM areas to permit DRAM read/write accesses. At this point, the ROMCS# generation bits that were previously necessary to access the original ROM code, must be disabled.
4. Write protect shadow RAM areas. To do this, the appropriate bits in SYSCFG 04h, 05h, and 06h should be set. These bits must be set so that reads from these segments will be executed out of DRAM, but writes will be directed to the ROM.
5. Cache shadow RAM areas in L2/L1 caches (optional). Caching of the individual code segments can be accomplished by setting the appropriate bits in SYSCFG 06h.

Although write protection control for the L2 cache is provided, the L1 cache does not have a write protection mechanism and the ROM code may be overwritten or modified if stored in the L1 cache.

4.3.5.1 Cacheability and Write Protection

The Viper-N Chipset allows certain ROM areas to be cacheable. C0000h-C7FFFh, E0000h-EFFFFh, and F0000h-FFFFFh have separate cache-related controls. See Table 4-10.

Both system DRAM and shadow RAM are cacheable in both the primary (L1) and/or secondary (L2) cache. Of these two areas, only the shadow RAM areas (system BIOS, video BIOS and DRAM) have the capability of being write-protected (Non-shadowed BIOS ROM areas are implicitly write-protected). Since the possibility exists that write-protected shadow RAM can be cached, there also exists the possibility that this data might be modified inside the cache and subsequently executed. To prevent this from occurring, an explicit control mechanism must be used that prevents the unexpected from happening. There are three methods for controlling write protection in the Viper-N Chipset. (See Table 4-13 for a summary of these methods.)

Table 4-10 Cacheability Area Control Bits

7	6	5	4	3	2	1	0	
PCIDV1 4Ah ROM Chip Select Register								Default = 00h
ROMCS# for segment F8000h-FFFFFh: 0 = Enable 1 = Disable	ROMCS# for segment F0000h-F7FFFh: 0 = Enable 1 = Disable	ROMCS# for segment E8000h-EFFFFh: 0 = Disable 1 = Enable	ROMCS# for segment E0000h-E7FFFh: 0 = Disable 1 = Enable	ROMCS# for segment D8000h-DFFFFh: 0 = Disable 1 = Enable	ROMCS# for segment D0000h-D7FFFh: 0 = Disable 1 = Enable	ROMCS# for segment C8000h-CFFFFh: 0 = Disable 1 = Enable	ROMCS# for segment C0000h-C7FFFh: 0 = Disable 1 = Enable	
PCIDV1 4Bh								Default = 00h
ROMCS# for segment FFFF8000h-FFFFFFFh: 0 = Enable 1 = Disable	ROMCS# for segment FFFF0000h-FFFF7FFFh: 0 = Enable 1 = Disable	ROMCS# for segment FFFE8000h-FFFEFFFFh: 0 = Disable 1 = Enable	ROMCS# for segment FFFE0000h-FFFE7FFFh: 0 = Disable 1 = Enable	ROMCS# for segment FFFD8000h-FFFDFFFFh: 0 = Disable 1 = Enable	ROMCS# for segment FFFD0000h-FFFD7FFFh: 0 = Disable 1 = Enable	ROMCS# for segment FFFC8000h-FFFC7FFFh: 0 = Disable 1 = Enable	ROMCS# for segment FFFC0000h-FFFC7FFFh: 0 = Disable 1 = Enable	
SYSCFG 04h Shadow RAM Control Register 1								Default = 00h
Read/write control for segment CC000h-CFFFFh: 00 = Read/write PCI bus 10 = Read from PCI/ write to DRAM 11 = Read from DRAM/ write to DRAM 01 = Read from DRAM/ write to PCI	Read/write control for segment C8000h-CBFFFh: Refer to SYSCFG 04h[7:6] for decode	Sync SRAM pipe 1-1-1 control: 0 = Pipeline according to SYSCFG 10h[5] 1 = Pipeline subsequent read bursts at 1-1-1-1 ⁽¹⁾	E0000h-EFFFFh cacheability control: 0 = Always non-cacheable 1 = Will be treated like F000 BIOS area ⁽²⁾	Read/write control for segment C0000h-C7FFFh Refer to SYSCFG 04h[7:6] for decode				
<p>(1) If read burst is set to X-1-1-1, setting this bit will enable the following read burst at 1-1-1-1, for X-1-1-1-1-1-1 operation (for standard sync SRAMs only).</p> <p>(2) Note that in this case, SYSCFG 06h[3:2] and 06h[1:0] must be set to the same values.</p>								
SYSCFG 05h Shadow RAM Control Register 2								Default = 00h
Read/write control for segment DC000h-DFFFFh: Refer to SYSCFG 04h[7:6] for decode	Read/write control for segment D8000h-DBFFFh: Refer to SYSCFG 04h[7:6] for decode	Read/write control for segment D4000h-D7FFFh: Refer to SYSCFG 04h[7:6] for decode	Read/write control for segment D0000h-D3FFFh: Refer to SYSCFG 04h[7:6] for decode					
SYSCFG 06h Shadow RAM Control Register 3								Default = 00h
DRAM hole in system memory from 80000h-9FFFFh: 0 = No hole 1 = Enable hole	CPU write-through mode wait for cycle access finish to do snooping ⁽¹⁾ . 0 = Don't wait 1 = Wait	Cacheability for segment C0000h-C7FFFh: 0 = No 1 = Yes in L1 and L2 ⁽²⁾	Cacheability for segment F0000h-FFFFFh: 0 = No 1 = Yes in L1 and L2 ⁽²⁾	Read/write control segment F0000h-FFFFFh: Refer to SYSCFG 04h[7:6] for decode	Read/write control segment E0000h-EFFFFh: Refer to SYSCFG 04h[7:6] for decode			
<p>(1) This is not necessary if CPU is in full speed.</p> <p>(2) L1 cacheability disabled by SYSCFG 08h[0].</p>								



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METHOD 1: In this method, the write protected areas are not cached in the L1 or the L2 cache. This is implemented by driving KEN# high for the first word with BRDY#, which will cause the CPU to not cache the data in its L1 cache and not do burst cycles. Data in the L2 cache is also not updated, so

all reads and writes to this area will go directly to or from the system memory or to/from system BIOS/video BIOS (if they are not shadowed). Table 4-11 shows the associated shadow control register bits.

Table 4-11 Shadow Control Register Bits

7	6	5	4	3	2	1	0
SYSCFG 04h Shadow RAM Control Register 1 Default = 00h							
Read/write control for segment CC000h-CFFFFh: 00 = Read/write PCI bus 10 = Read from PCI/write to DRAM 11 = Read from DRAM/write to DRAM 01 = Read from DRAM/write to PCI	Read/write control for segment C8000h-CBFFFh: Refer to SYSCFG 04h[7:6] for decode		Sync SRAM pipe 1-1-1 control: 0 = Pipeline according to SYSCFG 10h[5] 1 = Pipeline subsequent read bursts at 1-1-1 ⁽¹⁾	E0000h-EFFFFh cacheability control: 0 = Always non-cacheable 1 = Will be treated like F000 BIOS area ⁽²⁾	Read/write control for segment C0000h-C7FFFh Refer to SYSCFG 04h[7:6] for decode		
(1) If read burst is set to X-1-1-1, setting this bit will enable the following read burst at 1-1-1-1, for X-1-1-1-1-1-1-1 operation (for standard sync SRAMs only). (2) Note that in this case, SYSCFG 06h[3:2] and 06h[1:0] must be set to the same values.							
SYSCFG 05h Shadow RAM Control Register 2 Default = 00h							
Read/write control for segment DC000h-DFFFFh: Refer to SYSCFG 04h[7:6] for decode	Read/write control for segment D8000h-DBFFFh: Refer to SYSCFG 04h[7:6] for decode	Read/write control for segment D4000h-D7FFFh: Refer to SYSCFG 04h[7:6] for decode	Read/write control for segment D0000h-D3FFFh: Refer to SYSCFG 04h[7:6] for decode				
SYSCFG 06h Shadow RAM Control Register 3 Default = 00h							
DRAM hole in system memory from 80000h-9FFFFh: 0 = No hole 1 = Enable hole	CPU write-through mode wait for cycle access finish to do snooping⁽¹⁾: 0 = Don't wait 1 = Wait	Cacheability for segment C0000h-C7FFFh: 0 = No 1 = Yes in L1 and L2 ⁽²⁾	Cacheability for segment F0000h-FFFFFh: 0 = No 1 = Yes in L1 and L2 ⁽²⁾	Read/write control segment F0000h-FFFFFh: Refer to SYSCFG 04h[7:6] for decode	Read/write control segment E0000h-EFFFFh: Refer to SYSCFG 04h[7:6] for decode		
(1) This is not necessary if CPU is in full speed. (2) L1 cacheability disabled by SYSCFG 08h[0].							
SYSCFG 0Eh PCI Control Register 1 Default = 00h							
PCI master read wait state control for cache: 00 = X-4-4-4 01 = X-3-3-3 10 = X-2-2-2 11 = Rsvd	PCI master write wait state control for cache: 00 = X-4-4-4 01 = X-3-3-3 10 = X-2-2-2 11 = Rsvd	Parity check during master cycles: 0 = Enable 1 = Disable	HACALE control⁽¹⁾: 0 = HACALE high during HITM# before CPU ADS# 1 = HACALE low and CA4 always enabled during HITM cycle, to save external F126	BIOS write protection for L1: 0 = Disable 1 = Enable	PCI master line comparator: 0 = Use line comparator in PCI master cycle 1 = Generate inquire cycle for every new FRAME#		
(1) Must be set to 1 if an external F126 is not used for A3 and A4 of cache.							



METHOD 2: In this method, the write protected areas can be cached in the L2 cache but not in the L1 cache. This is implemented by driving KEN# high for the first word with BRDY#, which will cause the CPU to not cache the data in the L1 cache or do a burst cycle. This data can then be stored in the L2 cache, but only subsequent read requests by the CPU are serviced (discarding all writes), thus effectively write-protecting the data in the L2 cache. Read miss cycles are serviced by first performing a linefill burst from the DRAM into the L2 cache and then performing a normal non-cacheable (and non-burst) cycle to the CPU. In this method, writes to the system memory and to the L2 cache are write protected.

METHOD 3: This method is implemented by driving EADS#/WT# high during the read cycle. Data read from write protected areas are stored in both the L1 and L2 caches. Accesses from the CPU that are L2 cache read hits are serviced in burst mode and L2 cache read miss cycles are serviced by first performing a linefill burst read to the L2 cache from the write protected area and then performing a normal burst cycle to the CPU. Write cycles from the CPU to these areas are write-through and are discarded by the 82C557's cache controller. *However, L1 cache writes occur internally to the CPU in this mode and are therefore not write protected.* Table 4-12 shows the register bit associated with this function.

Table 4-12 SYSCFG 08h[0]

7	6	5	4	3	2	1	0
CPU Cache Control Register 1							
							Default = 00h
L2 cache bank select: 0 = Double bank (interleaved) ⁽¹⁾ 1 = Single bank (non-interleaved)	Line comparator for bus masters: ⁽²⁾ 0 = Disable 1 = Enable	CPU HITM# pin sample timing: 0 = Delay 1 more clock 1 = No delay	DRAM parity check: 0 = Disable 1 = Enable	Combined Tag/Dirty control: 0 = Tag and Dirty on different chips 1 = Tag and Dirty are on the same chip	CPU address pipelining: ⁽³⁾ 0 = Disable 1 = Enable	L1 cache write-back/write-through mode setting: 0 = Write-through only 1 = Write-back enabled	BIOS area cacheability in L1 cache: 0 = Cacheable 1 = Non-cacheable
(1) Interleaved on A3 for async SRAMs, interleaved on A17 for sync SRAMs. Note that for 2-1-1-1 sync SRAM operation, dual non-interleaved banks are not supported. Only single bank is supported. (2) For a master request if the subsequent read/write is within the same cache line, CPU 'Inquire' cycles are not done until there is a cache line miss. (3) Turn on for standard sync SRAMs in 3-1-1-1 R/W or for async SRAMs. This bit must be off for standard sync SRAMs in 2-1-1-1 R/W. Also refer to SYSCFG 11h[4]. At any time, either SYSCFG 08h[2] or 11h[4] can be active, but not both at the same time.							

Table 4-13 Cacheability Methods

Method	System DRAM		System BIOS		Video BIOS		Write Enabled Shadow RAM		Write Protected Shadow RAM	
	Read	Write	Read	Write	Read	Write	Read	Write	Read	Write
1	L1,L2	L1,L2	Single	None	Single	None	L1,L2	L1,L2	Single	None
2	L1,L2	L1,L2	L2	None	L2	None	L1,L2	L1,L2	L2	None
3	L1,L2	L1,L2	L1,L2	L1	L1,L2	L1	L1,L2	L1,L2	L1,L2	L1

Note: L1 = accessible to primary cache, L2 = accessible to secondary cache, none = no cycle performed (or discard). int = internal cycle to CPU, WT = write-through cycle, single = single word (non-burst) cycle, burst = burst cycle



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4.3.6 Synchronous SRAM Support

The Viper-N Chipset supports almost all the varieties of synchronous SRAMs available. As shown in Table 4-14, 3-1-1-1 read/write cycles are supported at 66MHz. Table 4-15 shows which signals change functionality to support a synchronous SRAM implementation. shows the register bits associated with SRAM support.

In addition to the standard synchronous SRAMs, the Viper Notebook Chipset supports pipelined synchronous SRAMs as well as the Intel standard BSRAM.

Tables 4-18 through 4-22 give additional details regarding SRAM usage in a Viper-N Chipset implementation.

4.3.6.1 Pipelined Synchronous SRAM support

Pipelined synchronous SRAMs are cheaper than their counterpart BiCMOS synchronous SRAMs (standard synchronous SRAMs). The timing requirement of the ADV# pin assertion is different for these SRAMs, and this is enabled by setting SYSCFG 17h[1] = 1 (i.e., enabling pipelined synchronous SRAM).

In a two bank synchronous SRAM implementation, there could be data contention when switching between banks. To avoid this, Intel has proposed a BSRAM standard. This standard requires the insertion of one "idle" cycle when switching between banks. The BSRAMs that support a one clock disable and a two clock enable timing, meet this standard. The Viper Notebook Chipset supports this standard. To enable this feature, SYSCFG 17h[5] should be set to 1.

Table 4-14 SRAM Requirements

Speed	Asynchronous SRAMs		Synchronous SRAMs	
	Cycles	Operation	Cycles	Operation
50MHz	3-2-2-2	Burst Read/Write	2-1-1-1	Burst Read/Write
60MHz	3-2-2-2	Burst Read/Write	3-1-1-1	Burst Read/Write
66.6MHz	3-2-2-2	Burst Read/Write	3-1-1-1	Burst Read/Write

Table 4-15 Signal Functionality for Synchronous SRAM Implementation

Asynchronous SRAM	Synchronous SRAM
CACS[7:0]#	CAWE[7:0]#
ECAWE#	CACS0# (Cache chip select 0)
OCAWE#	CACS10# (Cache chip select 1)
ECA4	ADSC#
OCA4/ECA3	ADV#
ECDOE#	ECDOE#
OCDOE#	OCDOE#

Table 4-16 Register Bits Associated with SRAM Support

7	6	5	4	3	2	1	0
SYSCFG 02h L2 Cache Control Register 1 Default = 00h							
Cache size selection: If SYSCFG 0Fh[0] = 0 00 = 64KB 01 = 128KB 10 = 256KB 11 = 512KB If SYSCFG 0Fh[0] = 1 00 = 1MB 01 = 2MB 10 = Rsvrd 11 = Rsvrd		Cache write policy: 00 = L2 cache write-through 01 = Adaptive Write-back Mode 1 10 = Adaptive Write-back Mode 2 11 = L2 cache write-back		Cache mode select: 00 = Disable L2 cache 01 = Test Mode 1 ⁽¹⁾ 10 = Test Mode 2 ⁽²⁾ 11 = Enable L2 cache		DRAM post write: 0 = Disable 1 = Enable	CAS precharge in CLKs: 0 = 2 CLKs 1 = 1 CLK
(1) Test Mode 1; External tag write (tag data write-through SYSCFG 07h) (2) Test Mode 2; External tag read (tag data read from SYSCFG 07h)							
SYSCFG 03h L2 Cache Control Register 2 Default = 00h							
Cache write burst mode CLKs: 00 = X-4-4-4 01 = X-3-3-3 10 = X-2-2-2 11 = X-1-1-1		Cache write leadoff cycle CLKs:⁽¹⁾ CPU Pipelining Off CPU Pipelining On 00 = 5-X-X-X 01 = 4-X-X-X 10 = 3-X-X-X 11 = 2-X-X-X 00 = 4-X-X-X 01 = 3-X-X-X 10 = 3-X-X-X 11 = 2-X-X-X (or 2-X-X-X if 10h[4] = 1) 11 = 2-X-X-X		Cache read burst mode CLKs: 00 = X-4-4-4 01 = X-3-3-3 10 = X-2-2-2 11 = X-1-1-1		Cache read leadoff cycle CLKs:⁽¹⁾ 00 = 5-X-X-X 01 = 4-X-X-X 10 = 3-X-X-X 11 = 2-X-X-X	
(1) Cache read or write leadoff of two cycles is allowed only for standard sync SRAMs at 50MHz or below.							
SYSCFG 04h Shadow RAM Control Register 1 Default = 00h							
Read/write control for segment CC000h-CFFFh: 00 = Read/write PCI bus 10 = Read from PCI/write to DRAM 11 = Read from DRAM/write to DRAM 01 = Read from DRAM/write to PCI		Read/write control for segment C8000h-CBFFFh: Refer to SYSCFG 04h[7:6] for decode		Sync SRAM pipe 1-1-1-1 control: 0 = Pipeline according to SYSCFG 10h[5] 1 = Pipeline subsequent read bursts at 1-1-1-1 ⁽¹⁾		E0000h-EFFFh cacheability control: 0 = Always non-cacheable 1 = Will be treated like F000 BIOS area ⁽²⁾	Read/write control for segment C0000h-C7FFFh Refer to SYSCFG 04h[7:6] for decode
SYSCFG 0Fh L2 Cache Control Register 3 Default = 00h							
PCI master cycle pre-snooping: 0 = Disabled 1 = Enabled ⁽¹⁾	Insert wait states for ISA master access: 0 = No 1 = Yes	Add 1 more WS for sync SRAM even bank access: 0 = No 1 = Yes	Resynchronize PCI master accesses to system DRAM: 0 = No 1 = Yes ⁽²⁾	Reserved	Generate ADSC# for sync SRAM 1 clock after CPU ADS# in read cycle:⁽³⁾ 0 = Yes 1 = No	Reserved	Cache size selection: 0 = Less than 1MB 1 = 1MB or greater (Refer to SYSCFG 02h[7:6])
(1) The 82C557 generates a pre-snoop cycle to the CPU assuming that the PCI master will do a burst. (2) If set to 1, in sync SRAM mode, PCI master access to system memory will force the master to wait for the current cycle to finish and the CPU-PCI clock to become sync. This is a conservative mode. (3) Must be set for pipeline sync cache or for standard sync cache when running in 2-1-1-1 R/W mode.							



Table 4-16 Register Bits Associated with SRAM Support (cont.)

7	6	5	4	3	2	1	0
SYSCFG 11h							
Miscellaneous Control Register 1				Default = 00h			
Reserved	SRAM activity during Idle state: 0 = Active 1 = Inactive (If inactive, cache CS# is turned off during non-cache cycles).	NA# generation mode: 0 = Generate NA# as soon as possible 1 = New NA# mode for sync SRAM ⁽¹⁾	L2 cache SRAM type: 0 = Async SRAM 1 = Sync SRAM	Page miss posted write: 0 = Enable 1 = Disable	ISA/DMA IOCHRDY control: 0 = No IOCHRDY during line hit 1 = Drive IOCHRDY low until cycle is finished	0 = Delay internal master cycles by one LCLK after inquire cycle: 0 = No 1 = Yes	
<p>*This bit has to be set if ADSP# of sync SRAM is connected to the CPU ADS#. NA# is generated one clock before the last BRDY# to the CPU. Set this bit if CPU pipelining is desired when using either pipelined sync SRAMs or standard sync SRAMs in 2-1-1-1 R/W mode. At any time either 11h[4] or 08h[2] can be set, however they can not be active at the same time.</p>							
SYSCFG 17h							
Miscellaneous Control Register 2				Default = 00h			
Generate NA# for PCI slave access in sync LCLK mode: 0 = No 1 = Yes	NA# generation for PCI slave access: 0 = Do not generate NA# 1 = Generate NA# for async LCLK mode	Sync two bank select: 0 = Rsvrd 1 = Set this bit to 1 when two banks of sync SRAM are installed	BRDY# control for PCI cycles: 0 = Normal BRDY# 1 = Fast BRDY#	Fast FRAME# generation for PCI cycles: 0 = Disable 1 = Enable	Pipelining during byte merge: 0 = Disabled 1 = Enabled	Sync SRAM type: 0 = Standard 1 = Pipelined	Burst type: 0 = Intel burst protocol 1 = Linear burst protocol

4.3.6.2 SONY SONIC-2WP (Cache Module) Support

The Sony SONIC-2WP is a single chip, write-back cache subsystem that integrates 256Kbytes of cache memory, tag RAM and all other associated control logic. The integrated 256Kbyte cache is direct-mapped and it supports 3-1-1-1 burst cycles, and operates at 3.3V. If this chip is used, SYSCFG 00h[5] should be set to 1. This causes a few changes in the signal functions of the 82C557. The TAG1 and the TAG2 signals are connected to the START# signal from the Sony cache module. This signal is asserted by the Sony cache module when a CPU cycle translates to a read

miss, write miss, or a write-through cycle. The assertion of this signal by the cache module causes the 82C557 to take control of the KEN# and BRDY# signals which it shares with the cache module. The TAG3 signal is connected to the BOFF# signal from the Sony cache module. The remainder of the TAG lines should be unconnected. All the other cache control signals of the 82C557 are not required and should be no connects. The ADS# input of the 82C557 should be connected to the SADS# output from the cache module. One note of caution, CPU pipelining must be disabled if using this cache module.

Table 4-17 Cache Module Register Support

7	6	5	4	3	2	1	0
SYSCFG 00h							Default = 00h
DRAM Configuration Register 1							
If 13h[7] = 1: Full Memory Decode							
Single memory write (non-cache) cycle CPU, pipelined enable: 0 = Disable 1 = Enable	Video memory byte/word prefetch control: 0 = Off 1 = On	Sony SONIC-2WP support: 0 = Sony SONIC-2WP module not installed 1 = Sony SONIC-2WP module installed	Byte merge control: 0 = Disable 1 = Enable	NA# generation during byte merge: (Used to kill CPU idle cycles during byte merge only.) 0 = Disable byte merge NA# 1 = Enable byte merge NA#	Byte/word merge time-out counter: (Access passed to PCI bus if this time-out period expires.) 00 = 4 CPU Clocks 01 = 8 CPU Clocks 10 = 12 CPU Clocks 11 = 16 CPU Clocks	Hold request block control during video byte merge: 0 = Let CPU to be put on hold while byte merge in progress if hold request arrives 1 = Block hold request if byte merge in progress	
SYSCFG 00h							Default = 00h
If 13h[7] = 0: 82C546/82C547 Memory Configurations Compatibility - Refer Section 4.4.6 for details							



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4.3.7 SRAM Requirements

The data RAMs are quad-word interleaved for the two bank configuration, which requires 64-bit wide SRAM. This allows

systems based on the Viper-N Chipset to perform a full 3-2-2-2 burst for reads and writes. If a single bank of DRAM is to be used, the cache controller will increase the burst wait state.

Table 4-18 Data SRAM Asynchronous Configurations

Cache Size	Data SRAMs		Tag SRAMs				Cacheable Range
	Qty	Type	Qty	Tag Address Field	Qty	Tag Dirty Bit Field	
64K Bytes	8	8Kx8	1	8Kx8	1	8Kx1	16MB
128K Bytes	16	8Kx8	1	8Kx8	1	8Kx1	32MB
256K Bytes	8	32Kx8	1	8Kx8	1	8Kx1	64MB
512K Bytes	16	32Kx8	1	16Kx8	1	16Kx1	128MB
1M Bytes	8	128Kx8	1	32Kx8	1	32Kx1	128MB
2M Bytes	16	128Kx8	1	64Kx8	1	64Kx1	128MB

Table 4-19 Data SRAM (Asynchronous) and Tag SRAM Speed Requirements

Parameter	Description	33MHz	50MHz	60MHz	66MHz
Data Async. SRAMs					
tAA	Address Access Time	35ns	25ns	15ns	15ns
tOE	OE# Access Time	20ns	12ns	8ns	8ns
tWP	Write Pulse Width	30ns	25ns	14.5ns	14.5ns
Tag RAMs					
tAA	Address Access Time	35ns	20ns	15ns	12ns

Table 4-20 Data SRAM (Synchronous) Configurations

Cache Size	Qty	Size
256K Bytes	4	32Kx18
512K Bytes	4	64Kx18

Table 4-21 Data SRAM (Synchronous) Speed Requirements

Parameter	Description	33MHz	50MHz	60MHz	66MHz
tCD/	Clock Access Time	18ns	12ns (2-1-1-1)/ 12ns (3-1-1-1)	9ns	9ns

Table 4-22 Tag SRAM Speed Requirements for Synchronous SRAMs

Parameter	Description	33MHz	50MHz	60MHz	66MHz
tAA	Address Access Time	25ns	10ns (2-1-1-1)/ 20ns (3-1-1-1)	15ns	12ns



Table 4-23 SRAM Comparisons

Cycles	Async.	Sync.	Pipelined Sync.	Pipelined BSRAM	Sony Cache Module
Read hit	3-2-2-2	3-1-1-1	3-1-1-1	3-1-1-1	3-1-1-1
CPU piped RH	2-2-2-2	1-1-1-1	1-1-1-1	1-1-1-1	3-1-1-1*
2 BKs piped RH	2-2-2-2	1-1-1-1**	2-1-1-1**	2-1-1-1	3-1-1-1*
Write hit	3-2-2-2	3-1-1-1	3-1-1-1	3-1-1-1	3-1-1-1
Write-back	N	N	N+4	N+4	N+BOFF
PCI read	x-2-2-2	x-2-2-2	x-3-3-3	x-3-3-3	x-2-2-2***
PCI write	x-2-2-2	x-2-2-2	x-2-2-2	x-2-2-2	x-2-2-2***
Cost	Lowest	High	Low	Low	High

- * No CPU pipelined for Sony Cache Module.
- ** Data bus conflict for sync. SRAM, minimum data bus conflict for pipelined SRAM with 82C557 OE# control.
- *** L2 needs "castout" dirty line before master access.

4.3.8 Skew Control

Timing requirements are very strict for the best L2 cache performance. The Viper-N Chipset provides clock skew adjustment bits to achieve this performance. By default, synchronous cache interface signals are driven synchronous to the CLK input. If need be, they can be driven synchronous to the ECLK input by setting SYSCFG 0Dh[7] = 1.

Table 4-24 Skew Control Bits

7	6	5	4	3	2	1	0
SYSCFG 0Dh Skew Adjust Register Default = 00h							
Sync SRAM clock source: 0 = CPUCLK 1 = ECLK	ECLK-CLK excessive skew indication (RO): 0 = Skew normal 1 = Skew too large	Automatically set 0Dh[4] = 1 if 0Dh[6] indicates excessive skew: 0 = No 1 = Yes	ADS# sampling clock for sync SRAM control signal generation: 0 = CPUCLK 1 = ECLK ⁽¹⁾	Enable A0000h-BFFFFh as system memory: 0 = No 1 = Yes	Add one more wait state during PCI master cycle with Intel-type address toggling: 0 = No 1 = Yes	Give the 82C557 control of the PCI bus on STOP# generation after HITM# is active: 0 = No 1 = Yes ⁽²⁾	CPU clock is expected to be slowed down to below 33MHz: 0 = No 1 = Yes
<p>(1) ECLK is used for sampling ADS# only if the ECLK-CLK skew is too large. Either set by BIOS after reading 0Dh[6], or automatically set by the 82C557 if 0Dh[5] = 1.</p> <p>(2) The 82C557 has control over the PCI bus until the write-back is completed during PCI snoop cycles.</p>							



4.4 DRAM Controller

The Viper Notebook Chipset DRAM controller uses a 64-bit wide DRAM data bus interface. It also uses the page mode technique for faster data access from the DRAMs.

Page mode is always used in the Viper Notebook Chipset for CPU accesses, both for bursts and between bursts. Page mode is performed by keeping RAS active while reading or writing multiple words within a DRAM page by changing only the column address and toggling CAS with the new column address. The DRAM page size is fixed at 4KB.

Hidden refresh is used to increase the CPU bandwidth by not having to put the CPU on hold every 15µs to refresh the DRAM. The DRAM can be refreshed in the background while the CPU is accessing the internal cache.

Asymmetric as well as **symmetric** DRAM sizes are supported and there are no restriction on which banks need to be populated as long as each logical bank has a 64-bit data path (*Asymmetric support is limited to DRAMs which have their number of row address bits = number of column address bits + 1*).

4.4.1 DRAM Configuration

The Viper N DRAM controller provides two means of configuring the size and arrangement of each DRAM bank:

- Flexible full decode mode, selected when SYSCFG 13h[7] = 1
- Lookup table mode, selected when SYSCFG 13h[7] = 0.

The lookup table mode must **not** be used on new designs. It is present only for compatibility with previous OPTi chipsets, and may not be provided in future chipset revisions.

In the following sections, only the full decode mode is described. Refer to the OPTi 82C546/547 Data Book for additional information on the lookup table mode.

4.4.2 Programming the DRAM Parameters

There are various parameters that can be obtained in the DRAM state machine - number of banks, DRAM configurations, timing parameters and drive strengths.

4.4.2.1 Number of DRAM banks

The Viper Notebook Chipset supports up to six banks of DRAM. The default condition is four banks of DRAM supporting up to 512Mbytes of system memory. MA11 is multiplexed with RAS4# and DIRYTWE# is multiplexed with RAS5#.

If DIRYTWE# is used as RAS5#, the following issues arise.

- If a separate tag/dirty RAM implementation is used, then the L2 cache write-back functionality is lost.
- If a combined tag/dirty RAM implementation is used, then the L2 cache can still be used in the write-back mode.
- If RAS5# is used and MA11 is not used as RAS4#, then the maximum amount of memory supported is 512Mbytes, with not more than 3 banks populated with 128Mbytes.

If both RAS4# and RAS5# are being used (i.e six banks of DRAM), then the maximum amount of memory supported is 192Mbytes.

If MA11 is used as RAS4#, then the maximum memory size supported decreases to 192Mbytes.

RAS4# and RAS5# are selected through SYSCFG 19h[7] (RAS5#), and 19h[3] (RAS4#).

Table 4-25 Full Memory Decode Mode and RAS Selection Bits

7	6	5	4	3	2	1	0
SYSCFG 13h Memory Sizing Register 1 Default = 00h							
Memory decode select: 0 = Table lookup (compatible to 82C547) 1 = Full decode	Full decode for logical Bank 1 (RAS1#) if SYSCFG 13h[7] set:			SMRAM: 0 = Disable 1 = Enable (depending on SYSCFG 14h[3])	Full decode for logical Bank 0 (RAS0#) if SYSCFG 13h[7] set:		
	000 = Disabled	100 = 2Mx36	000 = Disabled		100 = 2Mx36x2		
	001 = 256Kx36x2	101 = 4Mx36x2	001 = 256Kx36x2		101 = 4Mx36x2		
	010 = 512Kx36x2	110 = 8Mx36x2	010 = 512Kx36x2		110 = 8Mx36		
	011 = 1Mx36x2	111 = 16Mx36x2	011 = 1Mx36x2		111 = 16Mx36x2		
SYSCFG 19h Memory Sizing Register 3 Default = 00h							
RAS5# selection (on pin 196): 0 = Generate DIRTYWE# on pin 196 1 = Generate RAS5# on pin 196	Full decode for logical Bank 5 (RAS5#) if SYSCFG 13h[7] = 1 and 19h[7] = 1:			RAS4# selection (on pin 76): 0 = Generate MA11 on pin 76 1 = Generate RAS4# on pin 7	Full decode for logical Bank 4 (RAS4#) if SYSCFG 13h[7] = 1 and 19h[3] = 1:		
	000 = Disable	100 = 2Mx36x2	000 = Disable		100 = 2Mx36x2		
	001 = 256Kx36x2	101 = 4Mx36x2	001 = 256Kx36x2		101 = 4Mx36x2		
	010 = 512Kx36x2	110 = 8Mx36x2	010 = 512Kx36x2		110 = 8Mx36x2		
	011 = 1Mx36x2	111 = 16Mx36x2	011 = 1Mx36x2		111 = 16Mx36x2		

4.4.2.2 DRAM Size and Type

The DRAM configuration is selected through groups of three bits in SYSCFG 13h, 14h, and 19h. There is no required ordering for these selections: Any desired bank can be occupied or not. For example, if in the course of testing system

DRAM the BIOS POST code should find bank 3 (RAS3#) defective, it should simply set that bank to "disabled." The DRAM controller will automatically map around it and provide a contiguous memory map to the system.

Table 4-26 DRAM Configuration Related Register Bits

7	6	5	4	3	2	1	0	
SYSCFG 13h Memory Sizing Register 1 Default = 00h								
Memory decode select: 0 = Table lookup (compatible to 82C547) 1 = Full decode	Full decode for logical Bank 1 (RAS1#) if SYSCFG 13h[7] set: 000 = Disabled 100 = 2Mx36 001 = 256Kx36x2 101 = 4Mx36x2 010 = 512Kx36x2 110 = 8Mx36x2 011 = 1Mx36x2 111 = 16Mx36x2			SMRAM: 0 = Disable 1 = Enable (depending on SYSCFG 14h[3])	Full decode for logical Bank 0 (RAS0#) if SYSCFG 13h[7] set: 000 = Disabled 100 = 2Mx36x2 001 = 256Kx36x2 101 = 4Mx36x2 010 = 512Kx36x2 110 = 8Mx36 011 = 1Mx36x2 111 = 16Mx36x2			
SYSCFG 14h Memory Sizing Register 2 Default = 00h								
Reserved: Write 0.	Full decode for logical Bank 3 (RAS3#) if SYSCFG 13h[7] set: 000 = Disabled 100 = 2Mx36x2 001 = 256Kx36x2 101 = 4Mx36x2 010 = 512Kx36x2 110 = 8Mx36x2 011 = 1Mx36x2 111 = 16Mx36x2			If SMIACK# is inactive: 0 = Disable SMRAM 1 = Enable SMRAM If SMIACK# is active and SYSCFG 13h[3] = 1: 0 = Enable SMRAM for Code and Data 1 = Enable SMRAM for Code only	Full decode for logical Bank 2 (RAS2#) if SYSCFG 13h[7] set: 000 = Disabled 100 = 2Mx36x2 001 = 256Kx36x2 101 = 4Mx36x2 010 = 512Kx36x2 110 = 8Mx36x2 011 = 1Mx36x2 111 = 16Mx36x2			
SYSCFG 19h Memory Sizing Register 3 Default = 00h								
RAS5# selection (on pin 196): 0 = Generate DIRTYWE# on pin 196 1 = Generate RAS5# on pin 196	Full decode for logical Bank 5 (RAS5#) if SYSCFG 13h[7] = 1 and 19h[7] = 1: 000 = Disable 100 = 2Mx36x2 001 = 256Kx36x2 101 = 4Mx36x2 010 = 512Kx36x2 110 = 8Mx36x2 011 = 1Mx36x2 111 = 16Mx36x2			RAS4# selection (on pin 76): 0 = Generate MA11 on pin 76 1 = Generate RAS4# on pin 7	Full decode for logical Bank 4 (RAS4#) if SYSCFG 13h[7] = 1 and 19h[3] = 1: 000 = Disable 100 = 2Mx36x2 001 = 256Kx36x2 101 = 4Mx36x2 010 = 512Kx36x2 110 = 8Mx36x2 011 = 1Mx36x2 111 = 16Mx36x2			



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4.4.2.3 DRAM Address Muxing

Table 4-27 shows the DRAM address (MA) muxing. Note that the column address is the same for all configurations since this is the speed path. A3 and A4 must go through an internal burst counter, for the generation of the MA address to the DRAMs. The table shows MA line to address bit mapping for each DRAM size configuration.

4.4.2.4 Timing Parameters

The timing constraints to achieve optimum performance at 66MHz are met without making the system design overly critical. Timing variations that are required for different system speeds are handled by a selection of timing modes that vary the wait states used. Table 4-28 summarizes these timing modes.

Table 4-27 DRAM Row/Column MA to Address Bit Map

Addr.	256KB		512KB		1MB		2MB		4MB		8MB		16MB	
	Col	Row	Col	Row	Col	Row	Col	Row	Col	Row	Col	Row	Col	Row
MA0	A3	A12	A3	A12	A3	A12	A3	A12	A3	A12	A3	A12	A3	A12
MA1	A4	A13	A4	A13	A4	A13	A4	A13	A4	A13	A4	A13	A4	A13
MA2	A5	A14	A5	A14	A5	A14	A5	A14	A5	A14	A5	A14	A5	A14
MA3	A6	A15	A6	A15	A6	A15	A6	A15	A6	A15	A6	A15	A6	A15
MA4	A7	A16	A7	A16	A7	A16	A7	A16	A7	A16	A7	A16	A7	A16
MA5	A8	A17	A8	A17	A8	A17	A8	A17	A8	A17	A8	A17	A8	A17
MA6	A9	A18	A9	A18	A9	A18	A9	A18	A9	A18	A9	A18	A9	A18
MA7	A10	A19	A10	A19	A10	A19	A10	A19	A10	A19	A10	A19	A10	A19
MA8	A11	A20	A11	A20	A11	A20	A11	A20	A11	A20	A11	A20	A11	A20
MA9	-	-	-	A21	A22	A21	A22	A21	A22	A21	A22	A21	A22	A21
MA10	-	-	-	-	-	-	-	A23	A24	A23	A24	A23	A24	A23
MA11	-	-	-	-	-	-	-	-	-	-	-	A25	A26	A25

Table 4-28 DRAM Programmable Control

DRAM Timing Being Controlled	Variation in CLK
RAS address hold time	1 to 2
CAS pulse width for reads	2 to 3
CAS pulse width for writes	2 to 3
Address setup time to CAS for write page hit	1 to 2
CAS precharge time	1 to 2
RAS precharge time	3 to 6
RAS pulse width for refresh	4 to 7

4.4.2.5 Drive Strengths

Programmable current drive for the MA[11:0], RAS[5:0]# and the DWE# lines is provided. If SYSCFG 18h[4] = 0, then the current drive on these lines is 4mA. In this case, two F244 buffers will be required to drive each pair of DRAM banks. If SYSCFG 18h[4] = 1, then the current drive on these lines is increased to 16mA and it should be possible to drive the first pair of DRAM banks without any buffers.

4.4.3 DRAM Cycles

The fastest possible burst read is 8-3-3-3 which means the first quad-word is received in eight clocks and the next three quad-words are received after three clocks each. For a cache based system, it would mean the bursting to the cache and CPU for read miss cycles or write miss cycles. Table 4-31 summarizes the DRAM timing modes for read and write cycles respectively.

4.4.3.1 DRAM Read Cycle

The DRAM read cycle begins with the DRAM controller detecting a page hit or a page miss cycle at the end of the first T2. Based on the status of the current open page and the active RASx#, a page hit, a page miss with RAS inactive, or a page miss with RAS active cycle is executed.

Page Miss with RAS High Cycle: The row address is generated from the CPU address bus. Table 4-27 gives the row/column address mux map. After RASx# goes active, the row address is changed on the next clock edge (programmable to be two CLKs) to the column address. The CASx# will be active two CLKs after the column address is generated. (Refer to Figure 4-24 .)

Page Miss with RASx# Low Cycle: RAS is first precharged for the programmed number of CLKs and then driven active, after which it will be the same as a page miss with RAS high cycle.

Page Hit Cycle: The 82C557 generates the column address from the CPU address bus and CASx# is driven active for two clocks. Data flow from the CPU data bus to the memory data bus and vice versa is controlled by the DBCOE#[1:0], MDOE#, and HDOE# signals from the 82C557 to the 82C556. Data from the DRAM is latched by the 82C556 on the rising edge of each DLE (for CPU reads from DRAM, the DLE signals are identical to the CAS signal). The latched data is valid on the CPU data bus until the next rising edge of CASx#. During this time, the next read is started, CASx# signals are precharged for one or two clocks (programmable), and the next data from the DRAM is accessed and latched. The 82C556 latches the data from the DRAM and holds the data for the CPU while the DRAM controller begins the read for the next word in the burst cycle. The burst read from the DRAM is in effect pipelined into the CPU data bus by the Viper Notebook Chipset. This scheme reduces the constraints on the board layout so that routing for the CPU data bus, MD data bus, and CASx# signal lines are less critical and performance can be maintained.

Page Hit Cycle (Extended): Wait states can be added if slower DRAMs are used. In this mode, data from the DRAM is latched by the 82C556 at the end of each CAS cycle similar to the default mode. The only difference between the two modes is that the CAS low time on reads is increased by one T-state. This eases up on the page mode cycle time and CAS access time parameters.

The DRAM read cycle uses a CAS signal that is active for multiples of T-state boundaries rather than half T-state boundaries. This allows additional address decode setup time and MA bus setup time at the start of the cycle, making the fastest burst cycle 8-3-3-3.

Table 4-29 Drive Strength Control Bit

7	6	5	4	3	2	1	0
SYSCFG 18h							
Signal State Control Register							
Reserved						Default = 00h	
	CAS[X]# 3.3V/5.0V selection: 0 = 5.0V drive on CAS[X]# lines 1 = 3.3V drive on CAS[X]# lines	Drive strength on memory address lines, RAS lines, and write enable line: 0 = 4mA 1 = 16mA	CPU status during Suspend: 0 = Powered on 1 = Powered off	PCI bus tristate control during Suspend: 0 = PCI bus parked by 82C557 1 = Tristate ⁽¹⁾	Cache status during Suspend: 0 = Powered on 1 = Powered off	Global 82C557 leakage control: 0 = Disable 1 = Enable	
(1) Tristate AD[31:0], FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, C/BE#[3:0].							



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4.4.3.2 DRAM Write Cycle

Posted write to the DRAM improves the write cycle timing relative to the CPU and allows the Viper Notebook Chipset to perform an independent write burst cycle to DRAM without holding the CPU. The Viper Notebook Chipset maintains a one quad-word deep data buffer for DRAM writes so that the CPU write cycle is completed without waiting for the external DRAM cycle. For a burst write cycle, the leadoff cycle time is reduced to four clocks even if the cycle is a non-page hit cycle. For a page hit cycle, the burst write can be completed in 4-3-3-3 with posted write enabled. The posted write buffer in the 82C556 is controlled by the DLE[1:0]# signals from the 82C557. Effectively, the rising edge of these signals will latch

the high 32-bit and the low 32-bit new data respectively, from the CPU bus to the posted write buffer.

Single level posted write cycles are employed to achieve a 4-3-3-3 burst at 66MHz. The data from the CPU is latched in the 82C556's write buffer until CAS goes active one T-state after the first T2 (on a page hit). This provides a fast write mechanism and two wait state writes are maintained for the leadoff cycle within a page (even at 66MHz). The CAS pulse width can be extended by one more T-state to ease the timing constraints on the CAS pulse width requirement for speeds above 66MHz.

Table 4-30 DRAM Operation Programming Bits

7	6	5	4	3	2	1	0
SYSCFG 01h DRAM Control Register 1 Default = 00h							
Row address hold after RAS in CLKs: 0 = 2 CLKs 1 = 1 CLK	0 = Normal page mode for master cycle 1 = RAS inactive while entering master mode	RAS pulse width used for refresh in CLKs: 00 = 7 CLKs 01 = 6 CLKs 10 = 5 CLKs 11 = 4 CLKs	Read CAS pulse width in CLKs: 0 = 3 CLKs 1 = 2 CLKs	Write CAS pulse width in CLKs: 0 = 3 CLKs 1 = 2 CLKs	RAS precharge in CLKs: 00 = 6 CLKs 01 = 5 CLKs 10 = 4 CLKs 11 = 3 CLKs		
SYSCFG 02h L2 Cache Control Register 1 Default = 00h							
Cache size selection: If SYSCFG 0Fh[0] = 0 00 = 64KB 01 = 128KB 10 = 256KB 11 = 512KB		Cache write policy: 00 = L2 cache write-through 01 = Adaptive Write-back Mode 1 10 = Adaptive Write-back Mode 2 11 = L2 cache write-back		Cache mode select: 00 = Disable L2 cache 01 = Test Mode 1 ⁽¹⁾ 10 = Test Mode 2 ⁽²⁾ 11 = Enable L2 cache		DRAM post write: 0 = Disable 1 = Enable	CAS precharge in CLKs: 0 = 2 CLKs 1 = 1 CLK
(1) Test Mode 1; External tag write (tag data write-through SYSCFG 07h)							
(2) Test Mode 2; External tag read (tag data read from SYSCFG 07h)							
SYSCFG 0Ch DRAM Control Register 2 Default = 00h							
Reserved	Generate fast DRAM write BRDY# in three clocks (when write buffer enabled): 0 = No 1 = Yes	Generate HACALE one-half a clock cycle earlier: 0 = No 1 = Yes (may need to be set for CPU frequency greater than 50MHz)	Wider cache WE# pulse: The normal width is 1 CLK. This may be increased by 2.5-4.0ns by setting this bit. 0 = Disable 1 = Enable	DRAM Hole B starting address: BST[9:8] – HA[28:27]		DRAM Hole A starting address: AST[9:8] – HA[28:27]	



Table 4-31 DRAM Timing Mode Summary

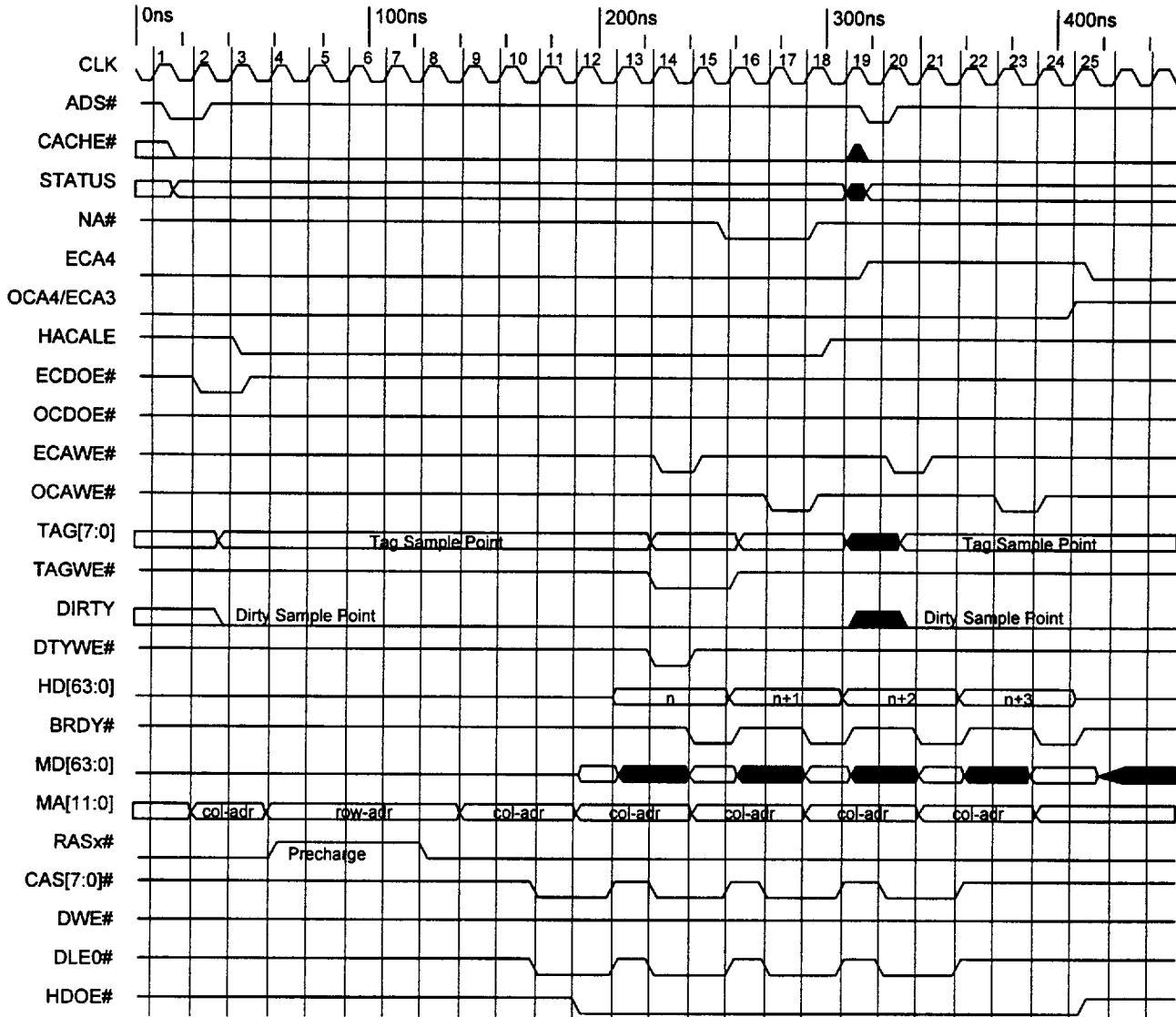
CPU Speeds (MHz)	Can be Used w/o Cache?	Page Hit	Page Miss RAS High	Page Miss RAS Active	CPU Pipeline Reduces Leadoff Cycle by:	Burst Cycle	DRAM Speed (ns)
Read Cycle							
33 to 66	yes	8 cycles	11 cycles	11+ precharge	5 clocks	3-3-3	70
80	yes	9 cycles	13 cycles	13+ precharge	5 clocks	5-5-5	70

CPU Speeds (MHz)	Can be Used w/o Cache?	Burst Page Hit	Page Miss Burst RAS High	Page Miss Burst RAS Active	CPU Pipeline Reduces Leadoff Cycle by:	DRAM Speed (ns)
Write Cycle						
33 to 66	yes	4-3-3-3	4-7-3-3	4-(7+pre)-3-3	1 clock	70
80	yes	6-5-5-5	6-9-5-5	6-(9+pre)-5-5	1 clock	70



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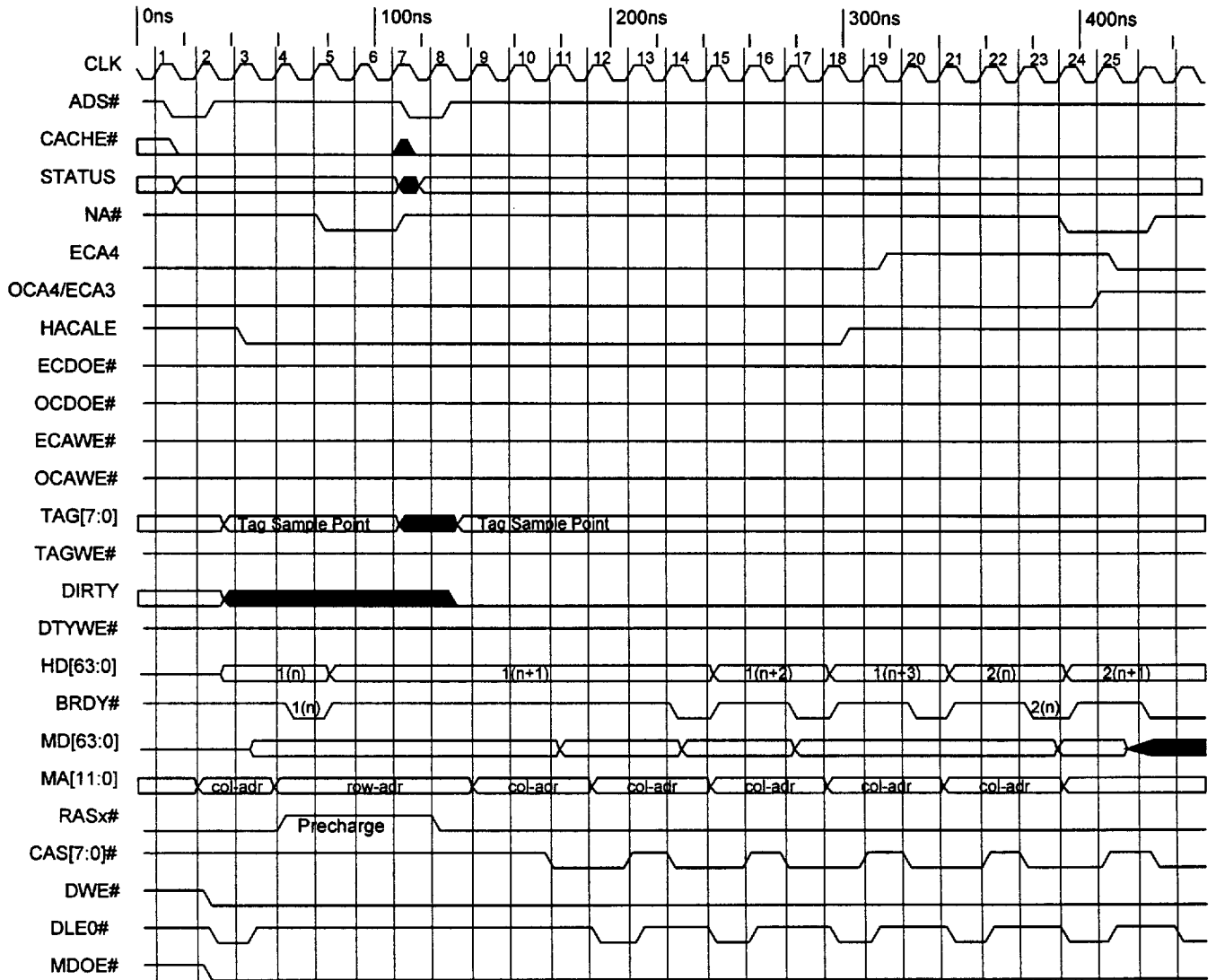
Figure 4-24 DRAM Read Page Miss with RAS Active Read Cycle



Note: For RAS inactive cycle, clocks 4 through 7 will not exist.



Figure 4-25 DRAM Page Miss with RAS Active Write Cycle



Note: For RAS inactive cycle, clocks 4 through 7 will not exist.

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4.4.3.3 DRAM Parity Generation/Detection Logic

During local DRAM write cycles, the 82C556 generates a parity bit for each byte written by the processor. Parity bits are stored in the local DRAM along with each data byte. During a DRAM read, the parity bit is checked for each data byte. If the logic detects incorrect parity, the 82C556 will assert the MPERR# signal to the 82C558N. If SYSCFG 08h[4] = 1 in the 82C557 (i.e parity has been enabled), then the 82C557 keeps the PEN# signal to the 82C558N asserted. When the 82C558N senses that MPERR# has been asserted by the 82C556 and if PEN# is also asserted, then it will assert a NMI interrupt to the CPU.

4.4.3.4 DRAM Refresh Logic

The 82C556 supports both normal and hidden refresh. Normal refresh refers to the classical refresh implementation which places the CPU on "hold" while a refresh cycle takes place to both the local DRAM and any ISA bus memory. This is the default condition at power-up. Hidden refresh is performed independently of the CPU and does not suffer from the performance restriction of losing processor bandwidth by forcing the CPU into its hold state.

Hidden refresh delivers higher system performance and is recommended over normal refresh. As long as the CPU does not try to access local memory or the ISA bus during a hidden refresh cycle, refresh will be transparent to the CPU. The CPU can continue to execute from its internal and secondary caches as well as execute internal instructions during hidden refresh without any loss in performance due to refresh arbitration. If a local memory or ISA bus access is required during a hidden refresh cycle, wait states will be added to the CPU cycle until the resource becomes available. Hidden refresh also separates refreshing of the ISA bus and local DRAM.

The DRAM controller arbitrates between CPU DRAM accesses and DRAM refresh cycles, while the ISA bus controller arbitrates between CPU accesses to the ISA bus, DMA and ISA refresh. The ISA bus controller (the 82C558N) asserts the RFSH# and MEMR# commands and outputs the refresh address during ISA bus refresh cycles.

The 82C557 implements refresh cycles to the local DRAM using CAS-before-RAS timing. The CAS-before-RAS refresh uses less power than RAS-only refresh which is important when dealing with large memory arrays. CAS-before-RAS refresh is used for both normal and hidden refresh to DRAM memory.

Table 4-32 DRAM Parity and Refresh Logic Associated Register Bits

7	6	5	4	3	2	1	0
SYSCFG 08h CPU Cache Control Register 1 Default = 00h							
L2 cache bank select: 0 = Double bank (interleaved) ⁽¹⁾ 1 = Single bank (non-interleaved)	Line comparator for bus masters: ⁽²⁾ 0 = Disable 1 = Enable	CPU HITM# pin sample timing: 0 = Delay 1 more clock 1 = No delay	DRAM parity check: 0 = Disable 1 = Enable	Combined Tag/Dirty control: 0 = Tag and Dirty on different chips 1 = Tag and Dirty are on the same chip	CPU address pipelining: ⁽³⁾ 0 = Disable 1 = Enable	L1 cache write-back/write-through mode setting: 0 = Write-through only 1 = Write-back enabled	BIOS area cacheability in L1 cache: 0 = Cacheable 1 = Non-cacheable
<p>(1) Interleaved on A3 for async SRAMs, interleaved on A17 for sync SRAMs. Note that for 2-1-1-1 sync SRAM operation, dual non-interleaved banks are not supported. Only single bank is supported.</p> <p>(2) For a master request if the subsequent read/write is within the same cache line, CPU 'Inquire' cycles are not done until there is a cache line miss.</p> <p>(3) Turn on for standard sync SRAMs in 3-1-1-1 R/W or for async SRAMs. This bit must be off for standard sync SRAMs in 2-1-1-1 R/W. Also refer to SYSCFG 11h[4]. At any time, either SYSCFG 08h[2] or 11h[4] can be active, but not both at the same time.</p>							
SYSCFG 12h Refresh Control Register Default = 00h							
Reserved	Reserved	Suspend mode refresh control: 00 = Timing for refresh based on SYSCFG 12h[3:2](with refresh timing based on CLK input) 01 = Self-refresh timing (refresh pulse width equals REFRESH# low time) 10 = 100ns refresh pulse width triggered by REFRESH# 11 = Rsvd	Slow refresh control: 00 = Refresh on every REFRESH# falling edge 01 = Refresh on one in two REFRESH# falling edges 10 = Refresh on one in four REFRESH# falling edges 11 = Refresh on every REFRESH# edge (both rising and falling)	Generate LA[23:17] from 08Fh (Refresh DMA Page Addr. Reg.) during refresh: 0 = Disable 1 = Enable	82C556 generates MP[7:4] for PCI master writes: 0 = No 1 = Yes		

The periodic refresh request signal output, from the 82C558N that occurs every 15 μ s, originates from the counter/timer of the integrated 82C206. Requests for refresh cycles are generated by two sources: the counter/timer of the integrated 82C206 or 16-bit ISA masters that activate refresh when they have bus ownership. These ISA masters must supply refresh cycles because the refresh controller cannot preempt the bus master to perform the necessary refresh cycles. 16-bit ISA masters that hold the bus longer than 15 μ s must supply refresh cycles.

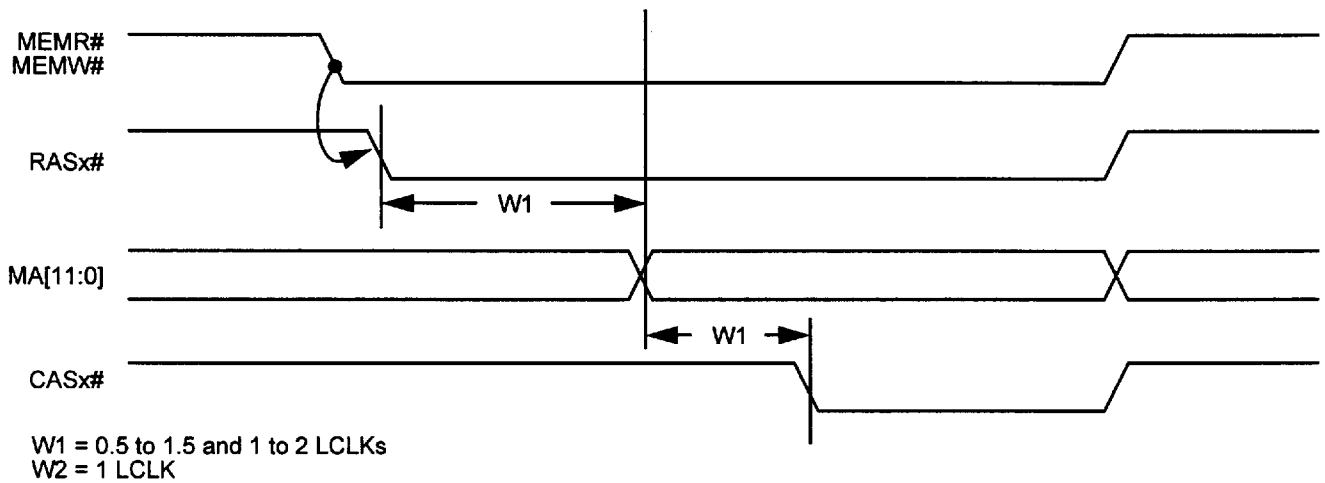
4.4.4 DRAM DMA/Master Cycles

For DMA and master cycles, the DRAM controller operates such that the MEMR# and MEMW# signals generate RASx#

synchronously. The generation of the DRAM column address is then synchronized with LCLK. The synchronization can be programmed to be 0.5 to 1.5 LCLKs and 1 to 2 LCLKs. The generation of CASx# is always one LCLK after the generation of the column address. The cycles can thus be completed without adding wait states. For cases when the CPU write-back cache is enabled, wait states need to be added to the DMA/master cycles. This is because the CPU can request a primary cache castout (always a burst write to the DRAMs) and only after the castout is completed can the requested data from the DRAM be fetched.

Note: ISA masters which ignore IOCHRDY may not work when CPU write-back is enabled.

Figure 4-26 ISA Master Synchronization



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4.4.5 DRAM Hole Control

The Viper-N Chipset allows system "holes" in DRAM, to which accesses can go to the PCI bus. DRAM holes can be

set through SYSCFG 09h[7:0], 0Ch[3:0], 0Ah[7:0], 0Bh[7:0], and 06h[7]. Table 4-33 shows these register bits.

Table 4-33 DRAM Hole Control Related Registers

7	6	5	4	3	2	1	0
SYSCFG 06h Shadow RAM Control Register 3 Default = 00h							
DRAM hole in system memory from 80000h-9FFFFh: 0 = No hole 1 = Enable hole	CPU write-through mode wait for cycle access finish to do snooping ⁽¹⁾ . 0 = Don't wait 1 = Wait	Cacheability for segment C0000h-C7FFFh: 0 = No 1 = Yes in L1 and L2 ⁽²⁾	Cacheability for segment F0000h-FFFFFh: 0 = No 1 = Yes in L1 and L2 ⁽²⁾	Read/write control segment F0000h-FFFFFh: Refer to SYSCFG 04h[7:6] for decode		Read/write control segment E0000h-EFFFFh: Refer to SYSCFG 04h[7:6] for decode	
(1) This is not necessary if CPU is in full speed.							
(2) L1 cacheability disabled by SYSCFG 08h[0].							
SYSCFG 09h System Memory Function Register 1 Default = 00h							
DRAM Hole B size: 00 = 512KB 01 = 1MB 10 = 2MB 11 = 4MB		DRAM Hole B control mode: 00 = Disable 01 = WT for L1 and L2 10 = Non-cacheable for L1 and L2 11 = Enable hole in DRAM		DRAM Hole A size: 00 = 512KB 01 = 1MB 10 = 2MB 11 = 4MB		DRAM Hole A control mode: 00 = Disable 01 = WT for L1 and L2 10 = Non-cacheable for L1 and L2 11 = Enable hole in DRAM	
SYSCFG 0Ah System Memory Address Decode Register 1 Default = 00h							
DRAM Hole A starting address AST[7:0]-HA[26:19]. Also see SYSCFG 0Ch[1:0].							
SYSCFG 0Bh System Memory Address Decode Register 2 Default = 00h							
DRAM Hole B starting address BST[7:0]-HA[26:19]. Also see SYSCFG 0Ch[3:2]							

4.4.6 Lookup Table DRAM Configuration Mode

The Viper-N Chipset provides the maximum flexibility for DRAM configurations if SYSCFG 13h[7] = 1. To maintain backward compatibility with OPTi's 82C546/547 Chipset, the fixed DRAM configurations of that chipset are also supported.

If SYSCFG 13h[7] = 0, then only the fixed DRAM configurations listed in Table 4-35 are supported, maintaining compatibility with OPTi's 82C546/82C547 (Python) Chipset. This mode should not be used in new designs.

Table 4-34 Register Bits Associated with Backward Compatibility for OPTi's 82C546/82C547 Chipset

7	6	5	4	3	2	1	0
SYSCFG 00h DRAM Configuration Register 1							
If 13h[7] = 0*: 82C546/82C547 Memory Configurations Compatibility Default = 00h							
Single memory write (non-cache) cycle CPU, pipelined enable: 0 = Disable 1 = Enable	Second bank: 512x36 SIMM	First bank: 512x36 SIMM	See Table 4-35 for decode.				
*If 13h[7] = 1: Full Memory Decode - Refer Section 4.4.1 for details.							

Table 4-35 DRAM Configurations

4 3 2 1 0	SIMM 0	SIMM 1	SIMM 2	SIMM 3	Total
0 0 0 0 0	256K	256K			2M
0 0 0 0 1	512K	512K	----	---	4M
0 0 0 1 0	1M	1M	---	---	8M
0 0 0 1 1	2M	2M		---	16M
0 0 1 0 0	4M	4M		---	32M
0 0 1 0 1	8M	8M			64M
0 0 1 1 0	256K	256K	256K	256K	4M
0 0 1 1 1	256K	256K	512K	512K	6M
0 1 0 0 0	512K	512K	512K	512K	8M
0 1 0 0 1	256K	256K	1M	1M	10M
0 1 0 1 0	512K	512K	1M	1M	12M
0 1 0 1 1	1M	1M	1M	1M	16M
0 1 1 0 0	256K	256K	2M	2M	18M
0 1 1 0 1	512K	512K	2M	2M	20M
0 1 1 1 0	1M	1M	2M	2M	24M
0 1 1 1 1	2M	2M	2M	2M	32M
1 0 0 0 0	256K	256K	4M	4M	34M
1 0 0 0 1	512K	512K	4M	4M	36M
1 0 0 1 0	1M	1M	4M	4M	40M
1 0 0 1 1	2M	2M	4M	4M	48M
1 0 1 0 0	4M	4M	4M	4M	64M
1 0 1 0 1	256K	256K	8M	8M	66M
1 0 1 1 0	512K	512K	8M	8M	68M
1 0 1 1 1	1M	1M	8M	8M	72M
1 1 0 0 0	2M	2M	8M	8M	80M
1 1 0 0 1	4M	4M	8M	8M	96M
1 1 0 1 0	8M	8M	8M	8M	128M

Note: These fixed configurations are for maintaining compatibility with OPTi's 82C546/82C547 (Python) Chipset.



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4.5 PCI Bus Interface

The Viper-N Chipset supports up to three PCI bus masters. Both synchronous and asynchronous modes of operation of the PCI bus, with respect to the CPU, are supported. The Viper-N Chipset supports a 32-bit PCI implementation and supports PCI bus operating frequencies up to 33MHz. The PCI local bus controller is present in the 82C557 and the PCI data bus buffering is done within the 82C558N. The 82C558N also functions as the PCI-to-ISA expansion bridge and performs the required data path conversion between the 32-bit PCI bus and the 8/16-bit ISA bus.

4.5.1 PCI Master Cycles

A PCI master is always allowed to access the system memory and system I/O spaces. Accesses to the ISA bus and the VL bus space can be individually disabled/enabled by programming PCIDV1 43h[2]. Refer to Table 4-36.

4.5.1.1 System Memory Access

The PCI master asserts FRAME# and puts out the address on the AD[31:0] bus. The 82C557 decodes that address and asserts LMEM# to the 82C558N if the access is to the system memory area. The 82C558N then provides the data path to the PCI master to access system memory. If the access is to the system memory space, then the 82C557 acts as the PCI slave and it generates the appropriate control signals to snoop the L1 cache for every access, or for every access to a new line (if the line comparator is enabled). The 82C556 performs the data steering and latching based on the control information received from the 82C557 over the MDOE#, HDOE#, DBCOE[1:0]#, and the DLE[1:0]# lines.

Table 4-36 ISA and VL Bus Space Access Bits

7	6	5	4	3	2	1	0
PCIDV0 04h							
Command Register							
Default = 07h							
Address/data stepping: Always set to 0.	PERR# output pin enable: Always set to 0.	Reserved (RO)	Memory write and invalidate cycle generation (RO): Always = 0. No memory write and invalidate cycles will be generated by the 82C557.	Special cycles (RO): Always = 0. The 82C557 does not respond to PCI special cycles.	Bus master operations (RO): Always = 1. Allows the 82C557 to perform bus master operations all the time. (Default = 1)	Memory access (RO): Always = 1. The 82C557 allows a PCI bus master access to memory all the time. (Default = 1)	I/O access (RO): Always = 1. The 82C557 allows a PCI bus master access to PCI I/O all the time. (Default = 1)
PCIDV1 04h							
Command Register							
Default = 07h							
Address/data stepping: Always set to 0.	Enable parity error output: 0 = Disable 1 = Enable	Reserved (RO)	Memory write and invalidate cycle generation (RO): Always = 0. No memory write and invalidate cycles will be generated by the 82C558N.	Special cycles: 0 = Disable 1 = Enable (82C558N responds to stop grant special cycle.)	Bus master operations: 0 = Disable 1 = Enable PCI cycle generation during DMA/ISA master may be disabled by this bit. (Default = 1)	Memory access (RO): Always = 1. The 82C558N allows a PCI bus master access to memory at any time. (Default = 1)	I/O access (RO): Always = 1. The 82C558N allows a PCI bus master access to I/O at any time. (Default = 1)
PCIDV1 43h							
(Part of IRQ Triggering Register)							
Default = 00h							
Reserved	Enable DMA or ISA master to preempt PCI Master 0 = Disable 1 = Enable	Fixed/rotating priority between PCI masters: 0 = Rotating 1 = Fixed	Back-to-back ISA I/O: 0 = Enable 1 = Disable	Reserved	PCI master access to VL/ISA: 0 = Enable 1 = Disable	ISA bus control signals for memory accesses greater than 16M: 0 = Enable 1 = Disable	



Table 4-8 and Table 4-9 (page 80) describe the sequence of events that take place during a master read/write cycle from/to system memory. Listed below is the data flow path for all such accesses by a PCI master. (Refer to Table 3-12 for a description on the state of the control signals from the 82C557 to the 82C556 for all cycles.)

Low order DRAM read:

The DRAM puts the data out on MD[31:0]#. The 82C556 latches the data, inverts it and puts it out onto MD[63:32] and drives it out to the 82C558N. The 82C558N then latches the data and puts it out on AD[31:0] for the PCI master.

Low order DRAM write:

The PCI master puts the data out on AD[31:0]. The 82C558N latches the data and puts it out on MD[63:32]. The 82C556 then latches the data, inverts it and puts it out onto MD[31:0]# and presents it to the DRAM.

Low order cache read:

The cache puts out the data on HD[31:0]. The 82C556 latches the data onto MD[63:32] and drives it out to the 82C558N. The 82C558N then latches the data and puts it out on AD[31:0] for the PCI master.

Low order cache write:

The PCI master puts out the data on AD[31:0]. The 82C558N latches the data and puts it out on MD[63:32]. The 82C556 latches this data and puts it out on HD[31:0] for the cache.

High order DRAM read:

The DRAM puts out the data on MD[63:32]. In this case, there is a direct path from the DRAM to the 82C558N and the 82C556 does not have to perform any latching or steering of data. The 82C558N latches the data available on MD[63:32] and puts it out on AD[31:0] for the PCI master.

High order DRAM write:

The PCI master puts out the data on AD[31:0]. The 82C558N latches the data and this puts it out on MD[63:32]. The 82C556 does not have to perform any steering or latching and the data is written directly to the DRAM.

High order cache read:

The cache puts out the data on HD[63:32]. The 82C556 latches the data onto MD[63:32] and drives it out to the 82C558N. The 82C558N then latches the data and puts it out on AD[31:0] for the PCI master.

High order cache write:

The PCI master puts out the data on AD[31:0] and the 82C558N latches the data and puts it out on MD[63:32]. The 82C556 latches this data and puts it out on HD[63:32] for the cache.

4.5.1.2 Non-Local Memory Access

The PCI master asserts FRAME# and puts out the address on the AD[31:0] bus. If the access is not to the system memory area, the 82C557 does not assert LMEM# to the 82C558N. The 82C558N then translates all PCI cycles to the VL bus and generates the local bus signals one LCLK after the assertion of FRAME#. The LDEV# signal is sampled at the end of the next LCLK and the 82C558N asserts DEVSEL# if the LDEV# was sampled asserted. For a read access from the VL bus, the local bus device puts out the data on MD[63:32]. This data is latched by the 82C558N and put out on AD[31:0] for the PCI master. For a write access to the VL bus, the PCI master puts out the data on AD[31:0]. This data is latched by the 82C558N and put out on MD[63:32] for the VL bus.

All other PCI slaves have up to three PCI CLKs after the start of the PCI cycle to assert DEVSEL#. All read/write access from/to PCI slaves is done directly over AD[31:0].

If neither a PCI slave nor a local bus device responds within three PCI CLKs after the start of the cycle, then the 82C558N starts an ISA cycle. For a read access from the ISA bus, the ISA device puts out the data on SD[15:0] or SD[7:0], depending on whether it is a 16- or 8-bit slave. The 82C558N latches this data and then performs the appropriate data bus conversions and steering (based on the IOCS16#, MEMCS16#, SBHE# signals) and puts the data out on AD[31:0]. For a write access to the ISA bus, the PCI master puts out the data on AD[31:0]. The 82C558N latches this data and then performs the appropriate data bus conversions and steering (based on the IOCS16#, MEMCS16#, SBHE# signals) and puts out the data on SD[15:0] or SD[7:0], depending on whether it is a 16- or 8-bit slave.

4.5.1.3 PCI Master Pre-Snoop

Pre-snooping is a technique with the aid of which a PCI master can sustain bursting to the local memory till a 4K page boundary is reached. If pre-snooping is enabled, then on the first TRDY# of the PCI master cycle, the state machine within the 82C557 increments the HA[12:5] address lines by one and asserts EADS# to the CPU after that. By this time, the earlier cache address would have been latched by HACALE. If the CPU responds with a HITM#, then the current PCI master cycle will be terminated at the line boundary to allow the write-back cycle to occur. Enabling pre-snooping allows the Viper-N Chipset to continue bursting past a line boundary.

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4.5.2 PCI Slave Cycles

4.5.2.1 CPU Master Cycles

Any CPU cycle that is not an access to the system memory area, the 82C557 translates that cycle to a PCI cycle and asserts FRAME# on the PCI bus. All PCI slaves have up to three PCI CLKs after the start of the cycle within which to assert DEVSEL#. The data flow path would be similar to the ones described in the previous section.

4.5.2.2 PCI Byte/Word Merge

This feature, if turned on, allows successive 8-/16-bit writes from the CPU to a PCI slave, to be merged into a 32-bit entity and then sent out to the PCI slave. This enhances PCI video performance by a substantial margin. Byte/word merge is controlled by MDLE# and IRDY# from the 82C557. The number of MDLE# pulses sent out by the 82C557 before it

asserts IRDY# determines how much data was sent out with each pulse. There is one additional control provided (in SYSCFG 00h[2:1]) for the byte/word merge implementation. This setting determines the maximum time difference within which consecutive PCI bytes/words could be merged.

To enable byte/word merge and to obtain the maximum performance benefit, PCIDV14Eh[3], PCIDV14Eh[1], SYSCFG 17h[2], and SYSCFG 00h[4:3] should be set to 1. Refer to Table 4-37 for information on these register bits.

4.5.2.3 ISA Master Cycles

If the ISA master cycle is not a system memory access, then the 82C558N becomes the initiator and commences a PCI cycle. The data flow path for an ISA master to a PCI slave access is between the SD[15:0]/SD[7:0] lines and the AD[31:0] lines. The 82C558N handles all the data bus conversion and steering logic.

Table 4-37 Byte/Word Merge Feature Register Bits

7	6	5	4	3	2	1	0
PCIDV1 4Eh							
Miscellaneous Control Register C							
Default = 00h							
0 = Test 4 Disabled 1 = Test 4 Enabled	0 = Test 3 Disabled 1 = Test 3 Enabled	0 = Test 2 Disabled 1 = Test 2 Enabled	0 = Test 1 Disabled 1 = Test 1 Enabled	Pipelined byte merge function: 0 = Disable 1 = Enable	EOP configuration: 0 = Output 1 = Input	Byte merge: 0 = Disable 1 = Enable	ISA master data swap: 0 = Enable 1 = Disable
SYSCFG 17h							
Miscellaneous Control Register 2							
Default = 00h							
Generate NA# for PCI slave access in sync LCLK mode: 0 = No 1 = Yes	NA# generation for PCI slave access: 0 = Do not generate NA# 1 = Generate NA# for async LCLK mode	Sync two bank select: 0 = Rsvrd 1 = Set this bit to 1 when two banks of sync SRAM are installed	BRDY# control for PCI cycles: 0 = Normal BRDY# 1 = Fast BRDY#	Fast FRAME# generation for PCI cycles: 0 = Disable 1 = Enable	Pipelining during byte merge: 0 = Disabled 1 = Enabled	Sync SRAM type: 0 = Standard 1 = Pipelined	Burst type: 0 = Intel burst protocol 1 = Linear burst protocol
SYSCFG 00h							
DRAM Configuration Register 1							
Default = 00h							
If 13h[7] = 1: Full Memory Decode							
Single memory write (non-cache) cycle CPU, pipelined enable: 0 = Disable 1 = Enable	Video memory byte/word prefetch control: 0 = Off 1 = On	Sony SONIC-2WP support: 0 = Sony SONIC-2WP module not installed 1 = Sony SONIC-2WP module installed	Byte merge control: 0 = Disable 1 = Enable	NA# generation during byte merge: (Used to kill CPU idle cycles during byte merge only.) 0 = Disable byte merge NA# 1 = Enable byte merge NA#	Byte/word merge time-out counter: (Access passed to PCI bus if this time-out period expires.) 00 = 4 CPU Clocks 01 = 8 CPU Clocks 10 = 12 CPU Clocks 11 = 16 CPU Clocks	Hold request block control during video byte merge: 0 = Let CPU to be put on hold while byte merge in progress if hold request arrives 1 = Block hold request if byte merge in progress	



4.6 VL Bus Interface

The Viper-N Chipset supports VL bus slaves only. The VL bus always operates at the PCI bus operating frequency. All the control and status signals are generated by the 82C558N and the data path is controlled by buffers in the 82C556. The 82C557 also does the data bus conversion to interface the 32-bit VL bus to the 64-bit CPU bus. The Viper-N Chipset supports VL bus speeds up to 33MHz, independent of the CPU speed. It assumes that an access outside the system memory area is either a PCI cycle, a VL slave cycle, or an ISA cycle. If the cycle is not a system memory cycle, then the 82C557 generates a PCI cycle and the 82C558N a VL cycle.

If the Viper Notebook Chipset has been configured to support VL bus slaves, then the 82C558N generates LADS# and other VL bus status signals one LCLK after FRAME# has been asserted. The VL slave can claim such an access by asserting LDEV#, which is sampled at the end of the next LCLK. If LDEV# is active when sampled, the 82C558N asserts DEVSEL# to the 82C557 and it will not execute an ISA cycle but will instead wait for the VL slave to generate LRDY#. On receiving an active LDEV#, the 82C558N asserts DEVSEL# to the 82C557. After LRDY# is sampled active, the Viper-N Chipset will terminate the cycle of the current active bus master by returning BRDY# or IOCHRDY.

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Figure 4-27 PCI Master Read from Local Memory

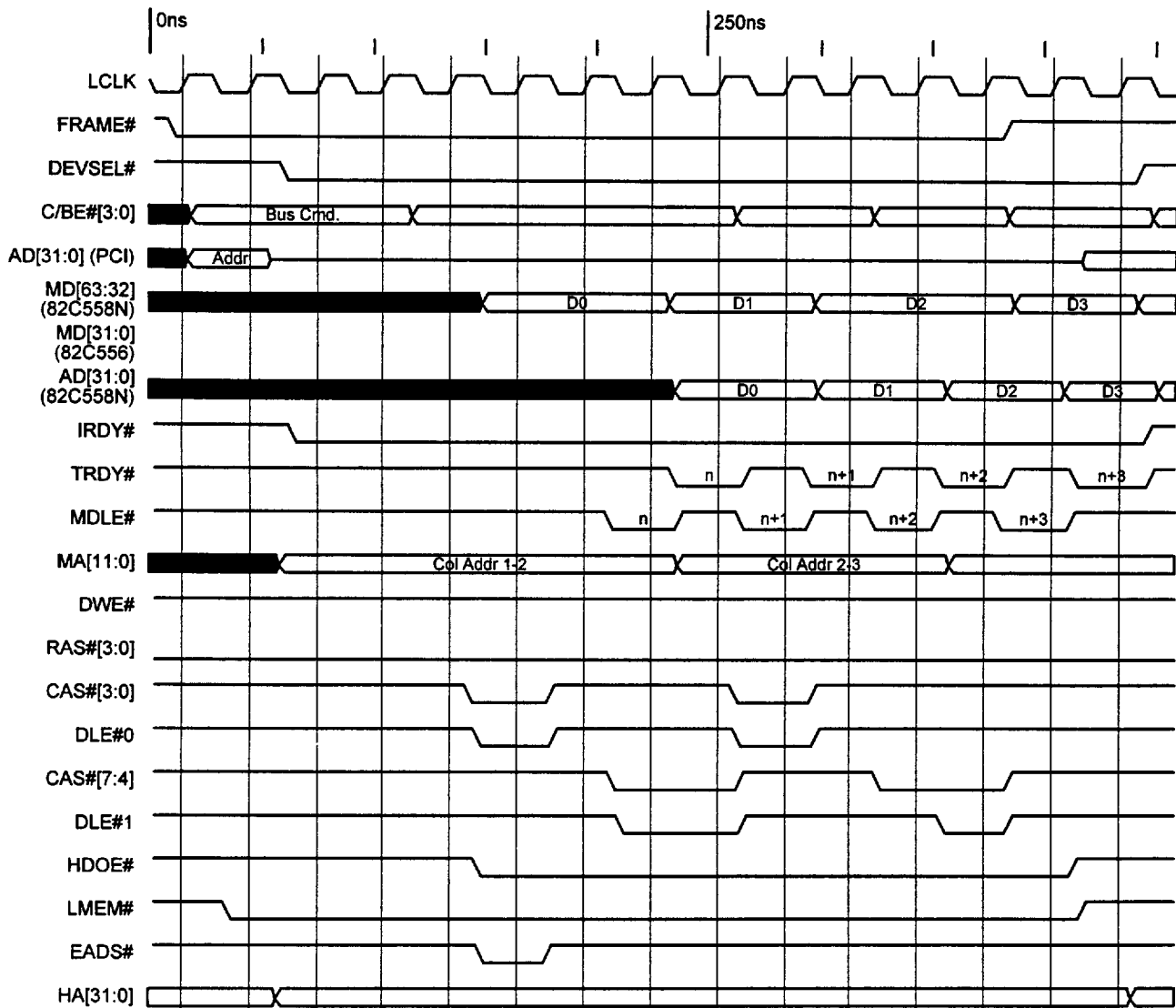
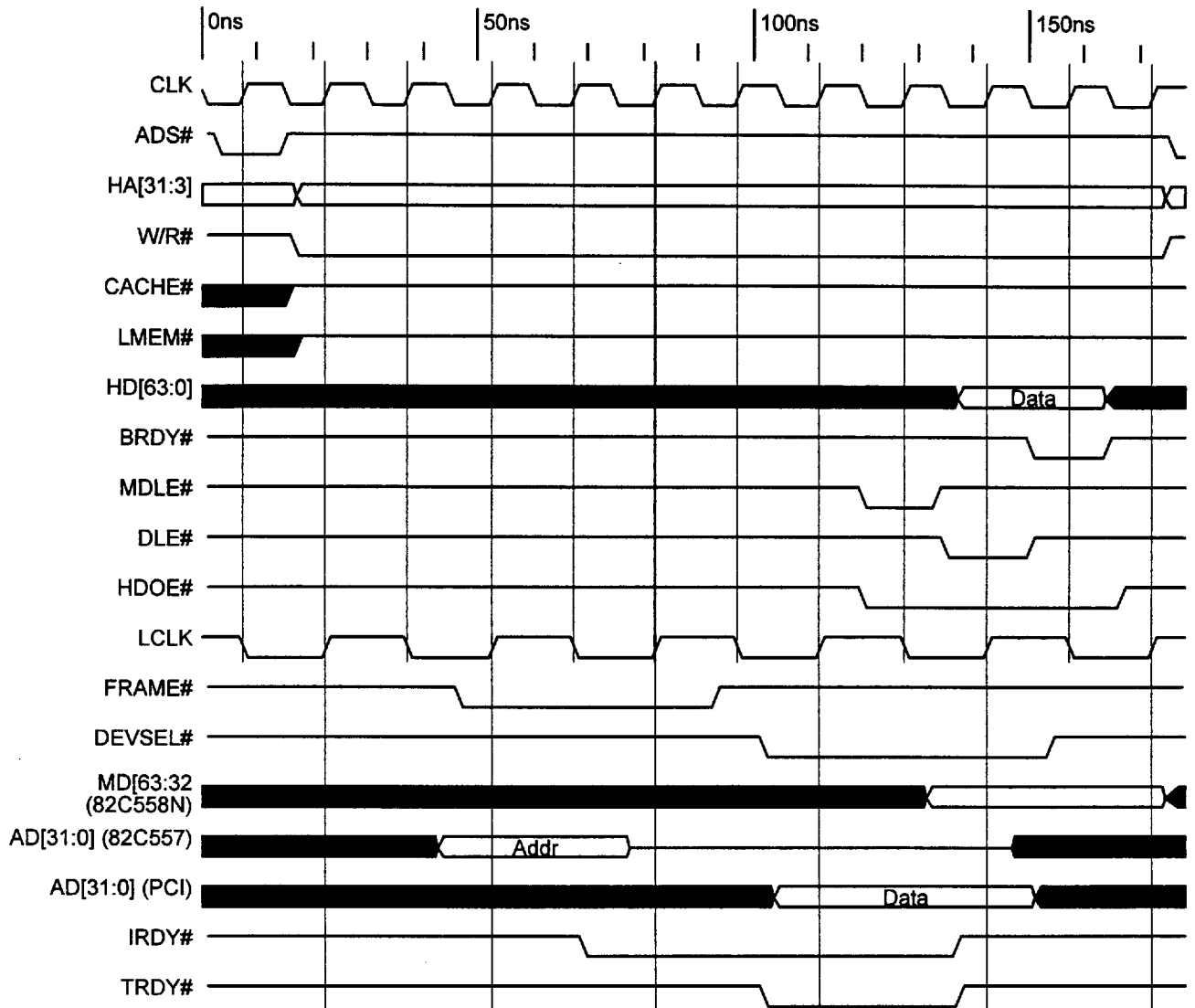


Figure 4-28 CPU Read from PCI, 32 Bits



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Figure 4-29 CPU Write to PCI, 32 Bits

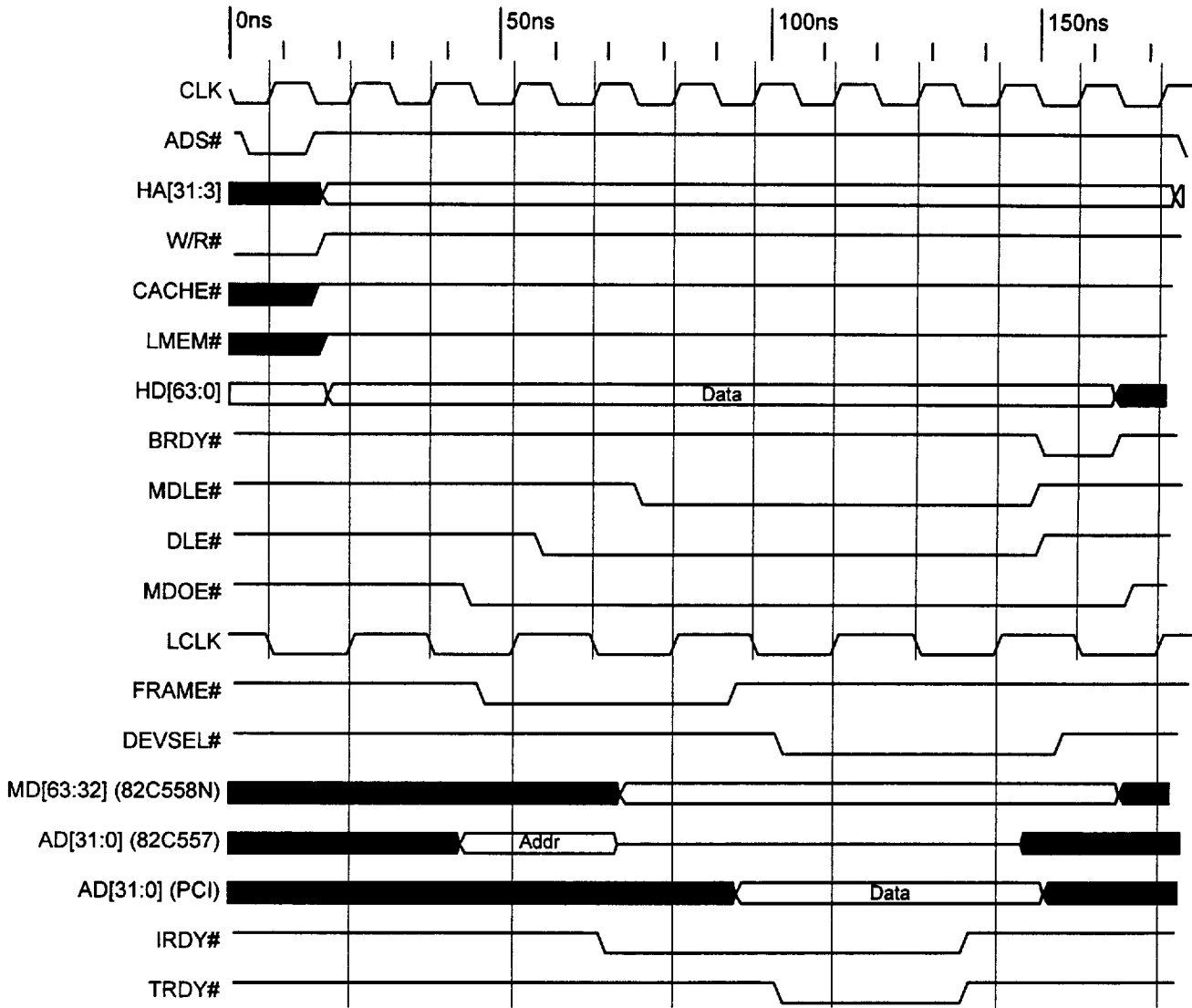
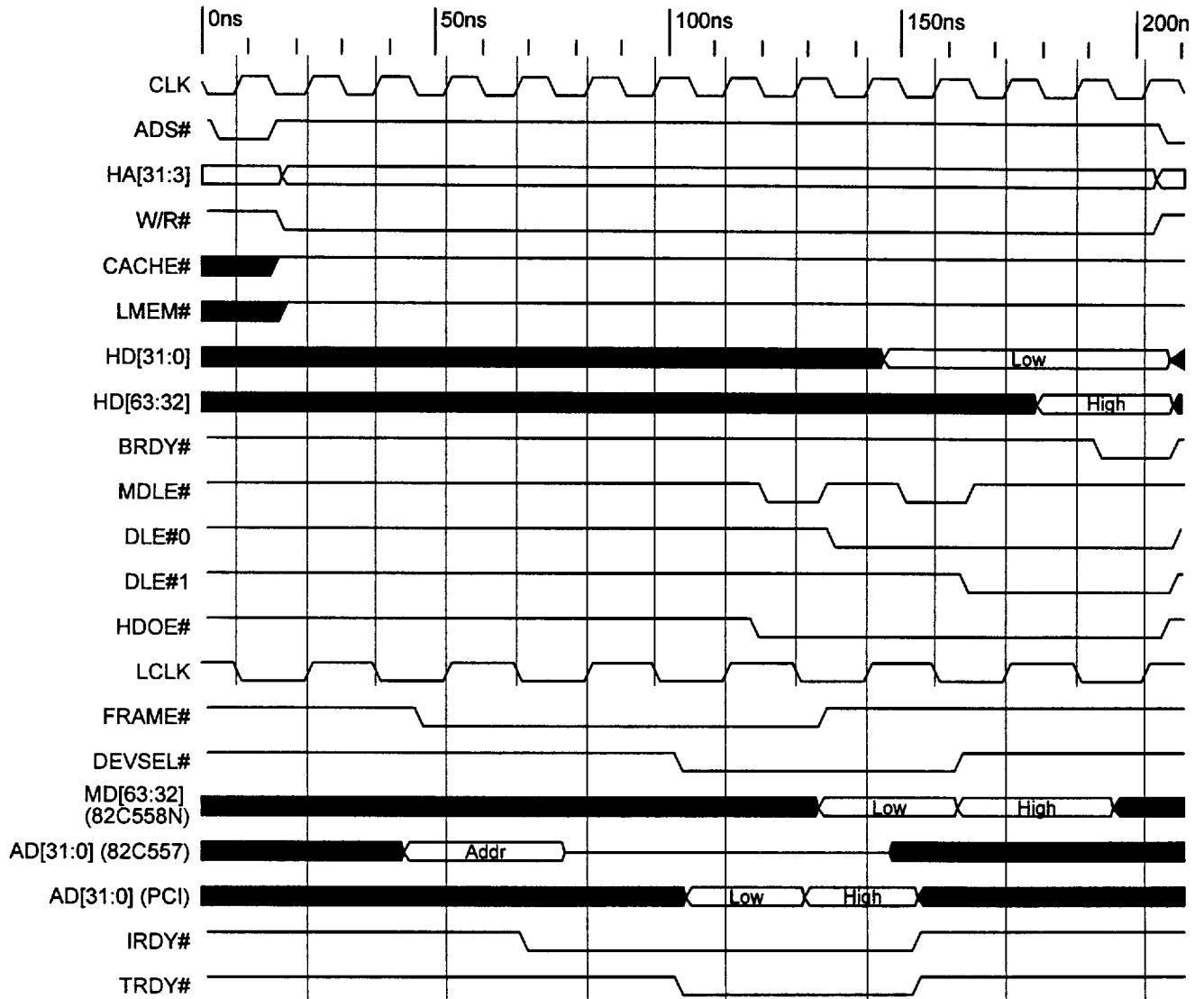


Figure 4-30 CPU Read from PCI, 64 Bits



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Figure 4-31 CPU Read from VL Slave

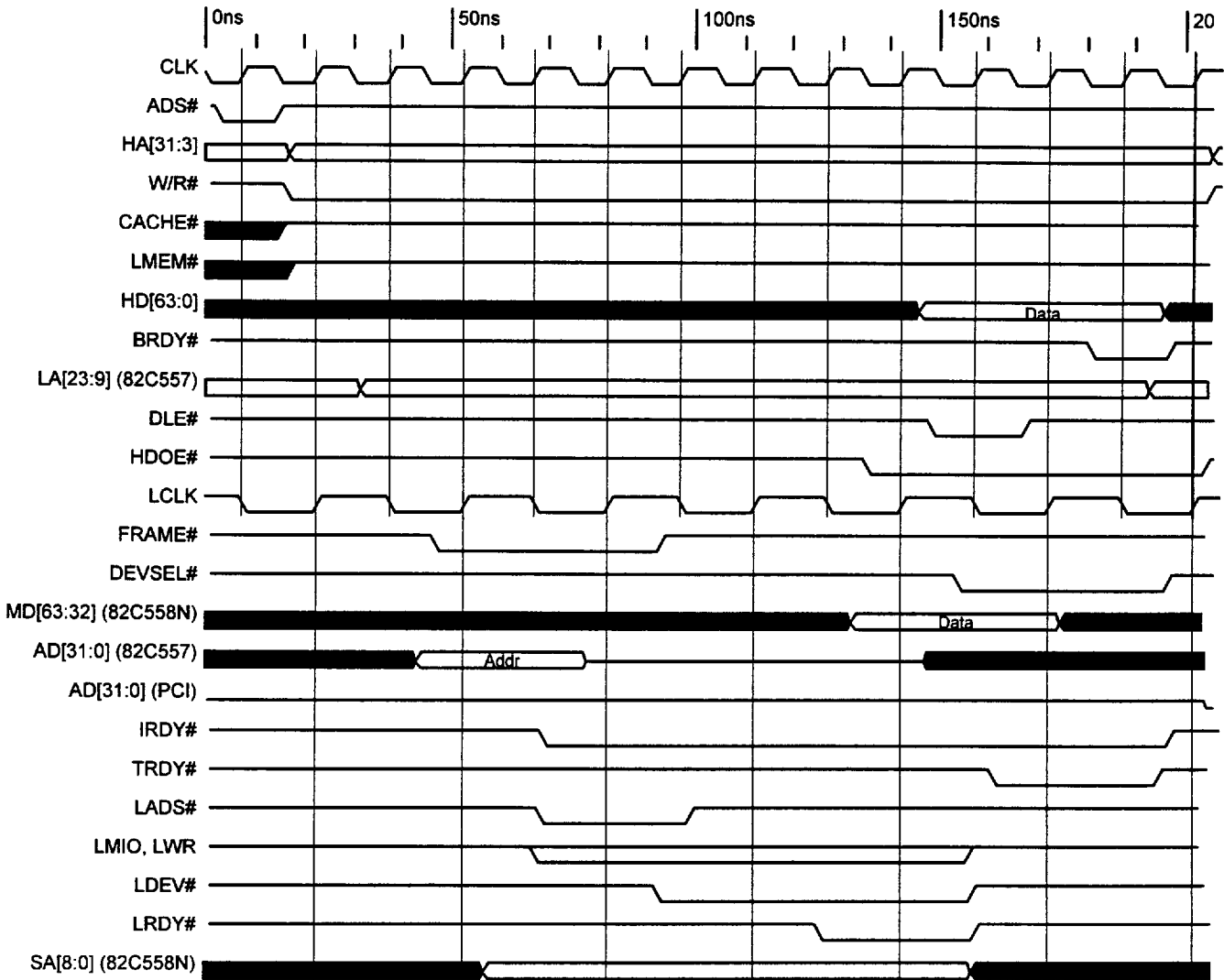
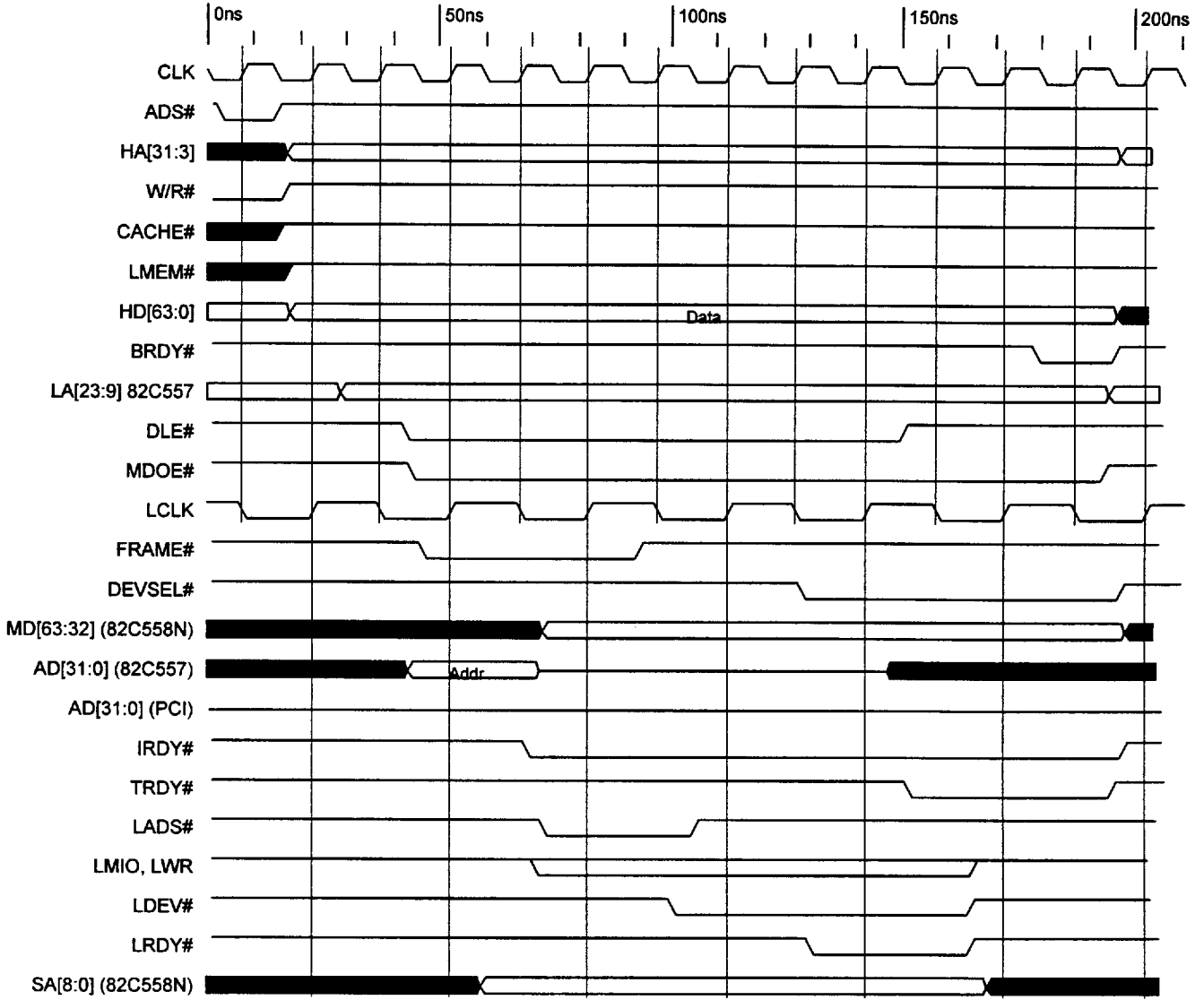


Figure 4-32 CPU Write to VL Slave



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Figure 4-33 ISA Master Read from PCI

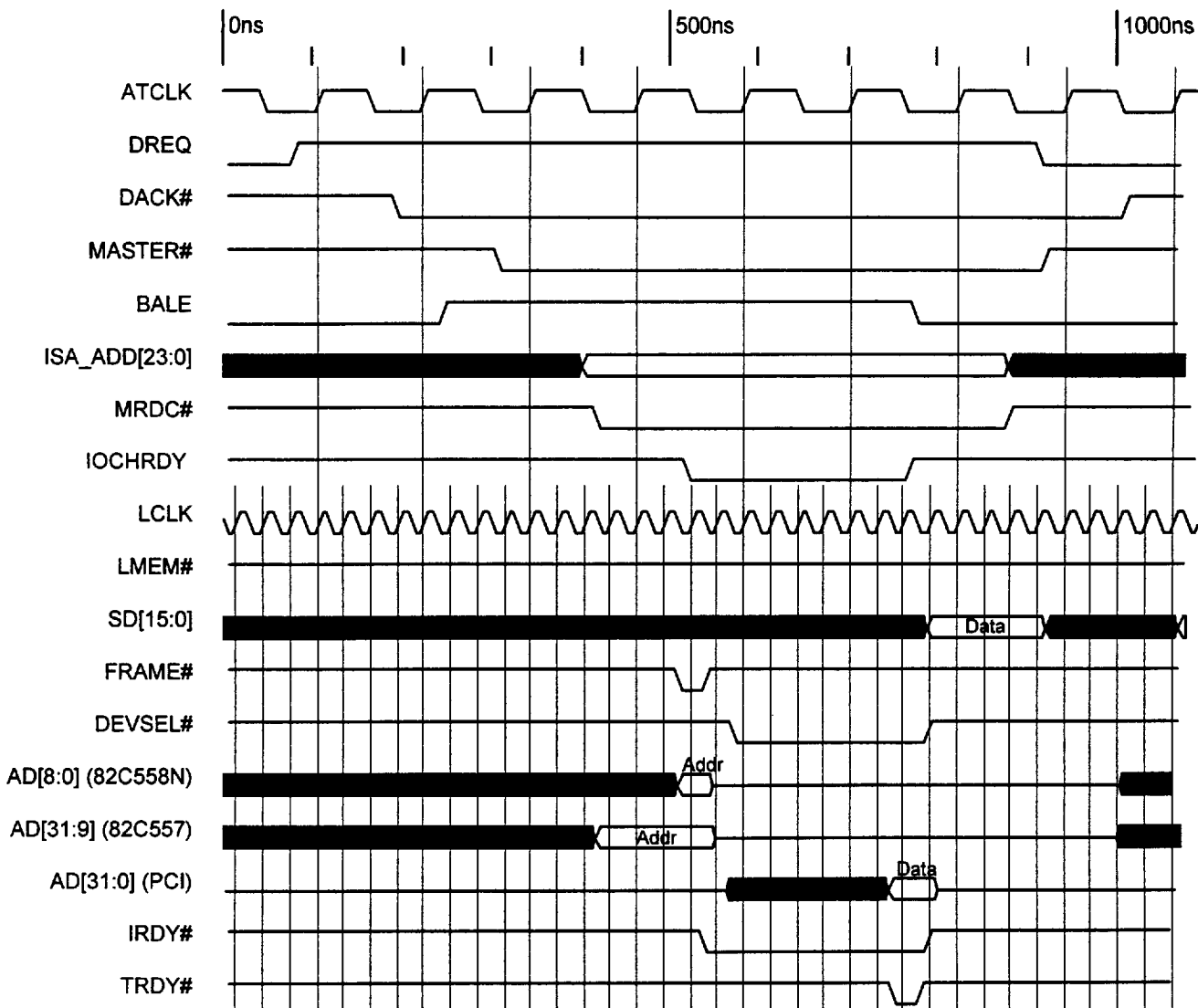
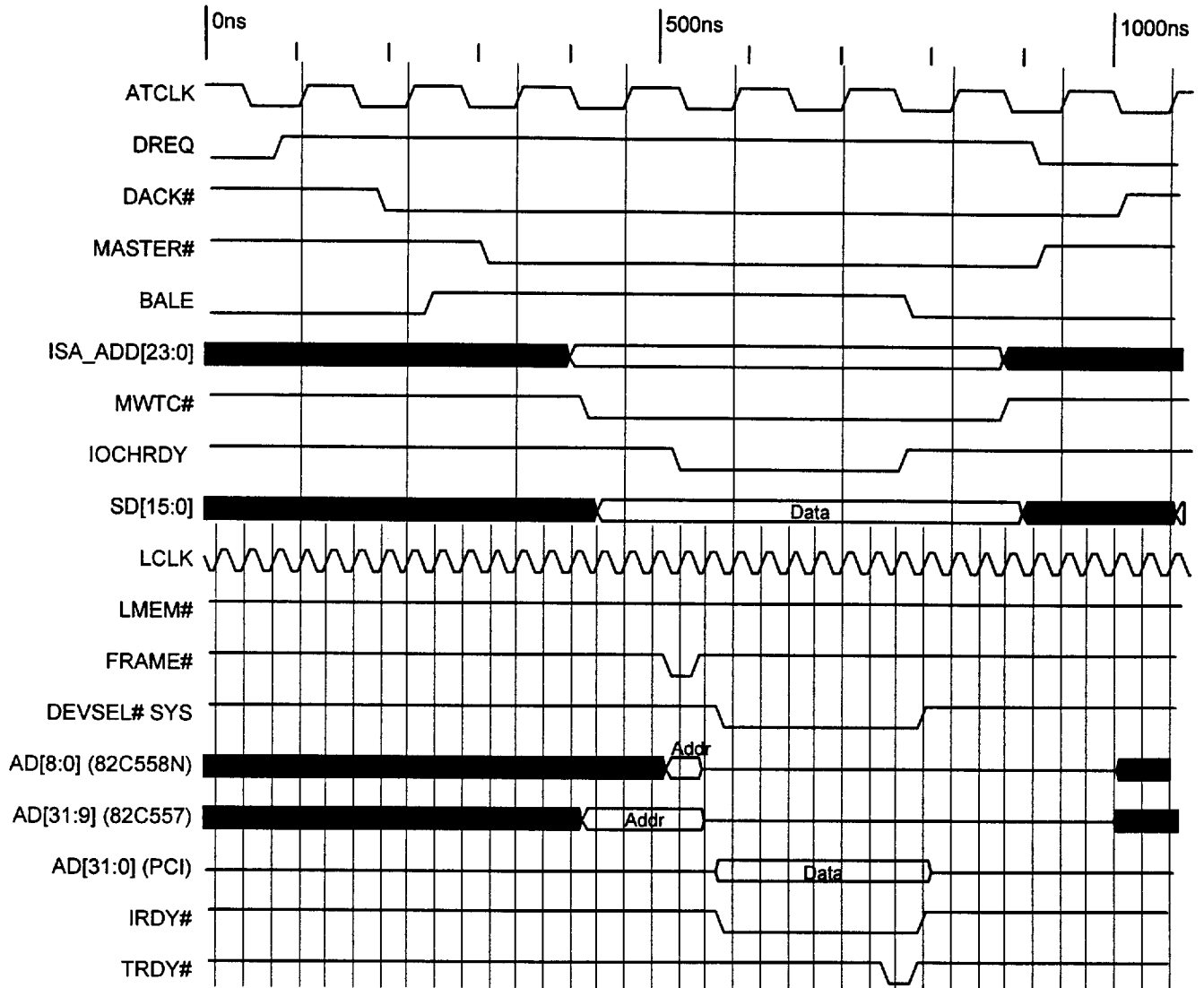


Figure 4-34 ISA Master Write to PCI



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Figure 4-35 ISA Master Read from ISA Slave

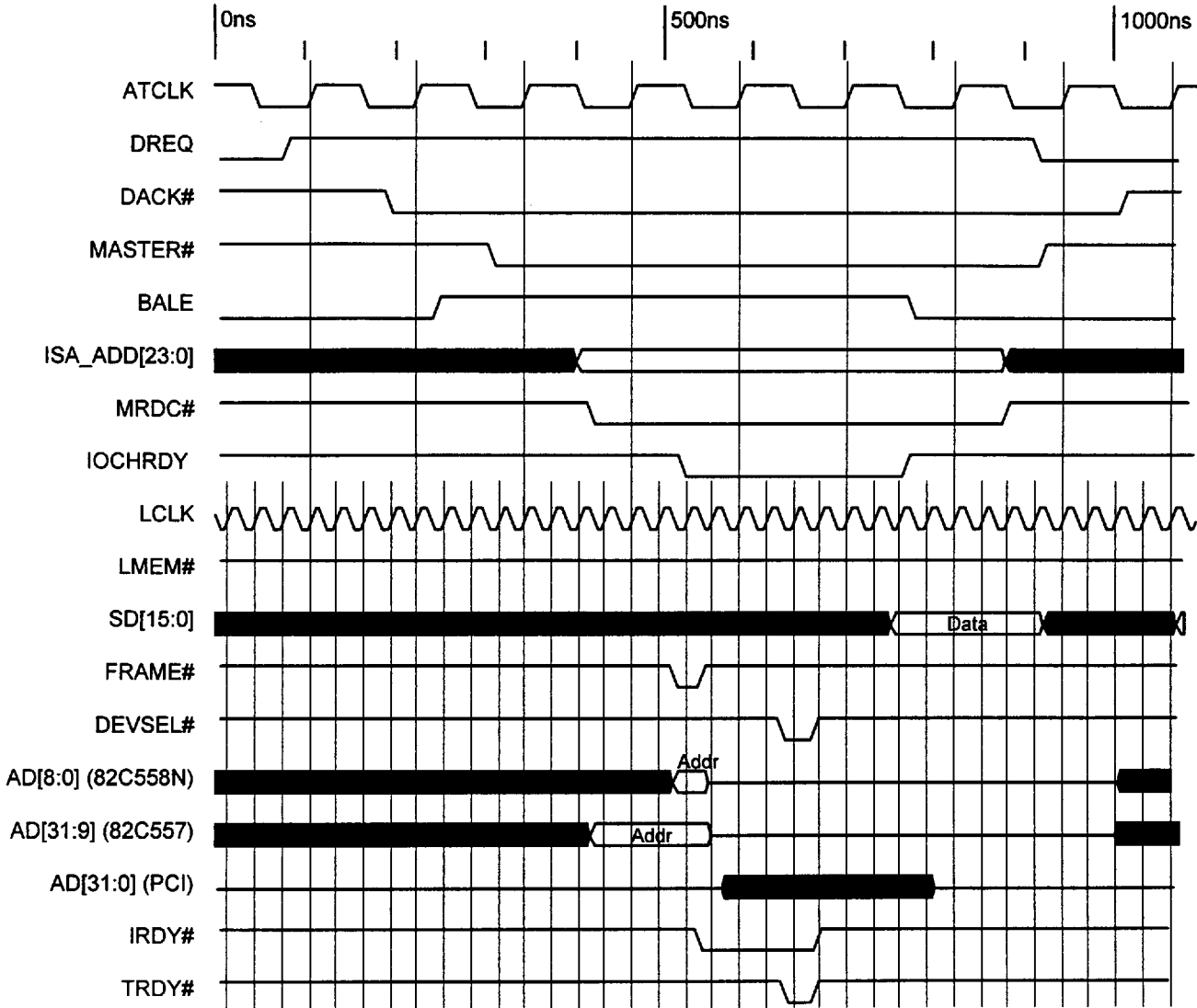
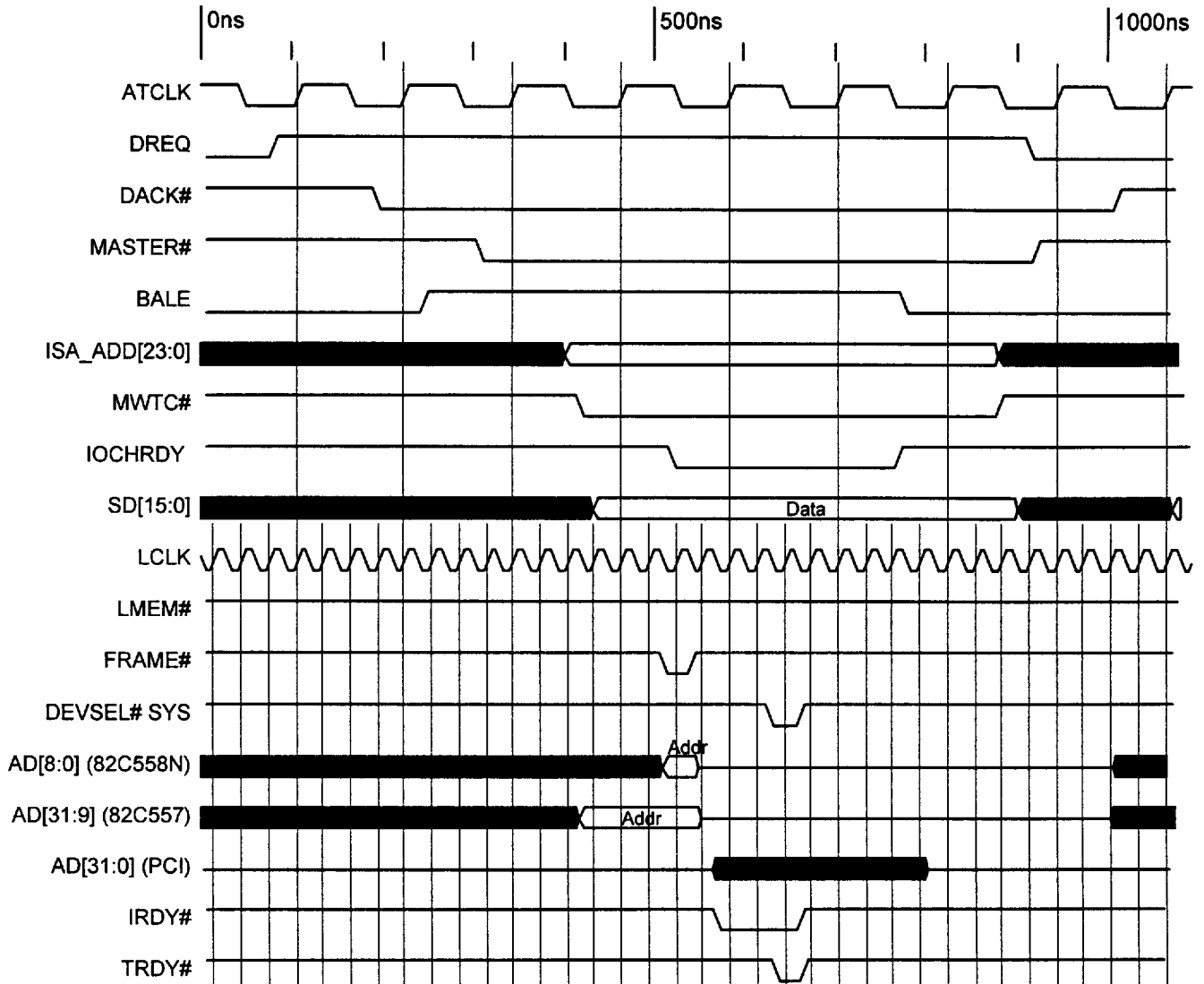


Figure 4-36 ISA Master Write to ISA Slave



4.7 ISA Bus Interface

The ISA bus state machine gains control when the decoding logic of the 82C558N detects that no PCI/VL device has claimed the cycle. It monitors status signals MEMCS16#, IOCS16#, IOCHRDY, and ZEROWS# and performs the necessary synchronization of control and status signals between the ISA bus and the microprocessor. The Viper-N Chipset supports 8- and 16-bit memory and I/O devices located on the ISA bus.

An ISA bus cycle is initiated by asserting BALE in ISA-TS1 state. On the trailing edge of BALE, M16# is sampled for a memory cycle to determine the bus size. It then enters ISA-TC state and provides the command signal. For an I/O cycle, IO16# is sampled after the trailing edge of ALE until the end of the command. The command cycle is extended when IOCHRDY is detected inactive or the cycle is terminated when the zero wait state request signal (ZEROWS#) from the ISA bus is active. Upon expiration of the wait states, the ISA state machine terminates itself and passes internal an READY to the CPU state machine to output a synchronous BRDY# to the CPU. The ISA bus state machine also routes data and address when an ISA bus master or DMA controller accesses system memory.

The delay between back-to-back ISA cycles is programmable and can be configured by programming PCIDV1 43h[3]. See Table 4-38.

4.8 XD Bus Interface

The XD bus is an 8-bit utility that is used to access the 8-bit keyboard controller, BIOS ROM, the real-time clock, and the non-volatile RAM (NVRAM). The XDIR output signal from the 82C558N is used for the XD bus data buffer direction control. A 1 indicates data transfer from the SD bus to the XD bus. Normally high, XDIR is low for the following conditions:

- 1) during BIOS ROM accesses, when ROMCS# and MEMR# are both active

- 2) during reads from I/O Ports 060h, 064h, 070h, and 071h
- 3) during read accesses from the NVRAM

4.9 Bus Arbitration Logic

The 82C557 provides arbitration between the CPU, DMA controller, ISA bus masters, PCI bus masters, and the refresh logic. During DMA, ISA bus master cycles, PCI bus master cycles, and conventional refresh cycles, the 82C557 asserts HOLD to the CPU. The CPU will respond to an active HOLD signal by generating HLDA (after completing its current bus cycle) and placing most of its output and I/O pins in a high impedance state. After the CPU relinquishes the bus, the 82C557 responds by issuing REFRESH# (refresh cycle) or AHOLD (PCI master, ISA bus master, or DMA cycle), depending on the requesting device. During hidden refresh, HOLD remains negated and the CPU continues its current program execution as long as it services internal requests or achieves cache hits.

Refresh cycles, DMA cycles, and master cycles are serviced on a first in-first out (FIFO) priority, but DRAM refresh requests (REFRESH#) are internally latched and serviced immediately after the current DMA or master finishes its request, if the refresh request was queued behind an ISA DMA or master (HREQ) request. The 82C557 now requests the CPU bus by asserting HOLD to the CPU. The CPU will complete the ongoing cycle and when it gives up the CPU bus, it will assert HLDA to the 82C557. The 82C557 will grant the CPU bus to the PCI master, ISA DMA or master and assert AHOLD. The HREQ signal must remain active to be serviced if a refresh request comes first. DMA and bus masters share the same request pin; HREQ. To distinguish between DMA and bus master requests during an active AHOLD period, the AEN signal can be used to distinguish between DMA and master cycles. If AEN is active, then it is a DMA cycle. When these signals are inactive, an external bus master controls the system bus.

Table 4-38 Delay Back-to-Back ISA Cycle Register Bit

7	6	5	4	3	2	1	0
PCIDV1 43h (Part of IRQ Triggering Register) Default = 00h							
Reserved	Enable DMA or ISA master to preempt PCI Master 0 = Disable 1 = Enable	Fixed/rotating priority between PCI masters: 0 = Rotating 1 = Fixed	Back-to-back ISA I/O: 0 = Enable 1 = Disable	Reserved	PCI master access to VL/ISA: 0 = Enable 1 = Disable	ISA bus control signals for memory accesses greater than 16M: 0 = Enable 1 = Disable	

4.10 Data Bus Conversion/Data Path Control Logic

Data bus conversion from the 64-bit CPU bus to the memory bus is done by the 82C556 (based on control signals from the 82C557). The data bus conversion from the higher order MD bus to the AD bus is done by the 82C558N, and the conversion to a 8/16-bit ISA bus is also done by the 82C558N. The 82C557 converts the CPU byte enables BE[7:0]# to address A2 and four byte enable signals C/BE[3:0]#, for the PCI bus, the VL bus, and the 82C558N. The 82C558N uses the C/BE[3:0]#, A2 and the other ISA address (A[1:0], SBHE# and IOCS16#/MEMCS16#) information to complete the 64-bit to 8/16-bit data conversion for the ISA bus. The 82C558N performs data bus conversion when the CPU accesses 16- or 8-bit devices through 16- or 32-bit instructions. It also handles DMA and ISA master cycles that transfer data between local DRAM or cache memory and locations on the ISA bus. The 82C557 provides all of the signals to control external bidirectional data buffers.

4.11 Special Cycles

4.11.1 System ROM BIOS Cycles

The 82C557 supports both 8- and 16-bit EPROM cycles. If the system BIOS is 16 bits wide, ROMCS# should be connected to MEMCS16# through an open collector gate indicating to the 82C558N that a 16-bit EPROM is responding. The system BIOS resides on the XD bus.

ROMCS# can generated for both the E0000h-EFFFFh and F0000h-FFFFFh segments through PCIDV1 4Ah and 4Bh. (Refer to Table 4-39.) If a combined video/system ROM BIOS is desired, these two segments should be used.

4.11.2 System Shutdown/Halt Cycles

The CPU provides special bus cycles to indicate that certain instructions have been executed or certain conditions have occurred internally. These special cycles, such as shutdown and halt, are covered by dedicated handling logic inside the 82C557. The Viper-N Chipset will generate INIT for a CPU shutdown cycle.

Table 4-39 Registers Associated with ROMCS#

7	6	5	4	3	2	1	0
PCIDV1 4Ah							
ROM Chip Select Register							Default = 00h
ROMCS# for segment F8000h-FFFFFh: 0 = Enable 1 = Disable	ROMCS# for segment F0000h-F7FFFh: 0 = Enable 1 = Disable	ROMCS# for segment E8000h-EFFFFh: 0 = Disable 1 = Enable	ROMCS# for segment E0000h-E7FFFh: 0 = Disable 1 = Enable	ROMCS# for segment D8000h-DFFFFh: 0 = Disable 1 = Enable	ROMCS# for segment D0000h-D7FFFh: 0 = Disable 1 = Enable	ROMCS# for segment C8000h-CFFFFh: 0 = Disable 1 = Enable	ROMCS# for segment C0000h-C7FFFh: 0 = Disable 1 = Enable
PCIDV1 4Bh							
ROMCS# for segment FFFF8000h-FFFFFFFh: 0 = Enable 1 = Disable	ROMCS# for segment FFFF0000h-FFFF7FFFh: 0 = Enable 1 = Disable	ROMCS# for segment FFFE8000h-FFFEFFFFh: 0 = Disable 1 = Enable	ROMCS# for segment FFFE0000h-FFFE7FFFh: 0 = Disable 1 = Enable	ROMCS# for segment FFFD8000h-FFFDFFFFh: 0 = Disable 1 = Enable	ROMCS# for segment FFFD0000h-FFFD7FFFh: 0 = Disable 1 = Enable	ROMCS# for segment FFFC8000h-FFFC7FFFh: 0 = Disable 1 = Enable	ROMCS# for segment FFFC0000h-FFFC7FFFh: 0 = Disable 1 = Enable



4.12 Internal Integrated Peripherals Controller

The following subsections give detailed operational information about the 82C558N's internal integrated peripheral controller (IPC) which includes two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 timer/counter and one 74612 memory mapper. It is register-compatible with the 82C206 chip.

For information on the design architecture of this unit, refer to the separate document on the 82C206 IPC. This document is available on request from OPTi.

4.12.1 Hardware Considerations

The 82C558N uses an external multiplexing scheme to read in many of the IRQ, DRQ, and external PMI inputs. The scheme uses the ATCLK and ATCLK/2 outputs to toggle a 74153-type multiplexer through four distinct sampling phases. While the system is active, ATCLK and ATCLK/2 are generated from the OSC input and sample each multiplexer input once every 120ns. During Suspend, if OSC14 is not present the 32KHz signal is used to generate ATCLK and ATCLK/2. Therefore, the inputs are sampled only once every 120µs in this case. If ATCLK and ATCLK/2 are driven low in Suspend, RINGI, SUS/RES#, IRQ1, and IRQ8# are always sampled on RQMX2+RQMX4, RQMX3+RQMX4, RQMX0, and RQMX1, respectively.

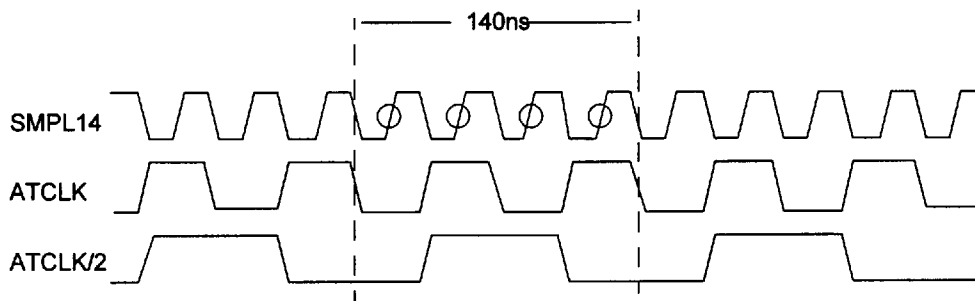
Sampling occurs between multiplexer input switching. For example, when in active mode and running off OSC, ATCLK and ATCLK/2 switch the multiplexer input every 35ns. The chipset samples the state of its input 17.5ns after the multiplexer has switched. Therefore, no "glitching" occurs on sampling. The sampling points are shown in Figure 4-37, where the "SMPL14" signal is a delayed internal version of the OSC input signal.

External peripheral devices that generate IRQs or external PMIs must therefore generate a pulse of sufficient duration to be seen by the sampling logic. The OPTi 82C602A Notebook Companion chip incorporates a latching mechanism to ensure that IRQ inputs that pulse low will be held low for at least one complete ATCLK/ATCLK/2 cycle (140ns or 120µs).

4.12.2 IPC Configuration Programming

The sole configuration register (see Table 4-40) of the internal IPC, separate from those of the 82C558N, is accessed by first writing the register index of interest to I/O Port 022h; the selected register information then becomes available for reading or writing at I/O Port 023h as opposed to Port 024h used by the 82C558N configuration registers

Figure 4-37 Multiplexed Input Sampling Points



82C558N samples multiplexed input four times for every ATCLK/2 cycle

Table 4-40 Internal IPC Configuration Bits.

7	6	5	4	3	2	1	0
Index 01h: IPC Configuration Register							
IPC register access wait states (ATCLKs): 00 = 1 wait states 01 = 2 wait states 10 = 3 wait states 11 = 4 wait states (Default)		16-bit DMA wait states: * 00 = 1 wait state (Default) 01 = 2 wait states 10 = 3 wait states 11 = 4 wait states		8-bit DMA wait states: * 00 = 1 wait state (Default) 01 = 2 wait states 10 = 3 wait states 11 = 4 wait states		Delay DMA MEMR# one clock from system MEMR#: 0 = Yes (AT-compatible - Default) 1 = No	DMA clock select: 0 = ATCLK/2, (Default) 1 = ATCLK

* Note that IOCHRDY can also be asserted by DMA devices to add wait states to DMA cycles.

4.12.3 IPC Register Programming

The IPC provides two peripheral interrupt controllers that are register compatible with the 8259 part. The registers of this logic module are listed below. These registers are accessed directly through the I/O subsystem (no index/data method is used).

4.12.3.1 Initialization Command Words

The Initialization Command Words (ICWs) are shown first and must always be written in sequence starting with ICW1. Two I/O port groups are listed. The first group refers to INTC1, the interrupt controller for IRQ[7:0] (see Table 4-41); the second refers to INTC2, the interrupt controller for IRQ[15:8] (see Table 4-42).

Table 4-41 INTC1 Initialization Command Words

7	6	5	4	3	2	1	0
Port 020h ICW1 (WO)							
Don't care			Always = 1	Trigger mode: 0 = Edge 1 = Level	Don't care	Cascade mode select: 0 = Yes (always), 1 = No	Don't care
Port 021h ICW2 (WO)							
V[7:3] - Upper bits of interrupt vector. For AT compatibility, write 08h.					Not used - lower bits of interrupt vector are generated by interrupt controller.		
Port 021h ICW3 (WO)							
S[7:0] - Slave mode controller connections. For AT compatibility, write 04h (IRQ2).							
Port 021h ICW4 (WO)							
Don't care			Enable multiple interrupts: 0 = No 1 = Yes	Don't care		Enable auto EOI command: 0 = No 1 = Yes	Don't care

Table 4-42 INTC2 Initialization Command Words

7	6	5	4	3	2	1	0
Port 0A0h ICW1 (WO)							
Don't care			Always = 1	Trigger mode: 0 = Edge 1 = Level	Don't care	Cascade mode select: 0 = Yes (always) 1 = No	Don't care
Port 0A1h ICW2 (WO)							
V[7:3] - Upper bits of interrupt vector. For AT compatibility, write 70h.					Not used - lower bits of interrupt vector are generated by interrupt controller.		
Port 0A1h ICW3 (WO)							
Don't care					ID[2:0] - Slave mode address. For AT compatibility, write 02h (IRQ2).		
Port 0A1h ICW4 (WO)							
Don't care			Enable multiple interrupts: 0 = No 1 = Yes	Don't care		Enable auto EOI command: 0 = No 1 = Yes	Don't care



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Enable Multiple Interrupts can be enabled to allow INTC2 to fully nest interrupts without being blocked by INTC1. Correct handling of this mode requires the CPU to issue a non specific EOI command to zero when exiting an interrupt service routine. If the feature is disabled, no command need be issued.

Automatic End-of-Interrupt can be enabled to allow the interrupt controller to generate a non specific EOI command on the trailing edge of the second interrupt acknowledge cycle from the CPU. The feature allows the interrupt currently in service to be cleared automatically on exit from the service

routine. This function should not be used with fully nested interrupts except by INTC1.

4.12.3.2 Operational Command Words

The Operational Command Words are used to program the interrupt controller during the course of normal operation. Two I/O port addresses are listed for each register. The first address refers to INTC1, the interrupt controller for IRQ[7:0]; the second refers to INTC2, the interrupt controller for IRQ[15:8].

Table 4-43 INTC1 and INTC2 Operational Command Words.

7	6	5	4	3	2	1	0
Port 021h, 0A1h OCW1 Mask Register							
IRQ7/15: 0 = Enable 1 = Mask	IRQ6/14: 0 = Enable 1 = Mask	IRQ5/13: 0 = Enable 1 = Mask	IRQ4/12: 0 = Enable 1 = Mask	IRQ3/11: 0 = Enable 1 = Mask	IRQ2/10: 0 = Enable 1 = Mask	IRQ1/9: 0 = Enable 1 = Mask	IRQ0/8: 0 = Enable 1 = Mask
Port 020h, 0A0h OCW2 Command Register (WO)							
000 = Disable auto-rotate, auto EOI mode 100 = Enable auto-rotate, auto EOI mode 001 = Generate non-specific EOI 011 = Generate specific EOI 101 = Rotate on non-specific EOI 111 = Rotate on specific EOI 110 = Set priority 010 = No operation			Always = 0 for OCW2	Always = 0 for OCW2	L[2:0]: Interrupt level acted on by "set priority" and "rotate of specific EOI"		
Port 020h, 0A0h OCW3 Command Register (WO)							
Always = 0	Allow bit 5 changes: 0 = No 1 = Yes	Special mask mode: 0 = Disable 1 = Enable	Always = 0 for OCW3	Always = 1 for OCW3	Polled mode: 0 = Disable (generate interrupt) 1 = Enable (poll 020/0A0h for interrupt)	Allow bit 0 changes: 0 = No 1 = Yes	In-service access: 0 = 020/0A0h reads return IRR 1 = Return ISR
Port 020h, 0A0h Interrupt Request Register OCW3[0] = 0 (RO)							
IRQ7/15 pending: 0 = No 1 = Yes	IRQ6/14 pending: 0 = No 1 = Yes	IRQ5/13 pending: 0 = No 1 = Yes	IRQ4/12 pending: 0 = No 1 = Yes	IRQ3/11 pending: 0 = No 1 = Yes	IRQ2/10 pending: 0 = No 1 = Yes	IRQ1/9 pending: 0 = No 1 = Yes	IRQ0/8 pending: 0 = No 1 = Yes
Port 020h, 0A0h In-Service Register OCW3[0] = 1 (RO)							
IRQ7/15 in service: 0 = No 1 = Yes	IRQ6/14 in service: 0 = No 1 = Yes	IRQ5/13 in service: 0 = No 1 = Yes	IRQ4/12 in service: 0 = No 1 = Yes	IRQ3/11 in service: 0 = No 1 = Yes	IRQ2/10 in service: 0 = No 1 = Yes	IRQ1/9 in service: 0 = No 1 = Yes	IRQ0/8 in service: 0 = No 1 = Yes
Port 020h, 0A0h Polled Mode Register OCW3[2] = 1 (RO)							
Interrupt pending: 0 = No 1 = Yes	Not used				IRQ[2:0]: Number of highest priority interrupt that is pending		



4.12.3.3 Interrupt Controller Shadow Registers

Values written to the interrupt controller are not always directly readable in the AT architecture. However, the 82C558N shadows these values as they are written so that they can be read back later through the configuration registers. Table 4-44 lists the correspondence of shadow indexes to the write-only registers in the interrupt controllers.

4.12.4 DMA Controller Programming Registers

The integrated IPC provides two direct memory access controllers (DMAC1 and DMAC2) and their associated memory mappers that are register compatible with AT-type systems. The registers of this logic module are listed below. These registers are accessed directly through the I/O subsystem (no index/data method is used). Each DMAC has four DMA channels. Channels 3 through 0 are in DMAC1 and Channels 7 through 4 are in DMAC2. Table 4-45 and Table 4-46 list the register locations.

Table 4-44 Interrupt Controller Shadow Register Index Values

Register	INTC1 Index	INTC2 Index
ICW1	80h	88h
ICW2	81h	89h
ICW3	82h	8Ah
ICW4	83h	8Bh
OCW2	85h	8Dh
OCW3	86h	8Eh

Table 4-45 DMA Address and Count Registers

Name	DMA Channel Address							
	0	1	2	3	4	5	6	7
Memory Address Register	000h R/W	002h R/W	004h R/W	006h R/W	0C0h R/W	0C4h R/W	0C8h R/W	0CCh R/W
Count Register	001h R/W	003h R/W	005h R/W	007h R/W	0C2h R/W	0C6h R/W	0CAh R/W	0CEh R/W
Page Address Register	087h R/W	083h R/W	081h R/W	082h R/W	08Fh R/W	08Bh R/W	089h R/W	08Ah R/W

Table 4-46 DMA Control and Status Registers

Command	Function	Command Port Address	
		DMA Channels 7-5	DMA Channels 3-0
Mode Register	Sets the function type for each channel. Group can be read back - see "Reset Mode Register Readback Counter" command.	Read/Write 0D6h	Read/Write 00Bh
Status Register	Returns channel request and terminal count information.	Read 0D0h	Read 008h
Command Register	Sets the DMAC configuration.	Write 0D0h, Read 0D4h	Write 008h, Read 00Ah
Request Register	Makes a software DMA request.	Read/Write 0D2h	Read/Write 009h
Mask Register	Enables or masks DMA transfers on selected channels.	Read/Write 0DEh	Read/Write 00Fh
Temporary Register	Not used in AT-compatible design.	Read 0DAh	Read 00Dh



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Table 4-47 DMAC1 Control and Status Bits

7	6	5	4	3	2	1	0
Port 008h DMAC1 Status Register							
Ch. 3 request pending: 0 = No 1 = Yes	Ch. 2 request pending: 0 = No 1 = Yes	Ch. 1 request pending: 0 = No 1 = Yes	Ch. 0 request pending: 0 = No 1 = Yes	Ch. 3 reached terminal count: 0 = No 1 = Yes	Ch. 2 reached terminal count: 0 = No 1 = Yes	Ch. 1 reached terminal count: 0 = No 1 = Yes	Ch. 0 reached terminal count: 0 = No 1 = Yes
Port 00Bh DMAC1 Mode Register							
Mode select: 00 = Demand 01 = Single		Address count: 0 = Increment 1 = Decrement		Auto-initialize: 0 = Disable 1 = Enable		Transfer select: 00 = Verify 01 = Mem. write	
10 = Block 11 = Cascade				10 = Mem. read 11 = Reserved		Channel select: 00 = Ch. 0 01 = Ch. 1 10 = Ch. 2 11 = Ch. 3	
Port 009h DMAC1, DMA Request Register							
Reserved: Write as 0.				Request: 0 = Clear 1 = Set		Channel select: 00 = Ch. 0 01 = Ch. 1 10 = Ch. 2 11 = Ch. 3	
Port 008h DMAC1 Command Register							
DACK active sense: 0 = Low 1 = High	DRQ active sense: 0 = High 1 = Low	Extended write: 0 = Disable 1 = Enable	Rotating priority: 0 = Disable 1 = Enable	Compressed timing: 0 = Disable 1 = Enable	DMAC operation: 0 = Enable 1 = Disable	Channel 0 address hold: 0 = Disable 1 = Enable	Memory-to-memory 0 = Disable 1 = Enable
Port 00Fh DMAC1 Mask Register							
Reserved: Write as 0.				Channel 3: 0 = Unmasked 1 = Masked	Channel 2: 0 = Unmasked 1 = Masked	Channel 1: 0 = Unmasked 1 = Masked	Channel 0: 0 = Unmasked 1 = Masked

Table 4-48 DMAC2 Control and Status Bits

7	6	5	4	3	2	1	0
Port 0D0h DMAC2 Status Register							
Ch. 7 request pending: 0 = No 1 = Yes	Ch. 6 request pending: 0 = No 1 = Yes	Ch. 5 request pending: 0 = No 1 = Yes	Ch. 4 request pending: 0 = No 1 = Yes	Ch. 7 reached terminal count: 0 = No 1 = Yes	Ch. 6 reached terminal count: 0 = No 1 = Yes	Ch. 5 reached terminal count: 0 = No 1 = Yes	Ch. 4 reached terminal count: 0 = No 1 = Yes
Port 0D6h DMAC2 Mode Register							
Mode select: 00 = Demand 01 = Single 10 = Block 11 = Cascade		Address count: 0 = Increment 1 = Decrement	Auto-initialize: 0 = Disable 1 = Enable	Transfer select: 00 = Verify 10 = Mem. read 01 = Mem. write 11 = Reserved		Channel select: 00 = Ch. 4 10 = Ch. 6 01 = Ch. 5 11 = Ch. 7	
Port 0D2h DMAC2 DMA Request Register							
Reserved: Write as 0.				Request: 0 = Clear 1 = Set	Channel Select: 00 = Ch. 4 10 = Ch. 6 01 = Ch. 5 11 = Ch. 7		
Port 0D0h DMAC2 Command Register							
DACK active sense: 0 = Low 1 = High	DRQ active sense: 0 = High 1 = Low	Extended write: 0 = Disable 1 = Enable	Rotating priority: 0 = Disable 1 = Enable	Compressed timing: 0 = Disable 1 = Enable	DMAC operation: 0 = Enable 1 = Disable	Channel 0 address hold: 0 = Disable 1 = Enable	Memory-to-memory: 0 = Disable 1 = Enable
Port 0DEh DMAC2 Mask Register							
Reserved: Write as 0.				Channel 7: 0 = Unmasked 1 = Masked	Channel 6: 0 = Unmasked 1 = Masked	Channel 5: 0 = Unmasked 1 = Masked	Channel 4: 0 = Unmasked 1 = Masked

Table 4-49 DMA Commands

Command	Function	Command Port Address	
		DMA Channels 7-5	DMA Channels 3-0
Set Single Mask Bits Register	Sets or clears individual mask register bits without having to do a read/modify/write of the Mask Register.	Write 0D4h: Bits [1:0] select the channel, bit 2 selects the new mask bit value.	Write 00Ah: Bits [1:0] select the channel, bit 2 selects the new mask bit value.
Clear Mask	Unmasks all DMA channels at once.	Write any value to 0DCh.	Write any value to 00Eh.
Reset Mode Register Readback Counter	Resets the Mode Register readback function to start at register 0. The next four Mode Register reads then return Channels 0, 1, 2, and 3 for that DMAC.	Read 0DCh (then read 0D6h four times to get the Mode Register values).	Read 00Eh (then read 00Bh four times to get the Mode Register values).
Master Clear	Clears all values, masks all channels, just like a hardware reset.	Write any value to 0DAh.	Write any value to 00Dh.
Clear Byte Pointer Flip-Flop	Resets the byte pointer flip-flop so that the next byte access to a word-wide DMA register is to the low byte.	Write any value to 0D8h.	Write any value to 00Ch.
Set Byte Pointer Flip-Flop	Sets the byte pointer flip-flop so that the next byte access to a word-wide DMA register is to the high byte.	Read 0D8h.	Read 00Ch.



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4.12.5 Timer Programming Registers

The integrated IPC provides an 8254-type timer with three channels that is register compatible with AT-type systems. The registers of this logic module are listed below. These reg-

isters are accessed directly through the I/O subsystem (no index/data method is used). Table 4-50 lists the register locations.

Table 4-50 Timer Control and Status Registers

Name	Function	Port Address Timer		
		Channel 0	Channel 1	Channel 2
Counter Registers Access	Used to write and read the word-wide count. Writes always program the base value. Reads return either the instantaneous count value or the latched count value.	040h	041h	042h
Counter Mode Command	Selects the operational mode for each timer counter.	Write 043h		
Counter Latch Command	Latches the count from the selected register for reading at the associated counter register access port.	Write 043h then read 040h, 041h, and/or 042h		
Readback Command	Selects whether count or status, or both, will be latched for subsequent reading at the associated counter register access port. If both are selected, status is returned first. This command can latch information from more than one counter at a time.	Write 043h then read 040h, 041h, and/or 042h		

Table 4-51 Timer Control Bits

7	6	5	4	3	2	1	0
Port 043h Counter Mode Command (WO)							
Counter select: 00 = Counter 0 01 = Counter 1 10 = Counter 2 11 = Readback command (see below)		Counter access: 00 = Counter latch command (see below) 01 = R/W LSB only 10 = R/W MSB only 11 = R/W LSB followed by MSB		Mode select: 000 = M0) Interrupt on terminal count 001 = M1) Hardware retrig. one-shot X10 = M2) Rate generator X11 = M3) Square wave generator 100 = M4) Software-triggered strobe 101 = M5) Hardware-triggered strobe			Count mode select: 0 = 16-bit binary 1 = 4-decade BCD
Port 043h Counter Latch Command (WO)							
Counter select: 00 = Counter 0 01 = Counter 1 10 = Counter 2 11 = Illegal		Counter latch command = 00		Don't care			
Port 043h Readback Command (WO)							
Readback command = 11		Latch count: 0 = Yes 1 = No	Latch status: 0 = Yes 1 = No	Counter 2 select: 0 = Yes 1 = No	Counter 1 select: 0 = Yes 1 = No	Counter 0 select: 0 = Yes 1 = No	Reserved: Write as 0.
Port 043h Status Byte (RO)							
OUT signal status	Null count, counter contents valid: 0 = Yes 1 = No (being updated)	Return bits [5:0] written in Counter Mode Command (see above)					



4.12.5.1 Shadow Registers To Support Timer

Values written to the timer are not always directly readable in the AT architecture. However, the 82C558N shadows these values as they are written so that they can be read back later through the configuration registers. The values from index

90h to 96h are valid only when a Counter Mode Command byte for the counter has been written to the timer register at I/O Port 043h. Setting bits 043h[5:4] = 11 starts the sequence.

Table 4-52 Timer Support Shadow Registers

7	6	5	4	3	2	1	0
Index 90h Channel 0 Low Byte Timer Channel 0 count low byte, A[7:0]							
Index 91h Channel 0 High Byte Timer Channel 0 count high byte, A[15:8]							
Index 92h Channel 1 Low Byte Timer Channel 1 count low byte, A[7:0]							
Index 93h Channel 1 High Byte Timer Channel 1 count high byte, A[15:8]							
Index 94h Channel 2 Low Byte Timer Channel 2 count low byte, A[7:0]							
Index 95h Channel 2 High Byte Timer Channel 2 count high byte, A[15:8]							
Index 96h Write Counter High/Low Byte Latch							
Unused	Ch. 2 read LSB toggle bit	Ch. 1 read LSB toggle bit	Ch. 0 read LSB toggle bit	Ch. 2 write LSB toggle bit	Ch. 1 write LSB toggle bit	Ch. 0 write LSB toggle bit	



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4.12.6 Writing/Reading I/O Port 070h

The AT architecture does not allow the readback of the NMI enable bit settings and the RTC index value written at I/O Port 070h. However, the 82C558N logic makes the NMI Enable bit setting, along with the last RTC index value written to I/O Port 070h, available for reading in its shadow register set.

4.12.6.1 RTC Index Shadow Register

This shadow register is read as a normal 82C558N configuration register: write 98h to I/O Port 022h followed immediately by an I/O read at I/O Port 024h.

4.12.7 IRQ8 Polarity

The recognition of the IRQ8 interrupt can be inverted through bit 50h[5]. In the normal AT architecture, IRQ8 is active low and driven by an open-collector output of the RTC against a pull-up resistor.

Table 4-53 RTC Index Register - I/O Port 070h (WO)

7	6	5	4	3	2	1	0
RTC/CMOS RAM Index							
NMI Enable: 0 = Disable 1 = Enable							

Table 4-54 RTC Index Shadow Register - Index 98h (RO)

7	6	5	4	3	2	1	0
CMOS RAM Index Last Written							
NMI Enable Setting							

Table 4-55 IRQ8 Polarity Bit - SYSCFG 50h

7	6	5	4	3	2	1	0
SYSCFG 50h PMU Control Register 4 Default = 00h							
Software start SMI: 0 = Clear SMI 1 = Start SMI	Reserved	IRQ8 polarity: 0 = Active low 1 = Active high	14.3MHz to 82C558N: 0 = Enable 1 = Disable	Write = 1 to start Doze Read: Doze status 0 = Counting 1 = Timed out	Ready to Resume (RO): 0 = Not in Resume 1 = Ready to Resume	PMU mode (RO): 0 = Nothing pending 1 = Suspend active (clear PMI #6)	Start Suspend (WO): 1 = Enter Suspend mode

4.12.8 Fast GATEA20 and Reset Emulation

The 82C557 will intercept commands to Ports 060h and 064h so that it can emulate the keyboard controller, allowing the generation of the fast GATEA20 and fast INIT signals. The decode sequence is software transparent and requires no BIOS modifications to function. The fast GATEA20 generation sequence involves writing "D1h" to Port 064h, then writing data "02h" to Port 060h. The fast CPU "warm reset" function is generated when a Port 064h write cycle with data "FEh" is decoded. A write to Port 064h with data "D0h" will enable the status of GATEA20 (bit 1 of Port 060h) and the warm reset (bit 0 of Port 060h) to be readable.

If keyboard emulation has been disabled (PCIDV1 41h[4] = 1), the 82C558N will still intercept reset and GATEA20 commands to Port 092h and generate INIT to the CPU. However, the 82C558N has to be programmed to accept the KBRST# and KBA20M signals from the keyboard controller to generate INIT and A20M# to the CPU because it will not intercept Port 060/064h commands. Figure 4-38 shows the connectivity when keyboard emulation has been disabled.

Figure 4-38 Connections with Keyboard Emulation Disabled

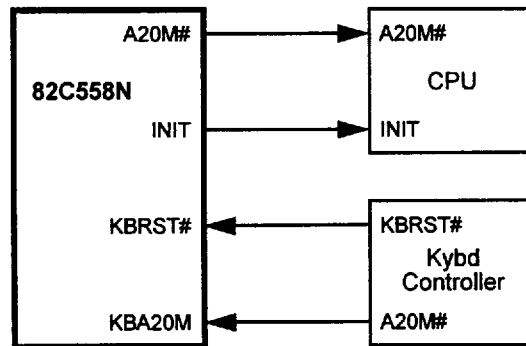


Table 4-56 Keyboard Emulation Disable Bit

7	6	5	4	3	2	1	0
PCIDV1 40h							
PCI IRQ Select Register							
Default = 00h							
P2IRQ[1:0]:		P1IRQ[2:0]:			P0IRQ[2:0]:		
Works with P2IRQ[2] to select which IRQ signal is generated when PCI interrupt request PCIRQ2# has been triggered: Refer to P3IRQ[2:0] for decode.		Selects which IRQ signal is generated when PCI interrupt request PCIRQ1# has been triggered: Refer to P3IRQ[2:0] for decode.			Selects which IRQ signal is generated when PCI interrupt request PCIRQ0# has been triggered: Refer to P3IRQ[2:0] for decode.		
PCIDV1 41h							
Default = 00h							
RDKBDPRT (RO):	WRKBDPRT (RO):	IMMINIT:	KBDEMU:	P3IRQ[2:0]:		P2IRQ[2]:	
Keyboard controller has received Command D0h and has not received the following 60h read.	Keyboard controller has received Command D1h and has not received the following 60h write.	Generate INIT immediately on FEh Command. 0 = Generate INIT immediately on FEh Command 1 = Wait for halt before INIT for keyboard reset	Keyboard emulation 0 = Enable 1 = Disable	Selects which IRQ signal is generated when PCI interrupt request PCIRQ3# has been triggered: 000 = Disabled 100 = IRQ11 001 = IRQ5 101 = IRQ12 010 = IRQ9 110 = IRQ14 011 = IRQ10 111 = IRQ15		Works with P2IRQ[1:0] to select which IRQ signal is generated when PCI interrupt request PCIRQ2# has been triggered:	



4.13 Integrated Local Bus Enhanced IDE Interface

Enhanced IDE support through the local bus is available on the 82C558N as a register programmable option. The proven OPTi 82C611 core logic is used to incorporate this option. Drivers used to control the 82C611 device can be used with the 82C558N. Refer to the documentation on the 82C611 controller for special register programming information. Note, however, that the write posting and read prefetching features of the separate 82C611 are not supported by the 82C558N.

4.13.1 Hardware Considerations

Local bus IDE support requires seven pins. Six of the signals are shared signals that also go to their active state (from the perspective of the IDE) during non-IDE cycles. Therefore, these signals must be qualified by DBE#; they cannot be connected directly to the IDE interface. The signals are defined as follows:

- HDRD#, Drive Read - Provides the read strobe signal for the IDE drive; also switches the data buffer direction toward the SD bus during read cycles. The 82C558N drives HDRD# on the SA4 line.
- HDWR#, Drive Write - Provides the write strobe signal for the IDE drive. The 82C558N drives DWR# on the SA3 line.
- HDA[2:0], Drive Address Lines 2:0 - Provided directly from the 82C558N SA[2:0] signals.
- HDCS1#, Drive Chip Select - Provides a stable version of SA9 for decoding. The 82C558N drives HDCS1# on the SA5 line.
- DBE#, Drive Buffer Enable - Enables the buffer for control lines HDRD#, HDWR#, HDCS1#, and HDA[2:0] to the IDE drive, as well as the data bus buffers.

The HDRD# and HDWR# signals and the other control signals are separated from the standard ISA bus I/O control signals to avoid the incompatibility that can occur when signals such as IOR# and IOW# are "short pulsed" as they would be for an IDE cycle. Short pulses on these lines can cause incorrect operation on some slower ISA peripheral devices, even if the read and write is not intended for those devices.

4.13.2 Performance and Power

Enhanced IDE uses the SD bus for its data transfers, but does not have to use slow ISA bus transfers because of its dedicated HDRD#, HDWR#, and DBE# signals. Essentially, the local bus IDE controller can run extremely short ISA-type cycles because all timing aspects of the cycle are directly programmable to meet the capabilities of the drive being used.

The Viper-N Chipset implementation of local bus IDE is designed to save power. The buffers to/from the IDE are tristated between cycles. Therefore, no power is wasted toggling the IDE data lines when the IDE is not in use.

An innovative method is used to handle Port 3F7h[7] from the external floppy controller. Bit 7 from the FDC must be attached to bits [6:0] from the IDE controller whenever an I/O read of Port 3F7h takes place, and normally requires a separate IDED7 line from the IDE. Two separate cycles occur whenever the an I/O read from Port 3F7h takes place. First, the local bus IDE cycle is run using HDRD# and DBE#. Then an ISA bus I/O cycle is run. When the Chipset returns a value to the CPU, it provides bits [6:0] read from the IDE and bit 7 from the ISA bus.

4.13.3 Signal Connection

The various ISA bus signals that are used for IDE command and chip select lines are signals that would normally require qualification by other signals; toggled by themselves, they should not cause any action or conflicts on the ISA bus.

4.13.4 Programming

The IDE interface is programmed through the bits shown in Table 4-57. Once set, the interface is enabled by writing SYSCFG ACh[3] = 1. Bit 3 defaults to 0 at power-up.

Table 4-57 IDE Interface Control

7	6	5	4	3	2	1	0
SYSCFG ACh IDE Interface Configuration Register							
Default = 00h							
LCLK frequency: 00 = Rsvd 01 = 33 MHz 10 = 25MHz 11 = 16MHz		IDE command pulse duration: 00 = 600ns 01 = 383ns 10 = 240ns 11 = 180ns		IDE interface enable: 0 = Disable 1 = Enable	IDE port address select: 0 = 1F0-7h, 3F6-7h 1 = 170-7h, 376-7h	3F7h[6:0] source: 0 = Local IDE 1 = ISA bus	IDE clock source: 0 = OSC 1 = LCLK

Notes: IDE Clock Source: The IDE controller needs a clock to generate the signals. This timing information may be derived from the OSC input to the 82C558N or the LCLK input. If set to 1, bits 7 and 6 specify LCLK frequency.

LCLK Frequency Bits, SYSCFG ACh[7:6]: The IDE controller uses this value to precisely calculate signal timing.

IDE Interface Enable Bit, SYSCFG ACh[3]: When this bit is set, the integrated IDE controller generates the control signals for the IDE interface on the SA[5:0] lines. When disabled, the 82C558N passes the IDE cycles to the ISA bus if the cycles were not already claimed on the PCI bus.

Port 3F7h Decode Disable Bit, SYSCFG ACh[1]: Prevents Port 3F7h reads from being combined with IDE controller reads in situations where this arrangement causes problems. When ACh[1] = 0, Port 3F7h[7] comes from the ISA bus; Port 3F7h[6:0] (or Port 377h[6:0] if bit 2 = 1) comes from local bus IDE. When ACh[1] = 1, Port 3F7h[7:0] comes from the ISA bus.

The setting in SYSCFG ACh[7:4] will select cycle timings according to the following scheme.

Table 4-58 Automatic Cycle Settings Available through SYSCGF ACh[7:4]

SYSCFG ACh[7:4]	Expected Input Clock Frequency (MHz)	Setup Time (Clocks)	Command Pulse (Clocks)	Recovery Time (Clocks)	Maximum Cycle Time (Clocks)
0100	33	3	6	11	20
0101		2	5	6	13
0110		2	4	2	8
0111		1	3	2	6
8-bit		--	10	9	20
1000	25	2	5	8	15
1001		2	4	4	10
1010		1	3	2	6
1011		1	2	2	5
8-bit		--	8	6	15
1100	16	2	3	5	10
1101		1	3	3	7
1110		1	2	2	5
1111		1	2	2	5
8-bit		--	5	4	10



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4.13.4.1 Precise Programming Method (Enhanced)

More precise control of IDE operation is available by using the "611" register set, so called because it is register-compatible with the register set used in OPTi's 82C611 stand-alone

local bus IDE controller. This register set is hidden behind the IDE drive I/O ports and is not normally accessible.

Table 4-59 611 Register Set

7	6	5	4	3	2	1	0
Port 1F0h/170h Read Cycle Timing Register							
Read pulse width: The value written to these bits, plus one, selects the DRD# pulse width for a read from the 16-bit data register.*				Read recovery time: The value written to these bits, plus two, determines the minimum time allowed between the end of DRD# and the start of the next IDE chip select (HDCS[1:0]#, derived from TC).*			
Port 1F1h/171h Write Cycle Timing Register							
Write pulse width: The value written to these bits, plus one, selects the DWR# pulse width for a write to the 16-bit data register.*				Write recovery time: The value written to these bits, plus two, determines the minimum time allowed between the end of DWR# and the start of the next IDE chip select (HDCS[1:0]#, derived from TC).*			
Port 1F2h/172h ID Register (WO)							
82C611 register access: 0X = Enable 10 = Two 1F1/171h reads to enable (default) 11 = Permanently disable		Reserved: Write as 0.			ID bits: These bits must always be written as 11.		
Port 1F3h/173h Control Register 1							
Timing register value select: 0 = Basic 1 = Enhanced	Reserved: Write as 0.		Drive 1 timing select: Basic 0 = ACh[5:4] 1 = Timing 0 Enhanced 0 = Timing 1 1 = Timing 0	Drive 0 timing select: Basic 0 = ACh[5:4] 1 = Timing 0 Enhanced 0 = Timing 1 1 = Timing 0	Reserved: Write as 0.	IDE operation: 0 = Disable 1 = Enable	
Port 1F5h/175h Status Register (RO)							
ISA 3F7h[7] status	Revision number: Returns 00 on present silicon revision.	IRQ14 status	SYSCFG ACh[5:4] setting	SYSCFG ACh[7:6] setting			
Port 1F6h/176h Status Register (RO)							
Secondary setup and hold timing register	Reserved: Write as 0.	Address setup time: The value written, plus one, selects the address setup time.*	Channel ready hold time: The value written, plus two, selects the delay for setting the command pulse inactive from when the controller sees IOCHRDY go high.*	Timing register load select: 0 = Timing 0 1 = Timing 1			

* The value indicates the width in terms of FBCLKIN cycles.



4.13.4.1.1 Timing 0 and Timing 1

The 611 register set supports two separate IDE drives on a single cable with independent timing requirements. Application software writes Port 1F6h[4] or 176h[4] to select between Drive 0 and 1 on the cable. The 611 core tracks writes to this I/O port and switches its timing. The correspondence is not necessarily direct, however, between Drive 0 and Timing 0, for example. Each drive can select its timing from two sources, which are themselves selectable according to Port 1F3/173h[7].

“Basic” choices when Port 1F3/173h[7] = 0:

1. The “easy method” timings from SYSCFG ACh[7:4].
2. Timing 0.

“Enhanced” choices when Port 1F3/173h[7] = 1:

1. Timing 1
2. Timing 0.

The basic or enhanced timing choices are made as follows. Internal to the 82C558N, there is a single 611 register set. The 611 registers are available only when enabled through a special unlocking procedure. Timing choices are made according to Table 4-60 and Table 4-61 through Ports 1F3/173h[3:2] for Drives 0 and 1, respectively. Once all programming is complete, the 611 register set again becomes hidden. From then on, accesses to the IDE Port 1F6/176h[4] are tracked to determine the timing to use.

4.13.4.1.2 Subset Registers for Timing 0 and 1

Within the single 611 register set, there are two subsets of registers to program the read pulse width, write pulse width,

read recovery time, and write recovery time separately for Timing 0 and Timing 1. The register set loaded by writing to 1F0/1h or 170/1h is selected by 1F6/176h[0]. Setting this bit to 0 allows writes to 1F0/1h or 170/1h to program Timing 0; setting the bit to 1 allows programming of Timing 1.

4.13.4.1.3 Step-by-Step Programming Procedure

Each phase of 611 programming is described below. Before accessing the 611 register set, the basic interface must be set up as follows.

1. Enable the external IDE controller interface by setting SYSCFG ACh[3] = 1.
2. Select the I/O range to be used through SYSCFG ACh[2]. For the purposes of this example, SYSCFG ACh[2] is set to 0 to select the 1F0-7h and 3F6-7h range. If the 170-7h and 376-7h range is selected instead, use the x7x port instead of the xFx port for each of the following steps.
3. Use SYSCFG ACh[1] to select whether 3F7h accesses will be directed to the IDE drive. If enabled, only bits [6:0] will come from the local bus IDE interface; bit 7 always comes from the ISA bus because it belongs to the floppy disk controller (if present).

The basic IDE interface is now available. SYSCFG ACh[7:4] can be used to select the fixed timings listed above. If these fixed timings are sufficient, there is no need to use the 611 register set.

Table 4-60 Operation with Primary I/O Range Selected

SYSCFG ACh[2]	I/O Range	SA7 Value	IDE Drive Setting (IDE Head/Drive Select Register)	Drive Selected	Timing Selected by Hidden 611 Register
0	Primary 1F0-7h, 3F6-7h	1	1F6h[4] = 0	0	1F3h[2]
			1F6h[4] = 1	1	1F3h[3]

Table 4-61 Operation with Secondary I/O Range Selected

SYSCFG ACh[2]	I/O Range	SA7 Value	IDE Drive Setting (IDE Head/Drive Select Register)	Drive Selected	Timing Selected by Hidden 611 Register
1	Secondary 170-7h, 376-7h	0	176h[4] = 0	0	173h[2]
			176h[4] = 1	1	173h[3]



4.13.4.1.4 Enabling Access to 611 Register Set

The 611 register set must be enabled through a very specific procedure.

1. Perform a word read of 1F1h two times. This operation makes the 611 register set accessible for the next I/O operation.
2. Write 00000011b (03h) to Port 1F2h. This programming keeps the 611 registers accessible indefinitely.

The 611 register set is now accessible. No IDE operation can take place as long as the register set access is enabled.

4.13.4.1.5 Setting Up Enhanced 611 Timing

Once the 611 register set is unlocked, Timing 0 and Timing 1 can be programmed.

1. Write 1F6h[0] = 0 to be able to program Timing 0.
2. Program the upper and lower nibbles of 1F0h and 1F1h with the correct values for Timing 0. The read and write pulse widths can be independently programmed to be as short as one clock, while the recovery time for these cycles can be as short as two clocks.
3. Write 1F6h[0] = 1 to be able to program Timing 1.
4. Program 1F0h and 1F1h with the correct values for Timing 1.
5. Write 1F6h[5:1] set to select the required address setup time and IOCHRDY recovery time. These values apply to both Timing 0 and Timing 1. Bit 0 can be left in any state.

The timing sets are now programmed. The next step is to assign one of the timing sets to each drive.

4.13.4.1.6 Associating Timing with Each Drive

Port 1F3h selects timing options for the drives, and is the last step necessary before "hiding" the 611 register set and enabling 611 operation. Prepare a programming byte in which:

1. Bit 7 = 1 to enable enhanced timing, thus allowing both drives to select between the precise timing sets Timing 0 and Timing 1.
2. Bit 2 selects Timing 0 or Timing 1 for Drive 0, and bit 3 does the same for Drive 1.
3. Bit 0 = 1 to enable all of the programming established to this point.

Set all other bits to 0, and write this value to 1F3h.

4.13.4.1.7 Enabling IDE Operation and Hiding 611 Register Set

The 611 register set must be hidden from standard access before IDE operation can begin. Two options are available.

- Write 1F2h with 11000011b (C3h) to disable 611 register access and fully enable IDE operation, and also prevent any future access to the 611 register set until the next hardware reset.
- Write 1F2h with 10000011b (83h) to disable 611 register access and fully enable IDE operation, but leave open the future possibility of accessing the 611 register set by restarting this whole procedure.

Application software can now control the drive selection and the timing with which it will be accessed through Port 1F6h[4].

4.14 Power Management

The synergistic incorporation of power management and system control features with the standard AT-subsystem controller of the 82C558N results in a compact design that handles multiple tasks with a simple, common interface. The power management unit (PMU) of the 82C558N is based on the implementation in the 82C465MV and is designed to be register compatible for easy upgrading. The following subsections detail the operation of the PMU.

- The power management interrupt (PMI) scheme provides system management code with a quick means of identifying and handling events that affect power control and consumption.
- Recognizes 33 separate PMI events. Within these events, many sub-events are also unidentifiable for a high degree of power management monitoring intelligence.
- Eleven of the PMI events have individual timers to indicate inactivity time-out situations.
- Eight external inputs are available for monitoring asynchronous system events. These are in addition to the ISA-compatible IRQ lines that can also be monitored as power management events.
- PMI generation on access allows SMI code to intercept status queries to powered down devices that do not actually need to be restarted simply to return an "idle" status.
- An activity tracking register of ten events allows SMI or non-SMI applications a means of determining whether

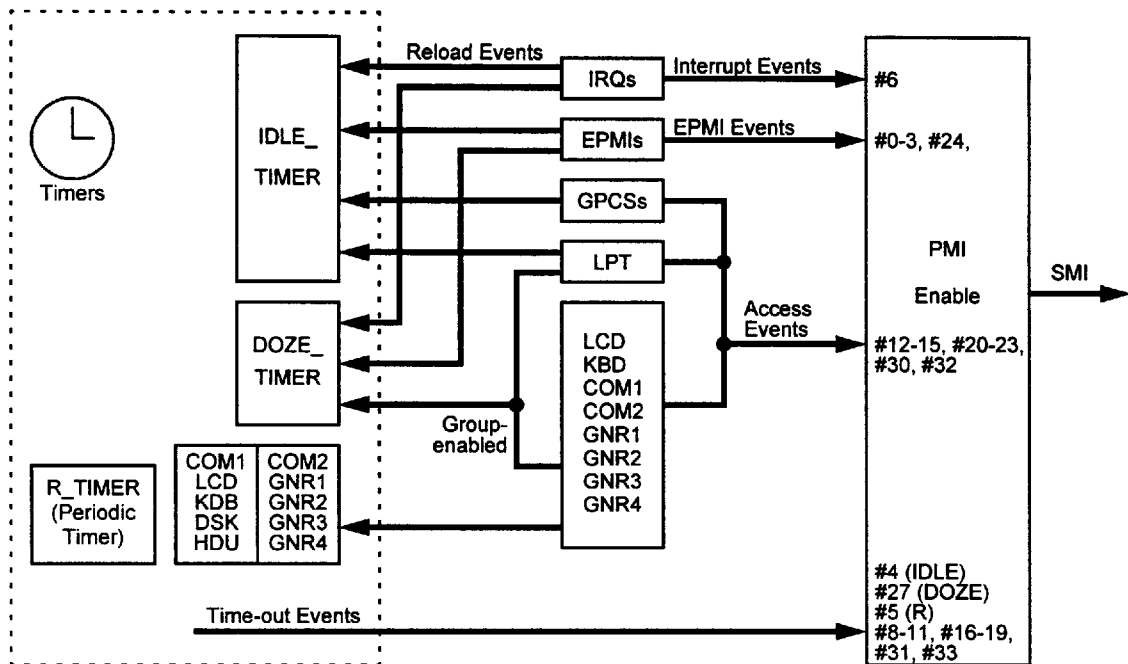
activity has occurred since the last time the register was checked. Polling of I/O activity can then be used instead of multiple SMIs for less significant events.

- Memory watchdog monitoring allows accesses to memory ranges (specified as programmed) to cause an SMI. ISA bus memory devices that are not being accessed can be programmed to cause a time-out SMI so that unused peripherals can be powered down.
- Supports system-level low power Suspend, low power Suspend with zero volt CPU Suspend, or total system zero volt Suspend.
- 16 peripheral power control pins provide exceptional flexibility in peripheral device control.
- Real-time clock (RTC) alarm or modem ring can wake-up the system from the low power Suspend mode.
- Suspend current leakage control ensures that negligible power will be consumed in Suspend mode without additional external buffering.

4.14.1 Power Management Unit (PMU)

The 82C558N provides a large amount of programmable logic for managing system power control on the most precise of levels. The basic concepts of the 82C558N power management scheme involve activity monitoring through time-outs and events. These concepts are illustrated in Figure 4-39 and described in detail in the following sections.

Figure 4-39 Activity Monitoring Block Diagram



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4.14.1.1 Activity Monitoring

Activity monitoring is based on time-outs of countdown timers, the events that can be enabled to reload the timers and forestall a time-out, and the system management interrupts that can be generated in either case.

4.14.1.1.1 Timers

The thirteen 82C558N timer registers all have `_TIMER` appended to their name.

The `IDLE_TIMER` times long periods of inactivity across all selected system peripherals to determine when a full power-down, called "Suspend" mode, is appropriate.

The `DOZE_TIMER` times short inactivity intervals (between keystrokes, for example) to put the system in an intermediate power-saving state called "Doze" mode.

The `R_TIMER` generates a periodic interrupt to allow system management code to poll for activity.

Ten other timers are available to monitor activity on specific peripheral devices so that system management software can shut each one down individually when possible while the rest of the system continues to operate.

Simply loading the timer with a countdown value presets the timers. Then the next access or interrupt event starts them counting down. A "dummy" access is needed in most cases to start the timer counting.

As each timer is clocked by its programmed source, it counts down to a time-out (zero) which generates a power management interrupt (PMI). The time-out PMI can, in turn, be enabled to generate an SMI (system management interrupt) on the SMI line that goes from the 82C558N to the CPU to trigger it into System Management Mode (SMM).

4.14.1.1.2 Events

Each timer has one or more events that can reload it with its original value, holding off the time-out. The events can be:

- Access Events
 - Those that are caused by CPU access to a certain I/O and or memory range associated with that timer.

- Internal Events
 - Triggered by ISA bus IRQ events or special external power management inputs (EPMIs).

All events can be enabled individually to generate a PMI; access events generate separately numbered PMIs, while interrupt events are combined into a single PMI (PMI#6).

As opposed to time-out caused PMIs, event PMIs can be enabled to:

- Reload the timer(s) and, if needed, restore the system clocks speed
- Generate an SMI
- Do both

Because of the flexibility of the 82C558N's power management logic, the interaction among these mechanisms can become complex. It is important to bear in mind the basic goal of the logic in order to deal with it effectively.

4.14.1.1.3 Timer Clock Sources

The 82C558N's logic implements thirteen distinct timer circuits. Each timer has a clock source associated with it. For all but the `DOZE_TIMER`, these are named `SQW0`, `SQW1`, `SQW2`, or `SQW3`; the `DOZE_TIMER` circuit works differently than the rest and is described separately in the Section 4.14.2.2, "Doze Mode", of this document. Table 4-63 shows the frequencies that can be applied to the rest of the `_TIMER` counters.

The `SQW3` through `SQW0` timings are based on the `SQWIN` input to the 82C558N's logic, which is a 32kHz clock input to the 82C558N. `SYSCFG 40h[2]` (as shown in Table 4-62) provides a secondary range of time intervals and applies globally to all `SQW3` through `SQW0` selections.

Table 4-63 lists the range of time-out delays that can be achieved by selecting each `SQWx + SYSCFG 40h[6]` combination. The register bit locations for each timer are shown in Table 4-64. The timer source is selected by bit combinations:

00 = `SQW0`, 01 = `SQW1`, 10 = `SQW2`, 11 = `SQW3`

Table 4-62 Timer Control Bits

7	6	5	4	3	2	1	0
PMU Control Register 1							
Default = 00h							
Reserved	Global timer divide: 0 = +1 1 = +4	LLOWBAT polarity: 0 = Active high 1 = Active low	LOWBAT polarity: 0 = Active high 1 = Active low	Reserved	EPMI1# polarity: 0 = Active high 1 = Active low	EPMIO# polarity: 0 = Active high 1 = Active low	Reserved



Table 4-63 Time Interval Choices Applicable to _TIMER Settings

Choice	Bits	SYSCFG 40h[6] = 0: No Base Clock Divisor			SYSCFG 40h[6] = 1: Divide Base Clock by 4		
		Frequency	Decrement Timer Every:	Maximum Delay	Frequency	Decrement Timer Every:	Maximum Delay
SQW0	00	32768Hz	30.5µs	7.81ms	8.192kHz	0.122ms	31.25ms
SQW1	01	512Hz	1.95ms	0.5s	128Hz	7.8ms	2s
SQW2	10	16Hz	62.5ms	16s	4Hz	0.25s	64s
SQW3	11	0.5Hz	2s	8.5 min.	0.125Hz	8s	34 min.

Table 4-64 Timer Clock Source Selection Registers

7	6	5	4	3	2	1	0
SYSCFG 42h Clock Source Register 1 Default = 00h							
Clock source for GNR1_TIMER		Clock source for KBD_TIMER		Clock source for DSK_TIMER		Clock source for LCD_TIMER	
SYSCFG B2h Clock Source Register 2 Default = 00h							
Clock source for HDU_TIMER		Clock source for COM2_TIMER		Clock source for COM1_TIMER		Clock source for GNR2_TIMER	
SYSCFG 68h Clock Source Register 3 Default = 00h							
R_TIMER clock source		IDLE_TIMER clock source		Resume recovery time: 00 = 8ms 10 = 128ms 01 = 32ms 11 = 30µs Note: Ignored if BEh[0] = 1.		PPWR[1:0] auto-toggle on entry and exit from Suspend: 0 = Disable 1 = Enable	
SYSCFG E6h Clock Source Register 4 Default = 70h							
BCLK source for STPCLK# modulation (For normal mode, Doze mode, thermal mgmt): 00 = 4KHz 01 = 32KHz (Default) 10 = 450KHz 11 = 900KHz		GNR4_ACCESS: 0 = DOZE_0 1 = DOZE_1	GNR3_ACCESS: 0 = DOZE_0 1 = DOZE_1	Clock source for GNR4_TIMER		Clock source for GNR3_TIMER	

4.14.1.1.4 Time-Out Count and Time-Out SMI

The timer source registers listed in Table 4-65 are used to load the initial time-out count. The following rules apply.

- A time-out count of five or greater indicates the countdown value. Time-out count values 1-4 should not be used: since the logic can take up to four clocks to reload a time-out count value, an invalid time-out could occur in the meantime.
- Writing a time-out count of 0 disables the timer.
- A dummy access in the appropriate address range for that timer triggers counting. From then on, additional accesses will reload the timer with its initial value and forestall a time-out.

- Reading the timer value will return only the value initially written, not the current count (except for R_TIMER, which does return the current count).

When a time-out occurs, it can do only one thing: trigger an SMI. Registers listed under the "Enabling of Events to Generate SMI" heading of the "System Management Interrupt" section enable each time-out event individually to cause an SMI.

Note that the DOZE_TIMER Register (SYSCFG 41h) is the time count bits for the DOZE_TIMER and monitors selected IRQs and EPIMIs. Unlike the other timer registers, the DOZE_TIMER uses its own time base selected through SYSCFG 41h[7:5]. A time-out generates PMI#27.



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Table 4-65 Timer Source Registers

7	6	5	4	3	2	1	0	
SYSCFG 44h LCD Timer Register Default = 00h Time count byte for LCD_TIMER - monitors LCD_ACCESS. Time-out generates PMI#8.								
SYSCFG 45h DSK_TIMER Register Default = 00h Time count byte for DSK_TIMER - monitors DSK_ACCESS. Time-out generates PMI#9.								
SYSCFG 46h KBD_TIMER Register Default = 00h Time count byte for KBD_TIMER - monitors KBD_ACCESS. Time-out generates PMI#10.								
SYSCFG B4h HDU_TIMER Register Default = 00h Time count byte for HDU_TIMER - monitors HDU_ACCESS. Time-out generates PMI#19.								
SYSCFG B5h COM1_TIMER Register Default = 00h Time count byte for COM1_TIMER - monitors COM1_ACCESS. Time-out generates PMI#17.								
SYSCFG B6h COM2_TIMER Register Default = 00h Time count byte for COM2_TIMER - monitors COM2_ACCESS. Time-out generates PMI#18.								
SYSCFG 47h GNR1_TIMER Register Default = 00h Time count byte for GNR1_TIMER - monitors GNR1_ACCESS. Time-out generates PMI#11.								
SYSCFG B7h GNR2_TIMER Register Default = 00h Time count byte for GNR2_TIMER - monitors GNR2_ACCESS. Time-out generates PMI#16.								
SYSCFG 4Fh IDLE_TIMER Register Default = 00h Time count byte for IDLE_TIMER - monitors selected IRQs and EPMLs. Time-out generates PMI#4.								
SYSCFG 69h R_TIMER Register Default = 00h Time count byte for R_TIMER - starts to count after a non-zero write to this register. Unlike the other timer registers, a read from this register returns the current count. Time-out generates PMI#5.								
SYSCFG 41h DOZE_TIMER Register 2 Default = 00h								
DOZE_0 time-out select: 000 = 2ms 001 = 4ms 010 = 8ms 011 = 32ms 100 = 128ms 101 = 512ms 110 = 2s 111 = 8s Time-out generates PMI#27.		Doze mode STPCLK# modulation (STPCLK# modulated by BCLK defined in E6h[7:6]): 000 = No Modulation (STPCLK# = 1) 001 = STPCLK# $t_{pi} = 0.75 * 16$ BCLKs 010 = STPCLK# $t_{pi} = 0.5 * 16$ BCLKs 011 = STPCLK# $t_{pi} = 0.25 * 16$ BCLKs 100 = STPCLK# $t_{pi} = 0.125 * 16$ BCLKs 101 = STPCLK# $t_{pi} = 0.0625 * 16$ BCLKs 110 = STPCLK# $t_{pi} = 0.03125 * 32$ BCLKs 111 = STPCLK# $t_{pi} = 0.015625 * 64$ BCLKs			ACCESS events reset doze mode: 0 = Disable 1 = Enable		Doze control select: 0 = Hardware 1 = Software	
SYSCFG E7h GNR3_TIMER Register Default = 00h Time count byte for GNR3_TIMER - monitors GNR3_ACCESS. Time-out generates PMI#29.								
SYSCFG E8h GNR4_TIMER Register Default = 00h Time count byte for GNR4_TIMER - monitors GNR4_ACCESS. Time-out generates PMI#30.								



4.14.1.1.5 ACCESS Events

CPU memory and I/O instructions to peripheral devices cause power management events known as ACCESS events.

- Most ACCESS events generate an access PMI directly, which in turn can be enabled to activate the SMI input to the CPU so that the event can be serviced.
- These same events can be programmed to reload an associated countdown timer, thus preventing a time-out PMI from occurring.
- Still other ACCESS events can only cause a timer reload, and cannot directly generate an SMI.

Table 4-66 lists all of the ACCESS events, how the ACCESS can reload its associated timer and reload the IDLE_TIMER.

Note that enabled ACCESS events, except for the GNR and GPCS events, can be globally enabled to reload the DOZE_TIMER by setting SYSCFG 41h[1] = 1. Refer to the "Doze Mode" section for details.

4.14.1.1.6 Serial (COMx) and Parallel Port (LPT) Access

Accesses to the LPT1, LPT2, and LPT3 I/O range group can be programmed to reload the IDLE_TIMER. For a greater degree of control, COM1 and COM2 can individually be enabled to cause COM1_ACCESS or COM2_ACCESS, reload the COM1_TIMER or COM2_TIMER, and reload the IDLE_TIMER.

Table 4-66 ACCESS Events and their Enabling Bit Locations

ACCESS Mnemonic	Monitored Range	ACCESS PMI#	Enable SMI on Current Access	Enable SMI on Next Access	Enable Reload of IDLE_TIMER
LPT	Reads/writes in I/O address ranges 378-Fh, 278-Fh, and 3B8-Fh (LPT1, 2, and 3)	--	--	--	4Eh[5]
COM1	Reads/writes in I/O address range 3F8-Fh.	21	DEh[5]	DBh[1]	BEh[4]
COM2	Reads/writes in I/O address range 2F8-Fh.	22	DEh[6]	DBh[2]	BEh[5]
DSK	FDD accesses to I/O Port 3F5h and/or HDD accesses to 1F0-1F7h+3F6h. Bits 57h[5:4] determine which ranges apply.	13	DEh[1]	5Bh[1]	4Eh[1]
KBD	Reads/writes to I/O ports 060h and 064h.	14	DEh[2]	5Bh[2]	4Eh[2]
LCD	Reads/writes in memory address range A000-BFFFFh and/or I/O address range 3B0-3DFh. Bits 43h[7:6] and 5Fh[7:6], determine which ranges apply.	12	DEh[0]	5Bh[0]	4Eh[0]
HDU	HDU accesses in the integrated IDE controller range: 1F0-7h + 3F6h (primary) or 170-7h + 376h (secondary). Bit ACh[2] determines which addresses apply.	23	DEh[7]	DBh[3]	BEh[2]
GPCS0	Defined in 4Ah[7:0], 4Bh[7:0], BFh[4,0]	--	--	--	4Eh[6]
GPCS1	Defined in 4Ch[7:0], 4Dh[7:0], BFh[5,1]	--	--	--	4Eh[7]
GPCS2	Defined in BCh[7:0], BDh[7:0], BFh[6,2]	--	--	--	BEh[6]
GPCS3	Defined in BAh[7:0], BBh[7:0], BFh[7,3]	--	--	--	BEh[7]
GNR1	Defined in bits 70h[7:0], 71h[7:0], 72h[7:0], 48h[7:0], 49h[7:0], and AEh[4,2,0]	15	DEh[3]	5Bh[3]	4Eh[3]
GNR2	Defined in bits 73h[7:0], 74h[7:0], 75h[7:0], B8h[7:0], B9h[7:0], and AEh[5,3,1]	20	DEh[4]	DBh[0]	BEh[3]
GNR3	Defined in bits E1h[7:0], E2h[7:0], and E5h[4,2,0]	31	E9h[1]	E9h[0]	4Eh[4]
GNR4	Defined in bits E3h[7:0], E4h[7:0], and E5h[5,3,1]	32	E9h[3]	E9h[2]	BEh[1]



4.14.1.1.7 ISA Bus Floppy and Hard Drive Access

DSK_ACCESS can come from either or both of two separate access types. If enabled, the DSK_ACCESS reloads the DSK_TIMER and the IDLE_TIMER as well, if desired.

- Floppy accesses to generate DSK_ACCESS if SYSCFG 57h[5] = 0. The range of addresses that are to be monitored are determined by SYSCFG D6h[7].
- Hard disk accesses to 1F0-1F7h and 3F6h generate DSK_ACCESS if SYSCFG 57h[4] = 0. Both ISA bus IDE accesses and VL bus IDE accesses will generate the access event.

Two separate and independent hard disk drives can be managed if the primary drive is on the ISA bus or VL bus and the secondary drive is managed by the integrated IDE controller. Refer to the HDU_ACCESS event regarding access events from the integrated local bus IDE controller.

4.14.1.2 Integrated Controller Hard Drive Access

Accesses to the integrated hard disk controller, in the primary range 1F0-1F7h and 3F6h or the secondary range 170-177h and 377h can cause HDU_ACCESS, reload the

HDU_TIMER, and reload the IDLE_TIMER. SYSCFG Ach[2] determines which addresses apply.

HDU_ACCESS is based solely on the decoding for the internal IDE controller. It is independent of the DSK_ACCESS decoding. Therefore, SYSCFG 57h[4] does not affect HDU_ACCESS. DSK_ACCESS can continue to monitor both floppy disk and primary external hard disk accesses if desired.

4.14.1.2.1 Keyboard Access

Keyboard accesses to I/O Ports 060h and 064h can cause KBD_ACCESS, reload the KBD_TIMER, and reload the IDLE_TIMER.

4.14.1.2.2 LCD Controller Access

Video controller accesses are to I/O Ports 3B0-3DFh and to memory locations A0000-BFFFFh if not masked by SYSCFG 43h[7:6].

The enabled accesses cause LCD_ACCESS, reload the LCD_TIMER, and reload the IDLE_TIMER if not masked in SYSCFG 5Fh[7:6].

Table 4-67 PMU Control Registers

7	6	5	4	3	2	1	0
SYSCFG 43h PMU Control Register 3 Default = 00h							
LCD_ACCESS includes I/O range 3B0h-3DFh: 0 = Yes 1 = No	LCD_ACCESS includes memory A0000-BFFFFh: 0 = Yes 1 = No	LOWBAT pin sample rate: (A PMI is generated each time LOWBAT is sampled active.) 00 = 32s 10 = 128s 01 = 64s 11 = Rsvrd		Reserved			
SYSCFG 57h PMU Control Register 5 Default = 00h							
Reserved	INTRGRP generates PMI#6: 0 = Disable 1 = Enable	DSK_ACCESS includes FDD: 0 = Yes 1 = No	DSK_ACCESS includes HDD: 0 = Yes 1 = No	Reserved			
SYSCFG D6h PMU Control Register 10 Default = 00h							
DSK_ACCESS: 0 = 3F5h only 1 = All FDC Ports (3F2,4,5,7h, & 372,4,5,7h)	DMA trap PMI#28 SMI: 0 = Disable 1 = Enable	DMAC1 byte pointer flip-flop (RO): 0 = Cleared 1 = Set	APM doze exit PMI#35: 0 = Disable 1 = Enable	SBHE# status trap (RO)	I/O port access trapped (RO): 0 = I/O read 1 = I/O write	Access trap bit A9 (RO)	Access trap bit A8 (RO)
SYSCFG 5Fh PMU Control Register 6 Default = 00h							
LCD_ACCESS includes ISA bus video access: 0 = Yes 1 = No	LCD_ACCESS includes local (VL/PCI) bus video access: 0 = No 1 = Yes	RSMGRP IRQs can Resume system: 0 = No 1 = Yes	Transitions on RING1 can Resume system: 0 = No 1 = Yes	Number of RING1 transitions to cause Resume			

4.14.1.3 Chip Select Generation (GPCS) Access

The GPCS[3:0]# lines can be programmed to generate a chip select based on either memory or I/O decoding of reads and/or writes. Even if the external logic necessary to implement the chip select lines is not in place, the chip select events themselves can be individually enabled to reload the IDLE_TIMER through SYSCFG 4Eh[7:6] and BEh[7:6].

4.14.1.3.1 General Purpose (GNR) Access

Four programmable ranges, GNR1, GNR2, GNR3, and GNR4 are provided, each with its own separate timer, to allow any four I/O or memory ranges to be monitored. As an example, the COM3 I/O range 3E8-3EFh could be monitored for reads and writes in order to determine whether the connected UART was in active use. As another example, a network card that uses memory in the D800-DFFFh half-segment could be monitored to determine whether the memory is being accessed regularly and, if not, a query could be sent through the network to ensure that the connection was still valid.

4.14.1.3.2 Memory Watchdog Feature

The 82C558N general purpose access register sets, GNR1, GNR2, GNR3, and GNR4 can be monitored for activity and can generate an SMI when no activity has occurred in a given amount of time. As an option, either or both of these register sets can be assigned to monitor memory space instead. In this case, instead of the bit values corresponding to I/O address bits A[9:0], the values correspond to memory address bits A[23:14]. The bits that select I/O read or I/O write cycles instead indicate memory read or memory write cycles.

Example:

To monitor memory write activity in the 16KB block from CC00:0 to CC00:3FFF requires first viewing the CC00 segment value as:

- 0000 1100 1100 0000 0000 0000

to determine the value of the upper ten bits, CA[23:14], which is:

- 0000110011

to write into the A[9:0] GNR address decode bits. The bits are set by writing:

- SYSCFG E1h (A[8:1]) = 00011001b, or 19h

- SYSCFG E2h (A9 + write decode + read decode + A[5:1] mask bits) = 01000000b, or 40h

- SYSCFG E5h (GNR4 cycle + GNR3 cycle + GNR4 A0 + GNR3 A0 + GNR4 A0 mask + GNR3 A0 mask) = 011000b, or 18h (GNR4 values must also be considered).

The timer values must then be entered, the PMI enabled, and then a dummy write access must be made to the CC000-CFFFFh range to start GNR3_TIMER. If no accesses are occurring, the timer will eventually expire and generate an SMI. If enabled, the next write access to this range will also cause an SMI and will reload the timer.

Of the four general purpose access register sets, two sets, GNR1 and GNR2, provide granularity for the memory watchdog function to monitor a minimum range of four bytes, while GNR3 and GNR4 provide granularity to monitor accesses in a 64KB range. If SYSCFG A0h[7] = 1 such that upper address bits must be zero, the GNR1 and GNR2 registers still decode the full 16 bits of the address as long as those upper bits are not masked off (default).

Table 4-68 General Purpose Access 1, 2, 3, and 4 Registers

7	6	5	4	3	2	1	0
SYSCFG 70h GNR1 Base Address Register 1 Default = 00h							
GNR1_ACCESS base address: A[13:6] for memory watchdog or A[15:10] for I/O (right-aligned).							
SYSCFG 71h GNR1 Control Register 1 Default = FFh							
GNR1_ACCESS mask bits: Mask for A[13:6] for memory watchdog or mask for A[15:10] for I/O (right-aligned).							
SYSCFG 72h GNR1 Control Register 2 Default = 00h							
GNR1_ACCESS base address: A[5:2] for memory watchdog or ignored for I/O.				GNR1_ACCESS mask bits: Mask for A[5:2] for memory watchdog or mask for A[9:6] for I/O.			
SYSCFG 48h GNR1 Base Address Register Default = 00h							
GNR1_ACCESS base address: A[8:1] (I/O) or A[22:15] (Memory)							
SYSCFG 49h GNR1 Control Register Default = 00h							
GNR1 base address: A9 (I/O) A23 (Memory)	Write decode: 0 = Disable 1 = Enable	Read decode: 0 = Disable 1 = Enable	GNR1 mask bits for address A[5:1] (I/O) or A[19:15] memory: A 1 in a particular bit means that the corresponding bit at 48h[4:0] is not compared. This is used to determine address block size.				



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Table 4-68 General Purpose Access 1, 2, 3, and 4 Registers (cont.)

7	6	5	4	3	2	1	0
SYSCFG 73h GNR2 Base Address Register 1 Default = 00h GNR2_ACCESS base address: A[13:6] for memory watchdog or A[15:10] for I/O (right-aligned).							
SYSCFG 74h GNR2 Control Register 1 Default = FFh GNR2_ACCESS mask bits: Mask for A[13:6] for memory watchdog or mask for A[15:10] for I/O (right-aligned).							
SYSCFG 75h GNR2 Control Register 2 Default = 00h							
GNR2_ACCESS base address: A[5:2] for memory watchdog or ignored for I/O.				GNR2_ACCESS mask bits: Mask for A[5:2] for memory watchdog or mask for A[9:6] for I/O.			
SYSCFG B8h GNR2 Base Address Register Default = 00h GNR2_ACCESS base address: A[8:1] (I/O) or A[22:15] (Memory)							
SYSCFG B9h GNR2 Control Register Default = 00h							
GNR2 base address: A9 (I/O) A23 (Memory)	Write decode: 0 = Disable 1 = Enable	Read decode: 0 = Disable 1 = Enable	GNR2 mask bits for address A[5:1] (I/O) or A[19:15] memory: A 1 in a particular bit means that the corresponding bit at B8h[4:0] is not compared. This is used to determine address block size.				
SYSCFG AEh GNR_ACCESS Feature Register Default = 03h							
Reserved	GNR2 cycle decode type: 0 = I/O 1 = Memory	GNR1 cycle decode type: 0 = I/O 1 = Memory	GNR2 base address: A0 (I/O) A14 (Memory)	GNR1 base address: A0 (I/O) A14 (Memory)	GNR2 mask bit: A0 (I/O) A14 (Memory)	GNR1 mask bit: A0 (I/O) A14 (Memory)	
SYSCFG 7Ah GNR3 Base Address Register 1 Default = 00h GNR3_ACCESS base address: A[13:6] for memory watchdog or A[15:10] for I/O (right-aligned).							
SYSCFG 7Bh GNR3 Control Register 1 Default = FFh GNR3_ACCESS mask bits: Mask for A[13:6] for memory watchdog or mask for A[15:10] for I/O (right-aligned).							
SYSCFG 7Ch GNR3 Control Register 2 Default = 00h							
GNR3_ACCESS base address: A[5:2] for memory watchdog or ignored for I/O.				GNR3_ACCESS mask bits: Mask for A[5:2] for memory watchdog or mask for A[9:6] for I/O.			
SYSCFG E1h GNR3 Base Address Register Default = 00h GNR3_ACCESS base address: A[8:1] (I/O) or A[22:15] (Memory)							
SYSCFG E2h GNR3 Control Register Default = 00h							
GNR3 base address: A9 (I/O) A23 (Memory)	Write decode: 0 = Disable 1 = Enable	Read decode: 0 = Disable 1 = Enable	GNR3 mask bits for address A[5:1] (I/O) or A[19:15] memory: A 1 in a particular bit means that the corresponding bit at E1h[4:0] is not compared. This is used to determine address block size.				
SYSCFG 7Dh GNR4 Base Address Register 1 Default = 00h GNR4_ACCESS base address: A[13:6] for memory watchdog or A[15:10] for I/O (right-aligned).							
SYSCFG 7Eh GNR4 Control Register 1 Default = FFh GNR4_ACCESS mask bits: Mask for A[13:6] for memory watchdog or mask for A[15:10] for I/O (right-aligned).							
SYSCFG 7Fh GNR4 Control Register 2 Default = 00h							
GNR4_ACCESS base address: A[5:2] for memory watchdog or ignored for I/O.				GNR4_ACCESS mask bits: Mask for A[5:2] for memory watchdog or mask for A[9:6] for I/O.			



Table 4-68 General Purpose Access 1, 2, 3, and 4 Registers (cont.)

7	6	5	4	3	2	1	0
SYSCFG E3h GNR4 Base Address Register Default = 00h GNR4_ACCESS base address: A[8:1] (I/O) or A[22:15] (Memory)							
SYSCFG E4h GNR4 Control Register Default = 00h							
GNR4 base address: A9 (I/O) A23 (Memory)	Write decode: 0 = Disable 1 = Enable	Read decode: 0 = Disable 1 = Enable	GNR4 mask bits for address A[5:1] (I/O) or A[19:15] memory: A 1 in a particular bit means that the corresponding bit at E3h[4:0] is not compared. This is used to determine address block size.				
SYSCFG E5h GNR_ACCESS Feature Register 2 Default = 03h							
Reserved	GNR4 cycle decode type: 0 = I/O 1 = Memory	GNR3 cycle decode Type: 0 = I/O 1 = Memory	GNR4 base address: A0 (I/O) A14 (Memory)	GNR3 base address: A0 (I/O) A14 (Memory)	GNR4 mask bit: A0 (I/O) A14 (Memory)	GNR3 mask bit: A0 (I/O) A14 (Memory)	

4.14.1.4 Activity Tracking Registers

The activity tracking registers at SYSCFG DFh and E0h allow events to be flagged even if they are not programmed to generate an SMI. In this way, code can check whether a key-stroke occurred since the last time the register was checked, for example, without actually generating an SMI for every keystroke.

The activity tracking registers record activity on all ten ACCESS events. No type of enabling is needed for any of these events to be registered. Reading this register returns flags indicating whether any of the events have taken place and automatically resets the entire register. The register can be written if desired to set the selected bits. In this way, a read-modify-write code sequence can be used to clear selected bits only.

Table 4-69 Activity Tracking Registers

7	6	5	4	3	2	1	0
SYSCFG DFh Activity Tracking Register Default = 00h							
HDU_ ACCESS activity: 0 = No 1 = Yes	COM2_ ACCESS activity: 0 = No 1 = Yes	COM1_ ACCESS activity: 0 = No 1 = Yes	GNR2_ ACCESS activity: 0 = No 1 = Yes	GNR1_ ACCESS activity: 0 = No 1 = Yes	KBD_ ACCESS activity: 0 = No 1 = Yes	DSK_ ACCESS activity: 0 = No 1 = Yes	LCD_ ACCESS activity: 0 = No 1 = Yes
SYSCFG E0h Activity Tracking Register 1 Default = 00h							
Reserved						GNR4_ ACCESS activity: 0 = No 1 = Yes	GNR3_ ACCESS activity: 0 = No 1 = Yes



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4.14.1.5 Reloading IDLE_TIMER

The 82C558N provides the IDLE_TIMER to monitor system-wide activity: I/O and memory accesses by the CPU, IRQs from ISA bus peripherals, and EPIMs from power control and management subsystems. The occurrence of an enabled event in any one of these areas will reload the IDLE_TIMER. Once there is inactivity for a sufficiently long time, the IDLE_TIMER will expire.

Expiration of the IDLE_TIMER generates PMI#4, which can be enabled to generate an SMI to inform system management code that the system is idle and that entry into the Suspend mode is appropriate. Refer to the Section 4.14.4.1,

"Suspend Mode" for complete information. Expiration of the IDLE_TIMER cannot cause automatic (hardware-controlled) entry into the Suspend mode, since important CPU processing could be interrupted.

The register bits that enable each event individually to reload the IDLE_TIMER and forestall entry into the Suspend mode are shown in Table 4-70. SYSCFG 63h and A3h are write-only; reads return no useful information.

Table 4-70 Idle Reload Source Registers

7	6	5	4	3	2	1	0
SYSCFG 4Eh Idle Reload Event Enable Register 1 Default = 00h							
GPCS1_ ACCESS: 0 = Disable 1 = Enable	GPCS0_ ACCESS: 0 = Disable 1 = Enable	LPT_ ACCESS: 0 = Disable 1 = Enable	GNR3_ ACCESS: 0 = Disable 1 = Enable	GNR1_ ACCESS: 0 = Disable 1 = Enable	KBD_ ACCESS: 0 = Disable 1 = Enable	DSK_ ACCESS: 0 = Disable 1 = Enable	LCD_ ACCESS: 0 = Disable 1 = Enable
SYSCFG BEh Idle Reload Event Enable Register 2 Default = 00h							
GPCS3#_ ACCESS: 0 = Disable 1 = Enable	GPCS2#_ ACCESS: 0 = Disable 1 = Enable	COM2_ ACCESS: 0 = Disable 1 = Enable	COM1_ ACCESS: 0 = Disable 1 = Enable	GNR2_ ACCESS: 0 = Disable 1 = Enable	HDU_ ACCESS: 0 = Disable 1 = Enable	GNR4_ ACCESS: 0 = Disable 1 = Enable	Override SYSCFG 68h[3:2]: 0 = No 1 = Recover time 1s
SYSCFG 63h Idle Time-Out Select Register 1 Default = 00h							
EPMI0# Level-trig'd: 0 = Disable 1 = Enable	IRQ13: 0 = Disable 1 = Enable	IRQ8: 0 = Disable 1 = Enable	IRQ7: 0 = Disable 1 = Enable	IRQ5: 0 = Disable 1 = Enable	IRQ4: 0 = Disable 1 = Enable	IRQ3: 0 = Disable 1 = Enable	IRQ0: 0 = Disable 1 = Enable
SYSCFG A3h Idle Time-Out Select Register 2 Default = 00h							
IRQ15: 0 = Disable 1 = Enable	IRQ14: 0 = Disable 1 = Enable	IRQ12: 0 = Disable 1 = Enable	IRQ11: 0 = Disable 1 = Enable	IRQ10: 0 = Disable 1 = Enable	IRQ9: 0 = Disable 1 = Enable	IRQ6: 0 = Disable 1 = Enable	IRQ1: 0 = Disable 1 = Enable

4.14.1.6 External PMI Events

The 82C558N logic can monitor a variety of inputs that are directly related to low-power, battery-operated system designs. Table 4-71 lists the external power management input (EPMI) pins provided. Note that all pins included here are considered external PMI pins, not just pins EPMI[3:0]#.

4.14.1.6.1 EPMI Programming

The chipset registers listed below are used to initialize the EPMI pins and enable them to cause PMI events.

Emergency Overtemp Sense Enable - Setting SYSCFG A1h[2] = 1 allows a level on the EPMI1# pin to force the chip into cool-down clocking mode as set by the thermal management registers. The thermal management feature itself does not need to be enabled to use this sense function. The polarity of the input is determined by SYSCFG 40h[2]. Once written to 1, this bit cannot be cleared without a hardware reset.

EPMI[1:0]# Status Latch - Setting SYSCFG A1h[0] = 1 allows the EPMI[1:0]# PMI events to be latched. The status returned by SYSCFG 5Ch[2:1] are **not** latched. Writing these same bits to 1 clears the status bits.

Table 4-71 External PMI Source Summary

Name	Description
LOWBAT	Activity on Low Battery pin
LLOWBAT	Activity on Very Low Battery pin
EPMI0#	Activity on External Power Management Input 0
EPMI1#	Activity on External Power Management Input 1
EPMI2#	Activity on External Power Management Input 2
EPMI3#	Activity on External Power Management Input 3
RESUME	SUS/RES# input has been toggled while in Suspend
SUSPEND	SUS/RES# input has been toggled while system is active
RINGI	Activity detected on RINGI

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Table 4-72 EPMI Programming Registers

7	6	5	4	3	2	1	0
SYSCFG 40h PMU Control Register 1 Default = 00h							
Reserved	Global timer divide: 0 = +1 1 = +4	LLOWBAT polarity: 0 = Active high 1 = Active low	LOWBAT polarity: 0 = Active high 1 = Active low	Reserved	EPMI1# polarity: 0 = Active high 1 = Active low	EPMI0# polarity: 0 = Active high 1 = Active low	Reserved
SYSCFG DBh Next Access Event Generation Register 2 Default = 00h							
I/O blocking control: 0 = Block I/O on next access trap 1 = Unblock	SMI on cool-down clocking entry/exit: 0 = Disable 1 = Enable	External EPMI3# pin polarity: 0 = Active high 1 = Active low	External EPMI2# pin polarity: 0 = Active high 1 = Active low	HDU_ACCESS PMI#23 on next access: 0 = No 1 = Yes	COM2_ACCESS PMI#22 on next access: 0 = No 1 = Yes	COM1_ACCESS PMI#21 on next access: 0 = No 1 = Yes	GNR2_ACCESS PMI#20 on next access: 0 = No 1 = Yes
SYSCFG 43h PMU Control Register 3 Default = 00h							
LCD_ACCESS includes I/O range 3B0h-3DFh: 0 = Yes 1 = No	LCD_ACCESS includes memory A0000-BFFFFh: 0 = Yes 1 = No	LOWBAT pin sample rate: (A PMI is generated each time LOWBAT is sampled active.) 00 = 32s 10 = 128s 01 = 64s 11 = Rsvrd		Reserved			
SYSCFG 61h Debounce Register Default = 00h							
LOWBAT, LLOWBAT debounce rate select: 00 = No debounce 01 = 250µs 10 = 8ms 11 = 500ms		SUS/RES# debounce rate select: 00 = Active low, edge-trig'd PMI 01 = Active low, level-controlled PMI 10 = Active high, level-sampled PMI in 16ms 11 = Active high, level-sampled PMI in 32ms (See Section 4.14.5.2, "SUS/RES# and RINGI Events")		PPWR0 auto-toggle in APM STPCLK mode: 0 = No PPWR0 auto-toggle 1 = Auto-toggle PPWR0 on entry and exit from APM STP-CLK mode	STPCLK# signal 0 = Disable 1 = Enable	APM STPCLK recovery time: 00 = 120µs 01 = 240µs 10 = 1ms 11 = 2ms	
SYSCFG A1h Feature Control Register 2 Default = 00h							
Reserved			Heavy drive on MD bus: 0 = Disable 1 = Enable	Heavy drive on ISA bus: 0 = Disable 1 = Enable	Emerg. over-temp sense: 0 = Disable 1 = Enable	Reserved	EPMI[1:0]# status latch: 0 = Dynamic 1 = Latched

- Notes:**
- 1) EPMI0# and EPMI1# need to be asserted until recognized by its SMI service routine, since these PMIs are not latched unless SYSCFG A1h[0] = 1.
 - 2) If EPMI0# and EPMI1# are used to place the system into Suspend, the EPMIx signal must be negated before the Suspend command (setting bit SYSCFG 50h[0] = 1) is written.



4.14.1.7 Power Management Event Status

The power management input pins can be monitored for their instantaneous state in the 82C558N. This feature can be used to poll for power management status without generating an SMI. The bits of the Power Management Event Status Register return instantaneous pin status; the state is not latched. Table 4-73 gives the bit definitions for SYSCFG DAh[5:0].

4.14.2 System Power Control

The power management unit logic provides two hardware means of controlling the CPU clock speed.

Doze mode hardware causes the clock to the CPU core to be stopped and started in a periodic manner, resulting in power savings when there is no significant activity. *Thermal management* hardware forces the action to avoid overheating the CPU when the system is running at full speed for too long.

Both of these mechanisms engage the *stop clock* mechanism to slow down the CPU.

4.14.2.1 STPCLK# Mechanism to Control CPU Power Dissipation

The 3.3V Pentium processor contains a phase-locked loop (PLL) frequency generator that takes the external clock frequency input and multiplies it before applying it to the CPU core. The CPU core may be cut off from the PLL output by asserting the STPCLK# signal, without any loss of information. The CPU then enters the Stop Grant state in which the power consumption is approximately 20% of the normal consumption. It may be restarted almost immediately by negating the STPCLK# signal. Since a significant amount of power savings may be achieved when the CPU is in the Stop Grant state, it is forced into this state by the Viper-N Chipset when there is no significant activity.

On receiving an active STPCLK#, the CPU will generate a special bus cycle, and when it receives BRDY# from the Viper-N Chipset, it will enter the Stop Grant state. The Viper-N Chipset may be programmed so that a system interrupt, such as initiated by a keystroke or a timer interrupt, can restart the CPU almost immediately. Stopping the CPU clock is usually initiated by software, but could also be initiated by the hardware Doze mechanism.

The power consumed by the CPU can be controlled in two ways. The first method is to keep the STPCLK# signal asserted until a pre-programmed event causes the Viper-N Chipset to negate it. This could be used for maximum power saving modes invoked by software for prolonged periods of CPU inactivity.

The other method could be used for applications that do not require the CPU to operate at full speed all the time; the STPCLK# signal may be periodically asserted and negated. Since the Pentium processor does not provide much control for changing the frequency of the input clock, STPCLK# modulation is a viable alternative for saving power. This mode could be invoked by either software or hardware. On the 82C558N, the STPCLK# signal can be modulated by a base frequency of 32kHz, with a wide range of duty cycles. The period of the 32kHz square wave that is used to modulate the STPCLK# signal is 31.25µs. The time for which STPCLK# is asserted (low) is defined as t_{low} , and the time for which it is not asserted is defined as t_{hi} . The sum of t_{hi} and t_{low} equals 31.25µs. In every 32kHz cycle the STPCLK# signal is asserted for $31.25\mu s - t_{hi}$. Different levels of power savings are obtained by programming the duration of t_{hi} through SYSCFG 41h[4:2].

Table 4-73 Power Management Event Status

7	6	5	4	3	2	1	0
SYSCFG DAh							
Power Management Event Status Register (RO)							
Default = 00h							
Reserved	LOWBAT state: 0 = Low 1 = High	LLOWBAT state: 0 = Low 1 = High	EPMI3# state: 0 = Low 1 = High	EPMI2# state: 0 = Low 1 = High	EPMI1# state: 0 = Low 1 = High	EPMI0# state: 0 = Low 1 = High	



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4.14.2.1.1 Programming

To enable STPCLK# operation, the registers shown below must be programmed as follows.

- For maximum power savings, set SYSCFG 66h[5] = 1 and 65h[6] = 1, or for slow operation, set SYSCFG 66h[5] = 0 and 65h[6] = 1.
- Enable the STPCLK# logic mechanism by setting SYSCFG 61h[2] = 1.
- Enable the Stop Grant protocol by setting SYSCFG 66h[0] = 1 to recognize the Stop Grant cycle.

The STPCLK# sequence will now be observed any time the hardware Doze feature modulates the STPCLK# signal, or when APM commands the clock to stop. For example, during an APM operation for maximum power savings, the 82C558N:

1. Asserts its STPCLK# output

2. Waits for a Stop Grant cycle
3. Returns BRDY# to the CPU
4. Awaits a restart event (such as an interrupt)
5. Negates the STPCLK# signal, and continues operation.

For reduced power consumption, the 82C558N:

1. Asserts its STPCLK# output
2. Waits for a Stop Grant cycle
3. Returns BRDY# to the CPU
4. Waits for (31.25µs - t_{hi})
5. Negates the STPCLK# signal
6. Waits for t_{hi} (as programmed in SYSCFG 41h[4:2])
7. Goes back to Step 1.

While in Step 6, the CPU continues to execute instructions.

The registers associated with the clock speed change mechanism are shown in Table 4-74.

Table 4-74 Register Bits Associated with STPCLK# Feature

7	6	5	4	3	2	1	0
SYSCFG 61h Debounce Register Default = 00h							
LOWBAT, LLOWBAT debounce rate select: 00 = No debounce 01 = 250µs 10 = 8ms 11 = 500ms	SUS/RES# debounce rate select: 00 = Active low, edge-trig'd PMI 01 = Active low, level-controlled PMI 10 = Active high, level-sampled PMI in 16ms 11 = Active high, level-sampled PMI in 32ms (See Section 4.14.5.2, "SUS/RES# and RINGI Events")		PPWR0 auto-toggle in APM STPCLK mode: 0 = No PPWR0 auto-toggle 1 = Auto-toggle PPWR0 on entry and exit from APM STPCLK mode	STPCLK# signal 0 = Disable 1 = Enable	APM STPCLK recovery time: 00 = 120µs 01 = 240µs 10 = 1ms 11 = 2ms		
SYSCFG 65h Doze Register Default = 00h							
All interrupts to CPU reset Doze mode: 0 = Disable 1 = Enable	Reserved	EPMI0# Doze reset: 0 = Disable 1 = Enable	Recognize SMI during STPCLK#: 0 = No 1 = Yes	IRQ1 Doze reset: 0 = Disable 1 = Enable	EPMI3# Doze reset: 0 = Disable 1 = Enable	EPMI2# Doze reset: 0 = Disable 1 = Enable	EPMI1# Doze reset: 0 = Disable 1 = Enable
SYSCFG 66h PMU Control Register 7 Default = 00h							
Self-refresh DRAM selection: 0 = Normal 1 = Self-refresh	Suspend mode ATCLK frequency: 0 = Derived from LCLK 1 = 32kHz (overridden by SYSCFG 79h[0])	Doze type: 0 = Modulate STPCLK# 1 = Keep STPCLK# asserted	Assert HOLD during suspend 0 = Yes 1 = No	Reserved		STPGNT cycle wait option: 0 = Do not wait 1 = Wait for STPGNT cycle before negating STPCLK#	



4.14.2.2 Doze Mode

The 82C558N's power management unit includes Doze mode control logic. Doze is the state in which the CPU is fully alive and operational, yet running at a speed that is greatly reduced in order to save power. The 82C558N engages the Doze mode when it sees no activity in certain pre-definable areas for a certain time period. The Viper-N Chipset provides a choice of two time-out timers for each device. When an interrupt for the device or access in the range associated with that device occurs, the event triggers a Doze reset that reloads the selected timer for that device with the time-out value associated with that timer. Only when both time-outs have expired will the system return to Doze mode operation. Once initialized by software, the process is completely controlled by hardware. No further software intervention is needed, but an SMI can be generated if desired.

Even though the Doze mode is intended to operate autonomously without application or BIOS intervention, the 82C558N provides logic hooks to software for software-based power control. The most common type of software-based power control follows the Microsoft Advanced Power Management (APM) specification, which allows applications to inform the operating system when they are idle or do not require full processing power. The operating system, in turn, makes BIOS calls that can do any of the following:

- Turn off or put into a standby mode any unneeded peripherals
- Slow system clock speeds
- Turn off clocks to the CPU

Therefore, the 82C558N power Doze mode logic provides for three Doze mode operations: hardware-controlled slowdown, software-controlled slowdown, and software-controlled Doze with a stopped CPU clock (the clock to the CPU core is cut off).

The three modes are very similar and are outlined in the sections below, followed by register descriptions that the three modes have in common. The 82C558N provides the stop clock logic described next.

4.14.2.2.1 Presetting Events to Reset Doze Mode

Before enabling Doze mode operation, whether hardware or software Doze mode, some preparation must be made for the event or events that will reset Doze mode and bring the system back to full operation. Otherwise, especially in the case of APM stop clock mode, there would be no way to execute CPU instructions to restart the CPU clock.

Therefore, it is first necessary to choose the source or sources that will perform a Doze reset. Doze reset will, if the system is currently in Doze mode, restore the system clocks to full operating speed. Doze reset also reloads the Doze timer with its originally programmed value.

- Setting SYSCFG 41h[1] = 1 enables LCD_ACCESS, KBD_ACCESS, DSK_ACCESS, HDU_ACCESS, GNR accesses, COM port accesses, and LPT accesses to reset Doze mode and reload the DOZE_TIMER. If the associated DOZE_TIMER has timed out and switched operation to Doze speed, this reload will change the system clocks back to their normal speed.
- SYSCFG 65h[5] selects the EPMIO# pin as a Doze reset trigger.
- SYSCFG 62h[7:0], A2h[5:0], and 65h[3] define individual IRQs that can trigger a Doze reset.
- SYSCFG 65h[7] allows all enabled interrupts (i.e., any event that toggles the INTR signal to the CPU, to reset Doze mode).

Once the Doze mode reset events have been programmed, either hardware or software Doze mode can be enabled.

Table 4-75 Doze Reset Bit

7	6	5	4	3	2	1	0
SYSCFG 79h							Default = 00h
DOZE_1 time-out select:				PMI# event triggers exit from Doze mode if the PMI event is enabled to generate SMI: ⁽¹⁾		Reserved	
000 = No delay (Default)		100 = 64ms		0 = No 1 = Yes		ATCLK, ATCLK/2 status in Suspend: 0 = Depends on 66h[6] 1 = Driven low	
001 = 1ms		101 = 256ms					
010 = 4ms		110 = 1s					
011 = 16ms		111 = 4s					
(1) For example, to let PMI#11 reset the Doze mode without generating SMI to the CPU, SYSCFG 5Ah[7:6] must be set to 11b and SYSCFG 5Bh[6] must be set.							



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Doze Reset Inside SMM

The 82C558N allows an SMI to reset Doze mode if STPCLK# is active from within System Management Mode. SYSCFG 65h[4] in the 82C558N enables Doze mode reset when the SMI signal goes active, but since SMI is masked on entry to SMM, an SMI triggered while the system is in SMM is not seen until some other trigger resets Doze mode.

Setting SYSCFG 79h[4] = 1 handles Doze reset only from within SMM. Set SYSCFG 65h[4] = 1 to handle SMI Doze mode exit from outside of SMM.

Table 4-76 Register Bits that Select Doze Mode Reset Events

7	6	5	4	3	2	1	0
SYSCFG 41h DOZE_TIMER Register 2 Default = 00h							
DOZE_0 time-out select: 000 = 2ms 001 = 4ms 010 = 8ms 011 = 32ms 100 = 128ms 101 = 512ms 110 = 2s 111 = 8s Time-out generates PMI#27.			Doze mode STPCLK# modulation (STPCLK# modulated by BCLK defined in E6h[7:6]): 000 = No Modulation (STPCLK# = 1) 001 = STPCLK# $t_{HI} = 0.75 * 16$ BCLKs 010 = STPCLK# $t_{HI} = 0.5 * 16$ BCLKs 011 = STPCLK# $t_{HI} = 0.25 * 16$ BCLKs 100 = STPCLK# $t_{HI} = 0.125 * 16$ BCLKs 101 = STPCLK# $t_{HI} = 0.0625 * 16$ BCLKs 110 = STPCLK# $t_{HI} = 0.03125 * 32$ BCLKs 111 = STPCLK# $t_{HI} = 0.015625 * 64$ BCLKs			ACCESS events reset doze mode: 0 = Disable 1 = Enable	Doze control select: 0 = Hardware 1 = Software
SYSCFG 62h IRQ Doze Register 1 Default = 00h							
IRQ13 Doze reset: 0 = Disable 1 = Enable	IRQ8 Doze reset: 0 = Disable 1 = Enable	IRQ7 Doze reset: 0 = Disable 1 = Enable	IRQ12 Doze reset: 0 = Disable 1 = Enable	IRQ5 Doze reset: 0 = Disable 1 = Enable	IRQ4 Doze reset: 0 = Disable 1 = Enable	IRQ3 Doze reset: 0 = Disable 1 = Enable	IRQ0 Doze reset: 0 = Disable 1 = Enable
SYSCFG A2h IRQ Doze Register 2 Default = 00h							
PCI/VL bus I/O access Doze reset: 0 = Disable 1 = Enable	PCI/VL memory access Doze reset: 0 = Disable 1 = Enable	IRQ15 Doze reset: 0 = Disable 1 = Enable	IRQ14 Doze reset: 0 = Disable 1 = Enable	IRQ11 Doze reset: 0 = Disable 1 = Enable	IRQ10 Doze reset: 0 = Disable 1 = Enable	IRQ9 Doze reset: 0 = Disable 1 = Enable	IRQ6 Doze reset: 0 = Disable 1 = Enable
SYSCFG 65h Doze Register Default = 00h							
All interrupts to CPU reset Doze mode: 0 = Disable 1 = Enable	Reserved	EPMI0# Doze reset: 0 = Disable 1 = Enable	Recognize SMI during STPCLK#: 0 = No 1 = Yes	IRQ1 Doze reset: 0 = Disable 1 = Enable	EPMI3# Doze reset: 0 = Disable 1 = Enable	EPMI2# Doze reset: 0 = Disable 1 = Enable	EPMI1# Doze reset: 0 = Disable 1 = Enable

4.14.2.2.2 Automatic (Hardware) Doze Mode

The chipset can be set up for hardware-controlled slowdown Doze mode by programming the following information.

1. Set up the hardware and programming to consider the stop clock mechanism as described in the Section 4.14.2.1, "STPCLK# Mechanism to Control CPU Power Dissipation".
2. Program the events that will reset Doze mode as described in the Section 4.14.2.2.1, "Presetting Events to Reset Doze Mode".
3. Associate the access event with their time-out counters (DOZE_0 or DOZE_1), by appropriately programming SYSCFG 76h through 78h.
4. Select the desired time-outs, that is, the time required after the last event before the system can be considered "inactive," in SYSCFG 41h[7:5] and in 79h[7:5]. A two second (2s) time-out is typical.
5. Select the STPCLK# duty cycle from SYSCFG 41h[4:2]. Time t_{hi} is defined as that time for which STPCLK# is not asserted in one 32kHz period.
6. Set SYSCFG 66h[5] = 0 for slowdown.
7. Set SYSCFG 65h[4] = 1 if the chipset should exit Doze mode for SMIs, or = 0 if the SMIs can run adequately at the Doze speed.
8. Finally, enable the hardware DOZE_TIMER by setting SYSCFG 41h[0] = 0.

After the selected period of inactivity, the hardware Doze mode is entered and the STPCLK# signal is modulated. In the event of any of the enabled accesses, SMIs, or IRQs, the CPU is switched back to full speed operation, and the Doze timer associated with the access event is reloaded.

4.14.2.2.3 APM (Software) Doze Mode

The Viper-N Chipset can be set up for software-initiated, reduced CPU power consumption or maximum power saving mode in a very straightforward manner.

1. Set up the hardware and programming to consider the stop clock mechanism as described in the "Clock Speed Control for CPU Clocks" section.
2. Program the events that will reset the Doze mode as described in the Section 4.14.2.2.1, "Presetting Events to Reset Doze Mode".
3. Set SYSCFG 65h[4] = 1 if the Viper-N Chipset should exit Doze mode for SMIs, or = 0 if the SMIs can run adequately at the Doze speed. Obviously, SYSCFG 65h[4] must be set to 1 if maximum power savings is desired, or else the SMI will be missed altogether.
4. Select the duty cycle for STPCLK# from SYSCFG 41h[4:2].
5. Disable the hardware DOZE_TIMER by setting SYSCFG 41h[0] = 1.

At this point the system is ready for APM control. When APM makes a call for low or very low power operation, the BIOS or power management code simply:

- For reduced CPU power consumption: Sets SYSCFG 66h[5] = 0, and bit 65h[6] = 1
– or –
For maximum power savings mode: Sets SYSCFG 65h[6] = 1 and bit 66h[5] = 1
- Sets SYSCFG 50h[3] = 1 to initiate the Doze mode

On the event of any of the enabled ACCESSES, SMIs, or IRQs, the clock to the CPU core will be enabled all the time, until the above two steps are repeated again.

Table 4-77 Hardware and Software Doze Mode Registers

7	6	5	4	3	2	1	0	
SYSCFG 76h Doze Reload Select Register 1								Default = 0Fh
LCD_ACCESS: 0 = DOZE_0 1 = DOZE_1	KBD_ACCESS: 0 = DOZE_0 1 = DOZE_1	DSK_ACCESS: 0 = DOZE_0 1 = DOZE_1	HDU_ACCESS: 0 = DOZE_0 1 = DOZE_1	COM1&2_ACCESS: 0 = DOZE_0 1 = DOZE_1	LPT_ACCESS: 0 = DOZE_0 1 = DOZE_1	GNR1_ACCESS: 0 = DOZE_0 1 = DOZE_1	GNR2_ACCESS: 0 = DOZE_0 1 = DOZE_1	
SYSCFG 77h Doze Reload Select Register 2								Default = 00h
IRQ8: 0 = DOZE_0 1 = DOZE_1	IRQ7: 0 = DOZE_0 1 = DOZE_1	IRQ6: 0 = DOZE_0 1 = DOZE_1	IRQ5: 0 = DOZE_0 1 = DOZE_1	IRQ4: 0 = DOZE_0 1 = DOZE_1	IRQ3: 0 = DOZE_0 1 = DOZE_1	IRQ1: 0 = DOZE_0 1 = DOZE_1	IRQ0: 0 = DOZE_0 1 = DOZE_1	
SYSCFG 78h Doze Reload Select Register 3								Default = 00h
PCI/VL: 0 = DOZE_0 1 = DOZE_1	IRQ15: 0 = DOZE_0 1 = DOZE_1	IRQ14: 0 = DOZE_0 1 = DOZE_1	IRQ13: 0 = DOZE_0 1 = DOZE_1	IRQ12: 0 = DOZE_0 1 = DOZE_1	IRQ11: 0 = DOZE_0 1 = DOZE_1	IRQ10: 0 = DOZE_0 1 = DOZE_1	IRQ9: 0 = DOZE_0 1 = DOZE_1	
SYSCFG 7Ah GNR3 Base Address Register 1								Default = 00h
GNR3_ACCESS base address: A[13:6] for memory watchdog or A[15:10] for I/O (right-aligned).								
SYSCFG 41h DOZE_TIMER Register 2								Default = 00h
DOZE_0 time-out select: 000 = 2ms 001 = 4ms 010 = 8ms 011 = 32ms 100 = 128ms 101 = 512ms 110 = 2s 111 = 8s Time-out generates PMI#27.		Doze mode STPCLK# modulation (STPCLK# modulated by BCLK defined in E6h[7:6]): 000 = No Modulation (STPCLK# = 1) 001 = STPCLK# $t_{HI} = 0.75 * 16$ BCLKs 010 = STPCLK# $t_{HI} = 0.5 * 16$ BCLKs 011 = STPCLK# $t_{HI} = 0.25 * 16$ BCLKs 100 = STPCLK# $t_{HI} = 0.125 * 16$ BCLKs 101 = STPCLK# $t_{HI} = 0.0625 * 16$ BCLKs 110 = STPCLK# $t_{HI} = 0.03125 * 32$ BCLKs 111 = STPCLK# $t_{HI} = 0.015625 * 64$ BCLKs			ACCESS events reset doze mode: 0 = Disable 1 = Enable		Doze control select: 0 = Hardware 1 = Software	
SYSCFG 79h PMU Control Register 11								Default = 00h
DOZE_1 time-out select: 000 = No delay (Default) 100 = 64ms 001 = 1ms 101 = 256ms 010 = 4ms 110 = 1s 011 = 16ms 111 = 4s		PMI# event triggers exit from Doze mode if the PMI event is enabled to generate SMI: ⁽¹⁾ 0 = No 1 = Yes	Reserved			ATCLK, ATCLK/2 status in Suspend: 0 = Depends on 66h[6] 1 = Driven low		
⁽¹⁾ For example, to let PMI#11 reset the Doze mode without generating SMI to the CPU, SYSCFG 5Ah[7:6] must be set to 11b and SYSCFG 5Bh[6] must be set.								
SYSCFG 50h PMU Control Register 4								Default = 00h
Software start SMI: 0 = Clear SMI 1 = Start SMI	Reserved	IRQ8 polarity: 0 = Active low 1 = Active high	14.3MHz to 82C558N: 0 = Enable 1 = Disable	Write = 1 to start Doze Read: Doze status 0 = Counting 1 = Timed out	Ready to Resume (RO): 0 = Not in Resume 1 = Ready to Resume	PMU mode (RO): 0 = Nothing pending 1 = Suspend active (clear PMI#6)	Start Suspend (WO): 1 = Enter Suspend mode	

4.14.2.2.4 Start Doze Bit

SYSCFG 50h[3] serves two purposes: to start the Doze mode and to read the DOZE_TIMER status.

- Write: Start APM Doze mode
 - 1 = Start Doze mode (if SYSCFG 40h[0]=1)
 - 0 = No effect
- Read: Hardware DOZE_TIMER time-out status bit
 - 1 = Hardware DOZE_TIMER has timed out
 - 0 = Hardware DOZE_TIMER still counting

4.14.2.2.5 Using Doze Time-out to Trigger an SMI

In addition to the ability to reset the Doze mode when an SMI is encountered, the 82C558N has the ability to generate PMI#27 when the DOZE_TIMER times out. Setting SYSCFG D9h[7:6] = 11 enables the PMI to generate an SMI.

4.14.2.3 DEVSEL# Doze Reset

Activity on the PCI bus can reset the Doze mode and cause a return to full operating speed. The 82C558N logic provides two bits to enable Doze reset separately for PCI I/O accesses and memory accesses. The Doze reset is triggered by DEVSEL# going active and is qualified by the M/IO# signal.

Table 4-78 SMI Generation on Doze Time-Out

7	6	5	4	3	2	1	0	
SYSCFG D9h				PMU Event Register 6				Default = 00h
DOZE_TIMER PMI#27 SMI: 00 = Disable 01 = Enable DOZE_0 10 = Enable DOZE_1 11 = Enable both		RINGI PMI#26 SMI: 00 = Disable 11 = Enable		EPMI3# cool-down clocking PMI#25 SMI: 00 = Disable 11 = Enable		EPMI2# PMI#24 SMI: 00 = Disable 11 = Enable		

Table 4-79 PCI Bus Doze Reset Registers

7	6	5	4	3	2	1	0	
SYSCFG A2h				IRQ Doze Register 2				Default = 00h
PCI/VL bus I/O access Doze reset: 0 = Disable 1 = Enable	PCI/VL mem-ory access Doze reset: 0 = Disable 1 = Enable	IRQ15 Doze reset: 0 = Disable 1 = Enable	IRQ14 Doze reset: 0 = Disable 1 = Enable	IRQ11 Doze reset: 0 = Disable 1 = Enable	IRQ10 Doze reset: 0 = Disable 1 = Enable	IRQ9 Doze reset: 0 = Disable 1 = Enable	IRQ6 Doze reset: 0 = Disable 1 = Enable	
SYSCFG 78h				Doze Reload Select Register 3				Default = 00h
PCI/VL: 0 = DOZE_0 1 = DOZE_1	IRQ15: 0 = DOZE_0 1 = DOZE_1	IRQ14: 0 = DOZE_0 1 = DOZE_1	IRQ13: 0 = DOZE_0 1 = DOZE_1	IRQ12: 0 = DOZE_0 1 = DOZE_1	IRQ11: 0 = DOZE_0 1 = DOZE_1	IRQ10: 0 = DOZE_0 1 = DOZE_1	IRQ9: 0 = DOZE_0 1 = DOZE_1	



4.14.3 CPU Thermal Management Unit

Thermal management hardware is implemented in the 82C558N for monitoring the level of CPU activity and the operating temperature of the device. A flexible hardware scheme assesses CPU activity to determine when it is necessary to enter cool-down clocking mode. In addition, an external sensor can force the 82C558N permanently into the cool-down clocking mode according to the parameters programmed for thermal management. In this way, a serious over-temperature condition cannot get out of control.

4.14.3.1 Prediction of Overtemp Activity

Thermal management hardware is implemented in the 82C558N for monitoring the level of CPU activity to determine its current draw, and thus approximate the operating temperature of the device. The most obvious way to do this would be to simply count the number of CPU clocks that occur in a given time period. However, a ripple counter running in the 20-40MHz range would consume a great deal of power. Instead, the 82C558N logic assesses CPU activity periodically and keeps track of how often the CPU exceeds the safety limits to determine whether automatic intervention is called for.

4.14.3.2 Operating Temperature Ranges

The 82C558N thermal management algorithm identifies the temperature limits of the CPU through activity level values that correspond with idle, equilibrium, and thermal runaway conditions.

Idle Condition

The CPU is cool to the touch. The 82C558N is using APM stop clock or hardware Doze mode to save power, and no real activity is taking place. This operational level constitutes the base level of activity, so it does not require a register to hold the value. It is associated in the 82C558N thermal management scheme with "zero".

Equilibrium Condition

The CPU is warm to the touch. It is operating at full capacity for short bursts but frequently is in low power modes. The heat generated by the CPU is dissipated at the same rate that it is produced. Most active computer usage falls into this category, where APM or hardware Doze mode operates frequently enough to allow safe operation. The 82C558N thermal management scheme associates this temperature with Equilibrium Level bits EQL[6:0]. The value of these bits is referred to as EQL throughout this section.

Thermal runaway Condition

The CPU is hot to the touch. It is running at its full rated speed and generating heat faster than it can be dissipated, so its temperature increases. The program being used is active enough that APM or hardware Doze mode cannot operate often enough to hold the temperature down. Operating in this mode for an extended period may cause the CPU to fail. The 82C558N thermal management scheme associates this temperature with Overtemp Limit bits OTL[7:0]. The value of these bits is referred to as OTL throughout this section.

4.14.3.3 Accounting for CPU Activity

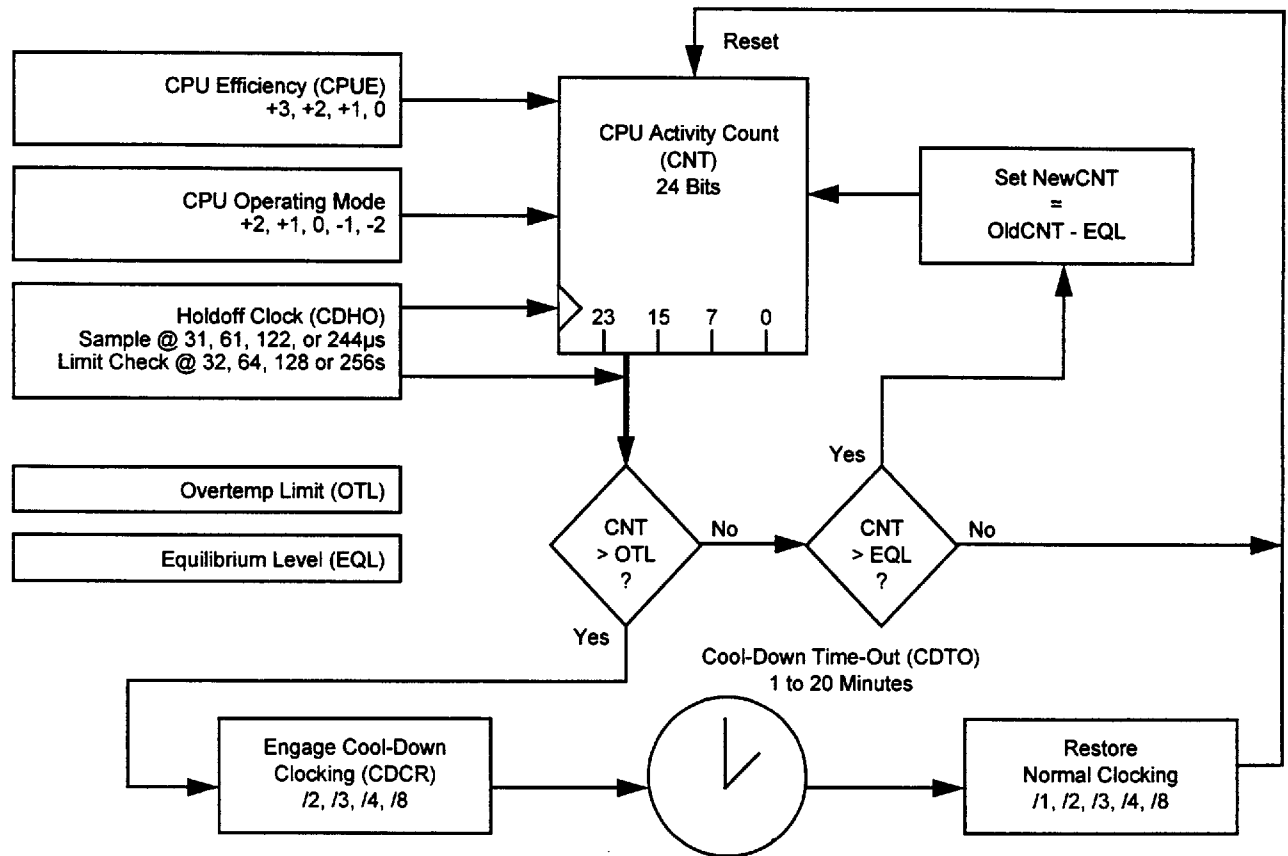
The 82C558N logic frequently assesses CPU activity, according to the current CPU running mode. The CPU could be in different power consumption modes depending on the duty cycle of the STPCLK# signal (see Section 4.14.2.1, "STPCLK# Mechanism to Control CPU Power Dissipation" for more details). Each CPU run mode is associated with a power level increment as shown in Table 4-80. Using these values, the 82C558N can keep a running tally of the average power being used by the CPU in the internal 24-bit CPU Activity Counter (CNT). See Figure 4-40 for implementation details.

The 82C558N must also be able to account for the CPU type. For example, a Pentium processor operating with an internal frequency of 100MHz will tend to heat up much faster at full speed, yet will cool down at approximately the same rate as a processor running at an internal frequency of 75MHz. The CPU Efficiency bits CPUE[1:0] are used to indicate the relative CPU current consumption and are explained next.

Table 4-80 Operating Mode Power Levels

Current CPU Operating Mode	Power Level Increment
Full Speed	+2
STPCLK# $t_{HI} = 0.75 * 31.25\mu s$	+1
STPCLK# $t_{HI} = 0.5 * 31.25\mu s$	0
STPCLK# $t_{HI} = 0.25 * 31.25\mu s$	-1
STPCLK# $t_{HI} = (0.125, \text{ or } 0.0625) * 31.25\mu s$	-2
APM Maximum Power Savings Mode	-2

Figure 4-40 Thermal Management Block Diagram



The thermal management hardware keeps track of CPU activity as follows. The logic checks the current CPU operating mode either 32k, 16k, 8k, or 4k times per second according to the CDHO[1:0] bits setting (as explained below). The thermal management logic notes the current operating mode to account for the instantaneous CPU current consumption by incrementing or decrementing the CPU Activity Counter as follows.

- For all CPU operating modes, the logic increments or decrements the counter by the value listed in Table 4-80 for the operating mode at that time.
- Only for those modes with a power level increment above zero, the logic also increments the CPU activity counter by the CPU Efficiency bits value.

For example, if the CPU is sampled at full speed (+2), and CPUE[1:0] = 2, the activity counter will be incremented by 4. However, if the CPU is sampled at divide by 8 (-1), the counter will simply be decremented by 1; the CPUE value is not added in if the power level increment is zero or below.

4.14.3.4 Operating Temperature Range Determination

Periodically, the thermal management logic compares the upper byte of the CPU activity counter to the Overtemp Limit (OTL) and to the Equilibrium Level (EQL). This comparison takes place every 32, 64, 128, or 256 seconds as programmed in the Cool-down Holdoff bits (CDHO[1:0]). These bits also select the frequency of sampling, at 32KB, 16KB, 8KB, or 4KB times per second respectively, such that the value accumulated in the CPU activity count will, on average, be the same whether a short or a long holdoff period is selected. The logic acts on the comparison results as follows.

- If the upper byte of the activity count is greater than or equal to OTL, the thermal management unit initiates cool-down clocking.
- If the upper byte of the activity count is above EQL but below OTL, EQL is subtracted from the upper byte of the CPU Activity Counter and the result is returned to the counter. This scheme handles operation consistently above equilibrium level that may, over time, result in excessively high CPU temperatures.

- If the upper byte of the activity count is equal to or below EQL, the CPU Activity Counter is simply cleared and the thermal management logic starts a new detection period from "zero" (idle condition).

Cool-down Clocking

Cool-down clocking takes place according to the reduced clock rate programmed into the Cool-down Clock Rate bits CDCR[1:0]. The 82C558N keeps the CPU running at the cool-down clocking rate speed for the Cool-down Holdoff period times the Cool-down Time-out value programmed. At the end of the period, the activity counter is cleared and normal clocking is restored. No activity accounting takes place while cool-down clocking is engaged.

4.14.3.4.1 Example

A 3.3V Pentium processor is used in a 50MHz system with its BF pin pulled low, resulting in an internal clock of 100MHz. The cool-down clock rate is set so that STPCLK# modulation is at 1/4. The CPU Efficiency bits are set to 3 because of the high internal clock frequency. Cool-down Holdoff is set for 64 seconds; Cool-down Time-out is set for 3x; the Equilibrium Level is set to 40h; and the Overtemp Limit is set to 7Fh.

Consider the situation after the CPU has run at full speed for one minute. The thermal management hardware is checking the CPU operating mode every 61 μ s (16,384 times per second), and each time increments the CPU Activity Counter by two to account for the CPU running at full speed and then by three to account for the CPU Efficiency setting. Thus, the count is incremented by 16,384 x 5 each second for 64 seconds, for a total count of 500000h. The value of the high byte is 50h; this value is compared to EQL, which was set to 40h. Since the activity count exceeds the equilibrium level, EQL is subtracted from the activity count and the result (10h) remains in the counter. However, the activity count of 50h does not exceed the OTL value of 7Fh. Therefore, no other action is taken.

Now consider the situation after the CPU has run at full speed for four minutes. After each 64-second interval, the high-order activity count byte has been incremented by 50h, and after the OTL comparison is made the EQL value of 40h has been subtracted off for a net increase of 10h. So after four minutes of operation, when the OTL comparison is made, the activity count of 80h is compared to the OTL value of 7Fh and an over limit situation is detected.

Therefore, the thermal management hardware engages cool-down clocking for three minutes (3 x 64 seconds). During this phase, the clock to the CPU core is cut off and turned on periodically (base frequency 32kHz), with the high time of the STPCLK# signal set to 1/(4*32kHz). It then resets the CPU Activity Counter, Resumes normal clocking and monitoring, and starts the whole detection process over again.

This situation would have been avoided if the APM stop clock mode had been entered for at least 10 seconds during each 64-second period. In that case, the thermal management hardware would have counted (16384 x 5 x 54) + (16384 x 2 x 10) = 3E8000h each time, just under the 40h equilibrium limit. The CPU Activity Counter would have been reset each time and no thermal buildup would have been detected.

4.14.3.4.2 Programming

Before programming thermal management, the STPCLK# mechanism must be set up for the CPU being used as described in Section 4.14.2.1, "STPCLK# Mechanism to Control CPU Power Dissipation". Enabling thermal management locks the STPCLK# bits and prevents them from being altered until the next hardware reset.

The thermal management option must be configured by setting the bits in SYSCFG A5h, A6h, and A7h, and then setting SYSCFG A5h[7] = 1. The register setting order is not important, but bit 7 of A5h must be set to 1 only after all other settings have been made. Once bit 7 is set, none of the thermal management registers, nor SYSCFG 61h[2] and 66h[0], can be written again without resetting the 82C558N device.

If the Doze mode is in progress when the thermal management unit engages (or vice-versa), the lower value of t_{hi} as set by the two schemes for STPCLK# modulation will be used.

4.14.3.4.3 SMI Generation

When the thermal management unit engages or disengages cool-down clocking, an SMI on PMI#25 can be generated. This feature is controlled through SYSCFG DBh[6]. When this SMI is being serviced, power management code can read SYSCFG A5h[7] to determine whether it was an entry into or an exit from cool-down clocking mode that caused the SMI.

PMI#25 is also shared with the EPMI3# event. If the SMI from EPMI3# is also enabled, on entry to the SMI software must check the state of the EPMI3# signal to determine whether the reason for the SMI is the external EPMI3# event or cool-down clocking entry/exit.

4.14.3.5 Emergency Overtemp Sense

It is possible for an external sensor to force the 82C558N permanently into cool-down clocking mode according to the parameters programmed for thermal management. When low, the EPMI1# input can cause the 82C558N to enter cool-down clocking mode. The existing SMI enable bits for EPMI1# are still operational regardless of the setting of the emergency overtemp enable bit. Therefore, an overtemp condition can also be programmed to cause an SMI so that the power management firmware will be made aware of the situation and instruct the user to shut down the system. In this way, a serious over-temperature condition cannot get out of control.

The chip will remain in cool-down clocking mode, using the rate specified in Thermal Management Register 3 (defaults to a 50% duty cycle for STPCLK#), as long as the EPMI1# input remains triggered. The trigger specifications are the same as those for triggering the SMI: SYSCFG 40h[2] selects whether a high- or a low-level is active, and this same bit selects whether a high- or a low-level will engage cool-down clocking. The thermal management unit does not need to be enabled to use this feature.

EPMI1# can be used as the overtemp sense input even when the EPMI1# function has been moved to an external 74153 multiplexer (when the standard DACKMUX interface feature has been selected).

4.14.3.5.1 Programming

This option is enabled by writing a bit in the Feature Control Register (described later in this document). Once written, this bit cannot be changed without a hard reset of the chip.

When SYSCFG DBh[6] = 1, entry into or exit from cool-down clocking mode causes PMI#25 and an SMI. If the EPMI1# event is also programmed to cause an SMI, the following situation can occur.

1. The thermal sensor input changes state, causing PMI#2 and an SMI.
2. Power management code services the SMI.
3. The thermal management unit enters cool-down clocking mode.
4. At this point, PMI#25 is generated along with *another* SMI.

Therefore, two SMIs will have been generated. On exit from cool-down clocking mode, only *one* SMI will be generated, since the active-to-inactive transition on EPMI1# does not cause another SMI. Power management software must be able to anticipate this situation and deal with it appropriately.

Table 4-81 Thermal Management Registers

7	6	5	4	3	2	1	0
SYSCFG A5h Thermal Management Register 1 Default = 00h							
Thermal Mgmt.:		Equilibrium Level (EQL[6:0]):					
0 = Disable 1 = Enable		This count corresponds to equilibrium operation. If the CPU Activity Counter exceeds EQL, EQL is simply subtracted from the upper activity count byte and sampling continues. If the count is below EQL, the count is cleared.					
SYSCFG A6h Thermal Management Register 2 Default = 00h							
Overtemp Limit (OTL[7:0]):							
This count corresponds to an over-temperature situation. If the CPU Activity Counter exceeds OTL, the 82C558N engages cool-down clocking.							
SYSCFG A7h Thermal Management Register 3 Default = 00h							
CPU efficiency (CPUE[1:0]):		Cool-down holdoff (CDHO[1:0]):		Reserved (See SYSCFG AAh[7:5])		Cool-down time-out (CDTO[1:0]):	
00 = Low power 01 = Moderate 10 = High 11 = Very high		00 = 32 seconds 01 = 64 seconds 10 = 128 seconds 11 = 256 seconds				00 = 2x CDHO 01 = 3x 10 = 4x 11 = 5x	
SYSCFG A5h Thermal Management Register 1 Default = 00h							

Thermal management enable, SYSCFG A5h[7] - Once written to 1, none of the thermal management registers can be cleared without a system reset. When read, this bit returns 1 only if cool-down clocking is currently taking place.

Cool-down holdoff, SYSCFG A7h[5:4] - Specify the time period of observation to allow before checking whether to enable cool-down clocking.

Cool-down clock rate, SYSCFG A7h[3:2] - Specify the STPCLK# modulation duty cycle to use during cool-down clocking.

Cool-down time-out, SYSCFG A7h[1:0] - Specify the length of time, in terms of the cool-down holdoff selected, that the cool-down clocking will continue before normal operation is restored.



4.14.4 Suspend and Resume

The 82C558N offers the ability to halt operations at extremely low power yet retain all its programming, called Suspend. The Viper-N Chipset will respond to interrupts to determine that a return to normal operation, called Resume, is necessary.

4.14.4.1 Suspend Mode

Suspend mode provides a significant level of power conservation. The Suspend initiation event, either a key or button depression or a time-out SMI, calls a software routine in SMM code to save the current state of the system for complete restoration at some later time. In this mode, most system power can be shut down while still retaining restorability. The lowest power consumption mode is that in which the DRAM is kept powered up (the system state is stored in the DRAM), the CPU is powered off, and the cache is also powered off. The 82C558N enters the Suspend mode when SYSCFG 50h[0] is set to 1. Software must control this event, even though a timer time-out may have initiated the process, because CPU processing must be completed in an orderly manner. Upon resuming from the Suspend mode, the controlling code **must** clear the Suspend PMI Event, PMI#7, by writing SYSCFG 5Ch[7] = 1. Otherwise, the 82C558N will never exit the Suspend mode the next time SYSCFG 50h[0] is set to 1.

The registers shown in Table 4-82 select the state of various signals during the Suspend mode. SYSCFG 59h[6] is used so that the system timers can be restarted to prevent false time-outs upon resuming from the Suspend mode. Refer to the Section 4.14.5, "Resume Event", to determine how to select the events that will cause the 82C558N to Resume operation after Suspend.

4.14.4.1.1 Suspend Mode Power Savings

While in the Suspend mode, the 82C558N can be programmed to save power in two ways: short-pulse refresh for normal DRAM or self-refresh for self-refresh DRAM, and slow interrupt scan.

4.14.4.1.2 Suspend Mode Refresh

The Suspend refresh rate is selected by programming the SYSCFG 12h[5:4] and/or 12h[3:2]. During the Suspend mode, refresh can be:

1. slow refresh based on the REFRESH#/32KHZ input to the 82C557, with a wide RAS# pulse width,
2. self-refresh initiated by 32kHz, or
3. short pulse width refresh based on the 32kHz clock.

The first option generates refresh in the same manner that refresh is generated during normal mode, with the RAS pulse width determined by SYSCFG 01h[5:4]. The second option can be used for self-refresh DRAMs with the initial control required to put the DRAM in self-refresh mode based on the 32kHz clock. The short pulse refresh mechanism is engaged for lowest DRAM power consumption during Suspend. In this mode, the refresh is based on the 32kHz clock, but the refresh pulse width is 100ns only. This pulse width is capable of retaining the DRAM data and results in lowest power consumption.

4.14.4.1.3 Multiplexed Inputs Scan Rate

The logic can scan for multiplexed inputs to the 82C558N interrupts at a slower rate during refresh. During normal mode, the sample rate is governed by the internally generated ATCLK. During Suspend mode, SYSCFG ADh[6] controls the frequency of ATCLK, and therefore, the sampling frequency. Note that a major reduction of power consumption can come from switching off all the clocks except the 32kHz clock during Suspend.

4.14.4.1.4 Suspend Mode HOLD Control

Asserting HOLD before stopping the clock is a common method used to tristate the CPU signals during Suspend, resulting in lower power consumption. Setting the Suspend mode HOLD control SYSCFG 66h[4] = 1 overrides this control, and is useful for zero volt CPU Suspend where all signals to the CPU must stay low.

Table 4-82 Suspend Control Register Bits

7	6	5	4	3	2	1	0
SYSCFG ADh Feature Control Register 3 Default = 00h							
Reserved		CPU power state in Suspend: 0 = Powered 1 = 0 volt	Reserved	INIT operation: 0 = Normal 1 = Toggle on Resume	Reserved		
SYSCFG 59h PMU Event Register 2 Default = 00h							
Allow software SMI: 0 = Disable 1 = Enable	Reload timers on Resume: 0 = No 1 = Yes	Resume INTRGRP PMI#6, Suspend PMI#7 SMI: 00 = Disable 11 = Enable	R_TIMER PMI#5 SMI: 00 = Disable 11 = Enable		IDLE_TIMER PMI#4 SMI: 00 = Disable 11 = Enable		
SYSCFG 50h PMU Control Register 4 Default = 00h							
Software start SMI: 0 = Clear SMI 1 = Start SMI	Reserved	IRQ8 polarity: 0 = Active low 1 = Active high	14.3MHz to 82C558N: 0 = Enable 1 = Disable	Write = 1 to start Doze Read: Doze status 0 = Counting 1 = Timed out	Ready to Resume (RO): 0 = Not in Resume 1 = Ready to Resume	PMU mode (RO): 0 = Nothing pending 1 = Suspend active (clear PMI#6)	Start Suspend (WO): 1 = Enter Suspend mode

Table 4-83 Suspend Mode Power Saving Feature Bits

7	6	5	4	3	2	1	0
SYSCFG 66h PMU Control Register 7 Default = 00h							
Self-refresh DRAM selection: 0 = Normal 1 = Self-refresh	Suspend mode ATCLK frequency: 0 = Derived from LCLK 1 = 32kHz. (overridden by SYSCFG 79h[0])	Doze type: 0 = Modulate STPCLK# 1 = Keep STPCLK# asserted	Assert HOLD during suspend 0 = Yes 1 = No	Reserved			STPGNT cycle wait option: 0 = Do not wait 1 = Wait for STPGNT cycle before negating STPCLK#
SYSCFG 12h Refresh Control Register Default = 00h							
Reserved	Reserved	Suspend mode refresh control: 00 = Timing for refresh based on SYSCFG 12h[3:2](with refresh timing based on CLK input) 01 = Self-refresh timing (refresh pulse width equals REFRESH# low time) 10 = 100ns refresh pulse width triggered by REFRESH# 11 = Rsrvd	Slow refresh control: 00 = Refresh on every REFRESH# falling edge 01 = Refresh on one in two REFRESH# falling edges 10 = Refresh on one in four REFRESH# falling edges 11 = Refresh on every REFRESH# edge (both rising and falling)	Generate LA[23:17] from 08Fh (Refresh DMA Page Addr. Reg.) during refresh: 0 = Disable 1 = Enable	82C556 generates MP[7:4] for PCI master writes: 0 = No 1 = Yes		



4.14.5 Resume Event

A certain set of interrupt events can be enabled to Resume the system from the Suspend mode. The desired interrupts are grouped into a single event, called RSMGRP. RSMGRP can be enabled to generate an SMI if desired. The RINGI input and the SUS/RES# input can also trigger a Resume, and can also be enabled to generate an SMI if desired. Any one or more of the RSMGRP, RINGI, and SUS/RES# events are called a Resume event.

4.14.5.1 EPMI/IRQ Events

SYSCFG 6Ah and B1h select the EPMI and IRQ source(s) that will be allowed to trigger the system out of the Suspend mode. Once selected, setting SYSCFG 5Fh[5] = 1 enables the RSMGRP globally. On Resume, an SMI can be generated either from the EPMI events (through SYSCFG 58h and D9h) or PMI#6 event (through SYSCFG 59h). However, since the system usually is still in SMM when the Resume takes place, SMI generation is not normally necessary.

The IRQ and EPMI Resume enabling bits are shown in Table 4-84. Default for all bits is disabled. A rising edge on the enabled signal causes the Resume event for all selections except IRQ8; it is a falling edge on IRQ8 that Resumes operation.

4.14.5.2 SUS/RES# and RINGI Events

When the RINGI input pin changes state and back enough to exceed the count set in SYSCFG 5Fh[3:0], and SYSCFG 5Fh[4] = 1, PMI#6 is generated to exit the Suspend mode. RINGI should be high for a minimum of 240ms and low for a minimum of 60ms when changing states. The RINGI input is sampled with a 32kHz clock; therefore rapid or unstable transitions may lead to unreliable counting.

The SUS/RES# input pin is always enabled to Resume the system, and should be pulled high to VCC if it will not be used in the system design. Resuming from SUS/RES# generates PMI#7.

Once a Resume event has occurred, SYSCFG 6Bh[2:0] should be read to determine the source(s). If SYSCFG 6Bh[1] = 1, a read of SYSCFG 6Ah and B1h will return the latched state of the any of the EPMI or IRQ lines that were originally enabled for Resume triggering. The latched Resume IRQ and EPMI source information in SYSCFG 6Ah and B1h is available until the PMI#6 bit (SYSCFG 5Ch[6]) is eventually written to 1 to clear the PMI generated. SYSCFG 50h[1] = 1 as long as the Resume PMI#6 remains active.

SYSCFG 61h[5:4] controls the debounce rate and polarity of SUS/RES#. These bits function as follows:

- 00 = Active low, edge triggered PMI. PMI#7 is triggered on any high-to-low edge of SUS/RES#. Once the PMI is triggered, software must write SYSCFG 5Ch[7] = 1 to clear PMI#7 and deassert SMI#.

- To Resume: Once the system is in the Suspend mode, the next high-to-low edge on SUS/RES# will Resume operation.
- 01 = Active low, level-controlled PMI. Setting SUS/RES# low causes PMI#7 to go active; setting SUS/RES# high causes PMI#7 to go inactive. There is no latching associated with this function, so it is not necessary to write bit 5Ch[7] = 1 to deassert the SMI#.
- To Resume: A low signal on SUS/RES# generates a resume function. Therefore, hardware/software must ensure that SUS/RES# is high before going into Suspend mode; otherwise, the system will Resume immediately.
- 10 = Active high, level-sampled PMI in 16ms. SUS/RES# must be sampled high for at least three 4ms clock edges before being recognized as a PMI. Therefore, it takes a maximum of 16ms for the SUS/RES# request to be recognized. Once the PMI is triggered, software must write bit 5Ch[7] = 1 to clear PMI#7 and deassert SMI#. Also, the SUS/RES# pin must be sampled low for four clock edges (20ms maximum) before the circuit is re-armed to generate the next PMI#7.
- To Resume: Once the system is in the Suspend mode, a high level sampled on SUS/RES# for three 4ms clocks will resume operation.
- 11 = Active high, level-sampled PMI in 32ms. Same as above, but the sampling clock is 8ms instead of 4ms. Therefore, SUS/RES# must be sampled high for a maximum of 32ms before being recognized as a PMI, and must remain low for 40ms before the circuit is re-armed.
- To Resume: Once the system is in suspend mode, a high level sampled on SUS/RES# for three 8ms clocks will resume operation.

These settings make the SUS/RES# function much more practical in a design where the switch is set to one specific level to command Suspend mode, and to the other level to command Resume mode.

Example:

A notebook design incorporates a lid switch that normally leaves SUS/RES# low during operation. SYSCFG 61h[5:4] are normally set to 11. When the lid is closed, SUS/RES# goes high. The 82C558N asserts SMI# 32ms later. Software services the SMI and recognizes PMI#7 active.

The software then prepares the system for the Suspend mode and reprograms SYSCFG 61h[5:4] = 00 to prepare for Resuming. Finally, the software writes SYSCFG 50h[0] = 1 to engage the Suspend mode.

Later the lid is raised and SUS/RES# goes low. Because SYSCFG 61h[5:4] = 00, the high-to-low edge on SUS/RES# generates a resume and PMI#7. Software then writes SYSCFG 61h[5:4] back to 11, clears PMI#7 by writing bit 5Ch[7] = 1, and returns to normal operation.

Table 4-84 SUS/RES# and Resume Event Associated Register Bits

7	6	5	4	3	2	1	0		
SYSCFG 61h Debounce Register								Default = 00h	
LOWBAT, LLOWBAT debounce rate select: 00 = No debounce 01 = 250µs 10 = 8ms 11 = 500ms		SUS/RES# debounce rate select: 00 = Active low, edge-trig'd PMI 01 = Active low, level-controlled PMI 10 = Active high, level-sampled PMI in 16ms 11 = Active high, level-sampled PMI in 32ms (See Section 4.14.5.2, "SUS/RES# and RINGI Events")		PPWR0 auto- toggle in APM STPCLK mode: 0 = No PPWR0 auto-toggle 1 = Auto-toggle PPWR0 on entry and exit from APM STP- CLK mode		STPCLK# signal 0 = Disable 1 = Enable		APM STPCLK recovery time: 00 = 120µs 01 = 240µs 10 = 1ms 11 = 2ms	
SYSCFG 6Ah RSGGRP IRQ Register 1								Default = 00h	
EPMI1# Resume: 0 = Disable 1 = Enable	EPMI0# Resume: 0 = Disable 1 = Enable	IRQ8 Resume: 0 = Disable 1 = Enable	IRQ7 Resume: 0 = Disable 1 = Enable	IRQ5 Resume: 0 = Disable 1 = Enable	IRQ4 Resume: 0 = Disable 1 = Enable	IRQ3 Resume: 0 = Disable 1 = Enable	IRQ1 Resume: 0 = Disable 1 = Enable		
SYSCFG B1h RSMGRP IRQ Register 2								Default = 00h	
EPMI3# Resume: 0 = Disable 1 = Enable	EPMI2# Resume: 0 = Disable 1 = Enable	IRQ15 Resume: 0 = Disable 1 = Enable	IRQ14 Resume: 0 = Disable 1 = Enable	IRQ12 Resume: 0 = Disable 1 = Enable	IRQ11 Resume: 0 = Disable 1 = Enable	IRQ10 Resume: 0 = Disable 1 = Enable	IRQ9 Resume: 0 = Disable 1 = Enable		
SYSCFG 5Fh PMU Control Register 6								Default = 00h	
LCD_ACCESS includes ISA bus video access: 0 = Yes 1 = No	LCD_ACCESS includes local (VL/PCI) bus video access: 0 = No 1 = Yes	RSMGRP IRQs can Resume system: 0 = No 1 = Yes	Transitions on RINGI can Resume system: 0 = No 1 = Yes	Number of RINGI transitions to cause Resume					

Table 4-85 Resume Source (Read Only)

7	6	5	4	3	2	1	0	
SYSCFG 50h PMU Control Register 4								Default = 00h
Software start SMI: 0 = Clear SMI 1 = Start SMI	Reserved	IRQ8 polarity: 0 = Active low 1 = Active high	14.3MHz to 82C558N: 0 = Enable 1 = Disable	Write = 1 to start Doze Read: Doze status 0 = Counting 1 = Timed out	Ready to Resume (RO): 0 = Not in Resume 1 = Ready to Resume	PMU mode (RO): 0 = Nothing pending 1 = Suspend active (clear PMI#6)	Start Suspend (WO): 1 = Enter Suspend mode	
SYSCFG 6Bh Resume Source Register (RO)								Default = 00h
Drive REFRESH# low during Suspend: 0 = No 1 = Yes	Reserved			SUS/RES# caused Resume: 0 = No 1 = Yes	RSMGRP caused Resume: 0 = No 1 = Yes	RINGI caused Resume: 0 = No 1 = Yes		



4.14.6 Chip-Level Power Conservation Features

A central design goal of the Viper-N Chipset was to incorporate power-reducing features wherever possible. To this end, several innovative methods of power conservation are implemented.

4.14.6.1 Automatic Keeper Resistors

Since there are times during normal operation in which the CPU tristates many of its output signals and no other source is driving these signals, the lines tend to float between logic transition levels. When this results in an oscillation, a substantial amount of current is consumed. For this reason, pull-up or pull-down resistors are typically connected on these lines through external resistor packs. Even if resistors are integrated into the chipset itself, considerable current would be consumed during normal operation when the logic is active and is driving against these resistors.

By appropriately strapping the 82C556, it can be made to automatically engage pull-down resistors on the CPU data bus and pull-ups on the memory data bus when the bus is idle. The 82C557 has keeper resistors that are automatically engaged as summarized in Table 3-9 (in Section 3.4, "82C557 Suspend Mode Support"). The keeper resistors on the 82C558N are engaged as summarized in Table 3-19 (in Section 3.7, "82C558N Suspend Mode Support").

4.14.6.2 Zero Volt CPU Suspend

The CPU interface of the Viper-N Chipset provides a zero volt Suspend option. Setting SYSCFG 18h[3], 18h[0], and ADh[5] = 1 enables zero volt CPU Suspend support. When set, the 82C557 and 82C558N will condition their outputs during Suspend assuming that the CPU has been powered down completely. The list of affected output signals are summarized in Table 3-9 and Table 3-19 (in the Signal Descriptions Sections for the 82C557 and 82C558N, respectively). Signals that would normally be maintained high to the CPU while in the Suspend mode are instead tristated.

This feature is generally used in conjunction with a feature on the INIT pin which, in this case, is used as the general purpose CPU reset (not as a software reset). By setting SYSCFG ADh[3] = 1, the INIT signal will toggle on Resume from Suspend to reset a CPU that has been powered down.

4.14.6.3 Stopping IPC Clock When Not In Use

Setting SYSCFG 50h[5] = 0 stops the clock going to the internal integrated 82C206. Primarily this setting affects the 8254-type clock/timer/counter circuit. If the timer will not be used to maintain the system clock, substantial power savings can be achieved by disabling this clock, and turning off the OSC clock generator if possible.

Table 4-86 Keeper Resistors, 0V CPU Suspend, and Stopping IPC Clock Register Bits

7	6	5	4	3	2	1	0
SYSCFG A0h Feature Control Register 1							
Default = 80h							
16-bit I/O decoding: 0 = Disable 1 = Enable	Global enable for automatic internal resistors: 0 = Disable 1 = Enable	Reserved					
SYSCFG 18h Signal State Control Register							
Default = 00h							
Reserved	CAS[X]# 3.3V/5.0V selection: 0 = 5.0V drive on CAS[X]# lines 1 = 3.3V drive on CAS[X]# lines	Drive strength on memory address lines, RAS lines, and write enable line: 0 = 4mA 1 = 16mA	CPU status during Suspend: 0 = Powered on 1 = Powered off	PCI bus tristate control during Suspend: 0 = PCI bus parked by 82C557 1 = Tristate ⁽¹⁾	Cache status during Suspend: 0 = Powered on 1 = Powered off	Global 82C557 leakage control: 0 = Disable 1 = Enable	
(1) Tristate AD[31:0], FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, C/BE#[3:0].							
SYSCFG ADh Feature Control Register 3							
Default = 00h							
Reserved	CPU power state in Suspend: 0 = Powered 1 = 0 volt	Reserved	INIT operation: 0 = Normal 1 = Toggle on Resume	Reserved			
SYSCFG 50h PMU Control Register 4							
Default = 00h							
Software start SMI: 0 = Clear SMI 1 = Start SMI	Reserved	IRQ8 polarity: 0 = Active low 1 = Active high	14.3MHz to 82C558N: 0 = Enable 1 = Disable	Write = 1 to start Doze Read: Doze status 0 = Counting 1 = Timed out	Ready to Resume (RO): 0 = Not in Resume 1 = Ready to Resume	PMU mode (RO): 0 = Nothing pending 1 = Suspend active (clear PM#6)	Start Suspend (WO): 1 = Enter Suspend mode



4.14.7 Power Control Latch

There are 16 peripheral power pins (PPWR[15:0]) that are used to control power to individual peripherals through external 74373 latches. Each latch pin is controlled with its individual control bits in SYSCFG 54h, 55h, ABh, and EEh.

The value latched by PPWRL from the SA bus extends from PPWR15 through PPWR0, providing useful power control signals for up to 16 devices if all 16 bits are latched.

4.14.7.1 Hardware Considerations

The power control scheme uses the ISA bus SS[7:0] signals to additionally provide the inputs to a 74373-type latch. If all 16 signals will be used, two '373 devices are needed. The PPWRL1 and PPWRL0 signals from the 82C558N are active high and latch the SA[7:0] signals on the latch output on their falling edges.

The pins PPWR1 and PPWR0 have a recovery delay time associated with them when doing the Suspend/Resume function. These two pins can be used as a delay control for some component that needs some time to become stable once

power is restored. For example, after turning off the power to the clock oscillator during the Suspend mode, the Resume function will restore power to the clock oscillator and wait until the clock has had time to stabilize before continuing the Resume process.

During reset, the PPWRx latch signals (PPWRL1 and PPWRL0) are pulsed to set the PPWRx signals to a known state. After reset:

- PPWR[11:8] and PPWR[3:0] are set to 0 and
- PPWR[15:12] and PPWR[7:4] are set to 1.

The PPWRx signals will remain in this state until they are updated by writing to SYSCFG 54h, 55h, ABh, and EEh.

4.14.7.2 Programming

SYSCFG 54h, 55h, ABh, and EEh set the power control latch outputs. The upper bits ([7:4]) of each register select whether the corresponding bits [3:0] should be used to change the latch; if the enable bit is 0, the current latch setting will not be changed when the register is written.

Table 4-87 Power Control Register Bits

7	6	5	4	3	2	1	0
SYSCFG 54h Power Control Latch Register 1 Default = 00h							
Enable [3:0] to write latch lines PPWR[3:0]: 0 = Disable 1 = Enable				RW data bits for PPWR[3:0]: 0 = Latch output low 1 = Latch output high			
SYSCFG 55h Power Control Latch Register 2 Default = 0Fh							
Enable [3:0] to write latch lines PPWR[7:4]: 0 = Disable 1 = Enable				RW data bits for PPWR[7:4] (Default = 1111): 0 = Latch output low 1 = Latch output high			
SYSCFG ABh Power Control Latch Register 3 Default = 00h							
Enable [3:0] to write latch lines PPWR[11:8]: 0 = Disable 1 = Enable				RW data bits for PPWR[11:8]: 0 = Latch output low 1 = Latch output high			
SYSCFG EEh Power Control Latch Register Default = 0Fh							
Enable [3:0] to write latch lines PPWR[15:12]: 0 = Disable 1 = Enable				RW data bits for PPWR[15:12] (Default = 1111): 0 = Latch output low 1 = Latch output high			

4.14.7.3 Resume Recovery Time

SYSCFG 68h[3:2] determine the recovery time from PPWR[1:0] active after a Resume until the end of reset. The clock is guaranteed to be active for at least the last one-eighth of the recovery time. These bits are not affected by SYSCFG 68h[1:0].

These bits can be overridden by setting SYSCFG BEh[0] = 1, in which case the Resume recovery time will always be one second.

4.14.7.4 PPWR[1:0] Suspend Auto Toggle Feature

SYSCFG 68h[1:0] enable PPWR1 and PPWR0, respectively, to automatically toggle when entering and exiting Suspend. Using PPWR0 as an example: When bit 0 = 1 and the Viper-N Chipset has gone into the Suspend mode, PPWR0 gets set to the inverse of SYSCFG 54h[0]; mask SYSCFG 54h[4] is ignored. When exiting Suspend, PPWR0 is set to SYSCFG 54h[0] setting, followed by the recovery time delay set in bits 68h[3:2] before continuing the Resume operation.

4.14.8 Programmable Chip Select Feature

The 82C558N provides programmable chip select features that require no chip signals to be sacrificed. A total of four programmable chip selects are available and can decode either memory cycles or I/O cycles. For I/O chip select decoding, granularity can be specified to-the-byte, decoding a total of 10 bits. For ROM chip select decoding, granularity is to 16KB blocks anywhere in the ISA bus address space (16MB).

Note that the memory chip select feature should be used cautiously for ROMs residing below 1MB. Since the ROM to be selected is on the SD bus, the XD bus buffer may be directed toward the 82C558N for memory reads and could conflict with SD bus ROMs.

The registers that control the programmability and relocation of the general purpose chip selects shown in Table 4-89.

Table 4-88 Resume Recovery and Suspend Auto Toggle Register Bits

7	6	5	4	3	2	1	0
SYSCFG 68h							
Clock Source Register 3				Default = 00h			
R_TIMER clock source		IDLE_TIMER clock source		Resume recovery time:		PPWR[1:0] auto-toggle on entry and exit from Suspend:	
				00 = 8ms 10 = 128ms		0 = Disable	
				01 = 32ms 11 = 30µs		1 = Enable	
Note: Ignored if BEh[0] = 1.							
SYSCFG BEh							
Idle Reload Event Enable Register 2							
Default = 00h							
GPCS3#_ACCESS:	GPCS2#_ACCESS:	COM2_ACCESS:	COM1_ACCESS:	GNR2_ACCESS:	HDU_ACCESS:	GNR4_ACCESS:	Override 68h[3:2]:
0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = Disable 1 = Enable	0 = No 1 = Recover time 1s



82C556/82C557/82C558N

Table 4-89 Programmable Chip Select Registers

7	6	5	4	3	2	1	0
SYSCFG 4Ah Chip Select 0 Base Address Register Default = 00h GPCS0# base address: A[8:1] (I/O) or A[22:15] (Memory)							
SYSCFG 4Bh Chip Select 0 Control Register Default = 00h							
GPCS0# base address: A9 (I/O) A23 (Memory)	Write decode: 0 = Disable 1 = Enable	Read decode: 0 = Disable 1 = Enable	Chip select active: 0 = w/Cmd 1 = Before ALE	GPCS0# mask bits for address A[4:1] (I/O) or A[18:15] memory: A 1 in a particular bit means that the corresponding bit at 4Ah[3:0] is not compared. This is used to determine address block size.			
SYSCFG 4Ch Chip Select 1 Base Address Register Default = 00h GPCS1# base address: A[8:1] (I/O) or A[22:15] (Memory)							
SYSCFG 4Dh Chip Select 1 Control Register Default = 00h							
GPCS1# base address: A9 (I/O) A23 (Memory)	Write decode: 0 = Disable 1 = Enable	Read decode: 0 = Disable 1 = Enable	Chip select active: 0 = w/Cmd 1 = before ALE	GPCS1# mask bits for address A[4:1] (I/O) or A[18:15] memory: A 1 in a particular bit means that the corresponding bit at 4Ch[3:0] is not compared. This is used to determine address block size.			
SYSCFG BAh Chip Select 2 Base Address Register Default = 00h GPCS2# base address: A[8:1] (I/O) or A[22:15] (Memory)							
SYSCFG BBh Chip Select 2 Control Register Default = 00h							
GPCS2# base address: A9 (I/O) A23 (Memory)	Write decode: 0 = Disable 1 = Enable	Read decode: 0 = Disable 1 = Enable	Chip select active: 0 = w/Cmd 1 = before ALE	GPCS2# mask bits for address A[4:1] (I/O) or A[18:15] memory: A 1 in a particular bit means that the corresponding bit at BAh[3:0] is not compared. This is used to determine address block size.			
SYSCFG BCh Chip Select 3 Base Address Register Default = 00h GPCS3# base address: A[8:1] (I/O) or A[22:15] (Memory)							
SYSCFG BDh Chip Select 3 Control Register Default = 00h							
GPCS3# base address: A9 (I/O) A23 (Memory)	Write decode: 0 = Disable 1 = Enable	Read decode: 0 = Disable 1 = Enable	Chip select active: 0 = w/Cmd 1 = before ALE	GPCS3# mask bits for address A[4:1] (I/O) or A[18:15] memory: A 1 in a particular bit means that the corresponding bit at SYSCFG BCh[3:0] is not compared. This is used to determine address block size.			
SYSCFG BFh Chip Select Granularity Register Default = 0Fh							
GPCS3# base address: A0 (I/O) A14 (Memory)	GPCS2# base address: A0 (I/O) A14 (Memory)	GPCS1# base address: A0 (I/O) A14 (Memory)	GPCS0# base address: A0 (I/O) A14 (Mem.)	GPCS3# mask bit: A0 (I/O) A14 (Memory)	GPCS2# mask bit: A0 (I/O) A14 (Memory)	GPCS1# mask bit: A0 (I/O) A14 (Memory)	GPCS0# mask bit: A0 (I/O) A14 (Memory)
SYSCFG B3h Chip Select Cycle Type Register Default = 00h							
GPCS3# ROM width: 0 = 8-bit 1 = 16-bit	GPCS2# ROM width: 0 = 8-bit 1 = 16-bit	GPCS1# ROM width: 0 = 8-bit 1 = 16-bit	GPCS0# ROM width: 0 = 8-bit 1 = 16-bit	GPCS3# cycle type: 0 = I/O 1 = ROMCS	GPCS2# cycle type: 0 = I/O 1 = ROMCS	GPCS1# cycle type: 0 = I/O 1 = ROMCS	GPCS0# cycle type: 0 = I/O 1 = ROMCS



4.15 System Management Interrupt (SMI)

The 3.3V Pentium processor offers a System Management Interrupt (SMI) that allows external logic to signal to the CPU that a high priority event has occurred and must be serviced but should not in any way interfere with the application currently being processed. When the CPU senses its SMI input active, it saves the context of its current application and loads the context of its System Management Mode (SMM) handler routine from a protected part of RAM. SMM code can then proceed to determine the reason for the interrupt, service it appropriately, and return to application processing through a special RESUME instruction that restores the context as it originally was before the SMI.

The 82C558N handles up to 36 Power Management Interrupt (PMI) events that can be selectively enabled to cause an SMI to the CPU. Since some of these PMI events are actually a single indication from a group of events (such as a single PMI #6 that indicates whether any of the selected IRQ lines has gone active), the effective number of events that can be indicated is actually much greater than 36.

The PMI events that can be programmed to generate an SMI are listed in Table 4-90.

Table 4-90 SMI Sources

Source	PMI Name	Description
IRQ, DRQ, and EPMI SMI Sources		
#3	LOWBAT	Activity on Low Battery Pin
#0	LLOWBAT	Activity on Very Low Battery Pin
#1	EPMI0#	Activity on External Power Management Input 1
#2	EPMI1#	Activity on External Power Management Input 2
#24	EPMI2#	Activity on External Power Management Input 3
#25	EPMI3#	Activity on External Power Management Input 4
#26	RINGI	Activity detected on RINGI
#7	SUS/RES#	SUS/RES# input has been toggled
#6	INTRGRP - or - RSMGRP	An interrupt from the INTRGRP set has occurred while the system was running -or- An interrupt from the RSMGRP has occurred and resumed the system from Suspend mode
#28	DMA TRAP	Activity on DMA DRQ lines
#33	DOZE RELOAD	Exit from hardware Doze mode
Time-Out Event SMI Sources		
#35	APM EXIT	Exit from APM (software) Doze mode
#4	IDLE_TIMER	IDLE_TIMER has timed out due to no I/O activity
#27	DOZE_TIMER	DOZE_TIMER has timed out due to inactivity
#5	R_TIMER	R_TIMER has timed out on its normal periodic basis
#8	LCD_TIMER	LCD_TIMER has timed out because of no screen activity
#9	DSK_TIMER	Floppy (and/or external hard) disk timer has timed out because of no activity
#19	HDU_TIMER	Time-out has occurred because no access has occurred in the internal IDE range
#10	KBD_TIMER	Keyboard timer has timed out because of no controller accesses
#11	GNR1_TIMER	Time-out has occurred because the memory or I/O range selected by GNR1 has had no activity
#16	GNR2_TIMER	Time-out has occurred because the memory or I/O range selected by GNR2 has had no activity
#30	GNR3_TIMER	Time-out has occurred because the memory or I/O range selected by GNR3 has had no activity
#32	GNR4_TIMER	Time-out has occurred because the memory or I/O range selected by GNR4 has had no activity
#17	COM1_TIMER	Time-out has occurred because no access has occurred in the COM1 range
Access Event SMI Sources		
#18	COM2_TIMER	Time-out has occurred because no access has occurred in the COM2 range
#14	KBD_ACCESS	Keyboard controller has been accessed, either before or after timer time-out depending on current/next access setting

Table 4-90 SMI Sources (cont.)

Source	PMI Name	Description
#12	LCD_ACCESS	LCD controller has been accessed, either before or after timer time-out depending on current/next access setting
#13	DSK_ACCESS	Floppy (or external hard) disk controller has been accessed, either before or after timer time-out depending on current/next access setting
#23	HDU_ACCESS	Internal IDE has been accessed, either before or after timer time-out depending on current/next access setting
#15	GNR1_ACCESS	GNR1 range has been accessed, either before or after timer time-out depending on current/next access setting
#20	GNR2_ACCESS	GNR2 range has been accessed, either before or after timer time-out depending on current/next access setting
#29	GNR3_ACCESS	GNR3 range has been accessed, either before or after timer time-out depending on current/next access setting
#31	GNR4_ACCESS	GNR4 range has been accessed, either before or after timer time-out depending on current/next access setting
#21	COM1_ACCESS	COM1 has been accessed, either before or after timer time-out depending on current/next access setting
#22	COM2_ACCESS	COM2 has been accessed, either before or after timer time-out depending on current/next access setting

4.15.1 SMI Operation and Initialization

The 3.3V Pentium CPU uses the SMI $\overline{ACT\#}$ pin to indicate that it is currently executing SMM code. While in SMM, the default addresses put out by the CPU are in the 3000h and 4000h segments to execute SMM code and to access SMM data. However, the SMBASE Register of the CPU is programmable, and can be set to any other segment if desired. These SMRAM addresses put out by the CPU must be mapped to the A000h-B000h segments. The Viper-N Chipset directs these accesses to translation is performed only during SMM when the Viper-N Chipset receives the SMI $\overline{ACT\#}$ signal from the CPU. The A000h-B000h segments of DRAM main memory are usually unused and not accessed during normal mode because accesses to this area are redirected to the ISA or local bus for video. These segments are utilized by initializing them with SMM code/data at boot-up and write protecting them during normal mode of operation.

4.15.1.1 Loading Initial SMM Code and Data

On system initialization, the system management code and data segments must be loaded from ROM with the appropriate information. This information will reside in the DRAM segments at physical starting addresses A0000h and B0000h and, once loaded, will be write-protected except when the system is operating in SMM.

Step 1: System Initialization (not in SMM)

On system initialization, the BIOS must load initial code and data into the protected SMM memory space. Normally the system will still be executing out of ROM at this point, but the

memory subsystem is configured and enabled. A mechanism is provided by which the A000h-B000h DRAM area may be accessed even if the CPU is not in SMM. This mechanism is used to initialize the A000h-B000h DRAM area with SMM handler code/data.

The registers that pertain to initialization are shown in Table 4-92. SYSCFG 13h[3] is the SMRAM Access Control and provides a global control for address translation. The value of SYSCFG 14h[3] has different meanings according to whether the CPU is in SMM or not. If SYSCFG 13h[3] = 1, and SYSCFG 14h[3] = 1, normal mode CPU accesses in the A000h-B000h range are redirected to the DRAM A000h-B000h area. This feature is used for initializing the DRAM A000h-B000h range.

Table 4-91 SMI $\overline{ACT\#}$ Interpretation

SYSCFG 14h[3]	SMI $\overline{ACT\#}$ Inactive (Normal CPU Mode)
0	Disable SMRAM
1	Direct A000h-B000h accesses to SRAM (if SYSCFG 13h[3] = 1)

Table 4-92 SMRAM Access Control Bits

7	6	5	4	3	2	1	0	
SYSCFG 13h								
Memory Sizing Register 1				Default = 00h				
Memory decode select: 0 = Table lookup (compatible to 82C547) 1 = Full decode	Full decode for logical Bank 1 (RAS1#) if SYSCFG 13h[7] set: 000 = Disabled 001 = 256Kx36x2 010 = 512Kx36x2 011 = 1Mx36x2			100 = 2Mx36 101 = 4Mx36x2 110 = 8Mx36x2 111 = 16Mx36x2	SMRAM: 0 = Disable 1 = Enable (depending on SYSCFG 14h[3])	Full decode for logical Bank 0 (RAS0#) if SYSCFG 13h[7] set: 000 = Disabled 001 = 256Kx36x2 010 = 512Kx36x2 011 = 1Mx36x2		
SYSCFG 14h)								
Memory Sizing Register 2				Default = 00h				
Reserved: Write 0.	Full decode for logical Bank 3 (RAS3#) if SYSCFG 13h[7] set: 000 = Disabled 001 = 256Kx36x2 010 = 512Kx36x2 011 = 1Mx36x2			100 = 2Mx36x2 101 = 4Mx36x2 110 = 8Mx36x2 111 = 16Mx36x2	If SMIACT# is inactive: 0 = Disable SMRAM 1 = Enable SMRAM If SMIACT# is active and SYSCFG 13h[3] = 1: 0 = Enable SMRAM for Code and Data 1 = Enable SMRAM for Code only	Full decode for logical Bank 2 (RAS2#) if SYSCFG 13h[7] set: 000 = Disabled 001 = 256Kx36x2 010 = 512Kx36x2 011 = 1Mx36x2		

SYSCFG 13h[3] and 14h[3] are used as follows when the CPU is not in SMM:

- 13h[3] = 0: No Relocation. This setting prevents application software from accessing SMI memory space.
- 13h[3] = 1:
 - If 14h[3] = 1, CPU addresses in the A000h-B000h segments go to SMI memory space - the DRAM segments at A000h-B000h. This setting provides the mechanism for initially loading SMI code to the A000h-B000h region.
 - If 14h[3] = 0, the A000h-B000h area in DRAM cannot be accessed.

The significance of 14h[3] during SMM is explained later.

The BIOS sets 13h[3] = 1 and 14h[3] = 1. It can then load code and data into DRAM segments A000h and B000h. This first load operation must be addressed to the A000h and B000h segments. Upon completing the loading of all initial SMM code and data, the BIOS clears 14h[3] to 0 to protect the SMM space.

Step 2: Loading the Code to Change the SMBASE Register of the CPU

Having loaded the code and data, the BIOS must now generate an SMI to enter SMM so that it can complete the SMM initialization process (changing SMBASE to A000h and for performing system-specific tasks; the SMBASE Register can only be changed from within SMM mode). The SMBASE Register of the CPU is by default 30000h, and the first code fetch in SMM is from 38000h. Before generating an SMI, the ROM BIOS must load code from physical address 38000h onwards to change the SMBASE Register of the CPU and to resume normal mode.

Step 3: Software generation of SMI

To allow software SMI generation to take place, SYSCFG 59h[7] must be written to 1. Writing SYSCFG 50h[7] = 1 asserts SMI# to the CPU to start SMM operation. Writing SYSCFG 50h[7] = 0 clears the SMI. The SMI routine must clear this bit; otherwise, SMI requests will be generated continuously.

Step 4: Reprogramming SMBASE

Once the system has entered SMM for the first time at 38000h, the CPU SMBASE value can be reprogrammed for future use.

1. SMM initialization code updates the SMBASE value in the CPU register save area to A0000h.
2. SMM initialization code clears the Software Start SMI (SYSCFG 50h[7]).
3. SMM initialization code generates a RESUME instruction to return control to the BIOS initialization code. The new SMBASE value gets written to the CPU registers.

4.15.1.2 Run-Time SMI Address Relocation

The Dynamic SMI Relocation feature provides full memory access control while in SMM. SMI relocation at run time is controlled by SYSCFG 14h[3] if SYSCFG 13h[3] = 1.

If SYSCFG 13h[3] is set, during SMM, either all CPU accesses to the A000h-B000h range, or only accesses to code may be mapped to the A000h-B000h range in DRAM memory. The active SMIACT# signal and the status of SYSCFG 14h[3] determine whether both code and data accesses or only code accesses are mapped to DRAM. If SYSCFG 14h[3] = 1, only code accesses are mapped to DRAM and data accesses are not translated to SMI space. This allows data in the A000h-B000h memory space to be accessed and saved to disk. If SYSCFG 14h[3] = 0, both code and data accesses are translated to SMI space.

4.15.2 SMI Event Generation

The registers shown in Table 4-94 control the events that are allowed to generate an SMI. The programming occurs as follows: time-out, access, and interrupt events must be programmed to generate a PMI, then the PMI event must be enabled to generate the SMI signal; finally, SMIs are globally unmasked to allow full operation.

4.15.2.1 Time-out Event Generation of SMI

For time-out events, simply loading a non-zero timer value and generating a dummy access presets PMI generation on the next time-out. Refer to the Section 4.14.1.1.1, "Timers" for information on programming the timers.

Table 4-93 Software SMI Enable Register Bits

7	6	5	4	3	2	1	0
SYSCFG 59h PMU Event Register 2 Default = 00h							
Allow software SMI: 0 = Disable 1 = Enable	Reload timers on Resume: 0 = No 1 = Yes	Resume INTRGRP PMI#6, Suspend PMI#7 SMI: 00 = Disable 11 = Enable	R_TIMER PMI#5 SMI: 00 = Disable 11 = Enable		IDLE_TIMER PMI#4 SMI: 00 = Disable 11 = Enable		
SYSCFG 50h PMU Control Register 4 Default = 00h							
Software start SMI: 0 = Clear SMI 1 = Start SMI	Reserved	IRQ8 polarity: 0 = Active low 1 = Active high	14.3MHz to 82C558N: 0 = Enable 1 = Disable	Write = 1 to start Doze Read: Doze status 0 = Counting 1 = Timed out	Ready to Resume (RO): 0 = Not in Resume 1 = Ready to Resume	PMU mode (RO): 0 = Nothing pending 1 = Suspend active (clear PMI#6)	Start Suspend (WO): 1 = Enter Suspend mode



4.15.2.2 Access Event Generation of SMI

Access events can be programmed to generate an SMI. The 82C558N classifies accesses as Current Access or a Next Access depending on whether the timer associated with that access range is still running or has timed out.

- Next Access - Occurs after a time-out, the first time software attempts to access the range that caused the time-out. The Next Access feature provides a way for I/O accesses to a peripheral whose timer has timed out to cause an SMI so that the peripheral can be powered up before the access takes place. Next access can also restart system clocks when the system is in the doze mode.
- Current Access - Occurs any time this feature is enabled for a range, whether or not the device has timed out. The Current Access PMI can be programmed to cause an SMI, but cannot provide any automatic means of controlling system clocks.

If both the Current Access and Next Access features are enabled for an event and the timer has timed out, an access will only cause a single SMI. Since both access types use the same PMI#, clearing either one clears both events.

The I/O blocking bit, SYSCFG DBh[7], operates as follows. This selection allows the I/O access that causes a Next Access PMI to be either blocked (if the peripheral is turned off, for example) or passed through. DBh[7] = 0 means the I/O will not be blocked; DBh[7] = 1 means the I/O on Next Access will be blocked and the CPU must be programmed to restart the I/O command if desired. The feature defaults to "blocked".

Table 4-94 Current and Next Access Registers

7	6	5	4	3	2	1	0	
SYSCFG 5Bh PMU Event Register 4								Default = 00h
Reserved	Global SMI control: 0 = Allow 1 = Mask	Reserved		GNR1 next access PMI#15: 0 = Disable 1 = Enable	KBD next access PMI#14: 0 = Disable 1 = Enable	DSK next access PMI#13: 0 = Disable 1 = Enable	LCD next access PMI#12: 0 = Disable 1 = Enable	
SYSCFG DBh Next Access Event Generation Register 2								Default = 00h
I/O blocking control: 0 = Block I/O on next access trap 1 = Unblock	SMI on cool-down clocking entry/exit: 0 = Disable 1 = Enable	External EPMI3# pin polarity: 0 = Active high 1 = Active low	External EPMI2# pin polarity: 0 = Active high 1 = Active low	HDU_ACCESS PMI#23 on next access: 0 = No 1 = Yes	COM2_ACCESS PMI#22 on next access: 0 = No 1 = Yes	COM1_ACCESS PMI#21 on next access: 0 = No 1 = Yes	GNR2_ACCESS PMI#20 on next access: 0 = No 1 = Yes	
SYSCFG DEh Current Access Event Generation Register								Default = 00h
HDU_ACCESS PMI#23 on current access: 0 = No 1 = Yes	COM2_ACCESS PMI#22 on current access: 0 = No 1 = Yes	COM1_ACCESS PMI#21 on current access: 0 = No 1 = Yes	GNR2_ACCESS PMI#20 on current access: 0 = No 1 = Yes	GNR1_ACCESS PMI#15 on current access: 0 = No 1 = Yes	KBD_ACCESS PMI#14 on current access: 0 = No 1 = Yes	DSK_ACCESS PMI#13 on current access: 0 = No 1 = Yes	LCD_ACCESS PMI#12 on current access: 0 = No 1 = Yes	
SYSCFG E9h PMU Event Register 7								Default = 00h
GNR4_TIMER PMI#30 SMI: 00 = Disable 11 = Enable		GNR3_TIMER PMI#29 SMI: 00 = Disable 11 = Enable		GNR4_ACCESS PMI#32 on current access: 0 = No 1 = Yes	GNR4_ACCESS PMI#32 on next access: 0 = No 1 = Yes	GNR3_ACCESS PMI#31 on current access: 0 = No 1 = Yes	GNR3_ACCESS PMI#31 on next access: 0 = No 1 = Yes	

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4.15.2.3 Interrupt Event Generation of SMI

Asynchronous events from peripheral devices requesting service from the CPU are known as interrupt events. Interrupts in this context include both the traditional AT architecture IRQs and additional inputs known as external power management inputs. For the 82C558N logic, the desired interrupts are all grouped into a single event called INTRGRP. INTRGRP can then be enabled to cause an SMI.

If it is desired to generate an SMI from the INTRGRP event, setting SYSCFG 57h[6] = 1 will allow any of the selected interrupt events to generate PMI #6. Once in the SMI handler, the SMM code can read the SYSCFG 64h and A4h to determine which of the interrupt(s) caused the event. The IRQs will remain latched for reading in these registers until PMI #6 is cleared, at which time any latched sources are cleared. The INTRGRP IRQ Select Registers are shown in Table 4-95.

4.15.2.4 DRQ Event Generation of SMI

The 82C558N allows activity on the DRQ pins to generate an SMI. The SMI takes place before the DMA transfer occurs, allowing SMM code to emulate or modify the operation. Writing the bit to clear the PMI allows any pending DMA operation to take place immediately. Note that there are certain latency limitations for DMA operations. For example, floppy disk DMA transfers generally must be serviced within 14µs from receipt of DRQ2 in order to avoid an overrun condition. Entry into SMM requires a considerable amount of time in itself. Therefore, SMM routines that trap DMA accesses must be structured concisely so that the DMA cycle is allowed to occur before the latency limit exceeded. Table 4-96 shows which register bits apply to this application.

Table 4-95 INTRGRP IRQ Select Register Bits

7	6	5	4	3	2	1	0
SYSCFG 64h INTRGRP IRQ Select Register 1 Default = 00h							
IRQ14: 0 = Disable 1 = Enable	IRQ8: 0 = Disable 1 = Enable	IRQ7: 0 = Disable 1 = Enable	IRQ6: 0 = Disable 1 = Enable	IRQ5: 0 = Disable 1 = Enable	IRQ4: 0 = Disable 1 = Enable	IRQ3: 0 = Disable 1 = Enable	IRQ1: 0 = Disable 1 = Enable
SYSCFG A4h INTRGRP IRQ Select Register 2 Default = 00h							
Test Bit: Write as 0	IRQ15: 0 = Disable 1 = Enable	IRQ13: 0 = Disable 1 = Enable	IRQ12: 0 = Disable 1 = Enable	IRQ11: 0 = Disable 1 = Enable	IRQ10: 0 = Disable 1 = Enable	IRQ9: 0 = Disable 1 = Enable	IRQ0: 0 = Disable 1 = Enable
SYSCFG 57h PMU Control Register 5 Default = 00h							
Reserved	INTRGRP generates PMI#6: 0 = Disable 1 = Enable	DSK_ACCESS includes FDD: 0 = Yes 1 = No	DSK_ACCESS includes HDD: 0 = Yes 1 = No	Reserved			

Table 4-96 DMA DRQ Trap SMI Register Bits

7	6	5	4	3	2	1	0
SYSCFG D6h PMU Control Register 10 Default = 00h							
DSK_ACCESS: 0 = 3F5h only 1 = All FDC Ports (3F2,4,5,7h, & 372,4,5,7h)	DMA trap PMI#28 SMI: 0 = Disable 1 = Enable	DMAC1 byte pointer flip-flop (RO): 0 = Cleared 1 = Set	APM doze exit PMI#35: 0 = Disable 1 = Enable	SBHE# status trap (RO)	I/O port access trapped (RO): 0 = I/O read 1 = I/O write	Access trap bit A9 (RO)	Access trap bit A8 (RO)
SYSCFG DDh PMU SMI Source Register 4 Default = 00h							
Reserved			PMI#28, DMA: 0 = Clear 1 = Active	PMI#27, DOZE_TIMER: 0 = Clear 1 = Active	PMI#26, RINGI: 0 = Clear 1 = Active	PMI#25, EPMI3# pin/cool-down clocking: 0 = Clear 1 = Active	PMI#24, EPMI2# pin: 0 = Clear 1 = Active



4.15.3 Enabling of Events to Generate SMI

The registers listed in Table 4-97 allow PMI events that are enabled to generate timer time-outs, accesses, and interrupts to cause SMIs. Before setting the SMI Event Enable Registers, time-outs, accesses, and interrupts must be individually enabled to generate PMI events as follows.

- For time-out events, loading a non-zero timer value and generating a dummy access presets PMI generation on the next time-out.
- For current access events, the appropriate current access enable bit must be set to preset PMI generation on the following access.
- For next access events, the appropriate next access enable bit must be set. Then, a valid time-out must take place to preset PMI generation on the following access.

- For interrupt events, the corresponding INTRGRP bit must be set and INTRGRP must be enabled to generate PMI #6. Then, on any enabled interrupt PMI #6 will occur.

Only after all desired PMI events have been enabled should the PMI be enabled to generate an SMI through the register set below. Setting SYSCFG 5Bh[6] = 1 then unmask all the SMIs previously enabled.

Note that a resume event can be enabled to generate PMI #6. Refer to the "Suspend and Resume" section for details on enabling resume events.

4.15.3.1 PMI #25 Triggers

The PMI #25 event is shared by both EPMI3# and the thermal management unit. SYSCFG D9h[3:2] enable SMI for EPMI3# only. SYSCFG DBh[6] enables SMI only for cool-down clocking entry and exit.

Table 4-97 SMI Event Enable Registers

7	6	5	4	3	2	1	0
SYSCFG 5Bh PMU Event Register 4 Default = 00h							
Reserved	Global SMI control: 0 = Allow 1 = Mask	Reserved		GNR1 next access PMI#15: 0 = Disable 1 = Enable	KBD next access PMI#14: 0 = Disable 1 = Enable	DSK next access PMI#13: 0 = Disable 1 = Enable	LCD next access PMI#12: 0 = Disable 1 = Enable
SYSCFG 58h PMU Event Register 1 Default = 00h							
LOWBAT PMI#3 SMI: 00 = Disable 11 = Enable		EPMI1# PMI#2 SMI: 00 = Disable 11 = Enable		EPMI0# PMI#1 SMI: 00 = Disable 11 = Enable		LLOWBAT PMI#0 SMI: 00 = Disable 11 = Enable	
SYSCFG D9h PMU Event Register 6 Default = 00h							
DOZE_TIMER PMI#27 SMI: 00 = Disable 01 = Enable DOZE_0 10 = Enable DOZE_1 11 = Enable both		RINGI PMI#26 SMI: 00 = Disable 11 = Enable		EPMI3# cool-down clocking PMI#25 SMI: 00 = Disable 11 = Enable		EPMI2# PMI#24 SMI: 00 = Disable 11 = Enable	
SYSCFG 5Ah PMU Event Register 3 Default = 00h							
GNR1_TIMER PMI#11 SMI: 00 = Disable 11 = Enable		KBD_TIMER PMI#10 SMI: 00 = Disable 11 = Enable		DSK_TIMER PMI#9 SMI: 00 = Disable 11 = Enable		LCD_TIMER PMI#8 SMI: 00 = Disable 11 = Enable	
SYSCFG D8h PMU Event Register 5 Default = 00h							
HDU_TIMER PMI#19 HDU_ACCESS PMI#23 SMI: 00 = Disable 11 = Enable		COM2_TIMER PMI#18 COM2_ACCESS PMI#22 SMI: 00 = Disable 11 = Enable		COM1_TIMER PMI#17 COM1_ACCESS PMI#21 SMI: 00 = Disable 11 = Enable		GNR2_TIMER PMI#16 GNR2_ACCESS PMI#20 SMI: 00 = Disable 11 = Enable	
SYSCFG 59h PMU Event Register 2 Default = 00h							
Allow software SMI: 0 = Disable 1 = Enable	Reload timers on Resume: 0 = No 1 = Yes	Resume INTRGRP PMI#6, Suspend PMI#7 SMI: 00 = Disable 11 = Enable		R_TIMER PMI#5 SMI: 00 = Disable 11 = Enable		IDLE_TIMER PMI#4 SMI: 00 = Disable 11 = Enable	



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Table 4-97 SMI Event Enable Registers (cont.)

7	6	5	4	3	2	1	0
SYSCFG DBh							
Next Access Event Generation Register 2							
Default = 00h							
I/O blocking control: 0 = Block I/O on next access trap 1 = Unblock	SMI on cool-down clocking entry/exit: 0 = Disable 1 = Enable	External EPMI3# pin polarity: 0 = Active high 1 = Active low	External EPMI2# pin polarity: 0 = Active high 1 = Active low	HDU_ACCESS PMI#23 on next access: 0 = No 1 = Yes	COM2_ACCESS PMI#22 on next access: 0 = No 1 = Yes	COM1_ACCESS PMI#21 on next access: 0 = No 1 = Yes	GNR2_ACCESS PMI#20 on next access: 0 = No 1 = Yes
SYSCFG E9h							
PMU Event Register 7							
Default = 00h							
GNR4_TIMER PMI#30 SMI: 00 = Disable 11 = Enable		GNR3_TIMER PMI#29 SMI: 00 = Disable 11 = Enable		GNR4_ACCESS PMI#32 on current access: 0 = No 1 = Yes	GNR4_ACCESS PMI#32 on next access: 0 = No 1 = Yes	GNR3_ACCESS PMI#31 on current access: 0 = No 1 = Yes	GNR3_ACCESS PMI#31 on next access: 0 = No 1 = Yes



4.15.4 Servicing an SMI

The register set shown in Table 4-98 is used by SMM code to enable system events to cause SMIs, to determine the events that caused an active SMI, and to clear the events. Determining the source of the SMI is an uncomplicated procedure.

1. Upon entry to SMM, read the SYSCFG 5Ch, 5Dh, DCh, DDh, and EAh. Any non-zero bits indicate PMI sources. More than one can be active.
2. The PMI number will indicate the source of the service request. If the PMI #6 is generated, also read SYSCFG

64h and A4h (described earlier in the "Interrupt Event Generation of SMI" section) to determine which IRQ line was responsible for the event.

3. Service the events in the order desired; upon completion of each service, write a 1 back to the event source register bit to clear that event. Continue in this manner until all events are serviced and all the service registers are clear.
4. Issue the proper CPU instruction to return from SMM operation. If any events are still pending, most CPUs will immediately re-enter SMM.

Table 4-98 SMI Service Registers

7	6	5	4	3	2	1	0
SYSCFG 5Ch							
PMI Source Register 1							Default = 00h
PMI#7, Suspend: 0 = Not Active 1 = Active	PMI#6, Resume or INTRGRP: 0 = Not Active 1 = Active	PMI#5, R_TIMER time-out: 0 = Not Active 1 = Active	PMI#4, IDLE_TIMER time-out: 0 = Not Active 1 = Active	PMI#3, LOWBAT: 0 = Not Active 1 = Active	PMI#2, EPMI#: 0 = Not Active 1 = Active	PMI#1, EPMI0#: 0 = Not Active 1 = Active	PMI#0, LLOWBAT: 0 = Not Active 1 = Active
SYSCFG 5Dh							
PMI Source Register 2							Default = 00h
PMI#15, GNR1_ ACCESS: 0 = None 1 = Active	PMI#14, KBD_ACCESS: 0 = Not Active 1 = Active	PMI#13, DSK_ACCESS: 0 = Not Active 1 = Active	PMI#12, LCD_ACCESS: 0 = Not Active 1 = Active	PMI#11, GNR1_TIMER: 0 = Not Active 1 = Active	PMI#10, KBD_TIMER: 0 = Not Active 1 = Active	PMI#9, DSK_TIMER: 0 = Not Active 1 = Active	PMI#8, LCD_TIMER: 0 = Not Active 1 = Active
SYSCFG DCh							
PMU SMI Source Register 3							Default = 00h
PMI#23, HDU_ ACCESS: 0 = None 1 = Active	PMI#22, COM2_ ACCESS: 0 = Clear 1 = Active	PMI#21, COM1_ ACCESS: 0 = Clear 1 = Active	PMI#20, GNR2_ ACCESS: 0 = Clear 1 = Active	PMI#19, HDU_ TIMER: 0 = Clear 1 = Active	PMI#18, COM2_ TIMER: 0 = Clear 1 = Active	PMI#17, COM1_ TIMER: 0 = Clear 1 = Active	PMI#16, GNR2_ TIMER: 0 = Clear 1 = Active
SYSCFG DDh							
Reserved			PMI#28, DMA: 0 = Clear 1 = Active	PMI#27, DOZE_TIMER: 0 = Clear 1 = Active	PMI#26, RINGI: 0 = Clear 1 = Active	PMI#25, EPMI3# pin/ cool-down clocking: 0 = Clear 1 = Active	PMI#24, EPMI2# pin: 0 = Clear 1 = Active
SYSCFG EAh							
PMU Source Register 5							Default = 00h
Reserved	APM Doze exit PMI#35: 0 = Inactive 1 = Active	Hot docking time-out SMI PMI#34 0 = Inactive 1 = Active	H/W DOZE_ TIMER reload PMI#33 0 = Inactive 1 = Active (on Doze exit)	GNR4_ ACCESS PMI#32 0 = Inactive 1 = Active	GNR3_ ACCESS PMI#31 0 = Inactive 1 = Active	GNR4_ TIMER PMI#30 0 = Inactive 1 = Active	GNR3_ TIMER PMI#29 0 = Inactive 1 = Active



4.15.4.1 PMI Source Register Details

SYSCFG 5Ch, 5Dh, DCh, DDh, and EAh indicate the SMI source. When a PMI event occurs, the corresponding bit will be set to 1 and the SMI# signal will then be generated. In the SMI service routine, SMM code must check these registers for the PMI source(s) and then clear them. Otherwise, for all but the EPMI pins, the latched PMI source will generate SMI# continuously. SMI code normally clears only one event at a time to keep track of the events as they are serviced, but all events can be cleared at once if desired. Note that clearing SYSCFG 5Ch[6] will clear SYSCFG 5Ch[7] also.

Refer to the "Suspend and Resume" section of this document for information on PMI #6 when it is used to indicate a resume event.

4.15.4.2 EPMI Pin PMI Sources

The EPMI[1:0]# pins' PMI source indicator bits behave a little differently than the rest of the PMI source indicator bits. For PMIs #1 and #2, the EPMI[1:0]# inputs are not latched by default, so SYSCFG 5Ch[2:1] are not latched. Therefore, an

external device could trigger an SMI by toggling one of the EPMI[1:0]# lines, but if the device returns the EPMI line to its inactive state before SMM code reads SYSCFG 5Ch[2:1], the code would not be able to recognize the event that triggered the SMI. Likewise, an EPMI[1:0]# edge could initiate a resume from suspend mode, but then would not be recognized if the EPMI pin went to its inactive state.

SYSCFG A1h[0] is provided to allow EPMI[1:0]# to be latched like other PMIs. If SYSCFG A1h[0] is written to 1, EPMI[1:0]# events will be latched at SYSCFG 5Ch[2:1]. Writing a 1 into the active bit(s) then clears the PMI.

For PMIs #24 and #25, the EPMI[3:2]# inputs are always latched, regardless of the A1h[0] setting.

4.15.5 I/O SMI Trap Indication

The 82C558N provides a means for SMM code to determine the I/O port whose access caused the SMI, a bit to indicate whether the access was a read or a write, as well as the write data with SBHE# status for write instructions. The registers that provide the above data are shown in Table 4-99.

Table 4-99 I/O SMI Trap Indication Registers

7	6	5	4	3	2	1	0
SYSCFG D6h							
PMU Control Register 10				Default = 00h			
DSK_ACCESS: 0 = 3F5h only 1 = All FDC Ports (3F2,4,5,7h, & 372,4,5,7h)	DMA trap PMI#28 SMI: 0 = Disable 1 = Enable	DMAC1 byte pointer flip-flop (RO): 0 = Cleared 1 = Set	APM doze exit PMI#35: 0 = Disable 1 = Enable	SBHE# status trap (RO)	I/O port access trapped (RO): 0 = I/O read 1 = I/O write	Access trap bit A9 (RO)	Access trap bit A8 (RO)
SYSCFG D7h							
Access Port Address Register 1				Default = 00h			
Access trap address bits A[7:0]: These bits, along with SYSCFG D6h[1:0] and SYSCFG EBh[7:0] provide the 16-bit address of the port access that caused the SMI trap. SYSCFG D6h[2] indicates whether an I/O read or an I/O write access was trapped. SYSCFG D6h[3] gives the status of the SBHE# signal for the I/O instruction that was trapped.							
SYSCFG EBh							
Reserved		Access trap address bits A[15:10]: These bits along with D6h[1:0] and D7h[7:0] provide the 16-bit address of the port access that caused the SMI trap. D6h[2] indicates whether an I/O read or an I/O write access was trapped. D6h[3] gives the status of the SBHE# signal for the I/O instruction that was trapped.					
SYSCFG ECh							
Write Trap Register 1 (RO)				Default = 00h			
I/O write data trap[15:8]: Along with SYSCFG EDh[7:0], this register provides the 16-bit write data for trapped I/O write instructions.							
SYSCFG EDh							
Write Trap Register 2 (RO)				Default = 00h			
I/O write data trap[7:0]: Along with SYSCFG ECh[7:0], this register provides the 16-bit write data for trapped I/O write instructions.							



4.16 Utility Registers

The registers below provide SMM code with a general purpose storage region and a means of generating warning beeps on the system speaker without modifying the AT-compatible I/O ports.

Table 4-100 Utility Registers

7	6	5	4	3	2	1	0	
SYSCFG 52h							Scratchpad Register 1 General purpose storage byte	Default = 00h
SYSCFG 53h							Scratchpad Register 2 General purpose storage byte	Default = 00h
SYSCFG 6Ch							Scratchpad Register 3 General purpose storage byte	Default = 00h
SYSCFG 6Dh							Scratchpad Register 4 General purpose storage byte	Default = 00h
SYSCFG 6Eh							Scratchpad Register 5 General purpose storage byte	Default = 00h
SYSCFG 6Fh							Scratchpad Register 6 General purpose storage byte	Default = 00h
SYSCFG 51h							Beeper Control Register	Default = 00h
Reserved						Beeper control: 00 = No Action 10 = Off 01 = 1kHz 11 = 2kHz		



4.17 ISA Bus Hot Docking Feature

The "hot" attachment of a docking station to a notebook computer requires the computer to have certain capabilities that are listed below:

1. A mechanism to sense the beginning and the end of docking.
2. The ability to tristate the ISA bus when docking is in progress and to not generate an ISA bus cycle during that period.
3. The capability of either continuing with normal operation, or of generating an SMI if the end of docking is not sensed within a certain time period

The docking station also needs to have the capability of indicating the start of docking and the capability to indicate the completion of docking. This is usually accomplished by using special dock connectors that have "early" and "late" connections. The male connector is on the docking station and has several long pins. During insertion, these pins make contact with their counterparts on the notebook earlier than the other pins. One of these pins (HDI - Hot Docking Indicator) may be asserted by the docking station and can be used to indicate the beginning of insertion. Later on, when all pins make contact, the HDI pin may be deasserted to indicate the completion of docking, following which the notebook may start driving the ISA bus again. Referring to Figure 4-41, traversal time may be defined as the time taken for the shorter pins to make contact after the longer pins have made contact. The ISA bus signals have to be tristated after the HDI pin is detected as active and before the shorter pins make contact. This is not expected to be a problem because traversal time is usually of the order of a few milliseconds, whereas the

longest back-to-back ISA cycles are of the order of a few microseconds; hot docking may therefore be detected and the ISA bus tristated well within the traversal time period.

The Viper-N Chipset implements this feature by making use of one of the EPMI# inputs as the HDI pin and a programmable time-out counter that is loaded with a value that is an estimate of the traversal time. Any one of the EPMI# inputs may be programmed to perform the HDI function. An active EPMI# input is an indication to the chipset that docking is in progress.

On the occurrence of an active signal on the selected EPMI# input, the time-out counter is started, as shown in Figure 4-42. The 82C558N logic then causes the CPU to stop operation after the current cycle is completed by placing it on hold to ensure that another ISA bus cycle is not started while docking is in progress. After the system completes the current ISA bus cycle, which could be in the order of a few microseconds for certain ISA bus cycles, the ISA bus signals are tristated, and remain tristated till either the time-out counter runs out, or the HDI input is deasserted, whichever occurs earlier. The HDI input is expected to be deasserted within the time-out period. If the HDI input is deasserted within the time-out period as shown in Figure 4-42, it indicates that docking was completed within the expected time of insertion, and that the ISA bus may be driven again. If it is not deasserted within the time-out period as shown in Figure 4-43, it may be construed that docking was not completed in the expected time. In this situation, the option of either generating an SMI or ignoring the time-out and driving the ISA bus again is provided. Figure 4-43 shows the case where an SMI is generated due to the time-out period elapsing.

Table 4-101 Hot Docking Control Register Bits

7	6	5	4	3	2	1	0	
SYSCFG EFh Hot Docking Control Register 1 Default = 00h								
Hot docking enable: 1 = Enable (Default) 0 = Disable	HDI input debounce rate: 00 = 100µs 01 = 512µs 10 = 1ms 11 = 2ms		HDI active level: 0 = Active high 1 = Active low (Valid only if pin 155 is programmed as dedicated HDI)	HDI SMI: 0 = No SMI on time-out (Default) 1 = Generate SMI on time-out	HDI time-out period: 000 = 1ms 001 = 8ms 010 = 64ms 011 = 256ms			100 = 512ms 101 = 2s 110 = 8s 111 = 16s
SYSCFG F0h Hot Docking Control Register 2 Default = 00h								
EPMI3# reload IDLE_TIMER: 0 = Disable 1 = Enable	EPMI2# reload IDLE_TIMER: 0 = Disable 1 = Enable	EPMI1# reload IDLE_TIMER: 0 = Disable 1 = Enable	ROM window feature: 0 = Disable 1 = Enable	ROM window size: 00 = 64KB 01 = 128KB 10 = 256KB 11 = 512KB		EPMI trigger for HDI: 00 = EPMI0# 01 = EPMI1# 10 = EPMI2# 11 = EPMI3# (Valid only if pin 155 is not programmed as dedicated HDI)		



Table 4-101 Hot Docking Control Register Bits (cont.)

7	6	5	4	3	2	1	0		
SYSCFG 40h								PMU Control Register 1	Default = 00h
Reserved	Global timer divide: 0 = +1 1 = +4	LLOWBAT polarity: 0 = Active high 1 = Active low	LOWBAT polarity: 0 = Active high 1 = Active low	Reserved	EPMI1# polarity: 0 = Active high 1 = Active low	EPMI0# polarity: 0 = Active high 1 = Active low	Reserved		
SYSCFG DBh								Next Access Event Generation Register 2	Default = 00h
I/O blocking control: 0 = Block I/O on next access trap 1 = Unblock	SMI on cool-down clocking entry/exit: 0 = Disable 1 = Enable	External EPMI3# pin polarity: 0 = Active high 1 = Active low	External EPMI2# pin polarity: 0 = Active high 1 = Active low	HDU_ACCESS PMI#23 on next access: 0 = No 1 = Yes	COM2_ACCESS PMI#22 on next access: 0 = No 1 = Yes	COM1_ACCESS PMI#21 on next access: 0 = No 1 = Yes	GNR2_ACCESS PMI#20 on next access: 0 = No 1 = Yes		
SYSCFG B1h								RSMGRP IRQ Register 2	Default = 00h
EPMI3# Resume: 0 = Disable 1 = Enable	EPMI2# Resume: 0 = Disable 1 = Enable	IRQ15 Resume: 0 = Disable 1 = Enable	IRQ14 Resume: 0 = Disable 1 = Enable	IRQ12 Resume: 0 = Disable 1 = Enable	IRQ11 Resume: 0 = Disable 1 = Enable	IRQ10 Resume: 0 = Disable 1 = Enable	IRQ9 Resume: 0 = Disable 1 = Enable		
SYSCFG 6Ah								RSGGRP IRQ Register 1	Default = 00h
EPMI1# Resume: 0 = Disable 1 = Enable	EPMI0# Resume: 0 = Disable 1 = Enable	IRQ8 Resume: 0 = Disable 1 = Enable	IRQ7 Resume: 0 = Disable 1 = Enable	IRQ5 Resume: 0 = Disable 1 = Enable	IRQ4 Resume: 0 = Disable 1 = Enable	IRQ3 Resume: 0 = Disable 1 = Enable	IRQ1 Resume: 0 = Disable 1 = Enable		
SYSCFG 58h								PMU Event Register 1	Default = 00h
LOWBAT PMI#3 SMI: 00 = Disable 11 = Enable		EPMI1# PMI#2 SMI: 00 = Disable 11 = Enable		EPMI0# PMI#1 SMI: 00 = Disable 11 = Enable		LLOWBAT PMI#0 SMI: 00 = Disable 11 = Enable			
SYSCFG D9h								PMU Event Register 6	Default = 00h
DOZE_TIMER PMI#27 SMI: 00 = Disable 01 = Enable DOZE_0 10 = Enable DOZE_1 11 = Enable both		RINGI PMI#26 SMI: 00 = Disable 11 = Enable		EPMI3# cool-down clocking PMI#25 SMI: 00 = Disable 11 = Enable		EPMI2# PMI#24 SMI: 00 = Disable 11 = Enable			
SYSCFG 5Bh								PMU Event Register 4	Default = 00h
Reserved	Global SMI control: 0 = Allow 1 = Mask	Reserved		GNR1 next access PMI#15: 0 = Disable 1 = Enable	KBD next access PMI#14: 0 = Disable 1 = Enable	DSK next access PMI#13: 0 = Disable 1 = Enable	LCD next access PMI#12: 0 = Disable 1 = Enable		



Initialization Procedure:

1. Select the EPMI# input on which HDI will be provided by appropriately setting SYSCFG F0h[1:0].
2. Set SYSCFG EFh[6:5] if debouncing is required on the selected EPMI# pin. It is recommended that debouncing be enabled.
3. Select the polarity of the HDI input by appropriately setting SYSCFG 40h[2], or 40h[1], or DBh[5], or DBh[4], depending on which EPMI# input is selected as the HDI input.
4. Docking may be done when the system is in suspend. If so desired, disable the capacity of the selected EPMI# to generate a resume by setting SYSCFG B1h[7], or B1h[6], or 64h[7], or 64h[6] to 0. If a resume operation on docking is desired, the appropriate bit must be set to 1.
5. Set the time-out period by programming SYSCFG EFh[2:0]. If the system is in suspend, a default time-out of 1ms generated from the 32kHz clock is used to override this setting.
6. If an SMI is to be generated on time-out, set SYSCFG EFh[4].
7. Enable the capacity of the selected EPMI# input to generate an SMI by setting SYSCFG 58h[5:4], or 58h[3:2], or D9h[3:2], or D9h[1:0] to 11b.
8. Enable hot docking by setting SYSCFG EFh[7] to 1.
9. Finally, enable the global SMI generation control by setting SYSCFG 5Bh[6] to 0.

Figure 4-41 Insertion Times

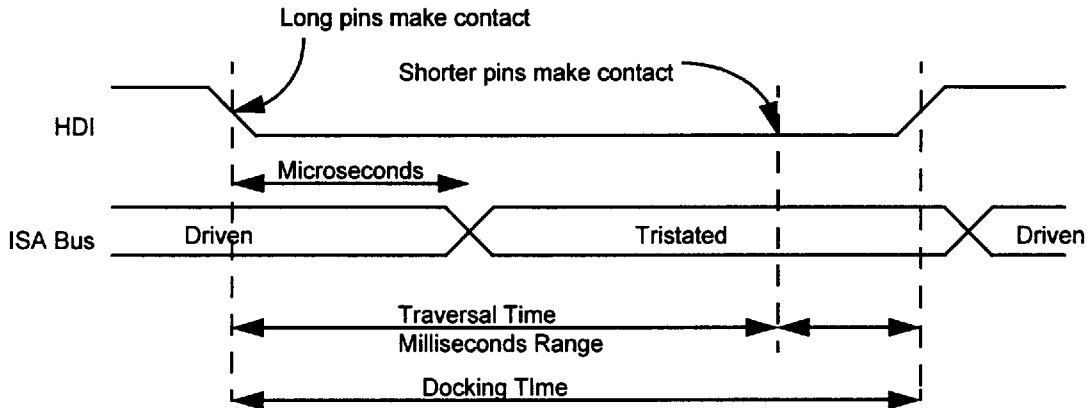


Figure 4-42 HDI Input Deasserted Within Time-out Period

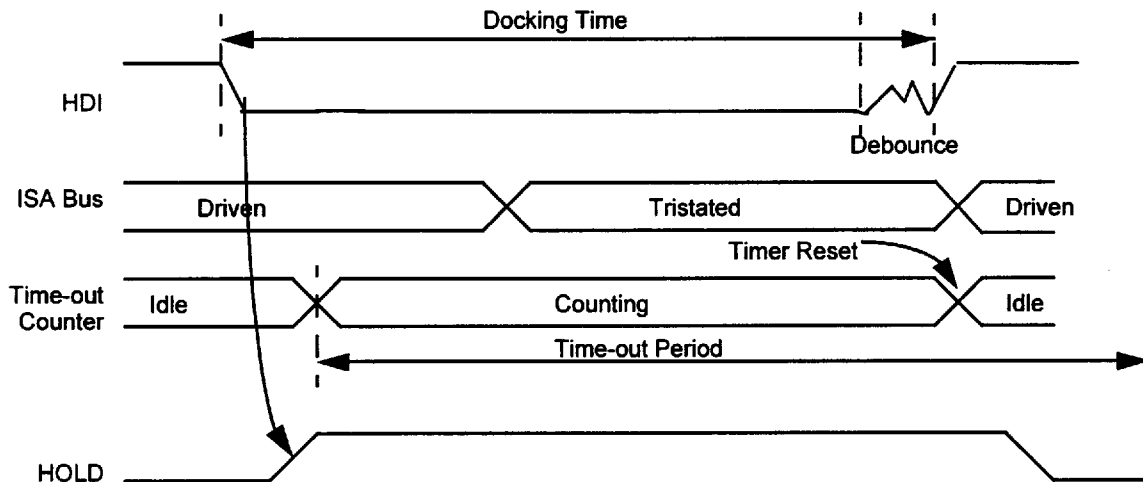
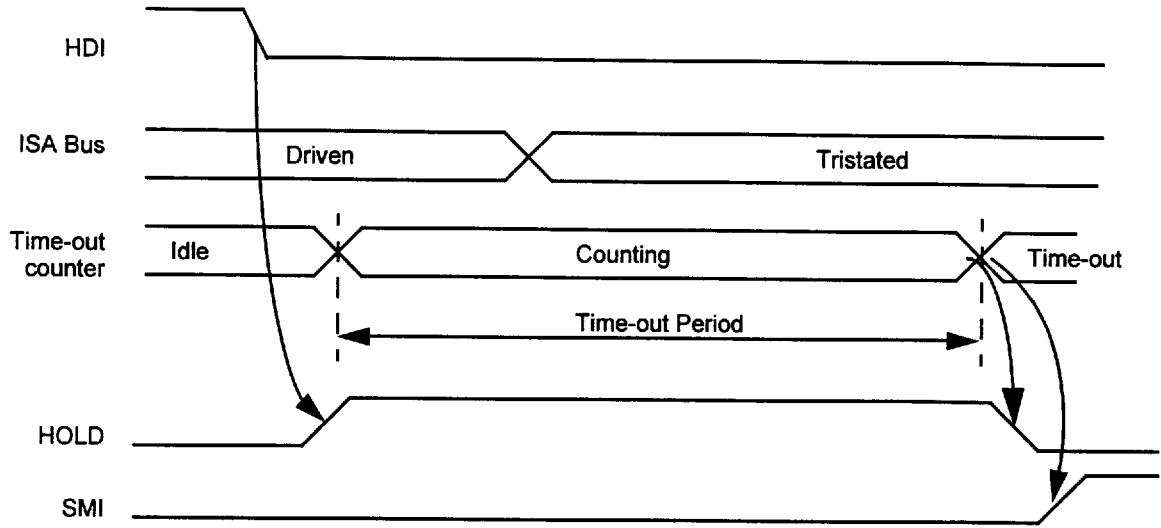


Figure 4-43 HDI Input Not Deasserted Within Time-out Period (SMI generated on time-out)



5.0 Register Descriptions

The register descriptions are organized in three broad classes:

- (i) PCI Configuration Registers,
- (ii) System Control Registers, and
- (iii) Power Management Registers.

There are PCI Configuration Registers in the 00h-3Fh range on both the 82C557 and 82C558N. They pertain only to PCI operation and are accessed by special PCI configuration mechanisms.

The System Control Registers are distributed between the 82C557 and the 82C558N. Some of the System Control Registers are accessed by an indexed method, and some are

located in the device-specific PCI address space of the 82C557 and the 82C558N, and are accessed via a PCI configuration mechanism.

The Power Management Registers are mostly located in the 82C558N and are accessed by an indexing scheme that is explained later. Table 5-1 summarizes the locations and access mechanisms for all the registers.

Note: All bit formats are read/write and their default value is 0 unless noted otherwise. RO = Read Only, R/W = Read/Write, and WO = Write Only.

Table 5-1 Register Locations and Access Mechanisms Summary

Parameter	PCI-Specific Configuration Registers		System Control Registers		PMU Registers
	82C557 PCI Registers (00h-43h)	82C558N PCI Registers (00h-3Fh)	82C557 System Control Registers (00h-19h)	82C558N System Control Registers (40h-FFh)	82C558N Power Manage- ment Registers (40h-F2h)
Access Mechanism	PCIDV0	PCIDV1	SYSCFG	PCDV1	SYSCFG
Reference Section	Section 5.1.1	Section 5.2.1	Section 5.1.2	Section 5.2.1	Section 5.2.2

- PCIDV0 is accessed through Configuration Mechanism #1 as: Bus #0, Device #0, Function #0 (relates to 82C557).
- PCIDV1 is accessed through Configuration Mechanism #1 as: Bus #0, Device #1, Function #0 (relates to 82C558N).
- SYSCFG is accessed through System I/O Space: with the index loaded at 022h the data is accessible at 024h.

Note: PCI-Specific Configuration Registers have to be accessed four bytes at a time.

5.1 82C557 Register Space

The 82C557 has two register spaces:

- 1) PCI Configuration Space
- 2) System Control Register Space

These register spaces are each accessed in different manners. The following subsections describe the register space access mechanisms and individual register bit formats.

- Bus #0,
- Device #0, and
- Function #0.

The registers at PCIDV0 00h-3Fh are used to implement PCI-specific functions.

Part of the device-specific PCI Configuration Register space of the 82C557 is used for system control. This 32-bit register (used for video control) is located at PCIDV0 40h.

5.1.1 82C557 PCI Configuration Registers

The 82C557's PCI Configuration Registers are accessed through Configuration Mechanism #1 as:

Table 5-2 82C557 PCI Configuration Registers - PCIDV0 00h-43h

7	6	5	4	3	2	1	0
Vender Identification Register (RO)							
PCIDV0 00h PCIDV0 01h							Default = 45h Default = 10h
Device Identification Register (RO)							
PCIDV0 02h PCIDV0 03h							Default = 57h Default = C5h
Command Register							
PCIDV0 04h Default = 07h							
Address/data stepping: Always set to 0.	PERR# output pin enable: Always set to 0.	Reserved (RO)	Memory write and invalidate cycle generation (RO): Always = 0. No memory write and invalidate cycles will be generated by the 82C557.	Special cycles (RO): Always = 0. The 82C557 does not respond to PCI special cycles.	Bus master operations (RO): Always = 1. Allows the 82C557 to perform bus master operations all the time. (Default = 1)	Memory access (RO): Always = 1. The 82C557 allows a PCI bus master access to memory all the time. (Default = 1)	I/O access (RO): Always = 1. The 82C557 allows a PCI bus master access to PCI I/O all the time. (Default = 1)
PCIDV0 05h Default = 00h							
Reserved (RO)						Fast back-to-back to different slaves: (must always be written 0) 0 = Disable 1 = Enable	SERR# output pin enable: Always set to 0.



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Table 5-2 82C557 PCI Configuration Registers - PCIDV0 00h-43h

7	6	5	4	3	2	1	0
PCIDV0 06h							
Status Register						Default = 80h	
Fast back-to-back capability (RO): Always set to 1 (capable). (Default = 1)		Reserved (RO)					
PCIDV0 07h							
Detected parity error (RO): Always 0.		SERR# status (RO): Always 0.	Master abort status (RO): Always set to 0.	Received target abort status (RO): 0 = No target abort 1 = Target abort occurred	Signaled target abort status (RO): Always 0.	DEVSEL# timing status (RO): Always set to 01. Medium timing is selected. The 82C557 asserts the DEVSEL# based on medium timing. (Default = 01)	Data parity detected (RO): Always 0.
PCIDV0 08h							
Revision Identification Register (RO)						Default = 00h	
Class Code Register (RO)							
PCIDV0 09h						Default = 00h	
PCIDV0 0Ah						Default = 00h	
PCIDV0 0Bh						Default = 06h	
PCIDV0 0Ch							
Reserved Register (RO)						Default = 00h	
PCIDV0 0Dh							
Master Latency Timer Register (RO)						Default = 00h	
PCIDV0 0Eh							
Header Type Register (RO)						Default = 00h	
PCIDV0 0Fh							
BIST (Built-In Self-Test) Register (RO)						Default = 00h	
PCIDV0 10h through 3Fh are reserved. Do not access these registers.							
PCIDV0 40h							
Video Control Register						Default = 00h	
Video frame buffer starting address A[29:22]							
PCIDV0 41h							
Video frame buffer starting address A[31:30]		Reserved (RO)			Video frame buffer post write control: 0 = Enable 1 = Disable	Video memory post write control: 0 = Disable 1 = Enable	I/O post write control: 0 = Disable 1 = Enable
PCIDV0 42h							
Reserved Register						Default = 00h	
PCIDV0 43h							
Reserved Register						Default = 00h	



5.1.2 82C557 System Control Registers

Port 022h is used as the Index Register and Port 024h is the Data Register. Each access to a control register consists of a:

- 1) write to Port 022h, specifying the desired register in the data byte,
- 2) followed by a read or write to Port 024h with the actual register data.

The index resets after every access; so every data access (via Port 024h) must be preceded by a write to Port 022h even if the same register is being accessed consecutively. Note that all reserved bits are to be set to zero unless otherwise noted.

Table 5-3 82C557 System Control Registers - SYSCFG 00h-19h

7	6	5	4	3	2	1	0
SYSCFG 00h DRAM Configuration Register 1 Default = 00h If 13h[7] = 1: Full Memory Decode							
Single memory write (non-cache) cycle CPU, pipelined enable: 0 = Disable 1 = Enable	Video memory byte/word prefetch control: 0 = Off 1 = On	Sony SONIC-2WP support: 0 = Sony SONIC-2WP module not installed 1 = Sony SONIC-2WP module installed	Byte merge control: 0 = Disable 1 = Enable	NA# generation during byte merge: (Used to kill CPU idle cycles during byte merge only.) 0 = Disable byte merge NA# 1 = Enable byte merge NA#	Byte/word merge time-out counter: (Access passed to PCI bus if this time-out period expires.) 00 = 4 CPU Clocks 01 = 8 CPU Clocks 10 = 12 CPU Clocks 11 = 16 CPU Clocks	Hold request block control during video byte merge: 0 = Let CPU to be put on hold while byte merge in progress if hold request arrives 1 = Block hold request if byte merge in progress	
SYSCFG 00h Default = 00h If 13h[7] = 0: 82C546/82C547 Memory Configurations Compatibility - Refer Section 4.4.6 for details							
Single memory write (non-cache) cycle CPU, pipelined enable: 0 = Disable 1 = Enable	Second bank: 512x36 SIMM	First bank: 512x36 SIMM	See Table 4-35 for decode.				
SYSCFG 01h DRAM Control Register 1 Default = 00h							
Row address hold after RAS in CLKs: 0 = 2 CLKs 1 = 1 CLK	0 = Normal page mode for master cycle 1 = RAS inactive while entering master mode	RAS pulse width used for refresh in CLKs: 00 = 7 CLKs 01 = 6 CLKs 10 = 5 CLKs 11 = 4 CLKs	Read CAS pulse width in CLKs: 0 = 3 CLKs 1 = 2 CLKs	Write CAS pulse width in CLKs: 0 = 3 CLKs 1 = 2 CLKs	RAS precharge in CLKs: 00 = 6 CLKs 01 = 5 CLKs 10 = 4 CLKs 11 = 3 CLKs		



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Table 5-3 82C557 System Control Registers - SYSCFG 00h-19h (cont.)

7	6	5	4	3	2	1	0	
SYSCFG 02h L2 Cache Control Register 1 Default = 00h								
Cache size selection: If SYSCFG 0Fh[0] = 0 00 = 64KB 01 = 128KB 10 = 256KB 11 = 512KB		Cache write policy: 00 = L2 cache write-through 01 = Adaptive Write-back Mode 1 10 = Adaptive Write-back Mode 2 11 = L2 cache write-back		Cache mode select: 00 = Disable L2 cache 01 = Test Mode 1 ⁽¹⁾ 10 = Test Mode 2 ⁽²⁾ 11 = Enable L2 cache		DRAM post write: 0 = Disable 1 = Enable	CAS precharge in CLKs: 0 = 2 CLKs 1 = 1 CLK	
(1) Test Mode 1; External tag write (tag data write-through SYSCFG 07h) (2) Test Mode 2; External tag read (tag data read from SYSCFG 07h)								
SYSCFG 03h L2 Cache Control Register 2 Default = 00h								
Cache write burst mode CLKs: 00 = X-4-4-4 01 = X-3-3-3 10 = X-2-2-2 11 = X-1-1-1		Cache write leadoff cycle CLKs:⁽¹⁾ CPU Pipelining Off 00 = 5-X-X-X 01 = 4-X-X-X 10 = 3-X-X-X 11 = 2-X-X-X		CPU Pipelining On 00 = 4-X-X-X 01 = 3-X-X-X 10 = 3-X-X-X 11 = 2-X-X-X (or 2-X-X-X if 10h[4] = 1)		Cache read burst mode CLKs: 00 = X-4-4-4 01 = X-3-3-3 10 = X-2-2-2 11 = X-1-1-1		Cache read leadoff cycle CLKs:⁽¹⁾ 00 = 5-X-X-X 01 = 4-X-X-X 10 = 3-X-X-X 11 = 2-X-X-X
(1) Cache read or write leadoff of two cycles is allowed only for standard sync SRAMs at 50MHz or below.								
SYSCFG 04h Shadow RAM Control Register 1 Default = 00h								
Read/write control for segment CC000h-CFFFFh: 00 = Read/write PCI bus 10 = Read from PCI/ write to DRAM 11 = Read from DRAM/ write to DRAM 01 = Read from DRAM/ write to PCI		Read/write control for segment C8000h-CBFFFh: Refer to SYSCFG 04h[7:6] for decode		Sync SRAM pipe 1-1-1-1 control: 0 = Pipeline according to SYSCFG 10h[5] 1 = Pipeline subsequent read bursts at 1-1-1-1 ⁽¹⁾		E0000h-EFFFFh cache-ability control: 0 = Always non-cacheable 1 = Will be treated like F000 BIOS area ⁽²⁾		Read/write control for segment C0000h-C7FFFh Refer to SYSCFG 04h[7:6] for decode
(1) If read burst is set to X-1-1-1, setting this bit will enable the following read burst at 1-1-1-1, for X-1-1-1-1-1-1-1 operation (for standard sync SRAMs only). (2) Note that in this case, SYSCFG 06h[3:2] and 06h[1:0] must be set to the same values.								
SYSCFG 05h Shadow RAM Control Register 2 Default = 00h								
Read/write control for segment DC000h-DFFFFh: Refer to SYSCFG 04h[7:6] for decode		Read/write control for segment D8000h-DBFFFh: Refer to SYSCFG 04h[7:6] for decode		Read/write control for segment D4000h-D7FFFh: Refer to SYSCFG 04h[7:6] for decode		Read/write control for segment D0000h-D3FFFh: Refer to SYSCFG 04h[7:6] for decode		

Table 5-3 82C557 System Control Registers - SYSCFG 00h-19h (cont.)

7	6	5	4	3	2	1	0
SYSCFG 06h Shadow RAM Control Register 3 Default = 00h							
DRAM hole in system memory from 80000h-9FFFFh: 0 = No hole 1 = Enable hole	CPU write-through mode wait for cycle access finish to do snooping⁽¹⁾: 0 = Don't wait 1 = Wait	Cacheability for segment C0000h-C7FFFh: 0 = No 1 = Yes in L1 and L2 ⁽²⁾	Cacheability for segment F0000h-FFFFFh: 0 = No 1 = Yes in L1 and L2 ⁽²⁾	Read/write control segment F0000h-FFFFFh: Refer to SYSCFG 04h[7:6] for decode	Read/write control segment E0000h-EFFFFh: Refer to SYSCFG 04h[7:6] for decode		
(1) This is not necessary if CPU is in full speed. (2) L1 cacheability disabled by SYSCFG 08h[0].							
SYSCFG 07h Tag Test Register Default = 00h If in Test Mode 1, data from this register is written to the tag. If in Test Mode 2, data from the tag is read into this register. (Refer to SYSCFG 02h.)							
SYSCFG 08h CPU Cache Control Register 1 Default = 00h							
L2 cache bank select: 0 = Double bank (interleaved) ⁽¹⁾ 1 = Single bank (non-interleaved)	Line comparator for bus masters:⁽²⁾ 0 = Disable 1 = Enable	CPU HITM# pin sample timing: 0 = Delay 1 more clock 1 = No delay	DRAM parity check: 0 = Disable 1 = Enable	Combined Tag/Dirty control: 0 = Tag and Dirty on different chips 1 = Tag and Dirty are on the same chip	CPU address pipelining:⁽³⁾ 0 = Disable 1 = Enable	L1 cache write-back/write-through mode setting: 0 = Write-through only 1 = Write-back enabled	BIOS area cacheability in L1 cache: 0 = Cacheable 1 = Non-cacheable
(1) Interleaved on A3 for async SRAMs, interleaved on A17 for sync SRAMs. Note that for 2-1-1-1 sync SRAM operation, dual non-interleaved banks are not supported. Only single bank is supported. (2) For a master request if the subsequent read/write is within the same cache line, CPU 'Inquire' cycles are not done until there is a cache line miss. (3) Turn on for standard sync SRAMs in 3-1-1-1 RW or for async SRAMs. This bit must be off for standard sync SRAMs in 2-1-1-1 RW. Also refer to SYSCFG 11h[4]. At any time, either SYSCFG 08h[2] or 11h[4] can be active, but not both at the same time.							
SYSCFG 09h System Memory Function Register 1 Default = 00h							
DRAM Hole B size: 00 = 512KB 01 = 1MB 10 = 2MB 11 = 4MB		DRAM Hole B control mode: 00 = Disable 01 = WT for L1 and L2 10 = Non-cacheable for L1 and L2 11 = Enable hole in DRAM		DRAM Hole A size: 00 = 512KB 01 = 1MB 10 = 2MB 11 = 4MB		DRAM Hole A control mode: 00 = Disable 01 = WT for L1 and L2 10 = Non-cacheable for L1 and L2 11 = Enable hole in DRAM	
SYSCFG 0Ah System Memory Address Decode Register 1 Default = 00h DRAM Hole A starting address AST[7:0]-HA[26:19]. Also see SYSCFG 0Ch[1:0].							
SYSCFG 0Bh System Memory Address Decode Register 2 Default = 00h DRAM Hole B starting address BST[7:0]-HA[26:19]. Also see SYSCFG 0Ch[3:2].							



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Table 5-3 82C557 System Control Registers - SYSCFG 00h-19h (cont.)

7	6	5	4	3	2	1	0
SYSCFG 0Ch DRAM Control Register 2 Default = 00h							
Reserved	Generate fast DRAM write BRDY# in three clocks (when write buffer enabled): 0 = No 1 = Yes	Generate HACALE one-half a clock cycle earlier: 0 = No 1 = Yes (may need to be set for CPU frequency greater than 50MHz)	Wider cache WE# pulse: The normal width is 1 CLK. This may be increased by 2.5-4.0ns by setting this bit. 0 = Disable 1 = Enable	DRAM Hole B starting address: BST[9:8] – HA[28:27]		DRAM Hole A starting address: AST[9:8] – HA[28:27]	
SYSCFG 0Dh Skew Adjust Register Default = 00h							
Sync SRAM clock source: 0 = CPUCLK 1 = ECLK	ECLK-CLK excessive skew indication (RO): 0 = Skew normal 1 = Skew too large	Automatically set 0Dh[4] = 1 if 0Dh[6] indicates excessive skew: 0 = No 1 = Yes	ADS# sampling clock for sync SRAM control signal generation: 0 = CPUCLK 1 = ECLK ⁽¹⁾	Enable A0000h-BFFFFh as system memory: 0 = No 1 = Yes	Add one more wait state during PCI master cycle with Intel-type address toggling: 0 = No 1 = Yes	Give the 82C557 control of the PCI bus on STOP# generation after HITM# is active: 0 = No 1 = Yes ⁽²⁾	CPU clock is expected to be slowed down to below 33MHz: 0 = No 1 = Yes
(1) ECLK is used for sampling ADS# only if the ECLK-CLK skew is too large. Either set by BIOS after reading 0Dh[6], or automatically set by the 82C557 if 0Dh[5] = 1.							
(2) The 82C557 has control over the PCI bus until the write-back is completed during PCI snoop cycles.							
SYSCFG 0Eh PCI Control Register 1 Default = 00h							
PCI master read wait state control for cache: 00 = X-4-4-4 01 = X-3-3-3 10 = X-2-2-2 11 = Rsvd		PCI master write wait state control for cache: 00 = X-4-4-4 01 = X-3-3-3 10 = X-2-2-2 11 = Rsvd		Parity check during master cycles: 0 = Enable 1 = Disable	HACALE control ⁽¹⁾ : 0 = HACALE high during HITM# before CPU ADS# 1 = HACALE low and CA4 always enabled during HITM cycle, to save external F126	BIOS write protection for L1: 0 = Disable 1 = Enable	PCI master line comparator: 0 = Use line comparator in PCI master cycle 1 = Generate inquire cycle for every new FRAME#
(1) Must be set to 1 if an external F126 is not used for A3 and A4 of cache.							

Table 5-3 82C557 System Control Registers - SYSCFG 00h-19h (cont.)

7	6	5	4	3	2	1	0
SYSCFG 0Fh L2 Cache Control Register 3							
Default = 00h							
PCI master cycle pre-snooping: 0 = Disabled 1 = Enabled ⁽¹⁾	Insert wait states for ISA master access: 0 = No 1 = Yes	Add 1 more WS for sync SRAM even bank access: 0 = No 1 = Yes	Resynchronize PCI master accesses to system DRAM: 0 = No 1 = Yes ⁽²⁾	Reserved	Generate ADSC# for sync SRAM 1 clock after CPU ADS# in read cycle: ⁽³⁾ 0 = Yes 1 = No	Reserved	Cache size selection: 0 = Less than 1MB 1 = 1MB or greater (Refer to SYSCFG 02h[7:6])
(1) The 82C557 generates a pre-snoop cycle to the CPU assuming that the PCI master will do a burst. (2) If set to 1, in sync SRAM mode, PCI master access to system memory will force the master to wait for the current cycle to finish and the CPU-PCI clock to become sync. This is a conservative mode. (3) Must be set for pipeline sync cache or for standard sync cache when running in 2-1-1-1 RW mode.							
SYSCFG 10h Timing Control Register 1							
Default = 00h							
CPU to PCI/VL/ISA slave cycle triggered after: 0 = Second T2 1 = First T2	Address changing control for async SRAMs: 0 = Compatible to 82C596/82C597 1 = Two bank cache: Delay write cycle CA4 by one-half clock cycle	Read pipelining control: 0 = Allow 3-X-X-X read to be piped into 3-X-X-X 1 = Allow 2-X-X-X read to be piped into 3-X-X-X read	2-X-X-X pipelined write hit cycles: 0 = Disable 1 = Enable	Move the write pulse one-half clock cycle later in X-2-2-2 write hit cycles: 0 = No 1 = Yes	Move the write pulse one-half clock cycle earlier in 3-X-X-X write hit cycles: 0 = No 1 = Yes	External 74F126 is installed for A3 and A4: [*] 0 = Yes 1 = No	LCLK select control: 0 = LCLK is async to CPUCLK 1 = LCLK is sync to the CPUCLK
*Must be set for sync and for async SRAM if an external 74F126 is not installed for A3 and A4 of the cache.							
SYSCFG 11h Miscellaneous Control Register 1							
Default = 00h							
Reserved	SRAM activity during Idle state: 0 = Active 1 = Inactive (If inactive, cache CS# is turned off during non-cache cycles).	NA# generation mode: 0 = Generate NA# as soon as possible 1 = New NA# mode for sync SRAM ⁽¹⁾	L2 cache SRAM type: 0 = Async SRAM 1 = Sync SRAM	Page miss posted write: 0 = Enable 1 = Disable	ISA/DMA IOCHRDY control: 0 = No IOCHRDY during line hit 1 = Drive IOCHRDY low until cycle is finished	0 = Delay internal master cycles by one LCLK after inquire cycle: 0 = No 1 = Yes	
⁽¹⁾ This bit has to be set if ADSP# of sync SRAM is connected to the CPU ADS#. NA# is generated one clock before the last BRDY# to the CPU. Set this bit if CPU pipelining is desired when using either pipelined sync SRAMs or standard sync SRAMs in 2-1-1-1 RW mode. At any time either 11h[4] or 08h[2] can be set, however they can not be active at the same time.							



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Table 5-3 82C557 System Control Registers - SYSCFG 00h-19h (cont.)

7	6	5	4	3	2	1	0	
SYSCFG 12h Refresh Control Register Default = 00h								
Reserved	Reserved	Suspend mode refresh control: 00 = Timing for refresh based on SYSCFG 12h[3:2](with refresh timing based on CLK input) 01 = Self-refresh timing (refresh pulse width equals REFRESH# low time) 10 = 100ns refresh pulse width triggered by REFRESH# 11 = Rsvd		Slow refresh control: 00 = Refresh on every REFRESH# falling edge 01 = Refresh on one in two REFRESH# falling edges 10 = Refresh on one in four REFRESH# falling edges 11 = Refresh on every REFRESH# edge (both rising and falling)		Generate LA[23:17] from 08Fh (Refresh DMA Page Addr. Reg.) during refresh: 0 = Disable 1 = Enable		82C556 generates MP[7:4] for PCI master writes: 0 = No 1 = Yes
SYSCFG 13h Memory Sizing Register 1 Default = 00h								
Memory decode select: 0 = Table lookup (compatible to 82C547) 1 = Full decode	Full decode for logical Bank 1 (RAS1#) if SYSCFG 13h[7] set: 000 = Disabled 001 = 256Kx36x2 010 = 512Kx36x2 011 = 1Mx36x2		100 = 2Mx36 101 = 4Mx36x2 110 = 8Mx36x2 111 = 16Mx36x2	SMRAM: 0 = Disable 1 = Enable (depending on SYSCFG 14h[3])	Full decode for logical Bank 0 (RAS0#) if SYSCFG 13h[7] set: 000 = Disabled 001 = 256Kx36x2 010 = 512Kx36x2 011 = 1Mx36x2			100 = 2Mx36x2 101 = 4Mx36x2 110 = 8Mx36 111 = 16Mx36x2
SYSCFG 14h Memory Sizing Register 2 Default = 00h								
Reserved: Write 0.	Full decode for logical Bank 3 (RAS3#) if SYSCFG 13h[7] set: 000 = Disabled 001 = 256Kx36x2 010 = 512Kx36x2 011 = 1Mx36x2		100 = 2Mx36x2 101 = 4Mx36x2 110 = 8Mx36x2 111 = 16Mx36x2	If SMIACT# is inactive: 0 = Disable SMRAM 1 = Enable SMRAM If SMIACT# is active and SYSCFG 13h[3] = 1: 0 = Enable SMRAM for Code and Data 1 = Enable SMRAM for Code only	Full decode for logical Bank 2 (RAS2#) if SYSCFG 13h[7] set: 000 = Disabled 001 = 256Kx36x2 010 = 512Kx36x2 011 = 1Mx36x2			100 = 2Mx36x2 101 = 4Mx36x2 110 = 8Mx36x2 111 = 16Mx36x2
SYSCFG 15h PCI Control Register 2 Default = 00h								
CPU master to PCI slave write IRDY# control: 00 = 3 LCLKs after data 01 = 2 LCLKs after data 10 = 1 LCLK after data 11 = 0 LCLK after data	CPU master to PCI slave memory write control: 00 = No posting, no bursting 01 = Posting only, no bursting 10 = Posting, with conservative bursting 11 = Posting, with aggressive bursting		Master retry timer - Selects the delay before retry is attempted: 00 = 10 PCICLKs 01 = 18 PCICLKs 10 = 34 PCICLKs 11 = 66 PCICLKs		Turnaround delay between address and data phase for CPU back-to-back write to PCI slave: 0 = 1 LCLK 1 = Controlled by PCIDV0 05h[1]	PCI FRAME# generation control: 0 = Conservative mode in CPU pipelined cycle 1 = Aggressive mode		

Table 5-3 82C557 System Control Registers - SYSCFG 00h-19h (cont.)

7	6	5	4	3	2	1	0
SYSCFG 16h L2 Cache Control Register 4 Default = 00h							
DIRTY pin control: 0 = Input only 1 = I/O (for a combined Tag/ Dirty SRAM)	Reserved	Tag size: 0 = 8-bit tag 1 = 7-bit tag	Single write hit leadoff cycle: ⁽¹⁾ 0 = 5 cycles for combined Tag/ Dirty 1 = 4 cycles	Pre-snoop control: 0 = Pre-snoop only for starting address of 0. 1 = Pre-snoop for all addresses except for line boundary.	Reserved	Assert DLE# one-half an LCLK cycle earlier during CPU read access from VL bus: 0 = No 1 = Yes	HDOE# ends one clock before the end of the cycle: 0 = No 1 = Yes
(1) This bit must be set only when the DIRTY bit is on a *1 part which has separate input and output.							
SYSCFG 17h Miscellaneous Control Register 2 Default = 00h							
Generate NA# for PCI slave access in sync LCLK mode: 0 = No 1 = Yes	NA# generation for PCI slave access: 0 = Do not generate NA# 1 = Generate NA# for async LCLK mode	Sync two bank select: 0 = Rsrvd 1 = Set this bit to 1 when two banks of sync SRAM are installed	BRDY# control for PCI cycles: 0 = Normal BRDY# 1 = Fast BRDY#	Fast FRAME# generation for PCI cycles: 0 = Disable 1 = Enable	Pipelining during byte merge: 0 = Disabled 1 = Enabled	Sync SRAM type: 0 = Standard 1 = Pipelined	Burst type: 0 = Intel burst protocol 1 = Linear burst protocol
SYSCFG 18h Signal State Control Register Default = 00h							
Reserved	CAS[X]# 3.3V/ 5.0V selection: 0 = 5.0V drive on CAS[X]# lines 1 = 3.3V drive on CAS[X]# lines	Drive strength on memory address lines, RAS lines, and write enable line: 0 = 4mA 1 = 16mA	CPU status during Suspend: 0 = Powered on 1 = Powered off	PCI bus tristate control during Suspend: 0 = PCI bus parked by 82C557 1 = Tristate ⁽¹⁾	Cache status during Suspend: 0 = Powered on 1 = Powered off	Global 82C557 leakage control: 0 = Disable 1 = Enable	
(1) Tristate AD[31:0], FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, C/BE#[3:0].							
SYSCFG 19h Memory Sizing Register 3 Default = 00h							
RAS5# selection (on pin 196): 0 = Generate DIRTYWE# on pin 196 1 = Generate RAS5# on pin 196	Full decode for logical Bank 5 (RAS5#) if SYSCFG 13h[7] = 1 and 19h[7] = 1: 000 = Disable 100 = 2Mx36x2 001 = 256Kx36x2 101 = 4Mx36x2 010 = 512Kx36x2 110 = 8Mx36x2 011 = 1Mx36x2 111 = 16Mx36x2		RAS4# selection (on pin 76): 0 = Generate MA11 on pin 76 1 = Generate RAS4# on pin 7	Full decode for logical Bank 4 (RAS4#) if SYSCFG 13h[7] = 1 and 19h[3] = 1: 000 = Disable 100 = 2Mx36x2 001 = 256Kx36x2 101 = 4Mx36x2 010 = 512Kx36x2 110 = 8Mx36x2 011 = 1Mx36x2 111 = 16Mx3x2			



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5.2 82C558N Register Space

The 82C558N has three register spaces:

- 1) PCI Configuration Register Space
- 2) System Control Register Space
- 4) Power Management Register Space

- On Bus #0,
- Device #1,
- Function #0.

The registers at PCIDV1 00h-3Fh (described in Table 5-4) are used for PCI-specific functions.

5.2.1 82C558N PCI Configuration Register Space

The PCI Configuration Registers of the 82C558N are accessed through Configuration Mechanism #1 as:

The registers at PCIDV1 40h-FFh (described in Table 5-5) are used for device-specific functions and are related to system control.

Table 5-4 82C558N PCI Configuration Registers - PCIDV1 00h-3Fh

7	6	5	4	3	2	1	0
Vender Identification Register (RO)							
PCIDV1 00h PCIDV1 01h							Default = 45h Default = 10h
Device Identification Register (RO)							
PCIDV1 02h PCIDV1 03h							Default = 58h Default = C5h
Command Register							
PCIDV1 04h Default = 07h							
Address/data stepping: Always set to 0.	Enable parity error output: 0 = Disable 1 = Enable	Reserved (RO)	Memory write and invalidate cycle generation (RO): Always = 0. No memory write and invalidate cycles will be generated by the 82C558N.	Special cycles: 0 = Disable 1 = Enable (82C558N responds to stop grant special cycle.)	Bus master operations: 0 = Disable 1 = Enable PCI cycle generation during DMA/ISA master may be disabled by this bit. (Default = 1)	Memory access (RO): Always = 1. The 82C558N allows a PCI bus master access to memory at any time. (Default = 1)	I/O access (RO): Always = 1. The 82C558N allows a PCI bus master access to I/O at any time. (Default = 1)
PCIDV1 05h Default = 00h							
Reserved (RO)						Fast back-to-back to different slaves (RO): (set to 0 always) 0 = Disable 1 = Enable	SERR# output pin: 0 = Disable 1 = Enable

Table 5-4 82C558N PCI Configuration Registers - PCIDV1 00h-3Fh (cont.)

7	6	5	4	3	2	1	0
PCIDV1 06h Status Register (RO) Default = 80h							
Fast back-to-back capability: 0 = Not capable 1 = Capable (Default = 1)		Reserved					
PCIDV1 07h Default = 02h							
Detected parity error: 0 = No parity error 1 = Parity error has occurred	SERR# status: 0 = No system error 1 = System error has occurred	Master abort status: Always set to 0.	Received target abort status: 0 = No target abort 1 = Target abort occurred	Signaled target abort status: Always 0.	DEVSEL# timing status: These bits always = 01. Medium timing is selected. The 82C558N asserts DEVSEL# based on medium timing. (Default = 01)		Data parity detected: 0 = No data parity detected 1 = Data parity detected
PCIDV1 08h Revision Identification Register (RO) Default = 00h							
Class Code Register							
PCIDV1 09h PCIDV1 0Ah PCIDV1 0Bh						Default = 00h Default = 01h Default = 06h	
PCIDV1 0Ch Reserved Register (RO) Default = 00h							
PCIDV1 0Dh Master Latency Timer Register (RO) Default = 00h							
PCIDV1 0Eh Header Type Register (RO) Default = 00h							
PCIDV1 0Fh BIST (Built-In Self-Test) Register (RO) Default = 00h							
PCIDV1 10h through 3Fh are reserved. Do not access these registers.							



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Table 5-5 82C558N System Control Registers - PCIDV1 40h-FFh

7	6	5	4	3	2	1	0
PCIDV1 40h PCI IRQ Select Register							
Default = 00h							
P2IRQ[1:0]: Works with P2IRQ[2] to select which IRQ signal is generated when PCI interrupt request PCIRQ2# has been triggered: Refer to P3IRQ[2:0] for decode.		P1IRQ[2:0]: Selects which IRQ signal is generated when PCI interrupt request PCIRQ1# has been triggered: Refer to P3IRQ[2:0] for decode.			P0IRQ[2:0]: Selects which IRQ signal is generated when PCI interrupt request PCIRQ0# has been triggered: Refer to P3IRQ[2:0] for decode.		
PCIDV1 41h							
Default = 00h							
RDKBDPRT (RO): Keyboard controller has received Command D0h and has not received the following 60h read.	WRKBDPRT (RO): Keyboard controller has received Command D1h and has not received the following 60h write.	IMMINIT: Generate INIT immediately on FEh Command. 0 = Generate INIT immediately on FEh Command 1 = Wait for halt before INIT for keyboard reset	KBDEMU: Keyboard emulation 0 = Enable 1 = Disable	P3IRQ[2:0]: Selects which IRQ signal is generated when PCI interrupt request PCIRQ3# has been triggered: 000 = Disabled 100 = IRQ11 001 = IRQ5 101 = IRQ12 010 = IRQ9 110 = IRQ14 011 = IRQ10 111 = IRQ15		P2IRQ[2]: Works with P2IRQ[1:0] to select which IRQ signal is generated when PCI interrupt request PCIRQ2# has been triggered:	
PCIDV1 42h IRQ Triggering Register							
Default = 00h							
Triggering for IRQ15: 0 = Edge 1 = Level	Triggering for IRQ14: 0 = Edge 1 = Level	Triggering for IRQ12: 0 = Edge 1 = Level	Triggering for IRQ11: 0 = Edge 1 = Level	Triggering for IRQ10: 0 = Edge 1 = Level	Triggering for IRQ9: 0 = Edge 1 = Level	Triggering for IRQ5: 0 = Edge 1 = Level	SUSPI pin control: 0 = Drive low during normal operation and drive high during suspend. 1 = Tristate during normal operation and drive high during Suspend
PCIDV1 43h							
Default = 00h							
Reserved	Enable DMA or ISA master to preempt PCI Master 0 = Disable 1 = Enable	Fixed/rotating priority between PCI masters: 0 = Rotating 1 = Fixed	Back-to-back ISA I/O: 0 = Enable 1 = Disable	Reserved	PCI master access to VL/ISA: 0 = Enable 1 = Disable	ISA bus control signals for memory accesses greater than 16M: 0 = Enable 1 = Disable	

Table 5-5 82C558N System Control Registers - PCIDV1 40h-FFh (cont.)

7	6	5	4	3	2	1	0
PCIDV1 44h Pin Programming Register A Default = 00h Reserved							
PCIDV1 45h Default = 00h							
Group 4 ⁽¹⁾ programming: 0 = Non-602A mode 1 = 602A mode	Group 3 ⁽²⁾ programming: 0 = Standard EPIMs 1 = Direct input KBC RESET or GA20	Reserved	Group 2 ⁽³⁾ programming: 00 = Thermal management 01 = VL bus 10 = Parity generation 11 = Direct input KBC RESET or GA20	Reserved	Group 1 ⁽⁴⁾ Programming: 0 = GPCS0# GPCS1# and discrete DACKs 1 = Encoded DACKs	Block IRQ that IRQA is mapped to: 0 = No 1 = Yes	
(1) Group 4 = Pins 116, 117, 120, 120, 121, 122, 123, 124, 128, 129, and 135. (2) Group 3 = Pins 126 and 132. (3) Group 2 = Pins 52, 112, 113, 115, 155, and 156. (4) Group 1 = Pins 108, 109, 110, and 111. For more specifics on pin programming, refer Section 3.5 (82C558N Signal Descriptions).							
PCIDV1 46h PCI Control Register B Default = 06h							
DMA/ISA access to PCI memory: 00 = Never 01 = When not LMEM# and not M16# 10 = When not LMEM# 11 = Rsvrd (Note: Master retry always unmasked after 16 LCLKs)	Conversion of PERR# to SERR#: 0 = Disable 1 = Enable	Address parity checking: 0 = Disable 1 = Enable	Generation of SERR# for target abort: 0 = Disable 1 = Enable	Fast back-to-back capability: 0 = Disable 1 = Enable Note: The change on this bit will reflect in PCIDV1 06h[7].	Subtractive decoding sample point: 0 = Typical sample point 1 = Slow sample point	Wait for IRDY# to generate VL cycle 0 = Disable 1 = Enable	
PCIDV1 47h Default = 00h							
Write protect ISA bus ROM: 0 = Disable ROMCS# for writes 1 = Enable ROMCS# for writes	Hidden refresh: 0 = Normal refresh 1 = Hidden refresh	ATCLK frequency: 00 = LCLK +4 01 = LCLK +3 10 = LCLK +2 11 = LCLK	CPU master to PCI slave write: (turn-around between address and data phases) 0 = 1 LCLK 1 = 0 LCLK	PCI master to PCI master preemption timer: (pre-empt after unserviced request pending for X LCLKs) 000 = No Preemption 100 = 36 LCLKs 001 = 260 LCLKs 101 = 20 LCLKs 010 = 132 LCLKs 110 = 12 LCLKs 011 = 68 LCLKs 111 = 5 LCLKs			



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Table 5-5 82C558N System Control Registers - PCIDV1 40h-FFh (cont.)

7	6	5	4	3	2	1	0								
PCIDV1 48h Pin Programming Register B Default = 00h															
Pin 122 functionality: Non-602AMode 602AMode 00 = DREQ1/6 00 = DREQ1 01 = DREQ1 01 = DREQ1/6 10 = DREQ6 10 = DREQ6 11 = Rsvrd 11 = DREQB		Pin 123 functionality: Non-602AMode 602AMode 00 = DREQ3/7 00 = DREQ3 01 = DREQ3 01 = DREQ3/7 10 = DREQ7 10 = DREQ7 11 = Rsvrd 11 = Rsvrd		Pin 124 functionality: Non-602A Mode 0 = IRQ1 1 = IRQ1/4 602AMode 0 = RQMX0 (IRQ1/3/10/12) 1 = Rsvrd		Pin 135 functionality: Non-602A Mode 0 = IRQ14 1 = Rsvrd 602AMode 0 = RQMX1 (IRQ8#/4/14/15) 1 = Rsvrd		Pin 128 functionality: Non-602A Mode 0 = IRQ6 1 = IRQ6/7 602AMode 0 = IRQ6 1 = Rsvrd							
Pin 129 functionality: Non-602A Mode 0 = IRQ7 1 = Rsvrd 602AMode 0 = IRQ7 1 = Rsvrd		PCIDV1 49h Default = 00h													
Pin 116 functionality: Non-602AMode 602AMode 00 = IRQ10/12 00 = DREQ5 01 = IRQ10 01 = Rsvrd 10 = IRQ12 10 = Rsvrd 11 = Rsvrd 11 = Rsvrd		Pin 117 functionality: Non-602AMode 602AMode 00 = IRQ3/4 00 = DREQ6 01 = IRQ3 01 = KBRST# 10 = IRQ4 10 = Rsvrd 11 = Rsvrd 11 = Rsvrd		Pin 120 functionality: Non-602AMode 602AMode 00 = IRQ8#/15 00 = DREQ7 01 = IRQ8# 01 = KBA20M 10 = IRQ15 10 = Rsvrd 11 = Rsvrd 11 = Rsvrd		Pin 121 functionality: Non-602AMode 602AMode 00 = DREQ0/5 00 = DREQ0 01 = DREQ0 01 = DREQ0/5 10 = DREQ5 10 = DREQ5 11 = Rsvrd 11 = DREQA		Note: Non-602A Mode: PCIDV1 45h[7] = 0, 602A Mode: PCIDV1 45h[7] = 1							
PCIDV1 4Ah ROM Chip Select Register Default = 00h															
ROMCS# for segment F8000h-FFFFh: 0 = Enable 1 = Disable	ROMCS# for segment F0000h-F7FFFh: 0 = Enable 1 = Disable	ROMCS# for segment E8000h-EFFFFh: 0 = Disable 1 = Enable	ROMCS# for segment E0000h-E7FFFh: 0 = Disable 1 = Enable	ROMCS# for segment D8000h-DFFFFh: 0 = Disable 1 = Enable	ROMCS# for segment D0000h-D7FFFh: 0 = Disable 1 = Enable	ROMCS# for segment C8000h-CFFFFh: 0 = Disable 1 = Enable	ROMCS# for segment C0000h-C7FFFh: 0 = Disable 1 = Enable								
PCIDV1 4Bh Default = 00h															
ROMCS# for segment FFFF8000h-FFFFFFFh: 0 = Enable 1 = Disable	ROMCS# for segment FFFF0000h-FFFF7FFFh: 0 = Enable 1 = Disable	ROMCS# for segment FFFE8000h-FFFEFFFFh: 0 = Disable 1 = Enable	ROMCS# for segment FFFE0000h-FFFE7FFFh: 0 = Disable 1 = Enable	ROMCS# for segment FFFD8000h-FFFD7FFFh: 0 = Disable 1 = Enable	ROMCS# for segment FFFD0000h-FFFD7FFFh: 0 = Disable 1 = Enable	ROMCS# for segment FFFC8000h-FFFC7FFFh: 0 = Disable 1 = Enable	ROMCS# for segment FFFC0000h-FFFC7FFFh: 0 = Disable 1 = Enable								
PCIDV1 4Ch Pin Programming Register C Default = 40h															
Include as part DREQA mapping description (PCIDV1 4Dh[1:0])	DREQB mapping: 000 = DREQ0 100 = Rsvrd 001 = DREQ1 101 = DREQ5 010 = DREQ2 110 = DREQ6 011 = DREQ3 111 = DREQ7			IRQA mapping:⁽¹⁾ 0000 = Rsvrd 0100 = IRQ4 1000 = IRQ8# 1100 = IRQ12 0001 = IRQ1 0101 = IRQ5 1001 = IRQ9 1101 = Rsvrd 0010 = Rsvrd 0110 = IRQ6 1010 = IRQ10 1110 = IRQ14 0011 = IRQ3 0111 = IRQ7 1011 = IRQ11 1111 = IRQ15											
PCIDV1 4Dh Default = 02h															
Reserved	Pin 73 functionality: 0 = XDIR 1 = GPCS2#	Reserved	Pin 125 functionality: 0 = PPWRL1 1 = RSMRST	2:1 mux clock: 00 = ATCLK 10 = OSC 01 = LCLK 11 = Rsvrd This setting is valid only for pins programmed to accept muxed inputs through a '157 type mux.		DREQA mapping: 000 = DREQ0 100 = Rsvrd 001 = DREQ1 101 = DREQ5 010 = DREQ2 110 = DREQ6 011 = DREQ3 111 = DREQ7									
(1) If pin 113 is programmed to be IRQA, then the interrupt that IRQA is mapped to will not be recognized through any pin that may be programmed to accept that interrupt (by itself or when muxed with other interrupts) when PCIDV1 45h[0] is set. For more specifics on pin programming, refer Section 3.5 (82C558N Signal Descriptions).															



Table 5-5 82C558N System Control Registers - PCIDV1 40h-FFh (cont.)

7	6	5	4	3	2	1	0
PCIDV1 4Eh							
Miscellaneous Control Register C							Default = 00h
0 = Test 4 Disabled 1 = Test 4 Enabled	0 = Test 3 Disabled 1 = Test 3 Enabled	0 = Test 2 Disabled 1 = Test 2 Enabled	0 = Test 1 Disabled 1 = Test 1 Enabled	Pipelined byte merge function: 0 = Disable 1 = Enable	EOP configuration: 0 = Output 1 = Input	Byte merge: 0 = Disable 1 = Enable	ISA master data swap: 0 = Enable 1 = Disable
PCIDV1 4Fh							
Reserved			AT clock wait state control: 0 = Extra WS for ISA cycles 1 = No extra WS	Reserved			
PCIDV1 50h							
PCI IRQ Control Register B							Default = 00h
Selects IRQ signal to be gener- ated when PCIRQ3# has been triggered:		Selects IRQ signal to be gener- ated when PCIRQ2# has been triggered:		Selects IRQ signal to be gener- ated when PCIRQ1# has been triggered:		Selects IRQ signal to be gener- ated when PCIRQ0# has been triggered:	
00 = Disabled 01 = IRQ3	10 = IRQ4 11 = IRQ7	00 = Disabled 01 = IRQ3	10 = IRQ4 11 = IRQ7	00 = Disabled 01 = IRQ3	10 = IRQ4 11 = IRQ7	00 = Disabled 01 = IRQ3	10 = IRQ4 11 = IRQ7
PCIDV1 51h							
Reserved (RO)				Triggering for IRQ3: 0 = Edge 1 = Level	Triggering for IRQ4: 0 = Edge 1 = Level	Triggering for IRQ7: 0 = Edge 1 = Level	
PCIDV1 52h through FDh are reserved. Do not access these registers.							
PCIDV1 FEh							
Stop Grant Cycle Data Register (RO)							Default = 00h
A byte write to this register indicates a Stop Grant cycle. The data is "don't care". Read from this register is undefined. The 82C557 propagates the CPU Stop Grant cycle as a configuration write to this register. The BIOS should never write to this configuration register. The 82C558N should ignore any write to this space unless it has driven STPCLK# active.							



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5.2.2 82C558N Power Management Register Descriptions

The Power Management Registers are part of the SYSCFG register group. They are located in the 82C558N and are accessed by an indexing scheme.

Port 022h is used as the Index Register and Port 024h is the Data Register. Each access to a control register consists of a:

- 1) write to Port 022h, specifying the desired register in the data byte,
- 2) followed by a read or write to Port 024h with the actual register data.

The index resets after every access; so every data access (via Port 024h) must be preceded by a write to Port 022h even if the same register is being accessed consecutively. Note that all reserved bits are to be set to zero unless otherwise noted.

Table 5-6 gives the Power Management Register's formats.

Note: In Table 5-6 all bit formats are read/write and their default value is 0 unless noted otherwise. RO = Read Only, R/W = Read/Write, and WO = Write Only.

Table 5-6 82C558N Power Management Registers: SYSCFG 40h-F2h

7	6	5	4	3	2	1	0
SYSCFG 40h PMU Control Register 1 Default = 00h							
Reserved	Global timer divide: 0 = +1 1 = +4	LLOWBAT polarity: 0 = Active high 1 = Active low	LOWBAT polarity: 0 = Active high 1 = Active low	Reserved	EPMI1# polarity: 0 = Active high 1 = Active low	EPMI0# polarity: 0 = Active high 1 = Active low	Reserved
SYSCFG 41h DOZE_TIMER Register 2 Default = 00h							
DOZE_0 time-out select: 000 = 2ms 001 = 4ms 010 = 8ms 011 = 32ms 100 = 128ms 101 = 512ms 110 = 2s 111 = 8s Time-out generates PMI#27.		Doze mode STPCLK# modulation (STPCLK# modulated by BCLK defined in E6h[7:6]): 000 = No Modulation (STPCLK# = 1) 001 = STPCLK# $t_{ij} = 0.75 * 16$ BCLKs 010 = STPCLK# $t_{ij} = 0.5 * 16$ BCLKs 011 = STPCLK# $t_{ij} = 0.25 * 16$ BCLKs 100 = STPCLK# $t_{ij} = 0.125 * 16$ BCLKs 101 = STPCLK# $t_{ij} = 0.0625 * 16$ BCLKs 110 = STPCLK# $t_{ij} = 0.03125 * 32$ BCLKs 111 = STPCLK# $t_{ij} = 0.015625 * 64$ BCLKs			ACCESS events reset doze mode: 0 = Disable 1 = Enable	Doze control select: 0 = Hardware 1 = Software	
SYSCFG 42h Clock Source Register 1 Default = 00h							
Clock source for GNR1_TIMER		Clock source for KBD_TIMER		Clock source for DSK_TIMER		Clock source for LCD_TIMER	
SYSCFG 43h PMU Control Register 3 Default = 00h							
LCD_ACCESS includes I/O range 3B0h-3DFh: 0 = Yes 1 = No	LCD_ACCESS includes memory A0000-BFFFFh: 0 = Yes 1 = No	LOWBAT pin sample rate: (A PMI is generated each time LOWBAT is sampled active.) 00 = 32s 10 = 128s 01 = 64s 11 = Rsvrd		Reserved			
SYSCFG 44h LCD Timer Register Default = 00h							
Time count byte for LCD_TIMER - monitors LCD_ACCESS. Time-out generates PMI#8.							
SYSCFG 45h DSK_TIMER Register Default = 00h							
Time count byte for DSK_TIMER - monitors DSK_ACCESS. Time-out generates PMI#9.							



Table 5-6 82C558N Power Management Registers: SYSCFG 40h-F2h (cont.)

7	6	5	4	3	2	1	0								
<p>SYSCFG 46h KBD_TIMER Register Default = 00h</p> <p style="text-align: center;">Time count byte for KBD_TIMER - monitors KBD_ACCESS. Time-out generates PMI#10.</p>															
<p>SYSCFG 47h GNR1_TIMER Register Default = 00h</p> <p style="text-align: center;">Time count byte for GNR1_TIMER - monitors GNR1_ACCESS. Time-out generates PMI#11.</p>															
<p>SYSCFG 48h GNR1 Base Address Register Default = 00h</p> <p style="text-align: center;">GNR1_ACCESS base address: A[8:1] (I/O) or A[22:15] (Memory)</p>															
<p>SYSCFG 49h GNR1 Control Register Default = 00h</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 12.5%;">GNR1 base address: A9 (I/O) A23 (Memory)</td> <td style="width: 12.5%;">Write decode: 0 = Disable 1 = Enable</td> <td style="width: 12.5%;">Read decode: 0 = Disable 1 = Enable</td> <td colspan="5">GNR1 mask bits for address A[5:1] (I/O) or A[19:15] memory: A 1 in a particular bit means that the corresponding bit at 48h[4:0] is not compared. This is used to determine address block size.</td> </tr> </table>								GNR1 base address: A9 (I/O) A23 (Memory)	Write decode: 0 = Disable 1 = Enable	Read decode: 0 = Disable 1 = Enable	GNR1 mask bits for address A[5:1] (I/O) or A[19:15] memory: A 1 in a particular bit means that the corresponding bit at 48h[4:0] is not compared. This is used to determine address block size.				
GNR1 base address: A9 (I/O) A23 (Memory)	Write decode: 0 = Disable 1 = Enable	Read decode: 0 = Disable 1 = Enable	GNR1 mask bits for address A[5:1] (I/O) or A[19:15] memory: A 1 in a particular bit means that the corresponding bit at 48h[4:0] is not compared. This is used to determine address block size.												
<p>SYSCFG 4Ah Chip Select 0 Base Address Register Default = 00h</p> <p style="text-align: center;">GPCS0# base address: A[8:1] (I/O) or A[22:15] (Memory)</p>															
<p>SYSCFG 4Bh Chip Select 0 Control Register Default = 00h</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 12.5%;">GPCS0# base address: A9 (I/O) A23 (Memory)</td> <td style="width: 12.5%;">Write decode: 0 = Disable 1 = Enable</td> <td style="width: 12.5%;">Read decode: 0 = Disable 1 = Enable</td> <td style="width: 12.5%;">Chip select active: 0 = w/Cmd 1 = Before ALE</td> <td colspan="4">GPCS0# mask bits for address A[4:1] (I/O) or A[18:15] memory: A 1 in a particular bit means that the corresponding bit at 4Ah[3:0] is not compared. This is used to determine address block size.</td> </tr> </table>								GPCS0# base address: A9 (I/O) A23 (Memory)	Write decode: 0 = Disable 1 = Enable	Read decode: 0 = Disable 1 = Enable	Chip select active: 0 = w/Cmd 1 = Before ALE	GPCS0# mask bits for address A[4:1] (I/O) or A[18:15] memory: A 1 in a particular bit means that the corresponding bit at 4Ah[3:0] is not compared. This is used to determine address block size.			
GPCS0# base address: A9 (I/O) A23 (Memory)	Write decode: 0 = Disable 1 = Enable	Read decode: 0 = Disable 1 = Enable	Chip select active: 0 = w/Cmd 1 = Before ALE	GPCS0# mask bits for address A[4:1] (I/O) or A[18:15] memory: A 1 in a particular bit means that the corresponding bit at 4Ah[3:0] is not compared. This is used to determine address block size.											
<p>SYSCFG 4Ch Chip Select 1 Base Address Register Default = 00h</p> <p style="text-align: center;">GPCS1# base address: A[8:1] (I/O) or A[22:15] (Memory)</p>															
<p>SYSCFG 4Dh Chip Select 1 Control Register Default = 00h</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 12.5%;">GPCS1# base address: A9 (I/O) A23 (Memory)</td> <td style="width: 12.5%;">Write decode: 0 = Disable 1 = Enable</td> <td style="width: 12.5%;">Read decode: 0 = Disable 1 = Enable</td> <td style="width: 12.5%;">Chip select active: 0 = w/Cmd 1 = before ALE</td> <td colspan="4">GPCS1# mask bits for address A[4:1] (I/O) or A[18:15] memory: A 1 in a particular bit means that the corresponding bit at 4Ch[3:0] is not compared. This is used to determine address block size.</td> </tr> </table>								GPCS1# base address: A9 (I/O) A23 (Memory)	Write decode: 0 = Disable 1 = Enable	Read decode: 0 = Disable 1 = Enable	Chip select active: 0 = w/Cmd 1 = before ALE	GPCS1# mask bits for address A[4:1] (I/O) or A[18:15] memory: A 1 in a particular bit means that the corresponding bit at 4Ch[3:0] is not compared. This is used to determine address block size.			
GPCS1# base address: A9 (I/O) A23 (Memory)	Write decode: 0 = Disable 1 = Enable	Read decode: 0 = Disable 1 = Enable	Chip select active: 0 = w/Cmd 1 = before ALE	GPCS1# mask bits for address A[4:1] (I/O) or A[18:15] memory: A 1 in a particular bit means that the corresponding bit at 4Ch[3:0] is not compared. This is used to determine address block size.											
<p>SYSCFG 4Eh Idle Reload Event Enable Register 1 Default = 00h</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 12.5%;">GPCS1_ACCESS: 0 = Disable 1 = Enable</td> <td style="width: 12.5%;">GPCS0_ACCESS: 0 = Disable 1 = Enable</td> <td style="width: 12.5%;">LPT_ACCESS: 0 = Disable 1 = Enable</td> <td style="width: 12.5%;">GNR3_ACCESS: 0 = Disable 1 = Enable</td> <td style="width: 12.5%;">GNR1_ACCESS: 0 = Disable 1 = Enable</td> <td style="width: 12.5%;">KBD_ACCESS: 0 = Disable 1 = Enable</td> <td style="width: 12.5%;">DSK_ACCESS: 0 = Disable 1 = Enable</td> <td style="width: 12.5%;">LCD_ACCESS: 0 = Disable 1 = Enable</td> </tr> </table>								GPCS1_ACCESS: 0 = Disable 1 = Enable	GPCS0_ACCESS: 0 = Disable 1 = Enable	LPT_ACCESS: 0 = Disable 1 = Enable	GNR3_ACCESS: 0 = Disable 1 = Enable	GNR1_ACCESS: 0 = Disable 1 = Enable	KBD_ACCESS: 0 = Disable 1 = Enable	DSK_ACCESS: 0 = Disable 1 = Enable	LCD_ACCESS: 0 = Disable 1 = Enable
GPCS1_ACCESS: 0 = Disable 1 = Enable	GPCS0_ACCESS: 0 = Disable 1 = Enable	LPT_ACCESS: 0 = Disable 1 = Enable	GNR3_ACCESS: 0 = Disable 1 = Enable	GNR1_ACCESS: 0 = Disable 1 = Enable	KBD_ACCESS: 0 = Disable 1 = Enable	DSK_ACCESS: 0 = Disable 1 = Enable	LCD_ACCESS: 0 = Disable 1 = Enable								
<p>SYSCFG 4Fh IDLE_TIMER Register Default = 00h</p> <p style="text-align: center;">Time count byte for IDLE_TIMER - monitors selected IRQs and EPMIs. Time-out generates PMI#4.</p>															
<p>SYSCFG 50h PMU Control Register 4 Default = 00h</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 12.5%;">Software start SMI: 0 = Clear SMI 1 = Start SMI</td> <td style="width: 12.5%;">Reserved</td> <td style="width: 12.5%;">IRQ8 polarity: 0 = Active low 1 = Active high</td> <td style="width: 12.5%;">14.3MHz to 82C558N: 0 = Enable 1 = Disable</td> <td style="width: 12.5%;">Write = 1 to start Doze Read: Doze status 0 = Counting 1 = Timed out</td> <td style="width: 12.5%;">Ready to Resume (RO): 0 = Not in Resume 1 = Ready to Resume</td> <td style="width: 12.5%;">PMU mode (RO): 0 = Nothing pending 1 = Suspend active (clear PMI#6)</td> <td style="width: 12.5%;">Start Suspend (WO): 1 = Enter Suspend mode</td> </tr> </table>								Software start SMI: 0 = Clear SMI 1 = Start SMI	Reserved	IRQ8 polarity: 0 = Active low 1 = Active high	14.3MHz to 82C558N: 0 = Enable 1 = Disable	Write = 1 to start Doze Read: Doze status 0 = Counting 1 = Timed out	Ready to Resume (RO): 0 = Not in Resume 1 = Ready to Resume	PMU mode (RO): 0 = Nothing pending 1 = Suspend active (clear PMI#6)	Start Suspend (WO): 1 = Enter Suspend mode
Software start SMI: 0 = Clear SMI 1 = Start SMI	Reserved	IRQ8 polarity: 0 = Active low 1 = Active high	14.3MHz to 82C558N: 0 = Enable 1 = Disable	Write = 1 to start Doze Read: Doze status 0 = Counting 1 = Timed out	Ready to Resume (RO): 0 = Not in Resume 1 = Ready to Resume	PMU mode (RO): 0 = Nothing pending 1 = Suspend active (clear PMI#6)	Start Suspend (WO): 1 = Enter Suspend mode								



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Table 5-6 82C558N Power Management Registers: SYSCFG 40h-F2h (cont.)

7	6	5	4	3	2	1	0
SYSCFG 51h Beeper Control Register Default = 00h							
Reserved						Beeper control: 00 = No Action 10 = Off 01 = 1kHz 11 = 2kHz	
SYSCFG 52h Scratchpad Register 1 Default = 00h General purpose storage byte							
SYSCFG 53h Scratchpad Register 2 Default = 00h General purpose storage byte							
SYSCFG 54h Power Control Latch Register 1 Default = 00h							
Enable [3:0] to write latch lines PPWR[3:0]: 0 = Disable 1 = Enable				Read/write data bits for PPWR[3:0]: 0 = Latch output low 1 = Latch output high			
SYSCFG 55h Power Control Latch Register 2 Default = 0Fh							
Enable [3:0] to write latch lines PPWR[7:4]: 0 = Disable 1 = Enable				Read/write data bits for PPWR[7:4] (Default = 1111): 0 = Latch output low 1 = Latch output high			
SYSCFG 56h Reserved Default = 00h							
SYSCFG 57h PMU Control Register 5 Default = 00h							
Reserved	INTRGRP generates PMI#6: 0 = Disable 1 = Enable	DSK_ACCESS includes FDD: 0 = Yes 1 = No	DSK_ACCESS includes HDD: 0 = Yes 1 = No	Reserved			
SYSCFG 58h PMU Event Register 1 Default = 00h							
LOWBAT PMI#3 SMI: 00 = Disable 11 = Enable		EPMI1# PMI#2 SMI: 00 = Disable 11 = Enable		EPMI0# PMI#1 SMI: 00 = Disable 11 = Enable		LLOWBAT PMI#0 SMI: 00 = Disable 11 = Enable	
SYSCFG 59h PMU Event Register 2 Default = 00h							
Allow software SMI: 0 = Disable 1 = Enable	Reload timers on Resume: 0 = No 1 = Yes	Resume INTRGRP PMI#6, Suspend PMI#7 SMI: 00 = Disable 11 = Enable		R_TIMER PMI#5 SMI: 00 = Disable 11 = Enable		IDLE_TIMER PMI#4 SMI: 00 = Disable 11 = Enable	
SYSCFG 5Ah PMU Event Register 3 Default = 00h							
GMR1_TIMER PMI#11 SMI: 00 = Disable 11 = Enable		KBD_TIMER PMI#10 SMI: 00 = Disable 11 = Enable		DSK_TIMER PMI#9 SMI: 00 = Disable 11 = Enable		LCD_TIMER PMI#8 SMI: 00 = Disable 11 = Enable	
SYSCFG 5Bh PMU Event Register 4 Default = 00h							
Reserved	Global SMI control: 0 = Allow 1 = Mask	Reserved		GMR1 next access PMI#15: 0 = Disable 1 = Enable	KBD next access PMI#14: 0 = Disable 1 = Enable	DSK next access PMI#13: 0 = Disable 1 = Enable	LCD next access PMI#12: 0 = Disable 1 = Enable



Table 5-6 82C558N Power Management Registers: SYSCFG 40h-F2h (cont.)

7	6	5	4	3	2	1	0
SYSCFG 5Ch							
PMI Source Register 1							Default = 00h
PMI#7, Suspend: 0 = Not Active 1 = Active	PMI#6, Resume or INTRGRP: 0 = Not Active 1 = Active	PMI#5, R_TIMER time-out: 0 = Not Active 1 = Active	PMI#4, IDLE_TIMER time-out: 0 = Not Active 1 = Active	PMI#3, LOWBAT: 0 = Not Active 1 = Active	PMI#2, EPMI1#: 0 = Not Active 1 = Active	PMI#1, EPMI0#: 0 = Not Active 1 = Active	PMI#0, LLOWBAT: 0 = Not Active 1 = Active
SYSCFG 5Dh							
PMI Source Register 2							Default = 00h
PMI#15, GNR1_ ACCESS: 0 = None 1 = Active	PMI#14, KBD_ACCESS: 0 = Not Active 1 = Active	PMI#13, DSK_ACCESS: 0 = Not Active 1 = Active	PMI#12, LCD_ACCESS: 0 = Not Active 1 = Active	PMI#11, GNR1_TIMER: 0 = Not Active 1 = Active	PMI#10, KBD_TIMER: 0 = Not Active 1 = Active	PMI#9, DSK_TIMER: 0 = Not Active 1 = Active	PMI#8, LCD_TIMER: 0 = Not Active 1 = Active
SYSCFG 5Eh							
Reserved							Default = 00h
SYSCFG 5Fh							
PMU Control Register 6							Default = 00h
LCD_ACCESS includes ISA bus video access: 0 = Yes 1 = No	LCD_ACCESS includes local (VL/PCI) bus video access: 0 = No 1 = Yes	RSMGRP IRQs can Resume system: 0 = No 1 = Yes	Transitions on RINGI can Resume system: 0 = No 1 = Yes	Number of RINGI transitions to cause Resume			
SYSCFG 60h							
R_Timer Count Register Read R_Timer original count							Default = 00h
SYSCFG 61h							
Debounce Register							Default = 00h
LOWBAT, LLOWBAT debounce rate select: 00 = No debounce 01 = 250µs 10 = 8ms 11 = 500ms	SUS/RES# debounce rate select: 00 = Active low, edge-trig'd PMI 01 = Active low, level-controlled PMI 10 = Active high, level-sampled PMI in 16ms 11 = Active high, level-sampled PMI in 32ms (See Section 4.14.5.2, "SUS/ RES# and RINGI Events")		PPWR0 auto- toggle in APM STPCLK mode: 0 = No PPWR0 auto-toggle 1 = Auto-toggle PPWR0 on entry and exit from APM STP- CLK mode	STPCLK# signal 0 = Disable 1 = Enable	APM STPCLK recovery time: 00 = 120µs 01 = 240µs 10 = 1ms 11 = 2ms		
SYSCFG 62h							
IRQ Doze Register 1							Default = 00h
IRQ13 Doze reset: 0 = Disable 1 = Enable	IRQ8 Doze reset: 0 = Disable 1 = Enable	IRQ7 Doze reset: 0 = Disable 1 = Enable	IRQ12 Doze reset: 0 = Disable 1 = Enable	IRQ5 Doze reset: 0 = Disable 1 = Enable	IRQ4 Doze reset: 0 = Disable 1 = Enable	IRQ3 Doze reset: 0 = Disable 1 = Enable	IRQ0 Doze reset: 0 = Disable 1 = Enable
SYSCFG 63h							
Idle Time-Out Select Register 1							Default = 00h
EPMI0# Level-trig'd: 0 = Disable 1 = Enable	IRQ13: 0 = Disable 1 = Enable	IRQ8: 0 = Disable 1 = Enable	IRQ7: 0 = Disable 1 = Enable	IRQ5: 0 = Disable 1 = Enable	IRQ4: 0 = Disable 1 = Enable	IRQ3: 0 = Disable 1 = Enable	IRQ0: 0 = Disable 1 = Enable



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Table 5-6 82C558N Power Management Registers: SYSCFG 40h-F2h (cont.)

7	6	5	4	3	2	1	0
SYSCFG 64h INTRGRP IRQ Select Register 1 Default = 00h							
IRQ14: 0 = Disable 1 = Enable	IRQ8: 0 = Disable 1 = Enable	IRQ7: 0 = Disable 1 = Enable	IRQ6: 0 = Disable 1 = Enable	IRQ5: 0 = Disable 1 = Enable	IRQ4: 0 = Disable 1 = Enable	IRQ3: 0 = Disable 1 = Enable	IRQ1: 0 = Disable 1 = Enable
SYSCFG 65h Doze Register Default = 00h							
All interrupts to CPU reset Doze mode: 0 = Disable 1 = Enable	Reserved	EPMI0# Doze reset: 0 = Disable 1 = Enable	Recognize SMI during STPCLK#: 0 = No 1 = Yes	IRQ1 Doze reset: 0 = Disable 1 = Enable	EPMI3# Doze reset: 0 = Disable 1 = Enable	EPMI2# Doze reset: 0 = Disable 1 = Enable	EPMI1# Doze reset: 0 = Disable 1 = Enable
SYSCFG 66h PMU Control Register 7 Default = 00h							
Self-refresh DRAM selection: 0 = Normal 1 = Self-refresh	Suspend mode ATCLK frequency: 0 = Derived from LCLK 1 = 32kHz (overridden by SYSCFG 79h[0])	Doze type: 0 = Modulate STPCLK# 1 = Keep STPCLK# asserted	Assert HOLD during suspend 0 = Yes 1 = No	Reserved			STPGNT cycle wait option: 0 = Do not wait 1 = Wait for STPGNT cycle before negating STPCLK#
SYSCFG 67h PMU Control Register 8 Default = 00h							
Reserved			Prevent STPCLK# generation by SYSCFG 50h[3] when INTR is active: 0 = Disable 1 = Enable	Normal mode STPCLK# modulation (read returns current STPCLK modulation setting only; STPCLK# modulated by BCLK defined in SYSCFG E6h[7:6]): 000 = No Modulation (STPCLK# = 1) 001 = STPCLK# $t_{HI} = 0.75 * 16$ BCLKs 010 = STPCLK# $t_{HI} = 0.5 * 16$ BCLKs 011 = STPCLK# $t_{HI} = 0.25 * 16$ BCLKs 100 = STPCLK# $t_{HI} = 0.125 * 16$ BCLKs 101 = STPCLK# $t_{HI} = 0.0625 * 16$ BCLKs 110 = STPCLK# $t_{HI} = 0.03125 * 32$ BCLKs 111 = STPCLK# $t_{HI} = 0.015625 * 64$ BCLKs			
SYSCFG 68h Clock Source Register 3 Default = 00h							
R_TIMER clock source	IDLE_TIMER clock source	Resume recovery time: 00 = 8ms 10 = 128ms 01 = 32ms 11 = 30µs Note: Ignored if BEh[0] = 1.		PPWR[1:0] auto-toggle on entry and exit from Suspend: 0 = Disable 1 = Enable			
SYSCFG 69h R_TIMER Register Default = 00h							
Time count byte for R_TIMER - starts to count after a non-zero write to this register. Unlike the other timer registers, a read from this register returns the current count. Time-out generates PMI#5.							

Table 5-6 82C558N Power Management Registers: SYSCFG 40h-F2h (cont.)

7	6	5	4	3	2	1	0
SYSCFG 6Ah RSGGRP IRQ Register 1 Default = 00h							
EPMI1# Resume: 0 = Disable 1 = Enable	EPMIO# Resume: 0 = Disable 1 = Enable	IRQ8 Resume: 0 = Disable 1 = Enable	IRQ7 Resume: 0 = Disable 1 = Enable	IRQ5 Resume: 0 = Disable 1 = Enable	IRQ4 Resume: 0 = Disable 1 = Enable	IRQ3 Resume: 0 = Disable 1 = Enable	IRQ1 Resume: 0 = Disable 1 = Enable
SYSCFG 6Bh Resume Source Register (RO) Default = 00h							
Drive REFRESH# low during Suspend: 0 = No 1 = Yes	Reserved				SUS/RES# caused Resume: 0 = No 1 = Yes	RSMGRP caused Resume: 0 = No 1 = Yes	RINGI caused Resume: 0 = No 1 = Yes
SYSCFG 6Ch Scratchpad Register 3 Default = 00h General purpose storage byte							
SYSCFG 6Dh Scratchpad Register 4 Default = 00h General purpose storage byte							
SYSCFG 6Eh Scratchpad Register 5 Default = 00h General purpose storage byte							
SYSCFG 6Fh Scratchpad Register 6 Default = 00h General purpose storage byte							
SYSCFG 70h GNR1 Base Address Register 1 Default = 00h GNR1_ACCESS base address: A[13:6] for memory watchdog or A[15:10] for I/O (right-aligned).							
SYSCFG 71h GNR1 Control Register 1 Default = FFh GNR1_ACCESS mask bits: Mask for A[13:6] for memory watchdog or mask for A[15:10] for I/O (right-aligned).							
SYSCFG 72h GNR1 Control Register 2 Default = 00h							
GNR1_ACCESS base address: A[5:2] for memory watchdog or ignored for I/O.				GNR1_ACCESS mask bits: Mask for A[5:2] for memory watchdog or mask for A[9:6] for I/O.			
SYSCFG 73h GNR2 Base Address Register 1 Default = 00h GNR2_ACCESS base address: A[13:6] for memory watchdog or A[15:10] for I/O (right-aligned).							
SYSCFG 74h GNR2 Control Register 1 Default = FFh GNR2_ACCESS mask bits: Mask for A[13:6] for memory watchdog or mask for A[15:10] for I/O (right-aligned).							
SYSCFG 75h GNR2 Control Register 2 Default = 00h							
GNR2_ACCESS base address: A[5:2] for memory watchdog or ignored for I/O.				GNR2_ACCESS mask bits: Mask for A[5:2] for memory watchdog or mask for A[9:6] for I/O.			
SYSCFG 76h Doze Reload Select Register 1 Default = 0Fh							
LCD_ACCESS: 0 = DOZE_0 1 = DOZE_1	KBD_ACCESS: 0 = DOZE_0 1 = DOZE_1	DSK_ACCESS: 0 = DOZE_0 1 = DOZE_1	HDU_ACCESS: 0 = DOZE_0 1 = DOZE_1	COM1&2_ACCESS: 0 = DOZE_0 1 = DOZE_1	LPT_ACCESS: 0 = DOZE_0 1 = DOZE_1	GNR1_ACCESS: 0 = DOZE_0 1 = DOZE_1	GNR2_ACCESS: 0 = DOZE_0 1 = DOZE_1



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Table 5-6 82C558N Power Management Registers: SYSCFG 40h-F2h (cont.)

7	6	5	4	3	2	1	0	
SYSCFG 77h Doze Reload Select Register 2 Default = 00h								
IRQ8: 0 = DOZE_0 1 = DOZE_1	IRQ7: 0 = DOZE_0 1 = DOZE_1	IRQ6: 0 = DOZE_0 1 = DOZE_1	IRQ5: 0 = DOZE_0 1 = DOZE_1	IRQ4: 0 = DOZE_0 1 = DOZE_1	IRQ3: 0 = DOZE_0 1 = DOZE_1	IRQ1: 0 = DOZE_0 1 = DOZE_1	IRQ0: 0 = DOZE_0 1 = DOZE_1	
SYSCFG 78h Doze Reload Select Register 3 Default = 00h								
PCI/VL: 0 = DOZE_0 1 = DOZE_1	IRQ15: 0 = DOZE_0 1 = DOZE_1	IRQ14: 0 = DOZE_0 1 = DOZE_1	IRQ13: 0 = DOZE_0 1 = DOZE_1	IRQ12: 0 = DOZE_0 1 = DOZE_1	IRQ11: 0 = DOZE_0 1 = DOZE_1	IRQ10: 0 = DOZE_0 1 = DOZE_1	IRQ9: 0 = DOZE_0 1 = DOZE_1	
SYSCFG 79h PMU Control Register 11 Default = 00h								
DOZE_1 time-out select: 000 = No delay (Default) 100 = 64ms 001 = 1ms 101 = 256ms 010 = 4ms 110 = 1s 011 = 16ms 111 = 4s		PMI# event triggers exit from Doze mode if the PMI event is enabled to generate SMI: ⁽¹⁾ 0 = No 1 = Yes	Reserved				ATCLK, ATCLK/2 status in Suspend: 0 = Depends on 66h[6] 1 = Driven low	
(1) For example, to let PMI#11 reset the Doze mode without generating SMI to the CPU, SYSCFG 5Ah[7:6] must be set to 11b and SYSCFG 5Bh[6] must be set.								
SYSCFG 7Ah GNR3 Base Address Register 1 Default = 00h								
GNR3_ACCESS base address: A[13:6] for memory watchdog or A[15:10] for I/O (right-aligned).								
SYSCFG 7Bh GNR3 Control Register 1 Default = FFh								
GNR3_ACCESS mask bits: Mask for A[13:6] for memory watchdog or mask for A[15:10] for I/O (right-aligned).								
SYSCFG 7Ch GNR3 Control Register 2 Default = 00h								
GNR3_ACCESS base address: A[5:2] for memory watchdog or ignored for I/O.				GNR3_ACCESS mask bits: Mask for A[5:2] for memory watchdog or mask for A[9:6] for I/O.				
SYSCFG 7Dh GNR4 Base Address Register 1 Default = 00h								
GNR4_ACCESS base address: A[13:6] for memory watchdog or A[15:10] for I/O (right-aligned).								
SYSCFG 7Eh GNR4 Control Register 1 Default = FFh								
GNR4_ACCESS mask bits: Mask for A[13:6] for memory watchdog or mask for A[15:10] for I/O (right-aligned).								
SYSCFG 7Fh GNR4 Control Register 2 Default = 00h								
GNR4_ACCESS base address: A[5:2] for memory watchdog or ignored for I/O.				GNR4_ACCESS mask bits: Mask for A[5:2] for memory watchdog or mask for A[9:6] for I/O.				
SYSCFG 80h ICW1 Shadow Register for INTC1 Default = 00h								
SYSCFG 81h ICW2 Shadow Register for INTC1 Default = 00h								
SYSCFG 82h ICW3 Shadow Register for INTC1 Default = 00h								
SYSCFG 83h ICW4 Shadow Register for INTC1 Default = 00h								
SYSCFG 84h DMA In-Progress Register (RO) Default = 00h								



Table 5-6 82C558N Power Management Registers: SYSCFG 40h-F2h (cont.)

7	6	5	4	3	2	1	0
Ch. 7 DMA in progress: 0 = No 1 = Possibly	Ch. 6 DMA in progress: 0 = No 1 = Possibly	Ch. 5 DMA in progress: 0 = No 1 = Possibly	DMAC2 byte pointer flip-flop. 0 = Cleared 1 = Set	Ch. 3 DMA in progress: 0 = No 1 = Possibly	Ch. 2 DMA in progress: 0 = No 1 = Possibly	Ch. 1 DMA in progress: 0 = No 1 = Possibly	Ch. 0 DMA in progress: 0 = No 1 = Possibly
SYSCFG 85h			OCW2 Shadow Register for INTC1				Default = 00h
SYSCFG 86h			OCW3 Shadow Register for INTC1				Default = 00h
SYSCFG 87h			Reserved				
SYSCFG 88h			ICW1 Shadow Register for INTC2				Default = 00h
SYSCFG 89h			ICW2 Shadow Register for INTC2				Default = 00h
SYSCFG 8Ah			ICW3 Shadow Register for INTC2				Default = 00h
SYSCFG 8Bh			ICW4 Shadow Register for INTC2				Default = 00h
SYSCFG 8Ch			Reserved				
SYSCFG 8Dh			OCW2 Shadow Register for INTC2				Default = 00h
SYSCFG 8Eh			OCW3 Shadow Register for INTC2				Default = 00h
SYSCFG 8Fh			Reserved				
SYSCFG 90h			Timer Channel 0 Low Byte Register Timer Channel 0 count low byte, A[7:0]				Default = 00h
SYSCFG 91h			Timer Channel 0 High Byte Register Timer Channel 0 count high byte, A[15:8]				Default = 00h
SYSCFG 92h			Timer Channel 1 Low Byte Register Timer Channel 1 count low byte, A[7:0]				Default = 00h
SYSCFG 93h			Timer Channel 1 High Byte Register Timer Channel 1 count high byte, A[15:8]				Default = 00h
SYSCFG 94h			Timer Channel 2 Low Byte Register Timer Channel 2 count low byte, A[7:0]				Default = 00h
SYSCFG 95h			Timer Channel 2 High Byte Register Timer Channel 2 count high byte, A[15:8]				Default = 00h
SYSCFG 96h			Write Counter High/Low Byte Latch				
Unused	Unused	Timer Ch. 2 read LSB toggle bit	Timer Ch. 1 read LSB toggle bit	Timer Ch. 0 read LSB toggle bit	Timer Ch. 2 write LSB toggle bit	Timer Ch. 1 write LSB toggle bit	Timer Ch. 0 write LSB toggle bit
SYSCFG 97h-9Ah			Reserved				Default = 00h

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Table 5-6 82C558N Power Management Registers: SYSCFG 40h-F2h (cont.)

7	6	5	4	3	2	1	0
SYSCFG 9Bh 3F2h + 3F7h Shadow Register							
Shadows 3F2h[7] "Mode Select" bit	Shadows 3F7h[1] "Disk Type" bit 1	Shadows 3F2h[5] "Drive 2 Motor" bit	Shadows 3F2h[4] "Drive 1 Motor" bit	Shadows 3F2h[3] "DMA Enable" bit	Shadows 3F2h[2] "Soft Reset" bit	Shadows 3F7h[0] "Disk Type" bit 0	Shadows 3F2h[0] "Drive Select" bit
SYSCFG 9Ch 372h + 377h Shadow Register Default = 00h							
Shadows 372h[7] "Mode Select" bit	Shadows 377h[1] "Disk Type" bit 1	Shadows 372h[5] "Drive 2 Motor" bit	Shadows 372h[4] "Drive 1 Motor" bit	Shadows 372h[3] "DMA Enable" bit	Shadows 372h[2] "Soft Reset" bit	Shadows 377h[0] "Disk Type" bit 0	Shadows 372h[0] "Drive Select" bit
SYSCFG 9Dh-9Eh Reserved Default = 00h							
SYSCFG 9Fh Port 064h Shadow Register Default = 00h							
Shadows I/O writes to Port 064h bits [7:0] (regardless of whether KBDCS# is inhibited). In this way, when an SMI occurs between a Port 064h write and the subsequent write to Port 060h, SMM code can access the keyboard controller as needed and then simply restore the Port 064h value just before leaving SMM.							
SYSCFG A0h Feature Control Register 1 Default = 80h							
16-bit I/O decoding: 0 = Disable 1 = Enable	Global enable for automatic internal resistors: 0 = Disable 1 = Enable	Reserved					
SYSCFG A1h Feature Control Register 2 Default = 00h							
Reserved			Heavy drive on MD bus: 0 = Disable 1 = Enable	Heavy drive on ISA bus: 0 = Disable 1 = Enable	Emerg. over-temp sense: 0 = Disable 1 = Enable	Reserved	EPMI[1:0]# status latch: 0 = Dynamic 1 = Latched
SYSCFG A2h IRQ Doze Register 2 Default = 00h							
PCI/VL bus I/O access Doze reset: 0 = Disable 1 = Enable	PCI/VL memory access Doze reset: 0 = Disable 1 = Enable	IRQ15 Doze reset: 0 = Disable 1 = Enable	IRQ14 Doze reset: 0 = Disable 1 = Enable	IRQ11 Doze reset: 0 = Disable 1 = Enable	IRQ10 Doze reset: 0 = Disable 1 = Enable	IRQ9 Doze reset: 0 = Disable 1 = Enable	IRQ6 Doze reset: 0 = Disable 1 = Enable
SYSCFG A3h Idle Time-Out Select Register 2 Default = 00h							
IRQ15: 0 = Disable 1 = Enable	IRQ14: 0 = Disable 1 = Enable	IRQ12: 0 = Disable 1 = Enable	IRQ11: 0 = Disable 1 = Enable	IRQ10: 0 = Disable 1 = Enable	IRQ9: 0 = Disable 1 = Enable	IRQ6: 0 = Disable 1 = Enable	IRQ1: 0 = Disable 1 = Enable
SYSCFG A4h INTRGRP IRQ Select Register 2 Default = 00h							
Test Bit: Write as 0	IRQ15: 0 = Disable 1 = Enable	IRQ13: 0 = Disable 1 = Enable	IRQ12: 0 = Disable 1 = Enable	IRQ11: 0 = Disable 1 = Enable	IRQ10: 0 = Disable 1 = Enable	IRQ9: 0 = Disable 1 = Enable	IRQ0: 0 = Disable 1 = Enable



Table 5-6 82C558N Power Management Registers: SYSCFG 40h-F2h (cont.)

7	6	5	4	3	2	1	0
SYSCFG A5h Thermal Management Register 1 Default = 00h							
Thermal Mgmt.:		Equilibrium Level (EQL[6:0]):					
0 = Disable 1 = Enable		This count corresponds to equilibrium operation. If the CPU Activity Counter exceeds EQL, EQL is simply subtracted from the upper activity count byte and sampling continues. If the count is below EQL, the count is cleared.					
SYSCFG A6h Thermal Management Register 2 Default = 00h							
Overtemp Limit (OTL[7:0]):							
This count corresponds to an over-temperature situation. If the CPU Activity Counter exceeds OTL, the 82C558N engages cool-down clocking.							
SYSCFG A7h Thermal Management Register 3 Default = 00h							
CPU efficiency (CPUE[1:0]):		Cool-down holdoff (CDHO[1:0]):		Reserved		Cool-down time-out (CDTO[1:0]):	
00 = Low power 01 = Moderate 10 = High 11 = Very high		00 = 32 seconds 01 = 64 seconds 10 = 128 seconds 11 = 256 seconds		(See SYSCFG AAh[7:5])		00 = 2x CDHO 01 = 3x 10 = 4x 11 = 5x	
SYSCFG A8h-A9h Default = 00h							
Reserved							
SYSCFG AAh Thermal Management Register 4 Default = 00h							
Cool-down clock rate (CDCR 2:0) (STPCLK# modulation by BCLK defined in SYSCFG E6h[7:6])			THMIN pin polarity:	EPMI trigger for thermal mgmt. (valid only if pin 156 is not programmed to be dedicated THMIN)		Reserved	
000 = No modulation (STPCLK# = 1) 001 = STPCLK# $t_{hi} = 0.75 * 16$ BCLKs 010 = STPCLK# $t_{hi} = 0.5 * 16$ BCLKs 011 = STPCLK# $t_{hi} = 0.25 * 16$ BCLKs 100 = STPCLK# $t_{hi} = 0.125 * 16$ BCLKs 101 = STPCLK# $t_{hi} = 0.0625 * 16$ BCLKs 110 = STPCLK# $t_{hi} = 0.03125 * 32$ BCLKs 111 = STPCLK# $t_{hi} = 0.015625 * 64$ BCLKs			0 = High 1 = Low (Ignored if pin 156 is not programmed to be THMIN)	00 = EPMI0# 01 = EPMI1# 10 = EPMI2# 11 = EPMI3#			
SYSCFG ABh Power Control Latch Register 3 Default = 00h							
Enable [3:0] to write latch lines PPWR[11:8]:				Read/write data bits for PPWR[11:8]			
0 = Disable		1 = Enable		0 = Latch output low		1 = Latch output high	
SYSCFG Ach IDE Interface Configuration Register Default = 00h							
LCLK frequency:		IDE command pulse duration:		IDE interface enable:	IDE port address select:	3F7h[6:0] source:	IDE clock source:
00 = Rsrvd 01 = 33 MHz 10 = 25MHz 11 = 16MHz		00 = 600ns 01 = 383ns 10 = 240ns 11 = 180ns		0 = Disable 1 = Enable	0 = 1F0-7h, 3F6-7h 1 = 170-7h, 376-7h	0 = Local IDE 1 = ISA bus	0 = OSC 1 = LCLK
SYSCFG Adh Feature Control Register 3 Default = 00h							
Reserved		CPU power state in Suspend:	Reserved	INIT operation:	Reserved		
		0 = Powered 1 = 0 volt		0 = Normal 1 = Toggle on Resume			



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Table 5-6 82C558N Power Management Registers: SYSCFG 40h-F2h (cont.)

7	6	5	4	3	2	1	0
SYSCFG AEh GNR_ACCESS Feature Register Default = 03h							
Reserved		GNR2 cycle decode type: 0 = I/O 1 = Memory	GNR1 cycle decode type: 0 = I/O 1 = Memory	GNR2 base address: A0 (I/O) A14 (Memory)	GNR1 base address: A0 (I/O) A14 (Memory)	GNR2 mask bit: A0 (I/O) A14 (Memory)	GNR1 mask bit: A0 (I/O) A14 (Memory)
SYSCFG AFh-B0h Reserved Default = 00h							
SYSCFG B1h RSMGRP IRQ Register 2 Default = 00h							
EPMI3# Resume: 0 = Disable 1 = Enable	EPMI2# Resume: 0 = Disable 1 = Enable	IRQ15 Resume: 0 = Disable 1 = Enable	IRQ14 Resume: 0 = Disable 1 = Enable	IRQ12 Resume: 0 = Disable 1 = Enable	IRQ11 Resume: 0 = Disable 1 = Enable	IRQ10 Resume: 0 = Disable 1 = Enable	IRQ9 Resume: 0 = Disable 1 = Enable
SYSCFG B2h Clock Source Register 2 Default = 00h							
Clock source for HDU_TIMER		Clock source for COM2_TIMER		Clock source for COM1_TIMER		Clock source for GNR2_TIMER	
SYSCFG B3h Chip Select Cycle Type Register Default = 00h							
GPCS3# ROM width: 0 = 8-bit 1 = 16-bit	GPCS2# ROM width: 0 = 8-bit 1 = 16-bit	GPCS1# ROM width: 0 = 8-bit 1 = 16-bit	GPCS0# ROM width: 0 = 8-bit 1 = 16-bit	GPCS3# cycle type: 0 = I/O 1 = ROMCS	GPCS2# cycle type: 0 = I/O 1 = ROMCS	GPCS1# cycle type: 0 = I/O 1 = ROMCS	GPCS0# cycle type: 0 = I/O 1 = ROMCS
SYSCFG B4h HDU_TIMER Register Default = 00h Time count byte for HDU_TIMER - monitors HDU_ACCESS. Time-out generates PMI#19.							
SYSCFG B5h COM1_TIMER Register Default = 00h Time count byte for COM1_TIMER - monitors COM1_ACCESS. Time-out generates PMI#17.							
SYSCFG B6h COM2_TIMER Register Default = 00h Time count byte for COM2_TIMER - monitors COM2_ACCESS. Time-out generates PMI#18.							
SYSCFG B7h GNR2_TIMER Register Default = 00h Time count byte for GNR2_TIMER - monitors GNR2_ACCESS. Time-out generates PMI#16.							
SYSCFG B8h GNR2 Base Address Register Default = 00h GNR2_ACCESS base address: A[8:1] (I/O) or A[22:15] (Memory)							
SYSCFG B9h GNR2 Control Register Default = 00h							
GNR2 base address: A9 (I/O) A23 (Memory)	Write decode: 0 = Disable 1 = Enable	Read decode: 0 = Disable 1 = Enable	GNR2 mask bits for address A[5:1] (I/O) or A[19:15] memory: A 1 in a particular bit means that the corresponding bit at B8h[4:0] is not compared. This is used to determine address block size.				
SYSCFG BAh Chip Select 2 Base Address Register Default = 00h GPCS2# base address: A[8:1] (I/O) or A[22:15] (Memory)							



Table 5-6 82C558N Power Management Registers: SYSCFG 40h-F2h (cont.)

7	6	5	4	3	2	1	0
SYSCFG BBh Chip Select 2 Control Register Default = 00h							
GPCS2# base address: A9 (I/O) A23 (Memory)	Write decode: 0 = Disable 1 = Enable	Read decode: 0 = Disable 1 = Enable	Chip select active: 0 = w/Cmd 1 = before ALE	GPCS2# mask bits for address A[4:1] (I/O) or A[18:15] memory: A 1 in a particular bit means that the corresponding bit at BAh[3:0] is not compared. This is used to determine address block size.			
SYSCFG BCh Chip Select 3 Base Address Register Default = 00h GPCS3# base address: A[8:1] (I/O) or A[22:15] (Memory)							
SYSCFG BDh Chip Select 3 Control Register Default = 00h							
GPCS3# base address: A9 (I/O) A23 (Memory)	Write decode: 0 = Disable 1 = Enable	Read decode: 0 = Disable 1 = Enable	Chip select active: 0 = w/Cmd 1 = before ALE	GPCS3# mask bits for address A[4:1] (I/O) or A[18:15] memory: A 1 in a particular bit means that the corresponding bit at SYSCFG BCh[3:0] is not compared. This is used to determine address block size.			
SYSCFG BEh Idle Reload Event Enable Register 2 Default = 00h							
GPCS3#_ACCESS: 0 = Disable 1 = Enable	GPCS2#_ACCESS: 0 = Disable 1 = Enable	COM2_ACCESS: 0 = Disable 1 = Enable	COM1_ACCESS: 0 = Disable 1 = Enable	GNR2_ACCESS: 0 = Disable 1 = Enable	HDU_ACCESS: 0 = Disable 1 = Enable	GNR4_ACCESS: 0 = Disable 1 = Enable	Override SYSCFG 68h[3:2]: 0 = No 1 = Recover time 1s
SYSCFG BFh Chip Select Granularity Register Default = 0Fh							
GPCS3# base address: A0 (I/O) A14 (Memory)	GPCS2# base address: A0 (I/O) A14 (Memory)	GPCS1# base address: A0 (I/O) A14 (Memory)	GPCS0# base address: A0 (I/O) A14 (Mem.)	GPCS3# mask bit: A0 (I/O) A14 (Memory)	GPCS2# mask bit: A0 (I/O) A14 (Memory)	GPCS1# mask bit: A0 (I/O) A14 (Memory)	GPCS0# mask bit: A0 (I/O) A14 (Memory)
SYSCFG C0h-D4h Reserved Default = 00h							
SYSCFG D5h (Default = 00h) Resistor Control Register							
Encoded DACK control during Suspend: 00 = Pull resistor equipped lines low, drive others low 01 = Tristate all lines 10 = Drive 100b on DACK[2:0] 11 = Rsrvd		SD control during Suspend: 0 = Ext PUs 1 = Engage int PUs always, except during Suspend.		Reserved			
SYSCFG D6h PMU Control Register 10 Default = 00h							
DSK_ACCESS: 0 = 3F5h only 1 = All FDC Ports (3F2,4,5,7h, & 372,4,5,7h)	DMA trap PMI#28 SMI: 0 = Disable 1 = Enable	DMAC1 byte pointer flip-flop (RO): 0 = Cleared 1 = Set	APM doze exit PMI#35: 0 = Disable 1 = Enable	SBHE# status trap (RO)	I/O port access trapped (RO): 0 = I/O read 1 = I/O write	Access trap bit A9 (RO)	Access trap bit A8 (RO)



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Table 5-6 82C558N Power Management Registers: SYSCFG 40h-F2h (cont.)

7	6	5	4	3	2	1	0
SYSCFG D7h Access Port Address Register 1 Default = 00h Access trap address bits A[7:0]: These bits, along with SYSCFG D6h[1:0] and SYSCFG EBh[7:0] provide the 16-bit address of the port access that caused the SMI trap. SYSCFG D6h[2] indicates whether an I/O read or an I/O write access was trapped. SYSCFG D6h[3] gives the status of the SBHE# signal for the I/O instruction that was trapped.							
SYSCFG D8h PMU Event Register 5 Default = 00h							
HDU_TIMER PMI#19 HDU_ACCESS PMI#23 SMI: 00 = Disable 11 = Enable		COM2_TIMER PMI#18 COM2_ACCESS PMI#22 SMI: 00 = Disable 11 = Enable		COM1_TIMER PMI#17 COM1_ACCESS PMI#21 SMI: 00 = Disable 11 = Enable		GNR2_TIMER PMI#16 GNR2_ACCESS PMI#20 SMI: 00 = Disable 11 = Enable	
SYSCFG D9h PMU Event Register 6 Default = 00h							
DOZE_TIMER PMI#27 SMI: 00 = Disable 01 = Enable DOZE_0 10 = Enable DOZE_1 11 = Enable both		RINGI PMI#26 SMI: 00 = Disable 11 = Enable		EPMI3# cool-down clocking PMI#25 SMI: 00 = Disable 11 = Enable		EPMI2# PMI#24 SMI: 00 = Disable 11 = Enable	
SYSCFG DAh Power Management Event Status Register (RO) Default = 00h							
Reserved		LOWBAT state: 0 = Low 1 = High	LLOWBAT state: 0 = Low 1 = High	EPMI3# state: 0 = Low 1 = High	EPMI2# state: 0 = Low 1 = High	EPMI1# state: 0 = Low 1 = High	EPMI0# state: 0 = Low 1 = High
SYSCFG DBh Next Access Event Generation Register 2 Default = 00h							
I/O blocking control: 0 = Block I/O on next access trap 1 = Unblock	SMI on cool-down clocking entry/exit: 0 = Disable 1 = Enable	External EPMI3# pin polarity: 0 = Active high 1 = Active low	External EPMI2# pin polarity: 0 = Active high 1 = Active low	HDU_ACCESS PMI#23 on next access: 0 = No 1 = Yes	COM2_ACCESS PMI#22 on next access: 0 = No 1 = Yes	COM1_ACCESS PMI#21 on next access: 0 = No 1 = Yes	GNR2_ACCESS PMI#20 on next access: 0 = No 1 = Yes
SYSCFG DCh PMU SMI Source Register 3 Default = 00h							
PMI#23, HDU_ACCESS: 0 = None 1 = Active	PMI#22, COM2_ACCESS: 0 = Clear 1 = Active	PMI#21, COM1_ACCESS: 0 = Clear 1 = Active	PMI#20, GNR2_ACCESS: 0 = Clear 1 = Active	PMI#19, HDU_TIMER: 0 = Clear 1 = Active	PMI#18, COM2_TIMER: 0 = Clear 1 = Active	PMI#17, COM1_TIMER: 0 = Clear 1 = Active	PMI#16, GNR2_TIMER: 0 = Clear 1 = Active
SYSCFG DDh PMU SMI Source Register 4 Default = 00h							
Reserved			PMI#28, DMA: 0 = Clear 1 = Active	PMI#27, DOZE_TIMER: 0 = Clear 1 = Active	PMI#26, RINGI: 0 = Clear 1 = Active	PMI#25, EPMI3# pin/cool-down clocking: 0 = Clear 1 = Active	PMI#24, EPMI2# pin: 0 = Clear 1 = Active

Table 5-6 82C558N Power Management Registers: SYSCFG 40h-F2h (cont.)

7	6	5	4	3	2	1	0
SYSCFG DEh Current Access Event Generation Register Default = 00h							
HDU_ACCESS PMI#23 on current access: 0 = No 1 = Yes	COM2_ACCESS PMI#22 on current access: 0 = No 1 = Yes	COM1_ACCESS PMI#21 on current access: 0 = No 1 = Yes	GNR2_ACCESS PMI#20 on current access: 0 = No 1 = Yes	GNR1_ACCESS PMI#15 on current access: 0 = No 1 = Yes	KBD_ACCESS PMI#14 on current access: 0 = No 1 = Yes	DSK_ACCESS PMI#13 on current access: 0 = No 1 = Yes	LCD_ACCESS PMI#12 on current access: 0 = No 1 = Yes
SYSCFG DFh Activity Tracking Register Default = 00h							
HDU_ACCESS activity: 0 = No 1 = Yes	COM2_ACCESS activity: 0 = No 1 = Yes	COM1_ACCESS activity: 0 = No 1 = Yes	GNR2_ACCESS activity: 0 = No 1 = Yes	GNR1_ACCESS activity: 0 = No 1 = Yes	KBD_ACCESS activity: 0 = No 1 = Yes	DSK_ACCESS activity: 0 = No 1 = Yes	LCD_ACCESS activity: 0 = No 1 = Yes
SYSCFG E0h Activity Tracking Register 1 Default = 00h							
Reserved						GNR4_ACCESS activity: 0 = No 1 = Yes	GNR3_ACCESS activity: 0 = No 1 = Yes
SYSCFG E1h GNR3 Base Address Register Default = 00h							
GNR3_ACCESS base address: A[8:1] (I/O) or A[22:15] (Memory)							
SYSCFG E2h GNR3 Control Register Default = 00h							
GNR3 base address: A9 (I/O) A23 (Memory)	Write decode: 0 = Disable 1 = Enable	Read decode: 0 = Disable 1 = Enable	GNR3 mask bits for address A[5:1] (I/O) or A[19:15] memory: A 1 in a particular bit means that the corresponding bit at E1h[4:0] is not compared. This is used to determine address block size.				
SYSCFG E3h GNR4 Base Address Register Default = 00h							
GNR4_ACCESS base address: A[8:1] (I/O) or A[22:15] (Memory)							
SYSCFG E4h GNR4 Control Register Default = 00h							
GNR4 base address: A9 (I/O) A23 (Memory)	Write decode: 0 = Disable 1 = Enable	Read decode: 0 = Disable 1 = Enable	GNR4 mask bits for address A[5:1] (I/O) or A[19:15] memory: A 1 in a particular bit means that the corresponding bit at E3h[4:0] is not compared. This is used to determine address block size.				
SYSCFG E5h GNR_ACCESS Feature Register 2 Default = 03h							
Reserved		GNR4 cycle decode type: 0 = I/O 1 = Memory	GNR3 cycle decode Type: 0 = I/O 1 = Memory	GNR4 base address: A0 (I/O) A14 (Memory)	GNR3 base address: A0 (I/O) A14 (Memory)	GNR4 mask bit: A0 (I/O) A14 (Memory)	GNR3 mask bit: A0 (I/O) A14 (Memory)



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Table 5-6 82C558N Power Management Registers: SYSCFG 40h-F2h (cont.)

7	6	5	4	3	2	1	0
SYSCFG E6h Clock Source Register 4 Default = 70h							
BCLK source for STPCLK# modulation (For normal mode, Doze mode, thermal mgmt): 00 = 4KHz 01 = 32KHz (Default) 10 = 450KHz 11 = 900KHz		GNR4_ACCESS: 0 = DOZE_0 1 = DOZE_1	GNR3_ACCESS: 0 = DOZE_0 1 = DOZE_1	Clock source for GNR4_TIMER		Clock source for GNR3_TIMER	
SYSCFG E7h GNR3_TIMER Register Default = 00h							
Time count byte for GNR3_TIMER - monitors GNR3_ACCESS. Time-out generates PMI#29.							
SYSCFG E8h GNR4_TIMER Register Default = 00h							
Time count byte for GNR4_TIMER - monitors GNR4_ACCESS. Time-out generates PMI#30.							
SYSCFG E9h PMU Event Register 7 Default = 00h							
GNR4_TIMER PMI#30 SMI: 00 = Disable 11 = Enable	GNR3_TIMER PMI#29 SMI: 00 = Disable 11 = Enable		GNR4_ACCESS PMI#32 on current access: 0 = No 1 = Yes	GNR4_ACCESS PMI#32 on next access: 0 = No 1 = Yes	GNR3_ACCESS PMI#31 on current access: 0 = No 1 = Yes	GNR3_ACCESS PMI#31 on next access: 0 = No 1 = Yes	
SYSCFG EAh PMU Source Register 5 Default = 00h							
Reserved	APM Doze exit PMI#35: 0 = Inactive 1 = Active	Hot docking time-out SMI PMI#34 0 = Inactive 1 = Active	H/W DOZE_TIMER reload PMI#33 0 = Inactive 1 = Active (on Doze exit)	GNR4_ACCESS PMI#32 0 = Inactive 1 = Active	GNR3_ACCESS PMI#31 0 = Inactive 1 = Active	GNR4_TIMER PMI#30 0 = Inactive 1 = Active	GNR3_TIMER PMI#29 0 = Inactive 1 = Active
SYSCFG EBh Access Port Address Register 2 Default = 00h							
Reserved		Access trap address bits A[15:10]: These bits along with D6h[1:0] and D7h[7:0] provide the 16-bit address of the port access that caused the SMI trap. D6h[2] indicates whether an I/O read or an I/O write access was trapped. D6h[3] gives the status of the SBHE# signal for the I/O instruction that was trapped.					
SYSCFG Ech Write Trap Register 1 (RO) Default = 00h							
I/O write data trap[15:8]: Along with SYSCFG EDh[7:0], this register provides the 16-bit write data for trapped I/O write instructions.							
SYSCFG EDh Write Trap Register 2 (RO) Default = 00h							
I/O write data trap[7:0]: Along with SYSCFG Ech[7:0], this register provides the 16-bit write data for trapped I/O write instructions							
SYSCFG Eeh Power Control Latch Register Default = 0Fh							
Enable [3:0] to write latch lines PPWR[15:12]: 0 = Disable 1 = Enable				Read/write data bits for PPWR[15:12] (Default = 1111): 0 = Latch output low 1 = Latch output high			



Table 5-6 82C558N Power Management Registers: SYSCFG 40h-F2h (cont.)

7	6	5	4	3	2	1	0
SYSCFG EFh Hot Docking Control Register 1 Default = 00h							
Hot docking enable: 1 = Enable (Default) 0 = Disable	HDI input debounce rate: 00 = 100µs 01 = 512µs 10 = 1ms 11 = 2ms		HDI active level: 0 = Active high 1 = Active low (Valid only if pin 155 is programmed as dedicated HDI)	HDI SMI: 0 = No SMI on time-out (Default) 1 = Generate SMI on time-out	HDI time-out period: 000 = 1ms 100 = 512ms 001 = 8ms 101 = 2s 010 = 64ms 110 = 8s 011 = 256ms 111 = 16s		
SYSCFG F0h Hot Docking Control Register 2 Default = 00h							
EPMI3# reload IDLE_TIMER: 0 = Disable 1 = Enable	EPMI2# reload IDLE_TIMER: 0 = Disable 1 = Enable	EPMI1# reload IDLE_TIMER: 0 = Disable 1 = Enable	ROM window feature: 0 = Disable 1 = Enable	ROM window size: 00 = 64KB 01 = 128KB 10 = 256KB 11 = 512KB		EPMI trigger for HDI: 00 = EPMI0# 01 = EPMI1# 10 = EPMI2# 11 = EPMI3# (Valid only if pin 155 is not programmed as dedicated HDI)	
SYSCFG F1h Low Order Start Address for ROM Window Default = 00h							
Start address bits A[23:19] for ROM window				A18 (for 64KB, 128KB, 256KB window sizes) Ignored for 512KB window size	A17 (for 64KB, 128KB window sizes) Ignored for 256KB and 512KB window sizes	A16 (for 64KB window size) Ignored for 128KB, 256KB, and 512KB window sizes	
SYSCFG F2h High Order Start Address for ROM Window Default = 00h							
Start address bits A[31:24] for ROM window							

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5.3 Miscellaneous System Control Registers

Table 5-7 is a register map that includes control registers that are present in either the 82C557 or in the 82C558N.

These registers are directly accessible in the System I/O Space.

Table 5-7 System I/O Space Register Map

Port	Name	Comment
DMAC1 Control Registers		
000h	Memory Address Register for DMA Channel 0	
001h	Count Register for DMA Channel 0	
002h	Memory Address Register for DMA Channel 1	
003h	Count Register for DMA Channel 1	
004h	Memory Address Register for DMA Channel 2	
005h	Count Register for DMA Channel 2	
006h	Memory Address Register for DMA Channel 3	
007h	Count Register for DMA Channel 3	
008h (Read)	Status Register	
008h (Write)	Command Register	
009h	Request Register	
00Ah (Read)	Command Register	
00Ah (Write)	Set Single Mask Bits	
00Bh	Mode Register	Read 00Eh, then read 00Bh four times to get the Mode Register values.
00Ch (Read)	Set Byte Pointer Flip-Flop	
00Ch (Write)	Clear Byte Pointer Flip-Flop	
00Dh (Read)	Temporary Register	
00Dh (Write)	Master Clear	
00Eh (Read)	Reset Mode Register Read-Back Counter	
00Eh (Write)	Clear Mask	
00Fh	Mask Register	
010h-01Fh	Reserved	
INTC1 Control Registers		
020h	Control Register (see text)	
021h	Control Register (see text)	
Chipset Configuration Registers		
022h	Integrated 82C206 and Chipset Configuration Index Register (SYSCFG)	
023h	Integrated 82C206 Configuration Data Register	
024h	Chipset Configuration Data Register (SYSCFG)	
025h-03Fh	Reserved	
Timer Registers		
040h	Timer Channel 0 Register	
041h	Timer Channel 1 Register	
042h	Timer Channel 2 Register	
043h	Timer Control Register	



Table 5-7 System I/O Space Register Map (cont.)

Port	Name	Comment
045h-05Fh	Reserved	
Keyboard Controller Registers		
060h	Reserved for External Keyboard Controller	Access monitored for fast A20M#/RESET
061h	System Control Port B	
062h-063h	Reserved	
064h	Reserved for External Keyboard Controller	Access monitored for fast A20M#/RESET
065h-06Fh	Reserved	
070h	RTC Index Register	Access monitored for RTC control generation and NMI enabling.
071h	RTC Data Register	Access monitored for RTC control generation.
072h-080h	Reserved	
DMA Page Registers		
081h	Page Address Register for DMA Channel 2	
082h	Page Address Register for DMA Channel 3	
083h	Page Address Register for DMA Channel 1	
084h-086h	Reserved	
087h	Page Address Register for DMA Channel 0	
088h	Reserved	
089h	Page Address Register for DMA Channel 6	
08Ah	Page Address Register for DMA Channel 7	
08Bh	Page Address Register for DMA Channel 5	
08Ch-08Eh	Reserved	
08Fh	Page Address Register for DMA Channel 4	
090h-091h	Reserved	
092h	System Control Port A	
093h-09Fh	Reserved	
INTC2 Control Registers		
0A0h	Control Register (see text)	
0A1h	Control Register (see text)	
0A2h-0BFh	Reserved	
DMAC2 Control Registers		
0C0h	Memory Address Register for DMA Channel 4	
0C1h	Reserved	
0C2h	Count Register for DMA Channel 4	
0C3h	Reserved	
0C4h	Memory Address Register for DMA Channel 5	
0C5h	Reserved	
0C6h	Count Register for DMA Channel 5	
0C7h	Reserved	
0C8h	Memory Address Register for DMA Channel 6	
0C9h	Reserved	

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Table 5-7 System I/O Space Register Map (cont.)

Port	Name	Comment
0CAh	Count Register for DMA Channel 6	
0CBh	Reserved	
0CCh	Memory Address Register for DMA Channel 7	
0CDh	Reserved	
0CEh	Count Register for DMA Channel 7	
0CFh	Reserved	
0D0h (Read)	Status Register	
0D0h (Write)	Command Register	
0D1h	Reserved	
0D2h	Request Register	
0D3h	Reserved	
0D4h (Read)	Command Register	
0D4h (Write)	Set Single Mask Bits	
0D5h	Reserved	
0D6h	Mode Register	Read 0DCh, then read 0D6h four times to get the Mode Register values.
0D7h	Reserved	
0D8h (Read)	Set Byte Pointer Flip-Flop	
0D8h (Write)	Clear Byte Pointer Flip-Flop	
0D9h	Reserved	
0DAh (Read)	Temporary Register	
0DAh (Write)	Master Clear	
0DBh	Reserved	
0DCh (Read)	Reset Mode Register Read-back Counter	
0DCh (Write)	Clear Mask	
0DDh	Reserved	
0DEh	Mask Register	
0DFh	Reserved	
0E0h-0FFh	Reserved	
100h-BFFh	Reserved	
C00h-CF7h	Reserved	
CF8h-CFBh	PCI Configuration Index Register (PCIDV0-1)	
CFCh-CFFh	PCI Configuration Data Register (PCIDV0-1)	
D00h-FFFh	Reserved	

6.0 Maximum Ratings

Stresses above those listed in the following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied.

6.1 Absolute Maximum Ratings

Symbol	Parameter	5.0 Volt		3.3 Volt		Unit
		Min	Max	Min	Max	
VCC	5.0V Supply Voltage		+6.5			V
VDD	3.3V Supply Voltage				+4.0	
VI	Input Voltage	-0.5	VCC + 0.5	-0.5	VDD + 0.5	V
VO	Output Voltage	-0.5	VCC + 0.5	-0.5	VDD + 0.5	V
TOP	Operating Temperature	0	+70	0	+70	°C
TSTG	Storage Temperature	-40	+125	-40	+125	°C

6.2 DC Characteristics: 5.0 Volt (VCC = 5.0V ±5%, TA = 0°C to +70°C)

Symbol	Parameter	Min	Max	Unit	Condition
VIL	Input low Voltage	-0.5	+0.8	V	
VIH	Input high Voltage	+2.0	VCC + 0.5	V	
VOL	Output low Voltage		+0.4	V	IOL = 4.0mA
VOH	Output high Voltage	+2.4		V	IOH = -1.6mA
IIL	Input Leakage Current		+10.0	µA	VIN = VCC
IOZ	Tristate Leakage Current		+10.0	µA	
CIN	Input Capacitance		+10.0	pF	
COUT	Output Capacitance		+10.0	pF	
ICC	Power Supply Current		240	mA	In a 60/90MHz system

6.3 DC Characteristics: 3.3 Volt (VDD = 3.3V ±5%, TA = 0°C to +70°C)

Symbol	Parameter	Min	Max	Unit	Condition
VIL	Input low Voltage	-0.5	+0.8	V	
VIH	Input high Voltage	+2.0	VDD + 0.5	V	
VOL	Output low Voltage		+0.4	V	IOL = 4.0mA
VOH	Output high Voltage	+2.4		V	IOH = -1.6mA
IIL	Input Leakage Current		+10.0	µA	VIN = VDD
IOZ	Tristate Leakage Current		+10.0	µA	
CIN	Input Capacitance		+10.0	pF	
COUT	Output Capacitance		+10.0	pF	
ICC	Power Supply Current		115	mA	In a 60/90MHz system

- Average power dissipation for a system running at 60/90MHz:
 - 82C556 = 400mW
 - 82C557 = 600mW
 - 82C558N = 600mW

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6.4 82C556 AC Characteristics (66MHz - Preliminary)

Symbol	Parameter	Min	Max	Unit	Condition
t101	HD[63:0] to MD[63:32] bus valid	2	22	ns	
t102	HD[31:0] to MD[31:0]# bus valid	2	22	ns	
t103	DLE1# high to HD[63:32] bus valid	2	22	ns	
t104	DLE0# high to HD[31:0] bus valid	2	22	ns	
t105	DLE1# high to MPERR# valid	2	22	ns	
t106	DLE0# high to MPERR# valid	2	22	ns	
t107	MD[31:0]# setup to DLE0# high	5		ns	
t108	MD[63:32] setup to DLE0# high	5		ns	
t109	MD[63:32] setup to DLE1# high	5		ns	
t110	HD[31:0] setup to DLE0# high	5		ns	
t111	HD[63:32] setup to DLE0# high	5		ns	
t112	MP[3:0]# setup to DLE0# high	5		ns	
t113	MP[7:4] setup to DLE0# high	5		ns	
t114	MP[7:4] setup to DLE1# high	5		ns	
t115	MD[31:0]# hold from DLE0# high	5		ns	
t116	MD[63:32] hold from DLE0# high	5		ns	
t117	MD[63:32] hold from DLE1# high	5		ns	
t118	HD[31:0] hold from DLE0# high	8		ns	
t119	HD[63:32] hold from DLE0# high	8		ns	
t120	MP[3:0]# hold from DLE0# high	5		ns	
t121	MP[7:4] hold from DLE0# high	5		ns	
t122	MP[7:4] hold from DLE1# high	5		ns	
t123	HDOE# high to HD[63:32] high-Z	2	11	ns	
t124	HDOE# high to HD[31:0] high-Z	2	11	ns	
t125	MDOE# high to MD[63:32] high-Z	2	15	ns	
t126	MDOE# high to MD[31:0]# high-Z	2	15	ns	

6.5 82C557 AC Characteristics (66MHz - Preliminary)

Symbol	Parameter	Min	Max	Unit	Condition
t201	ECLK to BRDY# active delay	5	15	ns	
t202	ECLK to BRDY# inactive delay	5	15	ns	
t203	ECA4, OCA4 delay from ECLK rising	5	15	ns	
t204	HACALE delay from ECLK rising	5	15	ns	
t205	ECDOE#, even bank cache, falling edge valid delay from ECLK rising	5	15	ns	
t206	OCDOE#, odd bank cache, falling edge valid delay from ECLK rising	5	15	ns	
t207	ADS# setup to CLK high	2		ns	
t208	ADS# hold time from CLK high	1		ns	
t209	M/IO#, D/C#, W/R#, CACHE# setup to CLK high	1		ns	Sampled one CLK after ADS#
t210	ECLK to DIRTYWE# active delay	5	14	ns	
t211	ECLK to DIRTYWE# inactive delay	5	14	ns	
t212	ECLK to TAGWE# active delay	5	14	ns	
t213	ECLK to TAGWE# inactive delay	5	14	ns	
t214	ECAWE#, even bank cache, falling edge valid delay from ECLK high	5	15	ns	
t215	OCAWE#, odd bank cache, falling edge valid delay from ECLK high	5	15	ns	
t216	ECLK to NA# active delay	5	15	ns	
t217	ECLK to NA# inactive delay	5	15	ns	
t218	TAG[7:0] data read to BRDY# low		5	ns	
t219	ECLK to ADSC# active delay (for sync. SRAM)	5	15	ns	
t220	ECLK to ADV# active delay (for sync. SRAM)	5	15	ns	
t221	ECLK to SYNC0#, SYNC1# active delay (for sync. SRAM)	5	15	ns	
t222	ECLK to CAWE[7:0]# active delay (for sync. SRAM)	5	15	ns	
t223	HA[31:3] valid delay from LCLK high	2	18	ns	
t224	HA[31:3] Float delay from LCLK high	2	18	ns	
t225	AHOLD valid delay from CLK high	5	15	ns	
t226	EADS# valid delay from CLK high	5	15	ns	
t227	RESET rising edge valid from CLK high	5	15	ns	
t228	RESET falling edge valid delay from CLK high	5	15	ns	
t229	KEN#/LMEM# valid delay from ECLK high	5	15	ns	
t230	RAS[3:0]# valid delay from CPUCLK high/LCLK high	2	15	ns	

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82C557 AC Characteristics (66MHz - Preliminary) (cont.)

Symbol	Parameter	Min	Max	Unit	Condition
t231	CAS[7:0]# valid delay from CPUCLK high/LCLK high	2	15	ns	
t232	MA[11:0] valid delay from CPUCLK high/LCLK high	2	15	ns	
t233	DWE# valid delay from CPUCLK high/LCLK high	2	15	ns	
t234	MA[11:0] propagation delay from HA[28:3]	2	22	ns	
t235	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, DEVSEL# valid delay from LCLK rising	2	11	ns	
t236	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, DEVSEL# active to float delay from LCLK rising	2	15	ns	
t237	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, DEVSEL# setup time to LCLK rising	7		ns	
t238	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, DEVSEL# hold time from LCLK rising	0		ns	
t239	AD[31:0] valid delay from LCLK high	2	11	ns	
t240	AD[31:0] setup time to LCLK high	7		ns	
t241	AD[31:0] hold time from LCLK high	0		ns	
t242	LRDY# setup time to LCLK high	5		ns	
t243	LRDY# hold time from LCLK high	2		ns	
t244	CLK delay from ECLK	3	6	ns	
t245	DBCOE[1:0]#, MDOE#, HDOE# valid delay from CLK/ LCLK high	2	15	ns	
t246	DLE[1:0]# valid delay from CLK\ LCLK high	2	15	ns	
t247	MDLE# valid delay from CLK\LCLK high		15	ns	
t248	PEN# valid delay from CLK\LCLK high		15	ns	
t249	NVMCS delay from CLK (2nd or 3rd T2)	2	35	ns	
t250	LA[23:9] valid delay from CLK high (2nd or 3rd T2)	2	25	ns	
t251	HREQ setup time to CLK high	2		ns	
t252	HOLD valid delay from CLK high	5	15	ns	
t253	HLDA setup time to CLK high	2		ns	
t268	HLDA hold time from CLK high	1		ns	

6.6 82C558N AC Characteristics (66MHz - Preliminary)

Symbol	Parameter	Min	Max	Unit	Condition
t301	FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, PAR, SERR#, PERR# valid delay from LCLK rising	2	11	ns	
t302	PGNT[2:0]# valid delay from LCLK rising	2	12	ns	
t303	MP7/LADS#, PIRQ[3:0]#/LRDY# valid delay from LCLK rising	2	16	ns	
t304	MD[63:32] valid delay from LCLK rising	2	20	ns	
t305	FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, PAR, SERR#, PERR# float delay from LCLK rising	2	20	ns	
t306	C/BE[3:0]#, AD[31:0], FRAME#, IRDY#, TRDY#, STOP#, DEVSEL#, PLOCK#, PAR, SERR#, PERR# setup time to LCLK rising	7		ns	
t307	C/BE[3:0]#, AD[31:0], FRAME#, IRDY#, TRDY#, STOP#, DEVSEL#, PLOCK#, PAR, SERR#, PERR# hold time from LCLK rising	0		ns	
t308	PREQ[2:0]# setup time to LCLK rising	12		ns	
t309	PREQ[2:0]# hold time from LCLK rising	0		ns	
t310	PIRQ[3:0]#/LRDY# setup time to LCLK rising	5		ns	
t311	PIRQ[3:0]#/LRDY# hold time from LCLK rising	3		ns	
t312	LMEM# setup time to LCLK rising	5		ns	
t313	INIT valid delay from LCLK rising	2	15	ns	
t314	ATCLK rising edge delay from LCLK rising edge	5	20	ns	
t315	SMI# valid delay from LCLK rising	2	15	ns	
t316	IOR#, IOW# high valid delay from ATCLK rising		15	ns	
t317	MEMR#, MEMW#, SMEMR#, SMEMW# valid delay from ATCLK rising		15	ns	
t318	BALE low valid delay from ATCLK rising		15	ns	
t319	XDIR valid delay from ATCLK rising		15	ns	
t320	STPCLK# valid delay from ATCLK rising		15	ns	
t321	RTCAS, RTCRD#, RTCWR#, ROMCS#/KBDCS# valid delay from ATCLK rising		15	ns	
t322	BALE high valid delay from ATCLK falling		15	ns	
t323	IOR#, IOW#, MEMR#, MEMW#, SMEMR#, SMEMW# low valid delay from ATCLK falling		15	ns	
t324	PPWRL# valid delay from ATCLK falling		15	ns	
t325	ZEROWS# setup time to ATCLK falling	0		ns	
t326	ZEROWS# hold time from ATCLK falling	5		ns	
t327	IOCHRDY setup time to ATCLK falling	5		ns	
t328	IOCHRDY hold time from ATCLK falling	5		ns	
t329	MD[63:32] setup time to MDLE# rising	5		ns	

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82C558N AC Characteristics (66MHz - Preliminary) (cont.)

Symbol	Parameter	Min	Max	Unit	Condition
t330	MD[63:32] hold time from MDLE# rising	5		ns	
t331	MPERR# setup time to PEN# rising	3		ns	
t332	MPERR# hold time from PEN# rising	3		ns	

6.7 AC Timing Diagrams

Figure 6-1 Setup Timing Waveform

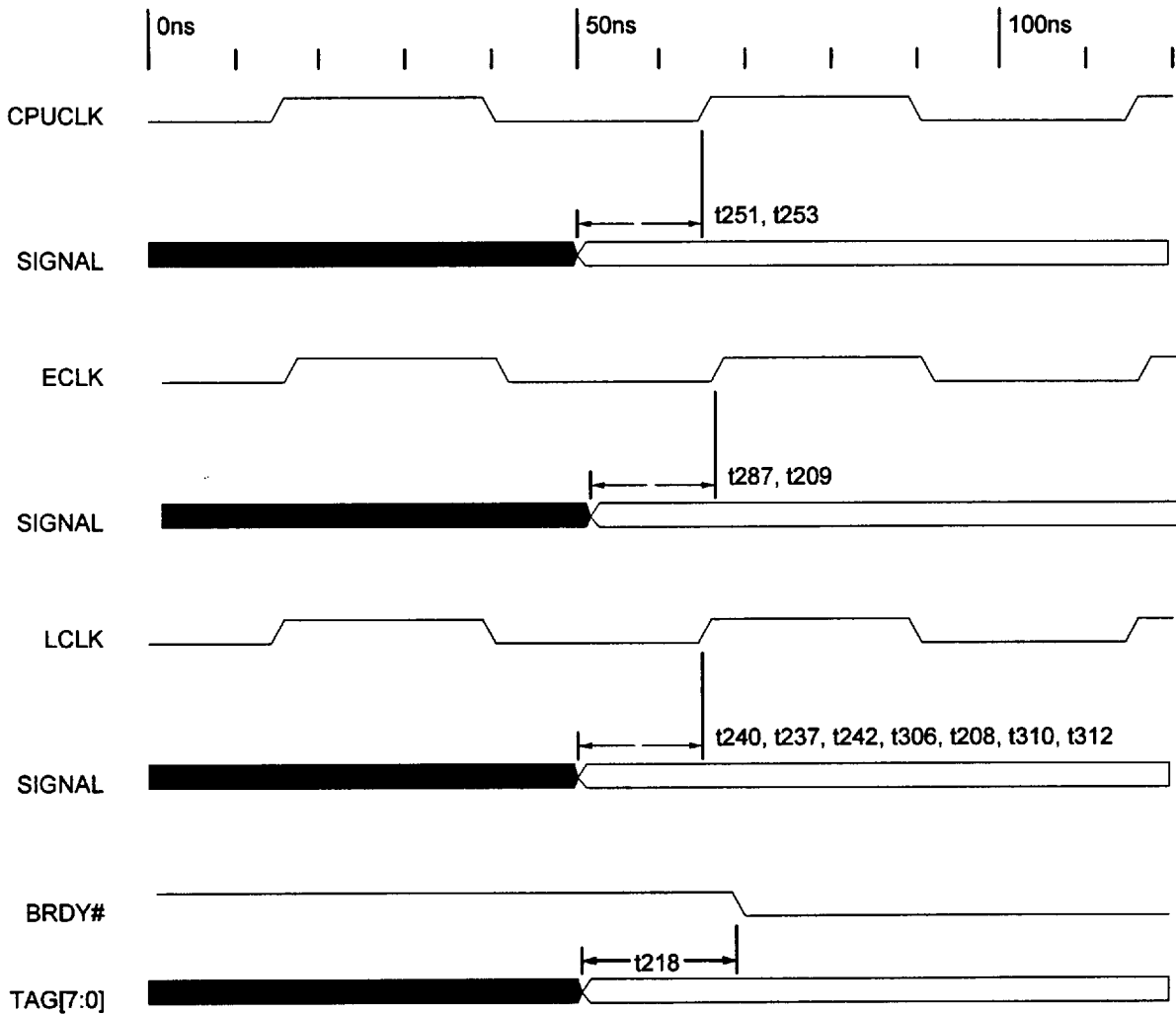


Figure 6-2 Hold Timing Waveform

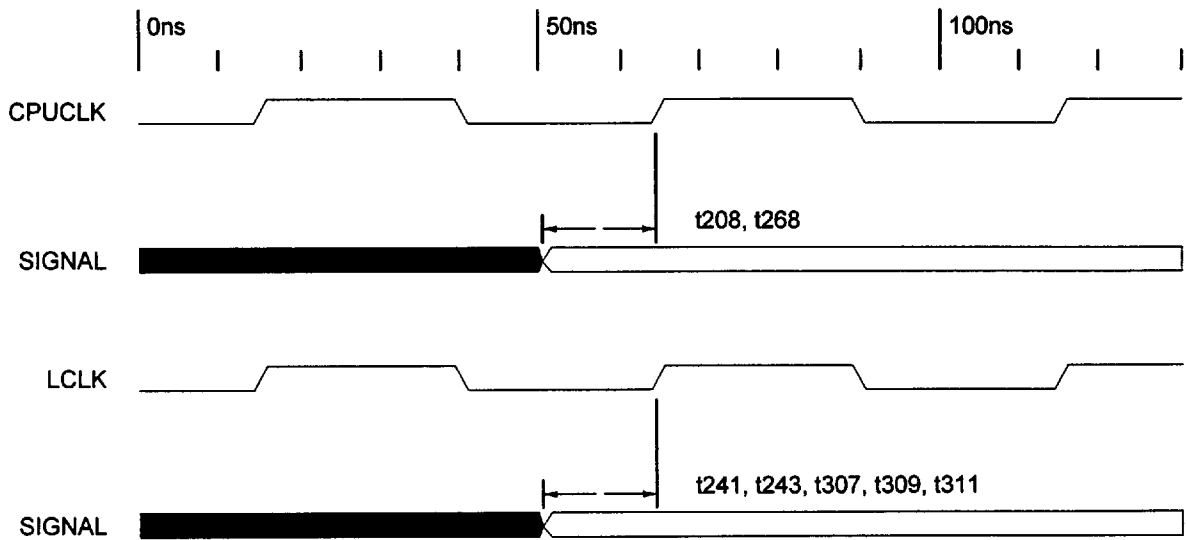
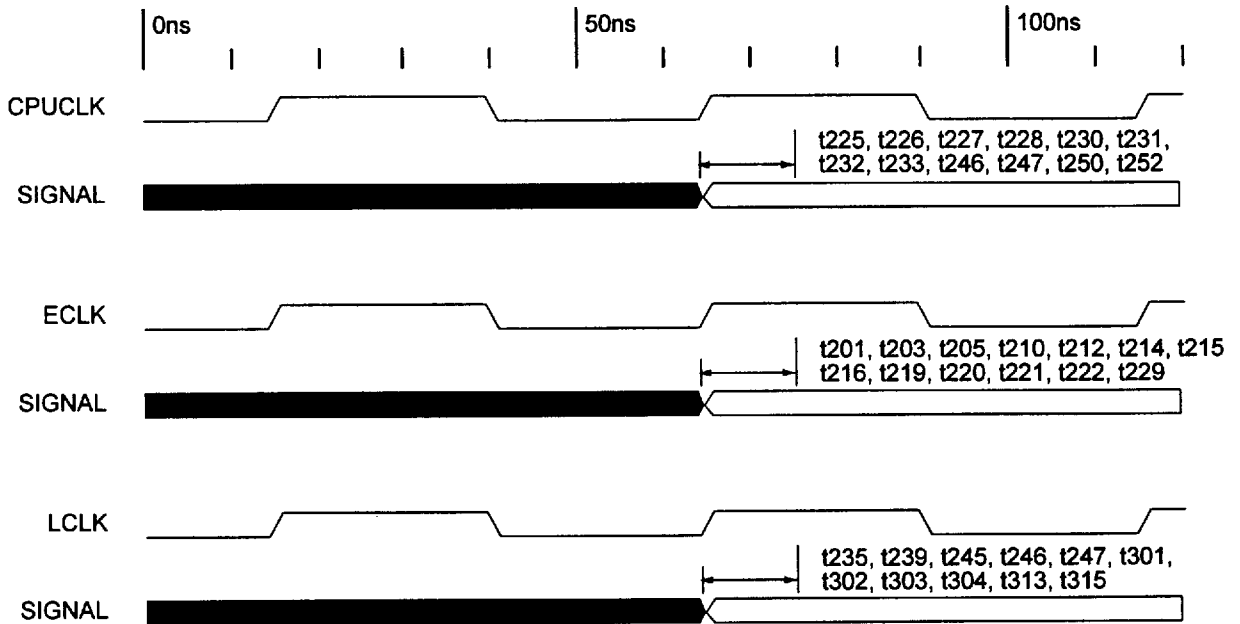
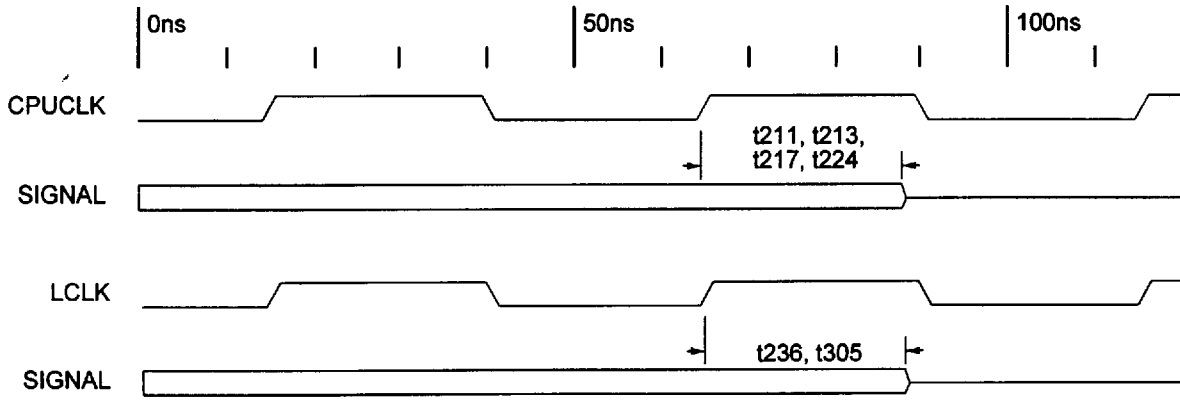


Figure 6-3 Output Delay Timing Waveform



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Figure 6-4 Float Delay Timing Waveform



7.0 Test Mode Information

Each device in the Viper-N Chipset can be forced into various test modes for board-level testing automatic test equipment (ATE).

- 82C556
 - Test Mode 0: All outputs and bidirectional pins are tristated.
 - Test Mode 1 (NAND tree test): All bidirectionals are tristated and the end of the input and bidirectional NAND chain is present on Pin 154.
- 82C557
 - Test Mode 0: All outputs and bidirectional pins are tristated.
 - Test Mode 1 (NAND tree test): All bidirectionals are tristated and the end of the input and bidirectional NAND chain is present on Pin 127.
- 82C558N
 - Test Mode 0: All outputs and bidirectional pins are tristated.
 - Test Mode 1 (NAND tree test): All bidirectionals are tristated and the end of the input and bidirectional NAND chain is present on Pin 92.
 - Test Mode 2: All even numbered output pins are driven high and all odd numbered output pins are driven low.
 - Test Mode 3: All even numbered output pins are driven low and all odd numbered output pins are driven high.

The following subsections will explain how to enable the devices in the Viper-N Chipset into the above mentioned test modes.

7.1 82C556 Testability

When the 82C556 decodes the RESET combination, it generates an internal reset signal and straps in the value of the MP[5:4] lines. The RESET combination defined below show the minimum number of required clocks. It is recommended that the user program higher values than these.

- DBCOE0#, DBCOE1#, HDOE#, MDOE#, DLE1#, and DLE0# all = 1
- 2 CPUCLKs later DBCOE1# changes to 0
- 2 CPUCLKs later HDOE# changes to 0
- 10 CPUCLKs later DLE1# changes to 0
- 20 CPUCLKs later DLE1# changes to 1
- 10 CPUCLKs later HDOE# changes to 1
- 2 CPUCLKs later DBCOE0# changes to 1

If MP4 is sampled low at the point that this RESET condition is decoded, then the 82C556 enters the test mode:

- MP4 = 0 - test mode is enabled
- MP4 = 1 - test mode is disabled

If the test mode has been enabled, then the strap information on MP5 decides which test mode has been enabled:

- MP5 = 0: Test Mode 0 is enabled (i.e., all outputs and bidirectional pins are tristated)
- MP5 = 1: Test Mode 1 (NAND tree test) is enabled (i.e., all bidirectionals are tristated and the end of the input and bidirectional NAND chain is present on Pin 154).

7.1.1 82C556 NAND Tree Test (Test Mode 1)

The NAND tree testing is enabled if the test mode has been enabled and if MP5 is held high, which enables Test Mode 1. The NAND tree mode is used to test input and bidirectional pins which will be part of the NAND tree chain. The NAND tree chain starts at Pin 155 and the output of the chain is Pin 154. Table 7-2 gives the pins of the NAND tree chain for the 176-pin TQFP and Table 7-2 for the 160-pin PQFP.

7.2 82C557 Testability

The 82C557 samples all its strap information during RESET. If the HREQ pin is sampled low during RESET, the 82C557 enters the test mode. Strap information is sampled 4096 LCLKs after the rising edge of PWRGD.

- HREQ = 0 at the rising edge of RESET - test mode is enabled
- HREQ = 1 at the rising edge of RESET - test mode is disabled

If the test mode has been enabled, then the strap information on the MASTER#, REFRESH#, and AEN lines decide which test mode has been enabled:

- MASTER# = 0, AEN = 0, and REFRESH# = 1: Test Mode 0 is enabled (i.e., all outputs and bidirectional pins are tristated)
- MASTER# = 0, AEN = 1, and REFRESH# = 1: Test Mode 1 (NAND tree test) is enabled (i.e., all bidirectionals are tristated and the end of the input and bidirectional NAND chain is present on Pin 127).

7.2.1 82C557 NAND Tree Test (Test Mode 1)

The NAND tree testing is enabled if the test mode has been enabled and if MASTER# = 0, AEN = 1, and REFRESH# = 1, to enable Test Mode 1. The NAND tree test is used to test input and bidirectional pins which will be part of the NAND tree chain. The NAND tree chain starts at Pin 126 and the output of the chain is Pin 127. Table 7-3 gives the pins of the NAND tree chain.

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Table 7-1 82C556 NAND Tree Test Mode Pins for 176-Pin TQFP

Pin No.	Remarks	Pin No.	Remarks	Pin No.	Remarks	Pin No.	Remarks
169	NAND tree input start	37	NAND tree input	80	NAND tree input	125	NAND tree input
170	NAND tree input	38	NAND tree input	81	NAND tree input	126	NAND tree input
171	NAND tree input	39	NAND tree input	82	NAND tree input	127	NAND tree input
172	NAND tree input	40	NAND tree input	83	NAND tree input	128	NAND tree input
173	NAND tree input	41	NAND tree input	84	NAND tree input	129	NAND tree input
174	NAND tree input	42	NAND tree input	85	NAND tree input	130	NAND tree input
3	NAND tree input	47	NAND tree input	86	NAND tree input	135	NAND tree input
4	NAND tree input	48	NAND tree input	91	NAND tree input	136	NAND tree input
5	NAND tree input	49	NAND tree input	92	NAND tree input	137	NAND tree input
6	NAND tree input	50	NAND tree input	93	NAND tree input	138	NAND tree input
7	NAND tree input	51	NAND tree input	94	NAND tree input	139	NAND tree input
8	NAND tree input	52	NAND tree input	95	NAND tree input	140	NAND tree input
9	NAND tree input	53	NAND tree input	96	NAND tree input	141	NAND tree input
10	NAND tree input	54	NAND tree input	97	NAND tree input	143	NAND tree input
11	NAND tree input	55	NAND tree input	98	NAND tree input	145	NAND tree input
12	NAND tree input	57	NAND tree input	99	NAND tree input	146	NAND tree input
13	NAND tree input	58	NAND tree input	102	NAND tree input	147	NAND tree input
14	NAND tree input	59	NAND tree input	103	NAND tree input	148	NAND tree input
15	NAND tree input	60	NAND tree input	104	NAND tree input	149	NAND tree input
16	NAND tree input	61	NAND tree input	105	NAND tree input	150	NAND tree input
17	NAND tree input	62	NAND tree input	106	NAND tree input	151	NAND tree input
18	NAND tree input	63	NAND tree input	107	NAND tree input	152	NAND tree input
19	NAND tree input	64	NAND tree input	108	NAND tree input	153	NAND tree input
20	NAND tree input	66	NAND tree input	109	NAND tree input	154	NAND tree input
21	NAND tree input	67	NAND tree input	111	NAND tree input	156	NAND tree input
23	NAND tree input	68	NAND tree input	114	NAND tree input	157	NAND tree input
24	NAND tree input	69	NAND tree input	115	NAND tree input	158	NAND tree input
27	NAND tree input	70	NAND tree input	116	NAND tree input	159	NAND tree input
28	NAND tree input	71	NAND tree input	117	NAND tree input	160	NAND tree input
29	NAND tree input	72	NAND tree input	118	NAND tree input	161	NAND tree input
30	NAND tree input	73	NAND tree input	119	NAND tree input	162	NAND tree input
31	NAND tree input	74	NAND tree input	120	NAND tree input	163	NAND tree input
33	NAND tree input	75	NAND tree input	121	NAND tree input	165	NAND tree input
34	NAND tree input	77	NAND tree input	122	NAND tree input	166	NAND tree input
35	NAND tree input	78	NAND tree input	123	NAND tree input	168	NAND tree output
36	NAND tree input	79	NAND tree input	124	NAND tree input		

Table 7-2 82C556 NAND Tree Test Mode Pins for 160-Pin PQFP

Pin No.	Remarks	Pin No.	Remarks	Pin No.	Remarks	Pin No.	Remarks
155	NAND tree input start	35	NAND tree input	74	NAND tree input	115	NAND tree input
156	NAND tree input	36	NAND tree input	75	NAND tree input	116	NAND tree input
157	NAND tree input	37	NAND tree input	76	NAND tree input	117	NAND tree input
158	NAND tree input	38	NAND tree input	77	NAND tree input	118	NAND tree input
159	NAND tree input	39	NAND tree input	78	NAND tree input	119	NAND tree input
160	NAND tree input	40	NAND tree input	79	NAND tree input	120	NAND tree input
1	NAND tree input	41	NAND tree input	80	NAND tree input	121	NAND tree input
2	NAND tree input	42	NAND tree input	81	NAND tree input	122	NAND tree input
3	NAND tree input	43	NAND tree input	82	NAND tree input	123	NAND tree input
4	NAND tree input	44	NAND tree input	83	NAND tree input	124	NAND tree input
5	NAND tree input	45	NAND tree input	84	NAND tree input	125	NAND tree input
6	NAND tree input	46	NAND tree input	85	NAND tree input	126	NAND tree input
7	NAND tree input	47	NAND tree input	86	NAND tree input	127	NAND tree input
8	NAND tree input	48	NAND tree input	87	NAND tree input	129	NAND tree input
9	NAND tree input	49	NAND tree input	88	NAND tree input	131	NAND tree input
10	NAND tree input	51	NAND tree input	89	NAND tree input	132	NAND tree input
11	NAND tree input	52	NAND tree input	92	NAND tree input	133	NAND tree input
12	NAND tree input	53	NAND tree input	93	NAND tree input	134	NAND tree input
13	NAND tree input	54	NAND tree input	94	NAND tree input	135	NAND tree input
14	NAND tree input	55	NAND tree input	95	NAND tree input	136	NAND tree input
15	NAND tree input	56	NAND tree input	96	NAND tree input	137	NAND tree input
16	NAND tree input	57	NAND tree input	97	NAND tree input	138	NAND tree input
17	NAND tree input	58	NAND tree input	98	NAND tree input	139	NAND tree input
18	NAND tree input	60	NAND tree input	99	NAND tree input	140	NAND tree input
19	NAND tree input	61	NAND tree input	101	NAND tree input	142	NAND tree input
21	NAND tree input	62	NAND tree input	104	NAND tree input	143	NAND tree input
22	NAND tree input	63	NAND tree input	105	NAND tree input	144	NAND tree input
25	NAND tree input	64	NAND tree input	106	NAND tree input	145	NAND tree input
26	NAND tree input	65	NAND tree input	107	NAND tree input	146	NAND tree input
27	NAND tree input	66	NAND tree input	108	NAND tree input	147	NAND tree input
28	NAND tree input	67	NAND tree input	109	NAND tree input	148	NAND tree input
29	NAND tree input	68	NAND tree input	110	NAND tree input	149	NAND tree input
31	NAND tree input	69	NAND tree input	111	NAND tree input	151	NAND tree input
32	NAND tree input	71	NAND tree input	112	NAND tree input	152	NAND tree input
33	NAND tree input	72	NAND tree input	113	NAND tree input	154	NAND tree output
34	NAND tree input	73	NAND tree input	114	NAND tree input		



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Table 7-3 82C557 NAND Tree Test Mode Pins

Pin No.	Remarks	Pin No.	Remarks	Pin No.	Remarks	Pin No.	Remarks
126	NAND tree input start	45	NAND tree input	3	NAND tree input	161	NAND tree input
125	NAND tree input	44	NAND tree input	2	NAND tree input	160	NAND tree input
124	NAND tree input	42	NAND tree input	207	NAND tree input	159	NAND tree input
123	NAND tree input	41	NAND tree input	206	NAND tree input	158	NAND tree input
122	NAND tree input	40	NAND tree input	205	NAND tree input	157	NAND tree input
121	NAND tree input	39	NAND tree input	204	NAND tree input	156	NAND tree input
120	NAND tree input	37	NAND tree input	203	NAND tree input	155	NAND tree input
118	NAND tree input	36	NAND tree input	202	NAND tree input	154	NAND tree input
117	NAND tree input	35	NAND tree input	199	NAND tree input	153	NAND tree input
116	NAND tree input	34	NAND tree input	198	NAND tree input	152	NAND tree input
115	NAND tree input	33	NAND tree input	197	NAND tree input	151	NAND tree input
113	NAND tree input	32	NAND tree input	195	NAND tree input	150	NAND tree input
112	NAND tree input	31	NAND tree input	188	NAND tree input	149	NAND tree input
111	NAND tree input	30	NAND tree input	187	NAND tree input	148	NAND tree input
110	NAND tree input	29	NAND tree input	186	NAND tree input	146	NAND tree input
109	NAND tree input	28	NAND tree input	185	NAND tree input	145	NAND tree input
108	NAND tree input	27	NAND tree input	183	NAND tree input	144	NAND tree input
107	NAND tree input	26	NAND tree input	180	NAND tree input	143	NAND tree input
106	NAND tree input	25	NAND tree input	178	NAND tree input	140	NAND tree input
105	NAND tree input	24	NAND tree input	177	NAND tree input	139	NAND tree input
57	NAND tree input	23	NAND tree input	176	NAND tree input	138	NAND tree input
56	NAND tree input	22	NAND tree input	175	NAND tree input	137	NAND tree input
55	NAND tree input	21	NAND tree input	174	NAND tree input	136	NAND tree input
54	NAND tree input	20	NAND tree input	173	NAND tree input	135	NAND tree input
53	NAND tree input	19	NAND tree input	172	NAND tree input	134	NAND tree input
52	NAND tree input	18	NAND tree input	171	NAND tree input	133	NAND tree input
51	NAND tree input	17	NAND tree input	170	NAND tree input	132	NAND tree input
50	NAND tree input	16	NAND tree input	169	NAND tree input	131	NAND tree input
49	NAND tree input	14	NAND tree input	168	NAND tree input	130	NAND tree input
48	NAND tree input	12	NAND tree input	167	NAND tree input	129	NAND tree input
47	NAND tree input	5	NAND tree input	166	NAND tree input	127	NAND tree output
46	NAND tree input	4	NAND tree input	162	NAND tree input		



7.3 82C558N Testability

The 82C558N samples all its strap information on the falling edge of RESET. If the HREQ pin is sampled low on the falling edge of RESET, the 82C558N enters the test mode.

- HREQ = 0 at the falling edge of RESET - test mode is enabled
- HREQ = 1 at the falling edge of RESET - test mode is disabled

If the test mode has been enabled, then the strap information on the IQR11 and IQR9 lines decide which test mode has been enabled:

IQR11 = 0 and IQR9 = 0: Test Mode 0 is enabled (i.e., all outputs and bidirectional pins are tristated)

IQR11 = 0 and IQR9 = 1: Test Mode 1 (NAND tree test) is enabled (i.e., all bidirectionals are tristated and the end of the input and bidirectional NAND chain is present on Pin 92).

IQR11 = 1 and IQR9 = 0: Test Mode 2 is enabled (i.e., all even numbered output pins are driven high and all odd numbered output pins are driven low).

IQR11 = 1 and IQR9 = 1: Test Mode 3 is enabled (i.e., all even numbered output pins are driven low and all odd numbered output pins are driven high).

7.3.1 82C558N NAND Tree Test (Test Mode 1)

The NAND tree testing is enabled if the test mode has been enabled and IQR11 = 0 and IQR9 = 1, to enable Test Mode 1. The NAND tree test is used to test input and bidirectional pins which will be part of the NAND tree chain. The NAND tree chain starts at Pin 2 and the output of the chain is Pin 92. Table 7-5 gives the pins of the NAND tree chain.

7.3.2 Drive High/Drive Low Test (Test Modes 2 and 3)

The 82C558N supports two type of drive high/drive low tests. If the test mode has been enabled, and if IQR11 = 1 and IQR9 = 0, then Test Mode 2 is enabled. In this mode, all even numbered output pins are driven high and all odd numbered output pins are driven low. Table 7-4 shows which pins are driven high/low during this test.

If the test mode has been enabled and if IQR11 = 1 and IQR9 = 1, then Test Mode 3 is enabled. In this mode, all odd numbered output pins are driven high and all even numbered output pins are driven low. Table 7-4 shows which pins are driven high/low during this test.

Table 7-4 Drive High/Drive Low Test Mode Pins

Even Number Pins	Odd Number Pins
2	3
8	9
52	13
74	53
80	81
84	85
92	105
106	107
108	109
110	111
112	113
148	115
150	149
154	

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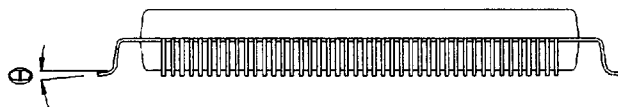
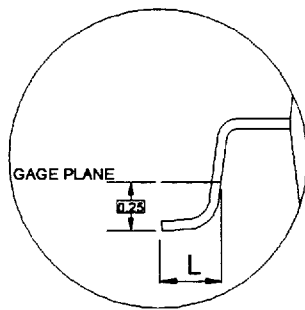
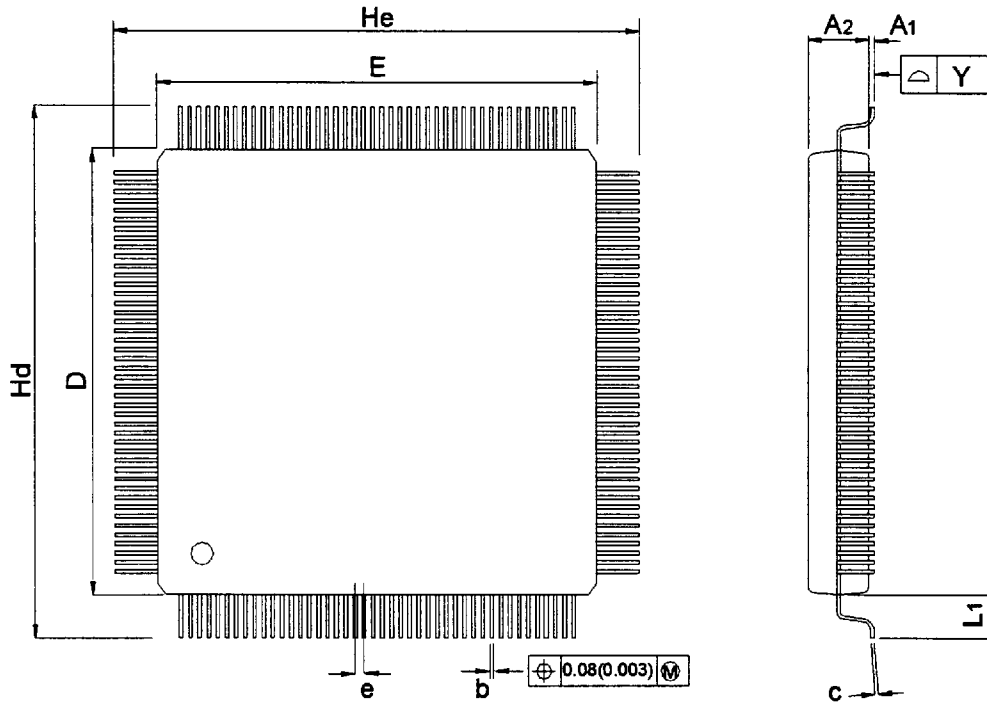
Table 7-5 82C558N NAND Tree Test Mode Pins

Pin No.	Remarks	Pin No.	Remarks	Pin No.	Remarks	Pin No.	Remarks
4	NAND tree input start	55	NAND tree input	117	NAND tree input	166	NAND tree input
5	NAND tree input	56	NAND tree input	118	NAND tree input	167	NAND tree input
6	NAND tree input	57	NAND tree input	120	NAND tree input	168	NAND tree input
7	NAND tree input	58	NAND tree input	121	NAND tree input	169	NAND tree input
11	NAND tree input	59	NAND tree input	122	NAND tree input	170	NAND tree input
12	NAND tree input	62	NAND tree input	123	NAND tree input	171	NAND tree input
16	NAND tree input	63	NAND tree input	124	NAND tree input	172	NAND tree input
17	NAND tree input	64	NAND tree input	125	NAND tree input	173	NAND tree input
18	NAND tree input	65	NAND tree input	126	NAND tree input	174	NAND tree input
19	NAND tree input	66	NAND tree input	127	NAND tree input	175	NAND tree input
20	NAND tree input	67	NAND tree input	128	NAND tree input	176	NAND tree input
21	NAND tree input	68	NAND tree input	129	NAND tree input	177	NAND tree input
22	NAND tree input	69	NAND tree input	130	NAND tree input	178	NAND tree input
23	NAND tree input	70	NAND tree input	131	NAND tree input	179	NAND tree input
24	NAND tree input	71	NAND tree input	132	NAND tree input	181	NAND tree input
25	NAND tree input	73	NAND tree input	133	NAND tree input	182	NAND tree input
27	NAND tree input	75	NAND tree input	134	NAND tree input	183	NAND tree input
28	NAND tree input	76	NAND tree input	135	NAND tree input	184	NAND tree input
29	NAND tree input	77	NAND tree input	136	NAND tree input	187	NAND tree input
30	NAND tree input	78	NAND tree input	138	NAND tree input	188	NAND tree input
31	NAND tree input	79	NAND tree input	139	NAND tree input	189	NAND tree input
32	NAND tree input	82	NAND tree input	140	NAND tree input	190	NAND tree input
33	NAND tree input	83	NAND tree input	141	NAND tree input	191	NAND tree input
34	NAND tree input	86	NAND tree input	143	NAND tree input	192	NAND tree input
35	NAND tree input	88	NAND tree input	144	NAND tree input	193	NAND tree input
36	NAND tree input	89	NAND tree input	145	NAND tree input	194	NAND tree input
39	NAND tree input	90	NAND tree input	146	NAND tree input	195	NAND tree input
40	NAND tree input	91	NAND tree input	151	NAND tree input	196	NAND tree input
41	NAND tree input	93	NAND tree input	152	NAND tree input	197	NAND tree input
42	NAND tree input	94	NAND tree input	153	NAND tree input	198	NAND tree input
44	NAND tree input	95	NAND tree input	155	NAND tree input	199	NAND tree input
45	NAND tree input	98	NAND tree input	156	NAND tree input	202	NAND tree input
46	NAND tree input	99	NAND tree input	157	NAND tree input	203	NAND tree input
47	NAND tree input	100	NAND tree input	158	NAND tree input	204	NAND tree input
48	NAND tree input	101	NAND tree input	159	NAND tree input	205	NAND tree input
49	NAND tree input	102	NAND tree input	160	NAND tree input	206	NAND tree input
50	NAND tree input	103	NAND tree input	161	NAND tree input	207	NAND tree input
51	NAND tree input	104	NAND tree input	162	NAND tree input	208	NAND tree input
54	NAND tree input	116	NAND tree input	163	NAND tree input	92	NAND tree output



8.0 Mechanical Package Outlines

Figure 8-1 176-Pin Thin Quad Flat Pack (TQFP)

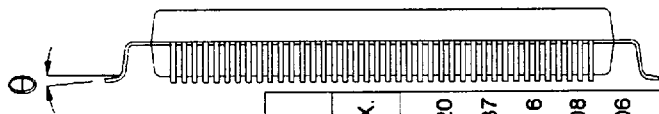
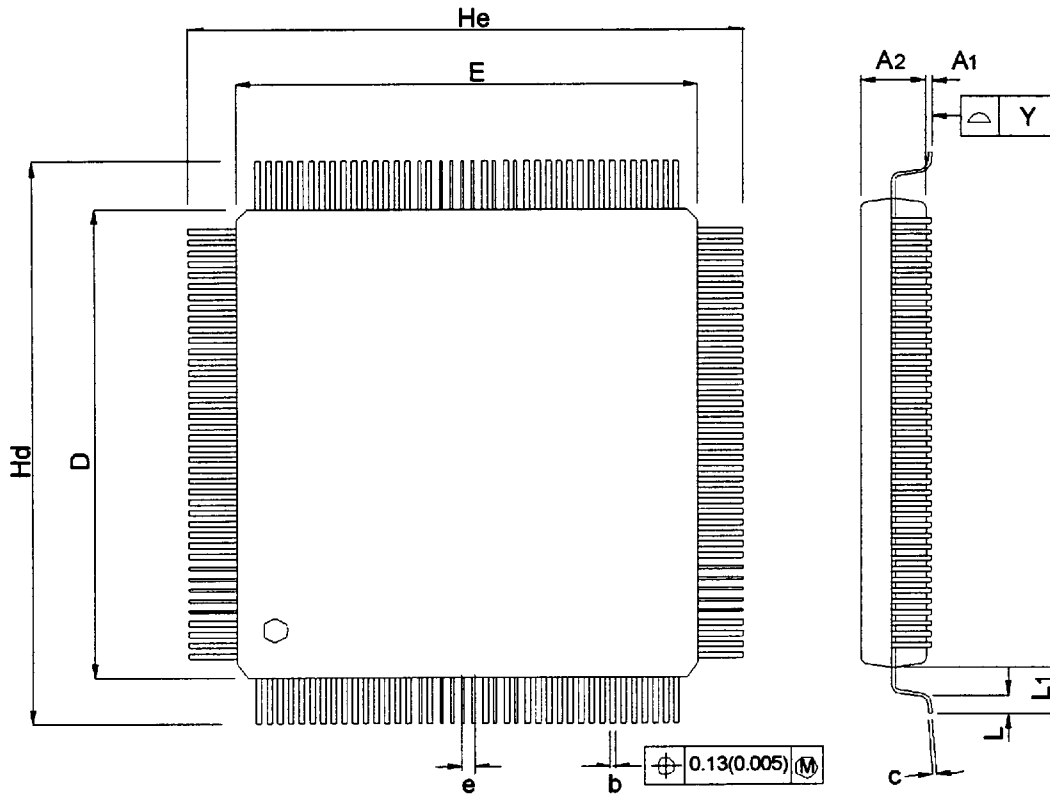


Dwg. No.:	AS176TQFP-001	
Dwg. Rev.:	A0	Unit: MM INCH

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.090		0.200	0.004		0.008
D	23.90	24.00	24.10	0.941	0.945	0.949
E	23.90	24.00	24.10	0.941	0.945	0.949
e		0.50			0.020	
Hd	25.90	26.00	26.10	1.020	1.024	1.028
He	25.90	26.00	26.10	1.020	1.024	1.028
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
Y			0.08			0.003
θ	0		7	0		7

82C556/82C557/82C558N

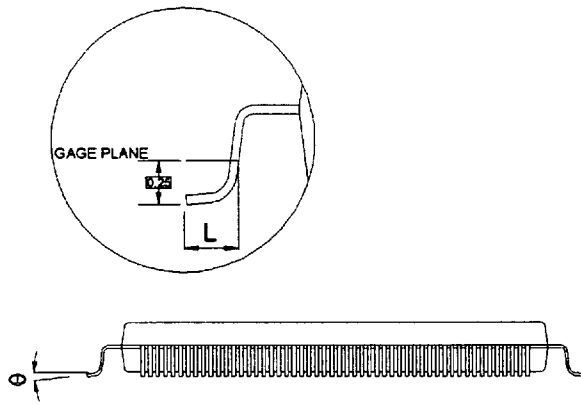
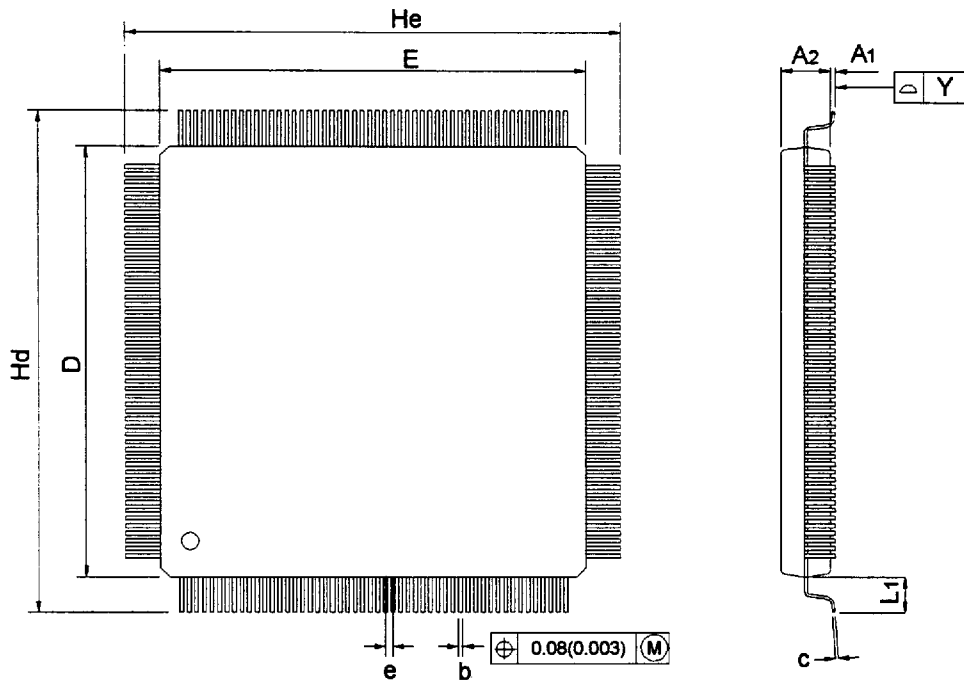
Figure 8-2 160-Pin Plastic Quad Flat Pack (PQFP)



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.05	0.25	0.50	0.002	0.010	0.020
A2	3.17	3.32	3.47	0.125	0.131	0.137
b	0.20	0.30	0.40	0.008	0.012	0.016
c	0.10	0.15	0.20	0.004	0.006	0.008
D	27.90	28.00	28.10	1.098	1.102	1.106
E	27.90	28.00	28.10	1.098	1.102	1.106
e		0.65			0.026	
H_d	31.65	31.90	32.15	1.246	1.256	1.266
H_e	31.65	31.90	32.15	1.246	1.256	1.266
L	0.65	0.80	0.95	0.025	0.031	0.037
L_1		1.95			0.077	
Y			0.08			0.003
θ	0		7	0		7

Dwg. No.:	AS160PQFP-001	
Dwg. Rev.:	A0	Unit: MM / INCH

Figure 8-3 208-Pin Thin Quad Flat Pack (TQFP)

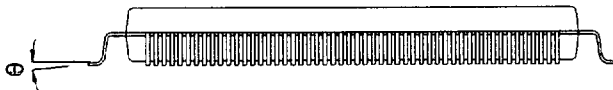
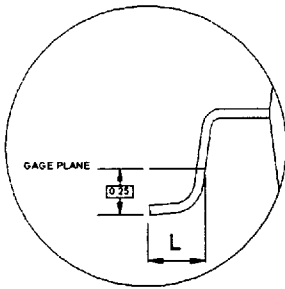
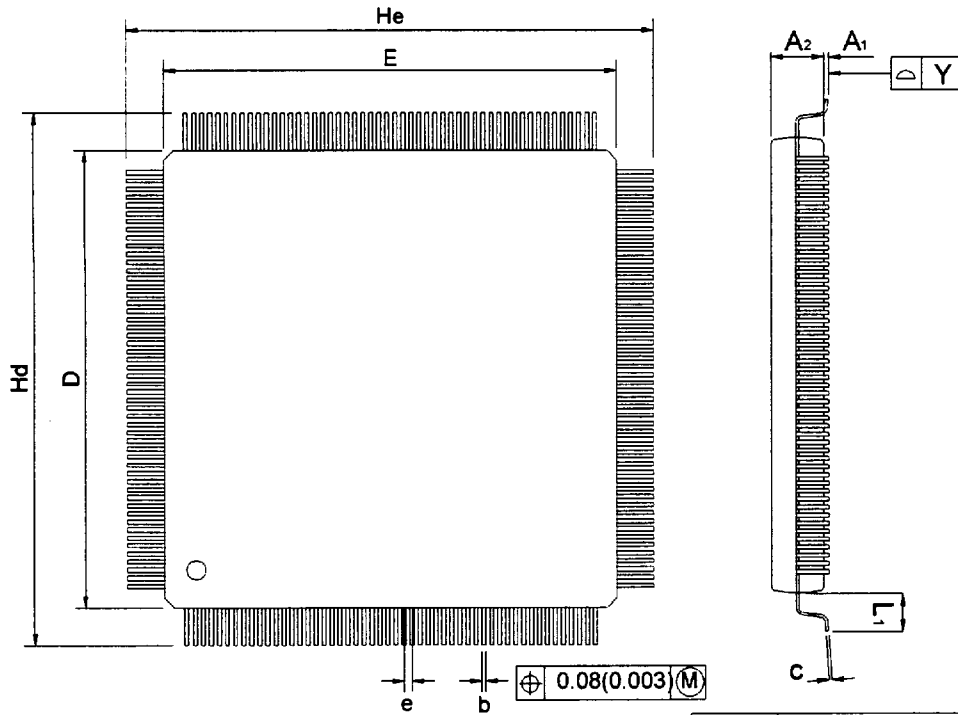


SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.090		0.200	0.004		0.008
D	27.90	28.00	28.10	1.098	1.102	1.106
E	27.90	28.00	28.10	1.098	1.102	1.106
e		0.50			0.020	
Hd	29.90	30.00	30.10	1.177	1.181	1.185
He	29.90	30.00	30.10	1.177	1.181	1.185
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
Y			0.08			0.003
⊕	0		7	0		7

Dwg. No.: AS208TQFP-001
 Dwg. Rev.: A0 Unit: MM / INCH

82C556/82C557/82C558N

Figure 8-4 208-Pin Plastic Quad Flat Package (PQFP)



$\oplus 0.08(0.003)(M)$

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A ₁	0.05	0.25	0.50	0.002	0.010	0.020
A ₂	3.17	3.32	3.47	0.125	0.131	0.137
b	0.10	0.20	0.30	0.004	0.008	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	27.90	28.00	28.10	1.098	1.102	1.106
E	27.90	28.00	28.10	1.098	1.102	1.106
e		0.50			0.020	
Hd	30.35	30.60	30.85	1.195	1.205	1.215
He	30.35	30.60	30.85	1.195	1.205	1.215
L	0.50	0.60	0.75	0.020	0.024	0.030
L ₁		1.30			0.051	
Y			0.08			0.003
θ	0		7	0		7

Dwg. No.:	AS208PQFP-001	
Dwg. Rev.:	A1	Unit: MM / INCH

A.0 Accessing the BBS

The OPTi BBS offers a wide range of useful files and utilities to our customers, from Evaluation PCB Schematics to HPGL/PostScript format Databooks that you can copy directly to your laser printer. The only requirements for accessing and using the BBS is a modem and an honest response to our questionnaire.

A.1 Paging the SYSOP

Currently, Paging the SYSOP is not a valid choice for the OPTi BBS. Once a full-time SYSOP is created, then there will be hours available for paging the SYSOP and getting immediate help.

For now, you must send [C] Comments to the SYSOP with any questions or problems you are experiencing. They will be answered promptly.

Note: Each conference has its own Co-SYSOP (the application engineer responsible for that product line), so specific conference questions can be addressed that way, but general, BBS-wide, questions should be sent to the SYSOP from the [0] - Private E-Mail conference.

A.2 System Requirements

The OPTi BBS will support any PC modem up to 14,400 baud, with 8 bits, no parity, and 1 stop bit protocol. The baud rate, handshaking, and system type will automatically be detected by the OPTi BBS.

A.3 Calling In/Hours of Operation

The OPTi BBS phone number is (408) 980-9774. The BBS is on-line 24 hours a day, seven days a week. Currently there is only one line, but as traffic requires additional lines will be installed.

A.4 Logging On for the First Time

To log on to the BBS for the first time,

1. Call (408) 980-9774 with your modem.
2. Enter your first name.
3. Enter your last name.
4. Verify that you have typed your name correctly.
5. Select a password (write it down).
6. Reenter the password to verify spelling.
7. You must then answer the questionnaire that follows.

After you have answered the questionnaire, you are given

Customer rights. To change your profile (security level, password, etc.), you must send a [C]omment to the SYSOP explaining why.

After you have logged on for the first time, each subsequent log on will bypass the questionnaire and put you directly at the bulletin request prompt. As bulletins will be added on a regular basis in the future, it is recommended that you read the new bulletins on a regular basis.

A.5 Log On Rules and Regulations

- As a FULLUSER you can download from any conference.
- You will be limited to 45 minutes per day of access time (note that once a download has started, it will finish, even if the daily time limit is exceeded). If you have not entered any keystrokes after 5 minutes, you will automatically be logged off.
- You can upload to the Customer Upload Conference¹ only. This area is used for our customers/contacts to send data to OPTi. You will not be able to download any files from this area.

A.6 Using the BBS

This section will describe how to use the BBS on a daily basis.

The BBS is divided into Conferences that are specific to a product (for example, the Viper Desktop Chipset), or an application group (for example, the Field Application Conference is used by OPTi Field Application Engineers to send data to their contacts in the field). As a general rule, the files in the application specific areas will be for specific application and may contain a password. If a file is password protected, and you know you need that file, you must contact your OPTi sales representative for the password.

The files in the Product Conferences are released data that can be used for evaluating the OPTi product line.

To access a feature of the BBS, you should type the letter in brackets that precedes each menu item. This document places the appropriate letter in brackets whenever you are told to access a feature.

A.6.1 Reading Bulletins

The OPTi BBS will present you with a set of bulletins each time you log on that are global bulletins applying to OPTi in general. In addition to these, each Product Conference will have its own set of bulletins that apply to that product. These bulletins will announce new product information, documentation updates, and bug fixes and product alerts.

1. See Section A.6.5 for more information on uploading.

Technical Support

It is recommended that you read any new bulletins on a regular basis to keep up to date on the OPTi product line.

A.6.2 Sending/Receiving Messages

The Message Menu can be used to send and receive messages from OPTi employees, or other BBS users. The Message menu can also be used to attach files for the receiver to download after they read the message. This method will be used often to send customer specific files to OPTi customers.

Messages to the SYSOP depend upon the conference you are in. Each Product Conference sends Comments and Messages to the SYSOP to the Application Engineer responsible for that conference.

A.6.3 Finding Information

To find information on the OPTi BBS, you must use the [J] Join a Conference option and then list all of the conferences available. They are arranged by product number and name.

Once you are in the correct conference, you should read all applicable bulletins and messages. Then you can [L] List all the files that are available from the File Menu.

A.6.4 Downloading Files From OPTi

The easiest way to download files from OPTi is to [L] List the files from the File Menu, the [M] Mark and files you want from the list. After you have marked all the files you need, you can [D] Download all the marked files and then logoff automatically.

A.6.5 Uploading Files To OPTi

There are two ways to upload a file to OPTi. The first is similar to the download option. You should [J] Join the Customer Upload Conference (this is the only conference that allows uploads from users) and [U] Upload the file to this conference.

If you are sending the file to a specific person, you should use the Message Menu to [E] Enter a new message to that person and then [A] Attach the file to the message. This way, the person receiving the message can download the file to his or her system without leaving behind a file that will not be used by anyone else on the BBS.

A.6.6 Logging Off

Once you have completed your visit to the OPTi BBS, you must say [G] Goodbye.

A.6.7 Logging Back on Again

To log back on to the BBS,

1. Call (408) 980-9774 with your modem.
2. Enter your first name.
3. Enter your last name.
4. Verify that you have typed your name correctly.
5. Enter your password.

You will not have to answer the questionnaire after the initial log-on. You will also be in the conference you were in when you last logged-on.

A.7 The Menus

There are four major menus that OPTi customers will use, the Main Menu, the File Menu, the Bulletin Menu and the Message Menu.

Note: The following menus are for the Customer Profile (FULLUSER) only, if your user profile has been changed, you may see slightly different menus.

Figure A-1 The Main Menu

```
MAIN MENU:
[ J ] Join a conference      [ F ] File menu
[ M ] Message menu         [ B ] Bulletin menu
[ C ] Comments to the sysop [ U ] Userlog list
[ Y ] Your settings        [ G ] Goodbye & logoff

Conf: "[0] - Private E-Mail", time on 0, with 45 remaining.
MAIN MENU: [J F M B C P U Y G] ?
```


Technical Support

- [E] Enter a new messageMenu(s): message
Send a new message to someone on the BBS.
- [F] File MenuMenu(s): main, message
Access the File Menu.
- [G] Goodbye and logoffMenu(s): main, message, file
Logoff the system.
- [J] Join a ConferenceMenu(s): main, message, file
Change conferences (product areas).
- [K] Kill a messageMenu(s): message
Delete a message.
- [L] List available filesMenu(s): file
List the files in the current conference. Note that most conferences have sub-categories of files (Schematics, JOB, etc.) that you will be asked for (or you can press enter the list all of the categories).
- [M] Message MenuMenu(s): main, file
Access the Message Menu.
- [Q] Quit to Main MenuMenu(s): message, file
Leave current menu and return to the Main Menu.
- [R] Read MessagesMenu(s): message
Read messages in the current conference or all conferences.
- [S] Scan for FilesMenu(s): file
Scan for particular files (by name, or extension, etc.).
- [S] Scan messagesMenu(s): message
Search for message by specific qualifier (date, sender etc.).
- [U] Upload a file(s)Menu(s): file
Send a file from your computer to OPTi. This can only be done in the Customer Upload Conference.
- [U] Userlog ListMenu(s): main
Lists the user database, in order of logon. This is useful if you are sending a message and are looking for the spelling of a persons name.
- [Y] Your settingsMenu(s): main
Show you settings and allow you to make changes. These include password, name, address, etc.