LOGICSTAR

DATA CONTROLLER
SL9020

PRELIMINARY

FEATURES

- Supports 80386, 80386 SX (P9), or 80286-based AT designs.
- Data In to Data Out time is 15 ns.
- 24 mA output buffers.
- Includes MD, SD & XD buffers.
- 16 bit data path can be used as Low or High buffer.
- 2 can be used in tandem to provide 32 bit data bus.
- Low to High byte Transfer.
- Fast CPU to Memory data path.
- Advance CMOS Technology.
- 100 pin Flatpack.

October 1988

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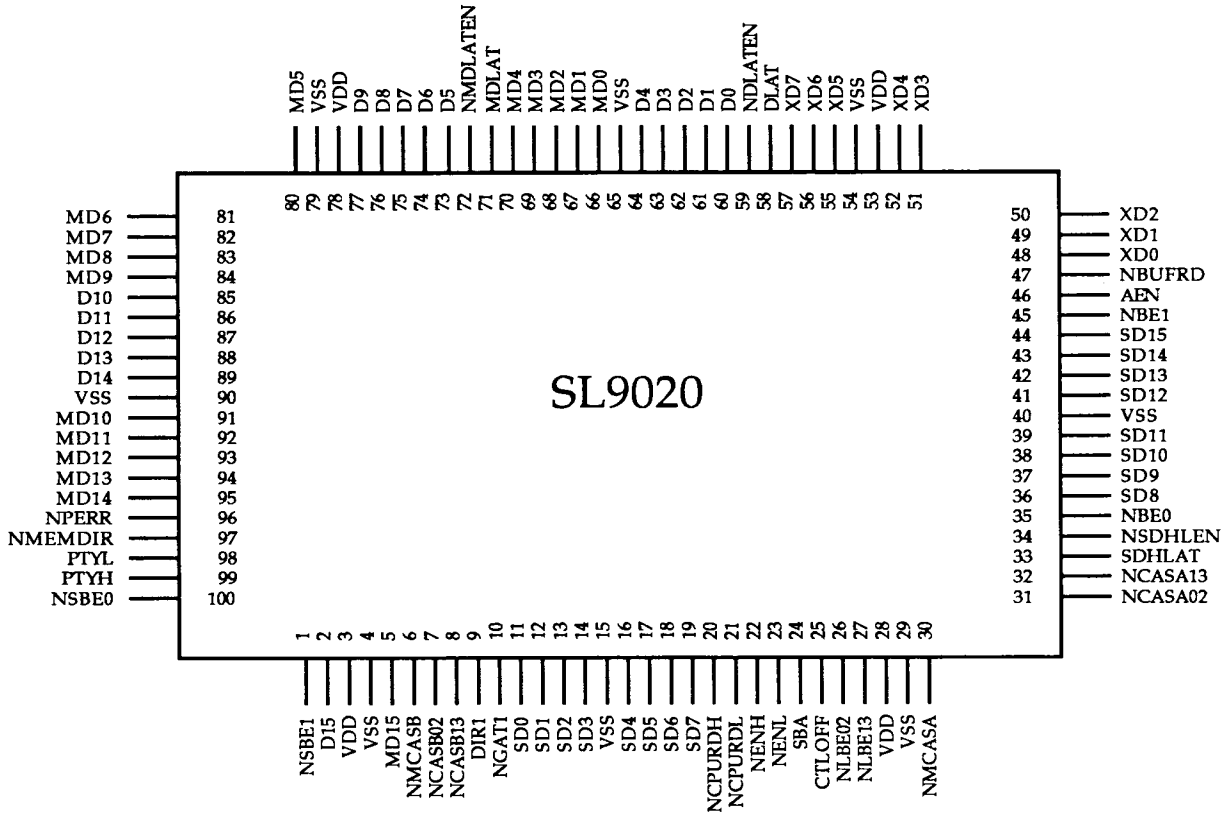
PINOUT



PIN DESCRIPTION SL9020

SYMBOL	PIN	TYPE	DESCRIPTION
AEN	46	I	When low, enables data buffers between XD Bus & SD Bus.
CTLOFF	25	I/O	Rising edge clocks data from SD [7:0] to D[7:0] latches during Bus-conversion cycles.
D0-D15	60,61,62,63,64 73,74,75,76,77 85,86,87,88,89,2	I/O	16 Bit local data Bus.
DIR1	9	I	Controls data transfer between SD[7:0] and SD[15:8].
DLAT	58	I	Latches local bus data for MD Bus when Pulled low. Should be left un-connected for non-cache-based designs.
MD0-MD15	66,67,68,69,70 80,81,82,83,84 91,92,93,94,95,5	I/O	16 Bit Memory data Bus.
MDLAT	71	I	Latches MD Bus data for local bus when pulled low. Should be left un-connected for non-cache-based designs.
NBE0,1	35,45	I	Active low Byte enable signals.
NBUFRD	47	I	Direction control for data buffer between SD Bus and XD Bus.
NCASA02,13	31,32	O	CAS0 and CAS1 for bank A.
NCASB02,13	7,8	O	CAS0 and CAS1 for bank B.
NCPURDH	20	I	High byte direction control between D Bus and SD Bus.
NCPURDL	21	I	Low Byte direction control between D Bus and XD bus.
NDLATEN	59	I	Selects Data from D Bus to MD Bus. When high, selects latched CPU data. Should be left un-connected for non-cache-based designs.
NENH	22	I	High Byte data transfer enable between D Bus and XD Bus.
NENL	23	I	Low Byte data transfer enable between D Bus and XD Bus.

PIN DESCRIPTION SL9020

SYMBOL	PIN	TYPE	DESCRIPTION
NGAT1	10	I	When low, enables byte transfer between SD Bus' low & high bytes.
NLBE02,13	26,27	O	Latched Byte enables.
NMCASA	30	I	Active low for DMA or CPU Memory Cycles for Bank A.
NMCASB	6	I	Active low for DMA or CPU Memory Cycles for Bank B.
NMDLATEN	72	I	Selects data from MD Bus to D Bus. When high, selects unlatched MD data. When low selects latched MD data. Should be left un-connected for non-cache-based designs.
NMEMDIR	97	I	Data transfer direction between D Bus and MD Bus.
NPERR	96	O	When low it indicates Parity error on the low or the high Byte. Active on read cycles only.
NSBE0,1	100,1	I	Latched Byte enables.
NSDHLEN	34	I	Selects data from SD Bus to MD Bus. When low it selects unlatched data from SD Bus to MD Bus.
PTYL,H	98,99	I/O	Parity Data Bus for low and high bytes. Parity is generated for write cycles. Parity is checked for read cycles.
SBA	24	I	When high it selects latched data afrom SD [7:0] to MD [7:0]. When low it selects unlatched data from SD Bus to MD Bus.
SD0-SD15	11,12,13,14 16,17,18,19 36,37,38,39 41,42,43,44	I/O	16 Bit I/O channel Data Bus.
SDHLAT	33	I	When low it selects latched Data from SD [15:8] to MD[15:8]. When high it selects unlatched data from SD Bus to MD Bus.
VDD	3,28,53,78	-	+5V Power.
VSS	4,15,29,40 54,65,79,90	-	0V Ground.
XD0-XD7	48,49,50,51 52,55,56,57	I/O	8 Bit peripheral Data Bus.

DC CHARACTERISTICS SL9020

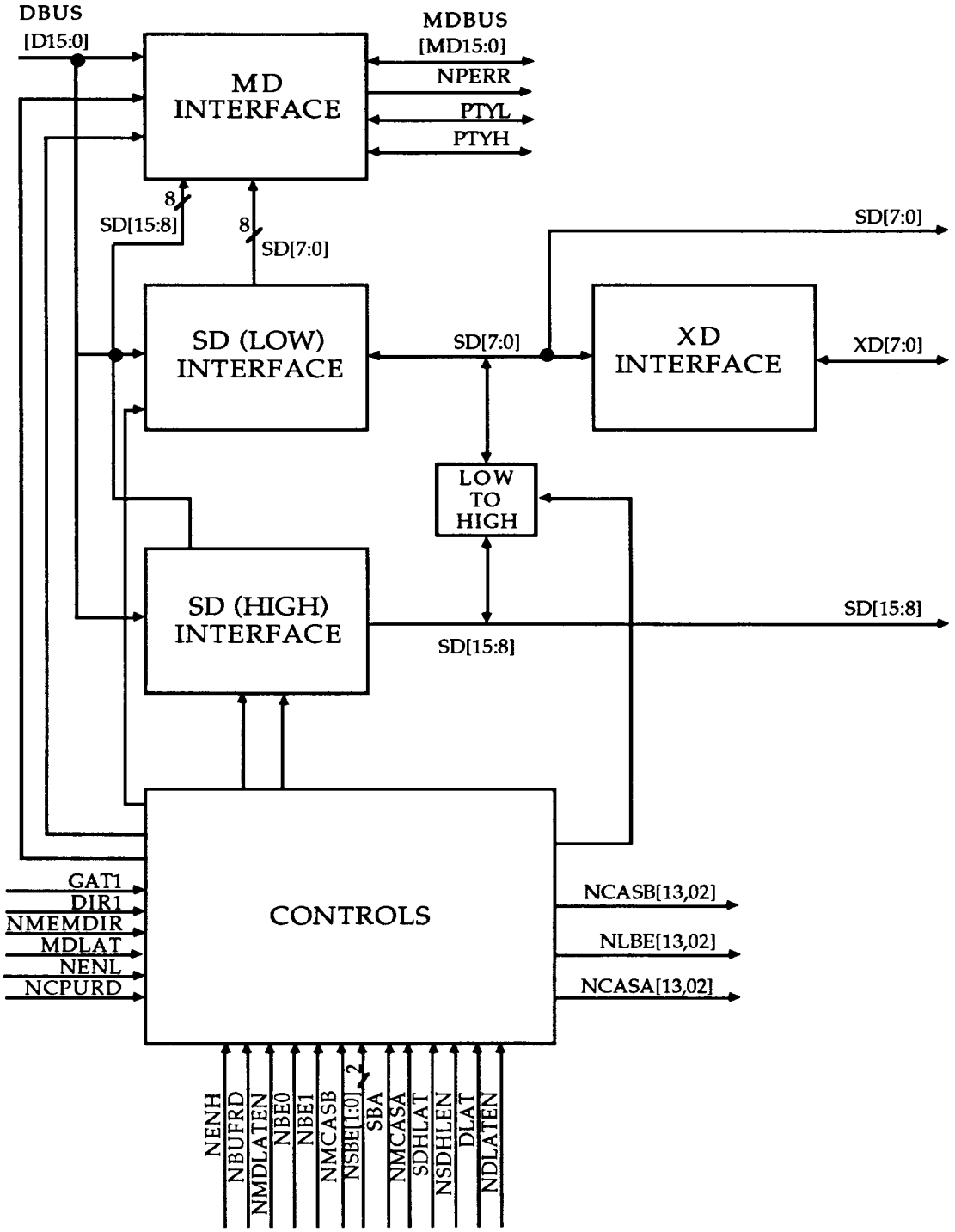
(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS	CONDITIONS
Power Supply Current	IDDS	0	100	µA	Steady state*
Output High Voltage for Normal Output (IOL = 3.2 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 8 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 12 mA)	VOH	4.0	VDD	V	IOH = - 4 mA
Output High Voltage for Driver Output (IOL = 24 mA)	VOH	4.0	VDD	V	IOH = - 8 mA
Output Low Voltage for Normal Output (IOL = 3.2 mA)	VOL	Vss	0.4	V	IOL = 3.2 mA
Output Low Voltage for Driver Output (IOL = 8 mA)	VOL	Vss	0.4	V	IOL = 8 mA
Output Low Voltage for Driver Output (IOL = 12 mA)	VOL	Vss	0.4	V	IOL = 12.0 mA
Output Low Voltage for Driver Output (IOL = 24mA)	VOL	Vss	0.5	V	IOL = 24.0 mA
Input High Voltage for TTL Input	VIH	2.2		V	
Input Low Voltage for TTL Input	VIL		0.8	V	
Input High Voltage for CMOS Input	VIH	0.7VDD		V	
Input Low Voltage for CMOS Input	VIL		0.3VDD	V	
Input Leakage Current	ILI	-10	10	µA	VI = 0 - VDD
Input Leakage Current	ILZ	-10	10	µA	Tri-state VI = 0 - VDD
Input Pull-up/Down Resistor	RP	25	100	KΩ	VIH = VDD

NOTES:

* VIH = VDD, VIL = Vss

BLOCK DIAGRAM



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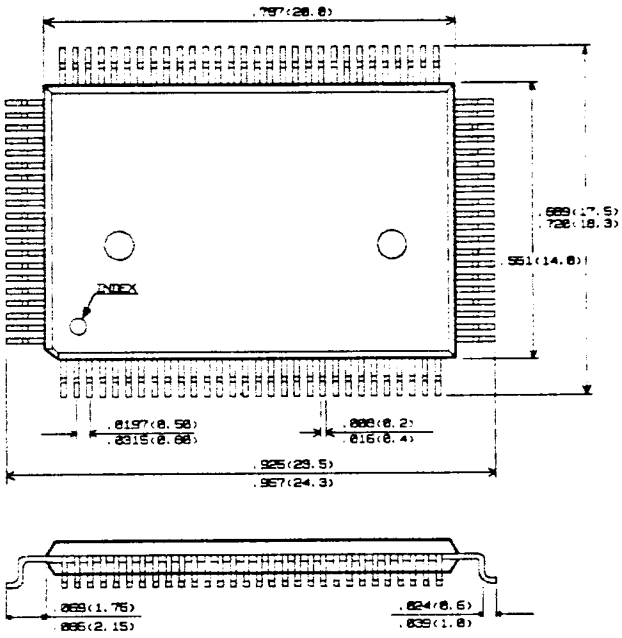
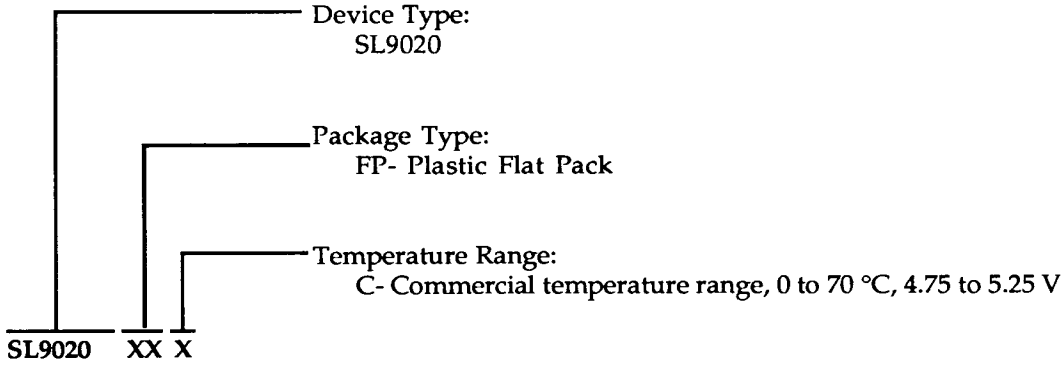
Package Information

100 Pin Flat Pack



ORDERING INFORMATION



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