Intel 450KX/GX PCIset Specification Update 82454KX/GX (PB) 82453KX/GX (MC) 82452KX/GX (DP) 82451KX/GX (MIC)

Release Date: August 1998

Order Number: 243109-015

The Intel 450KX/GX PCIset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

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The Intel 450KX/GX PCIset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

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REVISION HISTORY

Date of Revision	Version	Description
May 1996	-001	This document is the first Specification Update for the Intel 450KX/GX PCIset.
June 1996	-002	Updated 450KX PCIset Errata 6, 20, and 21, and 450GX PCIset Erratum 4. Added 450KX PCIset Errata 30 through 33 and 450GX PCIset Errata 12 through 15. Added 450KX and 450GX PCIset Specification Change 1.
July 1996	-003	Added 450KX and 450GX Specification Change 2. Added 450KX Errata 34 through 36 and 45GX Errata 16 through 19.
August 1996	-004	Updated 450KX and 450GX Specification Change 2, 450KX Erratum 35, 450GX Errata 13, 17, and 19, and 450KX and 450GX Documentation Change 1. Added 450KX and 450GX Specification Change 3, 450KX Errata 37 and 38, and 450GX Errata 20 through 22. Updated plans for 450KX Errata 4, 20, 21, 23 through 25, 27, and 30 through 34.
September 1996	-005	Updated 450KX and 450GX Documentation Change 1.
October 1996	-006	Added Documentation Change 2.
November 1996	-007	Updated 450KX and 450GX Specification Change 2, and 450GX Erratum 20.
December 1996	-008	Added 450GX Specification Changes 4 through 7 and 450GX Errata 23 and 24.
January 1997	-009	Added 450KX Erratum 39 and Specification Clarification 2. Added 450GX Erratum 25 and Specification Clarification 2.
March 1997	-010	Added 450GX Erratum 26. Updated 450GX PCIset Identification Information table.
May 1997	-011	Updated 450GX Erratum 26. Added engineering sample marking and identification information.
October 1997	-012	Added 450KX Documentation Change 3, and 450GX Erratum 27 and Documentation Change 3.
March 1998	-013	Updated 450GX Specification Change 4. Added 450GX Erratum 28.
April 1998	-014	Updated 450GX Basic Information Table.
August 1998	-015	Added 450GX Erratum 29.

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PREFACE

This document is an update to the specifications contained in the *Intel 450KX/GX PCIset* datasheet (Order Number 290523). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It contains Specification Changes, S-Specs, Errata, Specification Clarifications, and Documentation Changes.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

S-Specs are exceptions to the published specifications, and apply only to the units assembled under that s-spec.

Errata are design defects or errors. Errata may cause the Intel 450KX/GX PCIset's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Identification Information

The 82453 Memory Controller can be identified by the following values:

Vendor ID[1]	Device ID[1]
8086h	84C5h

The 82454 PCI Bridge can be identified by the following values:

Vendor ID[1]	Device ID[2]
8086h	84C4h

NOTES:

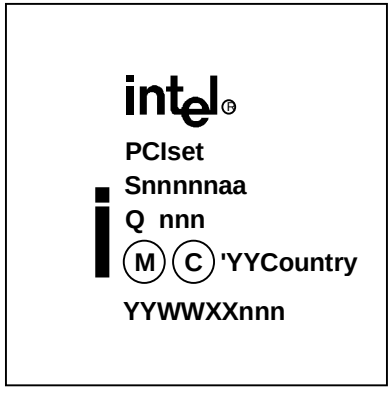
1. The Vendor ID corresponds to the value in the Vendor ID register of the device's PCI configuration space, at address offset 00-01h (the A2 stepping of the 82453KX MC located the Vendor ID register at address offset 04-05h).
2. The Device ID corresponds to the value in the Device ID register of the device's PCI configuration space, at address offset 02-03h (the A2 stepping of the 82453KX MC located the Device ID register at address offset 06-07h).

Part I: Specification Update for the Intel 450KX PCIset

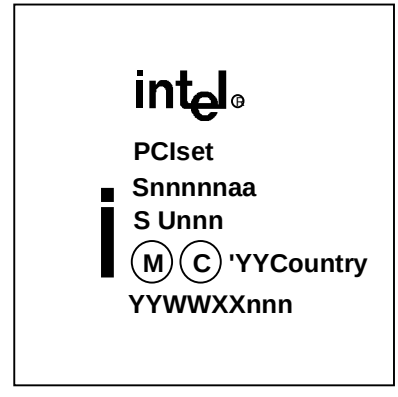
GENERAL INFORMATION

Top Markings

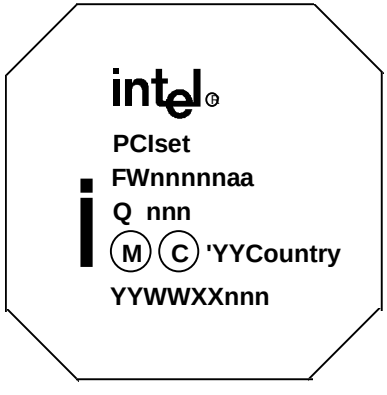
A- and B-Step Sample Units, QFP:



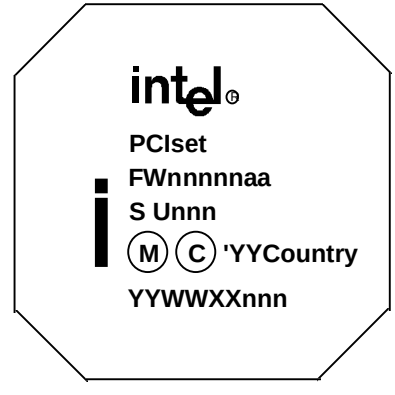
A- and B-step Production Units, QFP:



A- and B-step Sample Units, BGA:



A- and B-step Production Units, BGA:



NOTES:

- nnnnnaa = Product Number
- Q nnn = Sample Specification Number
- S Unnn = S-spec Number
- 'YY Country = Copyright Dates and Country of Origin
- YYWWXXnnn = Alternative Identification Number

Basic Intel 450KX PCIset Identification Information

Product Number	Vendor ID	Device ID	Revision ID	Product Stepping	Kit Steppings	S-Spec	V_{CC}	T_{CASE}	Notes
S82451KX	n/a[1]	n/a[1]	n/a[1]	A1	A2, B0	S U025	3.3 V ± 5%	0 °C - 85 °C	
S82451KX	n/a[1]	n/a[1]	n/a[1]	A1	A2, B0	S U039	3.3 V ± 5%	0 °C - 85 °C	
S82452KX	n/a[1]	n/a[1]	n/a[1]	A1	A2	S U026	3.3 V ± 5%	0 °C - 85 °C	
FW82452KX	n/a[1]	n/a[1]	n/a[1]	A1	A2	S U029	3.3 V ± 5%	0 °C - 85 °C	2
S82452KX	n/a[1]	n/a[1]	n/a[1]	A1	A2	S U040	3.3 V ± 5%	0 °C - 85 °C	
FW82452KX	n/a[1]	n/a[1]	n/a[1]	A1	A2	S U043	3.3 V ± 5%	0 °C - 85 °C	2
S82452KX	n/a[1]	n/a[1]	n/a[1]	A3	B0	S U061	3.3 V ± 5%	0 °C - 85 °C	
S82453KX	8086h[3]	84C5h[3]	2	A2	A2	S U027	3.3 V ± 5%	0 °C - 85 °C	
S82453KX	8086h[3]	84C5h[3]	2	A2	A2	S U041	3.3 V ± 5%	0 °C - 85 °C	
S82453KX	8086h	84C5h	4	A4	B0	S U062	3.3 V ± 5%	0 °C - 85 °C	
S82454KX	8086h	84C4h	2	A2	A2	S U022	3.3 V ± 5%	0 °C - 85 °C	
FW82454KX	8086h	84C4h	2	A2	A2	S U024	3.3 V ± 5%	0 °C - 85 °C	2
S82454KX	8086h	84C4h	2	A2	A2	S U028	3.3 V ± 5%	0 °C - 85 °C	
FW82454KX	8086h	84C4h	2	A2	A2	S U030	3.3 V ± 5%	0 °C - 85 °C	2
S82454KX	8086h	84C4h	2	A2	A2	S U042	3.3 V ± 5%	0 °C - 85 °C	
FW82454KX	8086h	84C4h	2	A2	A2	S U044	3.3 V ± 5%	0 °C - 85 °C	2
S82454KX	8086h	84C4h	4	A4	B0	S U064	3.3 V ± 5%	0 °C - 85 °C	

NOTES:

1. These components are not visible from the PCI bus, and so do not have Vendor, Device, or Revision ID registers at the PCI specification-defined locations.
2. These components have BGA (Ball Grid Array) packaging.
3. The A2 82453KX MC's Vendor and Device ID registers are not at the PCI specification-defined locations; the Vendor ID register is located at register offset 04-05h, and the Device ID is located at 06-07h.
4. These are engineering samples only, provided under an Intel 450KX PCIset loan agreement.

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the Intel 450KX PCIset. Intel intends to fix some of the errata in future steppings of the component(s), and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

X:	Specification Change, Erratum, Specification Clarification, or Documentation Change applies to the given stepping.
Doc:	Intel intends to update the appropriate documentation in a future revision.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
(No mark) or (blank box):	This item is fixed in or does not apply to the given kit stepping.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	A2	B0	Plans	SPECIFICATION CHANGES
1	X	X	Doc	PLLRST pin added
2	X	X	Doc	Valid memory timing parameters
3	X	X	Doc	CMOS overshoot/undershoot specification
NO.	**A2**	**B0**	**Plans**	**ERRATA**
1	X		Fixed	Stop Clock Acknowledge cycles may confuse buffers
2	X		Fixed	0-byte length write may cause subsequent write failure
3	X		Fixed	Inbound read may be accepted despite posted outbound write
4	X	X	NoFix	SMRAM addresses may not be decoded correctly
5	X		Fixed	Mixed read lines and partials may corrupt data
6	X		Fixed	Inbound write posting may cause write failure
7	X		Fixed	RMW with line write may cause data corruption
8	X		Fixed	Inbound write may collide with some special cycles
9	X		Fixed	Extended read-around-write may corrupt write data
10	X		Fixed	Outbound posted write after inbound read prefetch may hang
11	X		Fixed	Inbound posted write with 1:1 interleaving may corrupt data
12	X		Fixed	RAW may cause data corruption
13	X		Fixed	Data transfer order 3 may cause data to be issued out of order
14	X		Fixed	PCI address parity error may cause dropped transaction
15	X		Fixed	System hang with inbound write posting enabled
16	X		Fixed	RAW may cause data corruption during refresh

NO.	A2	B0	Plans	ERRATA
17	X		Fixed	GAT devices may time out during inbound read prefetch
18	X		Fixed	Data may be corrupted if RCD = 4 and LWC = 3
19	X		Fixed	T_{CO_MAX} specification not met for GTL+ signals
20	X	X	NoFix	RAW may hang 1:1 or 2:1 interleaved MP systems
21	X	X	NoFix	Mixed interleave increments may cause data corruption
22	X	X	NoFix	Parity error may occur for ADS# during BINIT#
23	X	X	NoFix	Hang with PCI-to-PCI bridges in MP systems
24	X	X	NoFix	PCI_RST# not asserted asynchronously
25	X	X	NoFix	BERR# to BINIT# conversion may prevent recovery from BINIT#
26	X		Fixed	Error reporting registers may not record error information correctly
27	X	X	NoFix	Combination of ECC errors may cause one error to be undetected
28	X		Fixed	16-Byte write may hang system
29	X	X	NoFix	16-Byte read with two ECC errors may not be reported correctly
30	X	X	NoFix	Inbound locked PCI transactions may hang system
31	X	X	NoFix	Retry on inbound read may corrupt outbound data
32	X	X	NoFix	ADS# in last clock of BINIT# prevents recovery
33	X	X	NoFix	Some signals indeterminate after RESET# deassertion
34	X	X	NoFix	Delayed read from PCI-to-PCI bridge may corrupt data
35	X	X	NoFix	Page Open Policy of “hold page open” may corrupt write data
36	X	X	NoFix	T_{CASE} drop plus voltage swing may cause DPLL failure
37	X	X	NoFix	Memory gap reclaiming may corrupt data
38	X	X	NoFix	RAW may corrupt write data in 1:1 interleaving
39	X	X	NoFix	BINIT# assertion may cause active RAS# negation
NO.	**A2**	**B0**	**Plans**	**SPECIFICATION CLARIFICATIONS**
1	X	X	Doc	Explicit writebacks claimed by 82454KX PB
NO.	**A2**	**B0**	**Plans**	**DOCUMENTATION CHANGES**
1	X	X	Doc	Register offset and default value correction
2	X	X	Doc	CMOS definition should be 3.3 V or 5 V
3	X	X	Doc	Pull-up resistor required on PCLK

SPECIFICATION CHANGES

1. PLLRST Pin Added

A PLLRST pin will be added to the definition of each device in the Intel 450KX PCIset. The pin numbers will be assigned as follows:

Device	Pin Number
82454KX PB QFP	301
82454KX PB BGA	A5
82453KX DC QFP	81
82452KX DP QFP	202
82452KX DP BGA	B12
82451KX MIC QFP	42

This signal will be added to the block diagram in Figure 1 of both Chapter 2 and Chapter 3.

Each of the specified PLLRST pins are 5 V tolerant signals.

The signal will be added to Chapter 2, Section 1.4 and to Chapter 3, Sections 1.1, 1.2 and 1.3 as signal "PLLRST", type "I, CMOS", and described as "This pin must be driven high for at least 2 clocks to reset the internal DPLL (Digital Phase Lock Loop). The DPLL should be reset after (or until) the clock input pins are stable at their final operating frequency. This pin does not have an edge rate requirement."

The following sentences will be added to Chapter 2, Section 3.7.2 and Chapter 3, Section 3.4: "The PLLRST pin must be driven high for at least 2 clocks to reset the internal DPLL. The DPLL should be reset after (or until) the clock input pins are stable at their final operating frequency."

Chapter 4 will be updated to include this pin information throughout.

2. Valid Memory Timing Parameters

The following is a list of timing values which have been validated by Intel. The list is the result of applying the rules set forth in the *Intel 450KX/GX PCIset* datasheet plus a set of filters to eliminate settings that Intel believes would not or could not be used in practice. Note that OEMs must still ensure that the timing parameters used meet the timing constraints for their system design, applicable clock rates, and supported DRAM speeds. See below for a list of acronyms used in the table.

RCD = 3, RCAD = 2, and CSR = 1 for all setting options listed below.

						1:1			2:1			4:1		
LWC	**RASPW**	**CAH**	**RCAS**	**WCAS**	**RP**	**CP**	**RBD**	**ACh**	**CP**	**RBD**	**ACh**	**CP**	**RBD**	**ACh**
2	5	1	2	2	3	1	2	2814	2	1	2834	1	0	2814
2	5	1	3	2	3	1	3	2914	1	1	2914	1	0	2914
2	5	1	3	3	3	1	3	2954	1	1	2954	1	0	2954
2	6	1	2	2	3	1	2	3014	2	1	3034	1	0	3014
2	6	1	3	2	3	1	3	3114	1	1	3114	1	0	3114
2	6	1	3	2	4	1	3	3115	1	1	3115	1	0	3115
2	6	1	3	3	3	1	3	3154	1	1	3154	1	0	3154
2	6	1	3	3	4	1	3	3155	1	1	3155	1	0	3155
2	6	2	3	2	3	1	3	3514	1	1	3514	1	0	3514
2	6	2	3	2	4	1	3	3515	1	1	3515	1	0	3515
2	6	2	3	3	3	1	3	3554	1	1	3554	1	0	3554
2	6	2	3	3	4	1	3	3555	1	1	3555	1	0	3555
2	6	2	4	3	3	1	4	3654	2	2	3674	1	0	3654
2	6	2	4	3	4	1	4	3655	2	2	3675	1	0	3655
3	5	1	2	2	3	2	3	4834	2	1	4834	1	0	4814
3	5	1	3	2	3	2	4	4934				1	0	4914
3	5	1	3	3	3	2	4	4974				1	0	4954
3	6	2	3	2	3	2	4	5534				1	0	5514
3	6	2	3	2	4	2	4	5535				1	0	5515
3	6	2	3	3	3	2	4	5574				1	0	5554
3	6	2	3	3	4	2	4	5575				1	0	5555
3	6	2	4	3	3	2	5	5674	2	2	5674	1	0	5654
3	6	2	4	3	4	2	5	5675	2	2	5675	1	0	5655
3	6	2	4	4	4	1	4	5695	2	2	56B5	1	0	5695

RCD = 3, RCAD = 2, and CSR = 2 for all setting options listed below.

						1:1			2:1			4:1		
LWC	**RASPW**	**CAH**	**RCAS**	**WCAS**	**RP**	**CP**	**RBD**	**ACh**	**CP**	**RBD**	**ACh**	**CP**	**RBD**	**ACh**
3	6	2	3	4	3	1	3	D594	1	1	D594	1	0	D594
3	6	2	4	3	4	2	5	D675	2	2	D675	1	0	D655
2	6	2	3	3	3	1	3	B554	1	1	B554	1	0	B554

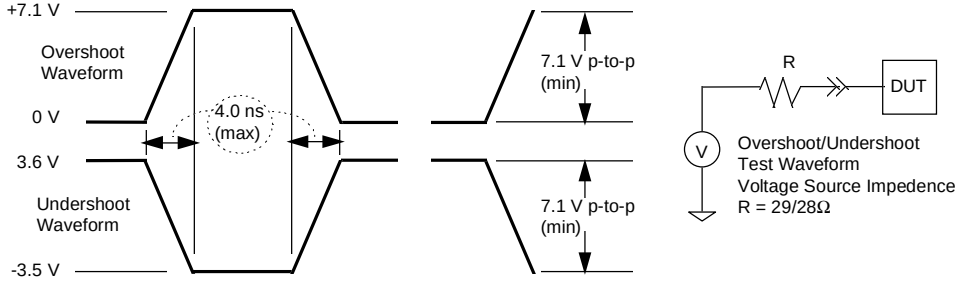
NOTE:
All above values are in number of cycles, not actual bit settings, except ACh (which is the actual bit setting, in hexadecimal).

RCD: RAS# to CAS# Delay: bits 3:2 of the Memory Timing Register (AC-AFh).
RCAD: RAS# to Column Address Delay: bit 4 of the Memory Timing Register (AC-AFh).
CSR: CAS# Setup to RAS# for CAS# before RAS# refresh: bit 15 of the Memory Timing Register (AC-AFh).
LWC: Last Write to CAS#: bits 14:13 of the Memory Timing Register (AC-AFh).
RASPW: RAS# Pulse Width: bits 12:11 of the Memory Timing Register (AC-AFh).
CAH: Column Address Hold Time: bit 10 of the Memory Timing Register (AC-AFh).
RCAS: Read CAS# Pulse Width: bits 9:8 of the Memory Timing Register (AC-AFh).
WCAS: Write CAS# Pulse Width: bits 7:6 of the Memory Timing Register (AC-AFh).
RP: RAS# Precharge Time: bits 1:0 of the Memory Timing Register (AC-AFh).
CP: CAS# Precharge Time: bit 5 of the Memory Timing Register (AC-AFh).
RBD: Read Burst Delay: bits 2:0 of the Command Register (4C-4Fh).
ACh: Actual hexadecimal value programmed into bits 15:0 of the Memory Timing Register (AC-AFh).

3. CMOS Overshoot/Undershoot Specification

The following will be added to Chapter 4, Section 2.4, “Intel 450KX/GX Undershoot Specification,” in the *Intel 450KX/GX PCIset* datasheet, and the section will be retitled “Intel 450KX/GX Overshoot/Undershoot Specifications.”

The 3.3 V tolerant CMOS signals of the processor bus allow for the following maximum AC waveforms:



Average duty cycle of 17.6%

Note: This test covers the AC operating conditions only.

ERRATA

1. Stop Clock Acknowledge Cycles May Confuse Buffers

PROBLEM: If a Stop Clock Acknowledge special cycle is issued from a processor bus agent, the 82454 PB may pipeline an outbound (host-to-PCI bus) read behind it if the IOQ (In Order Queue) depth is set to 8. The read and write buffer pointers which track these transactions may become confused, and the data buffer which contains the data for the outbound read may be deallocated incorrectly. A similar situation arises if the special cycle is issued concurrent with an inbound read. Even if the IOQ depth is 1, this may occur, if inbound (PCI-to-host bus) write-posting is enabled in the 82454 PB.

IMPLICATION: A Stop Clock Acknowledge special cycle may cause premature deallocation of a buffer holding outbound read (or inbound write) data, resulting in a system hang with DBSY# asserted.

WORKAROUND: BIOS code can contain a workaround for this erratum.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

2. 0-Byte Length Write May Cause Subsequent Write Failure

PROBLEM: If a 0-byte write occurs, a subsequent write to memory may fail, corrupting memory, or a resulting implicit writeback or line read may not complete, causing a system hang. This can happen if:

- Back-to-back 8-byte writes occur after the 0-byte write.
- The 0-byte write receives an implicit writeback response with RAW enabled in the 82453KX MC.
- The 0-byte write is followed by a line read and preceded by a 0-byte read.

IMPLICATION: The Pentium® Pro processor will not perform 0-byte writes. The only configurations identified by Intel where the failing sequence is issued are with 824731FB (PIIX) or 824731SB (PIIX3) controllers used as IDE bus masters behind the 82454 PB, with inbound write-posting enabled and an IOQ depth of 8. In this case, the 82454KX PB may issue 0-byte writes as well as pipelined back-to-back 8-byte writes (which may be issued by the 82454KX PB normally).

WORKAROUND: Ensure that no system bus agent issues 0-byte writes. If the 824731FB (PIIX) or 824731SB (PIIX3) controllers are used, they must not be used as IDE bus masters.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

3. Inbound Read May Be Accepted Despite Posted Outbound Write

PROBLEM: The 82454 PB may accept an inbound read even if a posted write is queued. This is an ordering violation.

IMPLICATION: An outbound access which follows the outbound posted write may be snoop stalled indefinitely. If a new, nonposted, inbound request is issued, BPRI# will be asserted even though the outbound posted write has not been issued to the PCI bus, causing a deadlock, and the system will hang.

WORKAROUND: Do not enable outbound write posting in the 82454 PB.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

4. SMRAM Addresses May Not Be Decoded Correctly

PROBLEM: While executing in SMM (System Management Mode), certain sequences of transactions may allow the CAS# signal to be asserted without a corresponding RAS# signal during a memory access to SMRAM. In the A2 stepping of the Intel 450KX PCIset, there are many such sequences. For the B0 stepping of the Intel 450KX PCIset, the sequences must be pipelined SMRAM requests (with the IOQ depth set to 8) as follows:

- An SMRAM request which opens a page (i.e., the transaction address accesses a block of DRAM with a new row address).
- An SMRAM request which is a page hit.
- Another SMRAM request which is a page hit.

The address phase of the third request must occur during the first clock of CAS# assertion for the second request to encounter this erratum. A second sequence is:

- An SMRAM request which is a page hit.
- Another SMRAM request whose ADS# assertion comes 5 or 6 clocks later than the ADS# assertion for the previous transaction, and which is also a page hit.

IMPLICATION: If these sequences occur while in SMM, data corruption may result.

WORKAROUND: For the A2 stepping of the Intel 450KX PCIset, SMM cannot be used. For the B0 stepping of the Intel 450KX PCIset, this erratum can be avoided by setting the IOQ depth to 1, thus preventing transactions from being pipelined together.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

5. Mixed Read Lines and Partials May Corrupt Data

PROBLEM: The 82453KX MC may not deallocate a data buffer correctly after the following sequence of transactions occurs:

1. A read line.
2. A read partial.
3. A read line which receives an implicit writeback response.

IMPLICATION: Stale data may be retrieved for a subsequent read line or read partial, resulting in corrupted data, or a protocol violation may be observed during a read line, causing a system shutdown.

WORKAROUND: If the following conditions are met, this erratum will not occur:

- In an MP system, all processors must have identical memory models, with all MTRRs for a particular region of memory mapped the same way.
- Mixed mode paging must not be used.
- All memory behind the 82453KX MC must be mapped to the same memory type.
- The IOQ depth must be set to 1.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

6. Inbound Write Posting May Cause Write Failure

PROBLEM: During an inbound posted write burst, the 82454 PB may use the same data buffer for two adjacent transactions. This causes the first write to use and deallocate the data from the second write, corrupting data

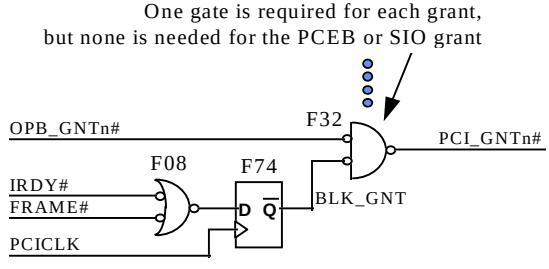
and incorrectly deallocating a data buffer. When the data phase for the second write arrives, DBSY# may be asserted for some time, with no data phase or DRDY# assertion. When the PCI master completes the write burst, the deallocated buffer is never rewritten, resulting in a system hang with DBSY# asserted.

IMPLICATION: Enabling inbound write posting may cause data corruption followed by a system hang. Disabling inbound write posting may result in significant I/O performance loss.

WORKAROUND: An external arbiter should be implemented which allows inbound posting to be enabled, and guarantees at least two idle cycles between inbound PCI requests.

This arbiter must not perform overlapped arbitration. One way to ensure this is to implement the circuit described below, external to the arbiter. The actual workaround involves waiting for a bus idle before allowing a new grant to be issued. The IOQ depth must still be set to 1, and 2:1 interleaving must be used, to work around other errata which may surface when inbound write posting is enabled (even with this workaround). Note that this latter restriction requires at least 4 SIMM DRAM modules to be loaded at all times.

This following circuit is an implementation of the described workaround:



This workaround will allow inbound write posting to be enabled on A2 450KX PCIset silicon, and will not affect the functionality of B0 450KX/GX PCIset silicon, though a slight performance loss may result if this workaround is used with the B0 stepping. Enabling inbound posting by using this workaround is a significant performance enhancement for systems with A2 450KX PCIset silicon; refer to Intel's World Wide Web site for more details on the performance loss incurred by disabling inbound write posting (at URL http://www.intel.com/procs/support/ppro/82450.htm).

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

7. RMW with Line Write May Cause Data Corruption

PROBLEM: If the 82453KX MC is performing a Read-Modify-Write (RMW) transaction due to a partial write to memory, and this is followed by a line write before the RMW completes, the byte enable signals for the RMW will be held too long, and only part of the line write will actually be written to memory.

IMPLICATION: A write may fail, corrupting data, if partial writes and line writes are pipelined together.

WORKAROUND: If the following conditions are met, this erratum will not occur:

- All processors in an MP system must have identical memory models, with all MTRRs for a particular region of memory mapped the same way.
- Mixed mode paging must not be used.
- All memory behind the 82453KX MC must be mapped to the same memory type.
- The IOQ depth must be set to 1.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

8. Inbound Write May Collide with Some Special Cycles

PROBLEM: A special cycle from a processor bus agent which occurs during a write from the PCI bus to the processor bus may corrupt the byte enable signals for the write, causing incorrect data to be written into memory. Special cycles include Shutdown, Flush, Halt, Sync, Flush Acknowledge, Stop Clock Acknowledge, and SMI Acknowledge. This can only occur with outbound write posting enabled.

IMPLICATION: Special cycles coincident with inbound traffic from the PCI bus may corrupt data. However, only Flush, Sync, and Flush Acknowledge special cycles will normally be issued from Pentium Pro processors using the A2 stepping of the Intel 450KX PCIset.

- Flush special cycles are issued upon execution of an INVD instruction. Note that this instruction intentionally removes modified lines from the cache without writing them back to memory; this results in the contents of memory being unusable. Therefore, the possibility of data corruption due to a Flush special cycle can be ignored.
- Flush Acknowledge special cycles are issued upon completion of flushing the caches after observation of a FLUSH# signal assertion. This signal is only asserted by the 82454KX PB when the system is in Deturbo mode. Therefore, these special cycles can be avoided by not enabling Deturbo mode in the affected systems.
- Sync special cycles are issued upon execution of a WBINVD instruction. This instruction is a privileged instruction which should only be executed by operating system level code. Intel has not identified any such code which uses this instruction during inbound traffic.

Since each of these special cycles are only issued when the contents of the cache are being invalidated, inbound traffic which hits a cached memory location is not valid. If all inbound traffic during these special cycles targets cached memory, no effect will be seen due to this erratum. However, inbound traffic targeting uncached main memory would be corrupted if Deturbo mode, INVD instructions, or WBINVD instructions were used simultaneously. Note that INVD and WBINVD instructions are very rare system events; execution of an INVD instruction removes modified lines from the cache without writing them back to memory, so incorrect data in memory will not cause further system problems.

WORKAROUND: Do not enable outbound write posting in the 82454KX PB.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

9. Extended Read-Around-Write May Corrupt Write Data

PROBLEM: In a sequence of transactions to two different pages in memory (page X and page Y), the row address strobe (RAS#) and memory address (MA#) signals may be asserted on the same clock, resulting in a protocol violation which corrupts the data as it is written into memory. The sequence of transactions is as follows:

1. A line read to page X.
2. A line read to page X.
3. A line read to page X.
4. A line write to page Y.
5. A line read to page X.
6. A line write to page Y.
7. A line read to page X.

8. A line read to page X.

This sequence will appear at the DRAM in the following order, with Read-Around-Write (RAW) and Extended Read-Around-Write (ERAW) enabled:

1 - 2 - 3 - 5 - 4 - 7 - 8 - 6

In this sequence, transaction 5 is issued to memory before transaction 4 due to RAW/ERAW. Transaction 6 is then detected, and transaction 4 is issued since no reordering may occur around multiple writes. At this point, transaction 6 is at the front of the queue, and is a row-hit/page-hit relative to transaction 4, so the RAS# signal is left asserted in preparation for transaction 6. ERAW then causes transactions 7 and 8 to be reordered in front of transaction 6; these transactions are not row-hit/page-hit transactions, and the MA# lines are updated on the same clock as RAS# is reasserted, causing the protocol violation. The data returned for transactions 7 and 8 will then be corrupted.

IMPLICATION: ERAW will corrupt data returned for this sequence of memory transactions.

WORKAROUND: Do not enable ERAW in the 82453KX MC.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

10. Outbound Posted Write After Inbound Read Prefetch May Hang

PROBLEM: If an outbound write closely follows an inbound read prefetch, the data buffer containing the outbound write's data may be rewritten by the data for the prefetch. This occurs when the outbound write is issued after the PCI master has disconnected, but before the last prefetch has been issued on the processor bus; in this situation, the outbound write will incorrectly be allowed to post.

IMPLICATION: This condition will result in improper deallocation of the data buffer before the outbound write completes, hanging the system.

WORKAROUND: Outbound write posting must be disabled in the 82454KX PB.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

11. Inbound Posted Write with 1:1 Interleaving May Corrupt Data

PROBLEM: In systems configured with 1:1 interleaved memory (with only 2 SIMMs, for example) and inbound write posting enabled, if a string of line write transactions receive implicit writeback responses, data may be corrupted for subsequent writes if a refresh cycle occurs during the line writes. This occurs when the refresh backs up the transactions to memory such that the first partial write following the line write sequence is issued to the 82451 MIC with line-size encoding. The SYSCMD# and MEMCMD# signals will be correct, however.

IMPLICATION: Corrupted data will be written to memory in this case, with the data which was supposed to be written shifted by 8 bytes (data chunks 0-1-2-3 will be written as X-0-1-2, where X is most likely all 0's).

WORKAROUND: Do not enable inbound write posting in the 82454KX PB if memory is 1:1 interleaved, and use an IOQ depth of 1.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

12. RAW May Cause Data Corruption

PROBLEM: If Read-Around-Write (RAW) is enabled in the 82453KX MC, some sequences of memory transactions may cause the 82453KX MC to issue the memory address (MA#) and row address strobe (RAS#)

signals on the same clock edge for a DRAM read cycle, causing data corruption. The sequence which encounters this behavior is as follows:

1. A read to the 82454KX PB is snoop stalled.
2. During the snoop stall, a read-for-ownership (i.e., read and invalidate line) occurs.
3. Also during the snoop stall, a line write which is a row-hit/page-hit occurs.
4. A code line read which is a row-miss/page-miss occurs at the end of the snoop stall, but before snoop status is available for transactions 2 and 3.

IMPLICATION: When this occurs, the 82453KX MC will not start the write cycle until the snoop status is available for the preceding read. By then, the second read is in the internal queues behind the write, MA# will be driven with RAS# still asserted, and incorrect data will be returned for transaction 3.

WORKAROUND: Do not enable RAW in the 82453KX MC.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

13. Data Transfer Order 3 May Cause Data to Be Issued Out of Order

PROBLEM: If a line write is issued which uses a data transfer order of 3 (with A[4:3] = 11, so that the chunks are issued in order 3-2-1-0) and receives an implicit writeback response, a line write immediately following this transaction may be issued with a reversed data transfer order, corrupting memory.

IMPLICATION: A line write whose address has A[4:3] = 11 (binary) will have a “critical chunk” of 3. According to the protocol established by the Intel486™ processor, this chunk must be written to memory first. A line write transaction which follows this one may have a different critical chunk (chunk 2, for example, issued in the order 2-3-0-1), but may be written to DRAM with a reversed order (1-0-3-2, in this case, or a data transfer order of 1). This causes the memory location to contain incorrect data. Note that neither the Pentium Pro processor nor the 450KX PCIset will issue line write transactions with this data transfer order (they will always have a data transfer order of 0). Third party agents which issue such transactions with a data transfer order of 3 will encounter this erratum.

WORKAROUND: Do not use third party agents which issue line writes with a data transfer order of 3 to the 82453KX MC.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

14. PCI Address Parity Error May Cause Dropped Transaction

PROBLEM: If PCI address parity checking is enabled in the 82454KX PB, an inbound (PCI to processor bus) transaction with bad address parity will cause the 82454KX PB to assert SERR#. The DEVSEL# signal may then remain deasserted incorrectly. If a second inbound transaction occurs after the error, it will not be forwarded to the processor bus.

IMPLICATION: Though a PCI address parity error may be detected and flagged, a second transaction after the one with the error may be dropped, possibly corrupting data.

WORKAROUND: The system can be configured to promote the SERR# resulting from the parity error to an NMI, allowing software to handle the failing I/O system normally.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

15. System Hang with Inbound Write Posting Enabled

PROBLEM: After a long write burst from the PCI to the processor bus, an outbound request will dynamically disable inbound write posting. The transaction immediately following the inbound burst may get a very fast retry. If this occurs, the 82454KX PB state machine may encounter a race condition which causes a bus hang on the next inbound request. The conditions for this to occur include:

- An inbound posted line write completes.
- The queue and data buffer for inbound transactions are full, or inbound write posting is dynamically disabled.
- The transaction after the inbound posted write is a nondual address transaction with A[4:2] = 5 or 6, with only one idle cycle between it and the inbound posted line write.

This has only been observed in sequences containing a WRINV command on the PCI bus.

IMPLICATION: If inbound write posting is enabled in the 82454KX PB and the WRINV command is being used by a PCI device, the PCI bus may hang. The next outbound transaction will then hang the processor bus with BNR# toggling or with an infinite snoop stall.

WORKAROUND: Ensure nonoverlapped PCI arbitration via the workaround documented under Erratum 34, *Inbound Write Posting May Cause Write Failure*. If this workaround is not used, inbound write posting must be disabled in the 82454KX PB to avoid this erratum.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

16. RAW May Cause Data Corruption During Refresh

PROBLEM: If Read-Around-Write (RAW) is enabled in the 82453KX MC and there are no transactions in its queues, a refresh which should occur next may cause improper transaction ordering. This boundary condition is as follows:

1. A line read transaction is issued.
2. From 2 to 6 clocks after the ADS# assertion for the read, a refresh is requested.
3. A line write transaction is issued.
4. A line read transaction is issued which is a row-miss.

In this case, the refresh will be recognized before the write appears at the head of the queue, and will block the write from being handled. This allows the second line read to be reordered by RAW to occur before the write.

IMPLICATION: This boundary condition may cause data to be corrupted, if the data for the line read is dependent on the line write. Intel has observed this erratum in 1:1 interleaved configurations, and to a lesser extent in 2:1 interleaved configurations.

WORKAROUND: Do not enable RAW in the 82453KX MC.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

17. GAT Devices May Time Out During Inbound Read Prefetch

PROBLEM: While in GAT (Guaranteed Access Time) mode, the 82454KX PB does not dynamically disable inbound read prefetching. Thus, a transaction which is issued immediately after MEMACK# is asserted may cause a prefetch to occur, tying up the bus and possibly allowing ISA or EISA devices configured for GAT to time out.

IMPLICATION: The 2.4 µs guaranteed access time may not be met for devices behind the 82454KX PB and an ISA or EISA bridge, resulting in spurious time-outs for such devices if inbound read prefetching is enabled, though most such devices will accept a longer access time.

WORKAROUND: If time-out problems occur while in GAT mode, disable inbound read prefetching in the 82454KX PB.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

18. Data May Be Corrupted If RCD = 4 and LWC = 3

PROBLEM: The memory timings RCD (RAS# to CAS# Delay) and LWC (Last Write to CAS#) interact in such a way that if RCD is set to 4 and LWC is set to 3, the following transaction sequence will cause a data read to be corrupted:

1. A line read which triggers an implicit writeback and results in a page miss.
2. A line read which triggers an implicit writeback.
3. A line read to the same line as transaction 2.

IMPLICATION: These timing values may cause read data to be corrupted if the writeback memory type is used.

WORKAROUND: Do not use an RCD value of 4.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

19. T_{CO_MAX} Specification Not Met for GTL+ Signals

PROBLEM: The T_{CO_MAX} specification for the GTL+ signals of the Intel 450KX PCIset is 6.0 ns. The actual value is 7.5 ns.

IMPLICATION: This value should be used when designing systems using the affected chipsets.

WORKAROUND: None identified.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

20. RAW May Hang 1:1 or 2:1 Interleaved MP Systems

PROBLEM: If Read-Around-Write (RAW) is enabled in the 82453KX MC, there is a potential for two reads being assigned to the same internal data buffer, causing the system to hang. The following transactions must be issued during a snoop stall for a previous read for this erratum to occur:

1. A line read transaction.
2. A 0-byte length read transaction.
3. An explicit writeback transaction.
4. A line read transaction.

Transactions 1 and 4 may target the same buffer (causing the system to hang) in this situation. In A2 450KX PCIset silicon, it is also possible for a read transaction to incorrectly pass a write transaction with the same line address, but different chunk address. Both of these conditions require multiple symmetric bus agents (such as processors).

IMPLICATION: Uniprocessor systems will not be affected by this erratum. Other Intel 450KX PCIset-based systems will hang if this sequence occurs during a snoop stall.

WORKAROUND: Do not enable RAW in the 82453KX MC.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

21. Mixed Interleave Increments May Cause Data Corruption

PROBLEM: If some DRAM module sizes are mixed together, some Intel 450KX PCIset-based systems may corrupt user or system data, resulting in incorrect calculations and/or system failure. This can only occur if:

- Interleave increments containing 8-Mbytes or 32-Mbytes of memory exist in conjunction with interleave increments which contain other amounts of memory, or
- One or more interleave increments have 8- or 32-Mbytes of memory, and there are no DRAM modules in the first row (row 0) of the memory subsystem.

Note that in systems with only one row of memory in use (i.e., 2 SIMMs in 1:1 interleave or 4 SIMMs in 2:1 interleave), or with all SIMMs or DIMMs the same size and configuration, only one interleave increment size is possible (since all memory in the same row must be the same size), so this erratum will not affect the system.

Also note that the BIOS of some (usually server) platforms may automatically downsize or eliminate a row of memory if a bad DRAM module is detected in that row. It is possible for this alteration of memory sizes to result in the system entering a vulnerable configuration (if memory is downsized to interleave increments of 8 or 32 Mbytes, or if row 0 is removed from the configuration). This can occur even with logically double-sided DRAM modules, which otherwise always have the same size interleave increments across their two rows.

IMPLICATION: Some systems only support one row of memory (i.e., 1:1 interleaving with 2 SIMMs or 2:1 interleaving with 4 SIMMs). In these systems, only one interleave increment size is possible (since all memory in the same row must be the same size), so they are not affected by this erratum. In systems which support two or more rows of memory (other than systems which support two rows of double-sided SIMM DRAM only), one must be careful not to mix DRAM of certain sizes. If there are 8 or 32 Mbytes of DRAM in any interleave increment, all other interleave increments must have the same amount of DRAM, and row 0 must be populated with DRAM modules to avoid data corruption due to this erratum.

The chart below gives the interleave increments for some common memory technologies:

SIMMs	DRAM	Technology	Interleave Increment
Two 4-Mbyte, single-sided	1-Mbit x 4	4-Mbit	8 Mbytes*
Two 8-Mbyte, double-sided	1-Mbit x 4	4-Mbit	8 Mbytes*
Two 8-Mbyte, single-sided	2-Mbit x 8	16-Mbit	16 Mbytes
Two 16-Mbyte, double-sided	2-Mbit x 8	16-Mbit	16 Mbytes
Two 16-Mbyte, single-sided	4-Mbit x 4	16-Mbit	32 Mbytes*
Two 32-Mbyte, double-sided	4-Mbit x 4	16-Mbit	32 Mbytes*
Two 32-Mbyte, single-sided	8-Mbit x 8	64-Mbit	64 Mbytes
Two 64-Mbyte, double-sided	8-Mbit x 8	64-Mbit	64 Mbytes
Two 64-Mbyte, single-sided	16-Mbit x 4	64-Mbit	128 Mbytes
Two 128-Mbyte, double-sided	16-Mbit x 4	64-Mbit	128 Mbytes

DIMMs	DRAM	Technology	Interleave Increment
One 8-Mbyte, single-sided	1-Mbit x 4	4-Mbit	8 Mbytes*
One 16-Mbyte, double-sided	1-Mbit x 16	16-Mbit	8 Mbytes*
One 16-Mbyte, single-sided	2-Mbit x 8	16-Mbit	16 Mbytes
One 32-Mbyte, double-sided	2-Mbit x 8	16-Mbit	16 Mbytes
One 32-Mbyte, single-sided	4-Mbit x 4	16-Mbit	32 Mbytes*
One 64-Mbyte, double-sided	4-Mbit x16	64-Mbit	32 Mbytes*
One 64-Mbyte, single-sided	8-Mbit x 8	64-Mbit	64 Mbytes
One 128-Mbyte, double-sided	8-Mbit x 8	64-Mbit	64 Mbytes
One 128-Mbyte, single-sided	16-Mbit x 4	64-Mbit	128 Mbytes

NOTE:
*To avoid corruption of data, do not mix 8-Mbyte or 32-Mbyte interleave increments with other increment sizes (including each other). If 8-Mbyte or 32-Mbyte interleave increments are used (exclusively), ensure that row 0 is populated with DRAM modules.

WORKAROUND: When upgrading memory:

- In systems which support multiple rows of memory, always populate row 0 with DRAM modules.
- Exercise caution when using 4-Mbyte or 16-Mbyte SIMMs (single- or double- sided), or when using 8-Mbyte or 32-Mbyte DIMMs. Note that exclusively using DRAM modules which are all the same size will always avoid this erratum.
- When writing a BIOS for an Intel 450KX-based system, the memory configurations susceptible to this erratum should be detected and flagged to alert the user of the problem. Ensure that such detection mechanisms are placed after any bad DRAM detection mechanisms so that vulnerable configurations are detected after memory downsizing has occurred.
- Refer to your system documentation, or contact your system vendor, for details on your system's support for the various interleaving modes and DRAM styles.

See the white paper *Mixing DRAM Sizes with the 82450KX/GX PCIset* on Intel's World Wide Web site at URL http://www.intel.com/procs/support/ppro/450kxgx.htm for more information.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

22. Parity Error May Occur for ADS# During BINIT#

PROBLEM: If BINIT# is asserted due to some catastrophic system event, the system will reset the bus and attempt to recover. If, however, ADS# is asserted for a request during the BINIT#, some of the signals associated with the request may not be driven when they should be. This results in an incorrect request parity and an assertion of AERR# 2 clocks after the BINIT# is complete, which is not a valid error phase.

IMPLICATION: A second (spurious) AERR# will be observed, resulting in a spurious SERR#. No data loss or hang is associated with this erratum, just an extra assertion of AERR# after detection of a catastrophic bus condition.

WORKAROUND: None identified.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

23. Hang with PCI-to-PCI Bridges in MP Systems

PROBLEM: If a PCI-to-PCI bridge is present in a system, either on a card or native on the motherboard, a "livelock" hang condition may be possible if pipelined transactions are allowed (i.e., the IOQ depth is set to 8). This may happen if the following events occur:

1. An ordering event (such as I/O reads, and I/O writes for some components) from one processor is followed by a second such event from another processor. These outbound events are directed through the 82454KX PB, and dynamically disable inbound write posting.
2. The PCI-to-PCI bridge is attempting to perform an inbound write through the 82454KX PB.

If this situation arises, the PCI-to-PCI bridge will retry the outbound transactions, but must follow ordering constraints on the I/O operations. The outbound transactions are then reissued on the processor bus faster than the 82454KX PB can prepare to service the inbound write request from the PCI-to-PCI bridge. Consequently, the inbound write cannot complete, and the I/O transactions are continuously retried and reissued on the processor bus, resulting in a "livelock" hang with neither side making forward progress.

IMPLICATION: PCI-to-PCI bridges present in an MP system may cause the system to hang.

WORKAROUND: Set the IOQ depth to 1. If this is not acceptable (multiprocessor systems may see significant performance degradation with this setting), a hardware workaround may be implemented using a programmable logic component. This workaround allows the outbound transactions to complete after they are retried by the PCI-to-PCI bridge, by putting the 82454KX PB in non-GAT (as opposed to GAT, or Guaranteed Access Time, mode) for 64 processor clocks after an outbound request is retried once, or after an inbound request is retried 8 times.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

24. PCI_RST# Not Asserted Asynchronously

PROBLEM: The 82454KX PB requires a valid BCLK to assert the PCI_RST# signal, due to clocked logic in the assertion paths of these signals.

IMPLICATION: This signal is not asynchronous, as was intended.

WORKAROUND: Ensure a valid BCLK is provided before attempting to reset the PCI bus.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

25. BERR# to BINIT# Conversion May Prevent Recovery From BINIT#

PROBLEM: If an error on a bus split operation occurs which causes an assertion of both BERR# and BINIT#, and BERR# to BINIT# conversion is enabled in the 82454KX PB, BINIT# will be driven a second time, 2 bus clocks after the first completes. At this time, another 450KX agent may still be driving BNR# for the first BINIT#, and other devices may then try to drive BNR# for the second BINIT#. This results in the system being unable to recover successfully from the BINIT#, hanging the system.

IMPLICATION: After a double assertion of BINIT# due to detection of a catastrophic error, the bus may not be reset properly, resulting in a system hang.

WORKAROUND: Do not enable BERR#-to-BINIT# conversion in the 82454KX PB. BERR#-to-SERR# conversion can be used instead.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

26. Error Reporting Registers May Not Record Error Information Correctly

PROBLEM: The error reporting functionality of the 82453KX MC is limited in the following ways:

1. If a transaction occurs which contains an SBC (single-bit correctable) error, the error is detected, corrected, and logged (if ECC error detection, correction, and logging are enabled in the 82453KX MC). If a subsequent transaction contains an SBC error on one chunk (an 8-byte block of data) and an UNC (uncorrectable, double-bit) error on another, both will be detected, and the SBCERR# and BERR# signals will be asserted normally, but only the SBC error will actually be logged in the error reporting registers of the 82453KX MC.
2. If a transaction occurs with an UNC error, the error is tracked via an internal error buffer, and BERR# is asserted (if this feature is enabled). If the system does not shut down due to this error, and an SBC error occurs such that the UNC error is being popped from the error buffer at the same time that the SBC error is pushed into the buffer, the UNC error will not be logged into the error reporting registers of the 82453KX MC.

IMPLICATION: Under some circumstances, some errors will not be reported properly when detected in combination with other errors. This will result in an error not being logged into the error reporting registers of the 82453KX MC. However, this erratum does not affect the detection and correction of SBC errors or the detection of UNC errors.

WORKAROUND: None identified.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

27. Combination of ECC Errors May Cause One Error to Be Undetected

PROBLEM: The 82452KX DP may not detect a memory ECC error during pipelined line reads, when there are multiple SBC and/or UNC errors across cache line boundaries. The error combinations which are affected are as follows:

1. An SBC error will detected and corrected, but not reported to the 82453KX MC, if it occurs on chunk 3 of the first line read when there is an UNC error on chunk 2 of the first line read and an SBC on chunk 0 of the second line read. In this case, no error record will exist for the first SBC, but data will not be corrupted.
2. An UNC error will be detected by the 82452KX DP but not reported to the 82453KX MC, if it occurs on chunk 3 of the first line read when there is an SBC error on chunk 2 of the first line read and either type of error on chunk 0 of the second line read. In this case, no error record will exist for the first UNC, and BERR# will not be driven if the third error is an SBC.

Note that these are the only combinations of errors affected by this erratum; other combinations of errors (including cache lines with **more** errors than specified) will all be detected, and any subsequent UNC errors which occur will cause BERR# to be driven by the 82453KX MC (assuming this feature is enabled).

IMPLICATION: An error will not be detected if it occurs with these very specific combinations, possibly resulting in corrupted data. The other errors in these combinations, as well as all other errors which occur on other transactions which do not fall within this pattern, will be detected correctly.

WORKAROUND: None identified.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

28. 16-Byte Write May Hang System

PROBLEM: If a 16-byte partial write is issued in the middle of a sequence of line writes, the line write immediately after the 16-byte write may fail. A subsequent read transaction will hang the processor bus. Note that neither the

Pentium Pro processor nor any Intel 450KX PCIset agent will generate 16-byte writes. Only systems containing third-party bus agents may be affected by this erratum.

IMPLICATION: If third-party agents which issue 16-byte writes are present in a system, the system may hang after a sequence of write transactions.

WORKAROUND: Do not use third-party agents which issue 16-byte writes.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

29. 16-Byte Read with Two ECC Errors May Not Be Reported Correctly

PROBLEM: If a line read contains either type of error in chunk 3, and the line read is followed by a 16-byte read which has either an SBC error in chunk 0 and an UNC error in chunk 1 or an UNC error in chunk 1 and an SBC in chunk 0, a stale error record will be left in the error reporting registers which does not correspond to the last errors detected. All errors in this combination will be detected, however, and BERR# will be driven for UNC errors (assuming this feature is enabled). Note that neither the Pentium Pro processor nor any Intel 450KX PCIset agent will generate 16-byte reads; only systems containing third-party bus agents may be affected by this case.

IMPLICATION: Under some circumstances, some errors will not be reported properly when detected in combination with other errors. This may result in an error not being logged into the error reporting registers of the 82453KX MC at all, or it may result in incorrect error information being logged. This erratum does not affect the detection and correction of SBC errors or the detection of UNC errors.

WORKAROUND: Do not use third-party agents which issue 16-byte reads.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

30. Inbound Locked PCI Transactions May Hang System

PROBLEM: This erratum manifests itself in the following sequence:

1. A locked read request is issued on the PCI bus, and targets the processor bus. The 82454KX PB asserts DEVSEL#.
2. The transaction is entered into the 82454KX PB's request queue, which then asserts BPRI#.
3. Before the ADS# for this transaction occurs, a pipelined retry response is received for the previous request.
4. ADS# is asserted on the processor bus for the locked read. In the sequence which causes the system to hang, the 82454KX PB confuses the retry for the previous transaction with a retry for this locked read. LOCK# is then asserted for only one clock, but the PCI LOCK# signal remains asserted.
5. The locked read's response phase completes on the processor bus and TRDY# is asserted on the PCI bus, completing the first part of the lock. Note that BPRI# is still asserted.
6. The locked write which is the second half of the inbound lock is issued on the PCI bus, and the 82454KX PB asserts DEVSEL#.
7. The locked write transaction is entered into the queue. However, the 82454KX PB cannot issue the transaction on the processor bus until PCI LOCK# is deasserted. The PCI bus cannot deassert PCI LOCK# until the write completes. This deadlock results in the system hanging.

IMPLICATION: If a PCI device driver allows the device to issue a locked transaction targeting the processor bus, and the IOQ depth is set to 8, a retry response for a transaction may cause the system to hang.

WORKAROUND: Drivers that are capable of issuing inbound locked PCI transactions are very rare. When using these drivers in a system, use an IOQ depth of 1.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

31. Retry on Inbound Read May Corrupt Outbound Data

PROBLEM: If an inbound read is retried by a third-party agent, and DBSY# is still asserted from a normal data response for a pipelined read directed through the 82453KX MC, an outbound write can be issued while the outbound data buffer and status pointer are out of synch. This results in incorrect data being used for the outbound write.

IMPLICATION: Using third-party devices which issue pipelined retry responses may result in data corruption.

WORKAROUND: If third-party devices which issue retry responses are used in the system, use an IOQ depth of 1. Alternatively, a third-party device can delay its retry response until DBSY# is deasserted from the previous response.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

32. ADS# in Last Clock of BINIT# Prevents Recovery

PROBLEM: If an ADS# assertion for a transaction targeting the 82453KX MC occurs during the last clock of an assertion of BINIT#, the ADS# will not be canceled correctly. The system will hang instead of recovering from the catastrophic condition which resulted in the BINIT# assertion.

IMPLICATION: BINIT# is only asserted upon detection of a catastrophic bus condition. If this occurs, the system may not generally be able to recover. This erratum decreases the possibility of being able to recover from this condition, but does not cause any additional incorrect behavior.

WORKAROUND: None identified.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

33. Some Signals Indeterminate After RESET# Deassertion

PROBLEM: There exists a window of a single bus clock after RESET# has been deasserted where simulation has shown a possibility of the 82453KX MC sending a spurious command via the MEM_CMD# and/or MIC_CMD# signals to the 82452KX DP and/or 82451KX MICs.

IMPLICATION: If this were to occur, it might result in the 82452KX DP and/or 82451KX MICs attempting to execute a false command, most likely resulting in a system hang on startup. However, Intel has not identified any silicon 450KX component that has ever exhibited this condition, either under test or in actual systems; the MEM_CMD# and MIC_CMD# signals have always been observed to come up in a deterministic fashion.

WORKAROUND: None identified.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

34. Delayed Read from PCI-to-PCI Bridge May Corrupt Data

PROBLEM: There exists a boundary condition in the 82454KX PB which may cause corruption of read data in an MP system, if the following sequence of events occurs:

1. A processor performs a destructive read directed towards a device below a PCI 2.1 Local Bus Specification compliant PCI-to-PCI bridge. The bridge delays the read and the 82454KX PB gives a retry response to the transaction. When this occurs, the PCI-to-PCI bridge starts a timer. The PCI-to-PCI bridge discards the read data from the target device if this timer expires.
2. A different processor initiates a configuration access (read or write) to a nonexistent device with a device ID of greater than 15. These accesses are allowed to time out on the processor bus (and are claimed by the 82454KX PB's watchdog timer), and are not forwarded to the PCI bus by the 82454KX PB.
3. Another processor issues a nonposted write to the 82454KX PB, or an inbound request targets the 82454KX PB before the first processor can retry the destructive read. If this occurs, the read cannot be forwarded to the PCI bus until the 82454KX PB's watchdog timer expires.

The PCI-to-PCI bridge's timer will expire after 2^{15} PCI bus clocks (which is less than the 82454KX PB's minimum watchdog timer value of 1.5 ms). After this, it will discard the data, as required by the PCI 2.1 Local Bus Specification. Since the read was destructive, the data is lost.

IMPLICATION: This erratum would typically occur when a driver is scanning for populated PCI device numbers in the system. If delayed reads are enabled in the PCI-to-PCI bridge, data corruption may result.

WORKAROUND: Do not enable delayed reads in PCI 2.1 Local Bus Specification compliant PCI-to-PCI bridge devices.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

35. Page Open Policy of "Hold Page Open" May Corrupt Write Data

PROBLEM: If Read-Around-Write (RAW) is enabled, the Page Open Policy is set to "hold page open," and the IOQ depth is set to 8, there is a potential for data corruption after a configuration cycle is issued during a sequence of memory transactions, as follows:

1. A read from memory.
2. A write to the Configuration Address register.
3. A write to memory which is a page miss.
4. A read from memory which is a page hit (relative to transaction #1).

Or,

1. A read from memory with an ECC error logged.
2. A write to memory which is a page miss.
3. A read from memory which is a page hit (relative to transaction #1).

These sequences, with the configuration detailed above, will cause the data for the write to memory to be corrupted.

IMPLICATION: With all of these features enabled, data corruption may occur, resulting in unpredictable system failure.

WORKAROUND: Use the default Page Open Policy (close page). Disabling RAW and ERAW or using an IOQ depth of 1 will also prevent this erratum, but may have a larger impact on performance.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

36. T_{CASE} Drop Plus Voltage Swing May Cause DPLL Failure

PROBLEM: Analysis of the DPLL (Digital Phase Lock Loop) units of the Intel 450KX PCIset components has shown that a DPLL failure can occur during certain changes in temperature and/or voltage within the Intel 450KX PCIset component specification, resulting in a loss of DPLL functionality for between 2 and 500 bus clocks.

The current specification states that the Intel 450KX/ PCIset is operational over a T_{CASE} range of 0 - 85 °C and a V_{CC} range of 3.3 V ± 5%.

After a device has undergone a hard reset of the DPLL (via the PLLRST pin), a drop in T_{CASE} accompanied by an increase in V_{CC} may cause this erratum to occur. The magnitude of the temperature drop and supply voltage increase required to cause this failure is graphed below:

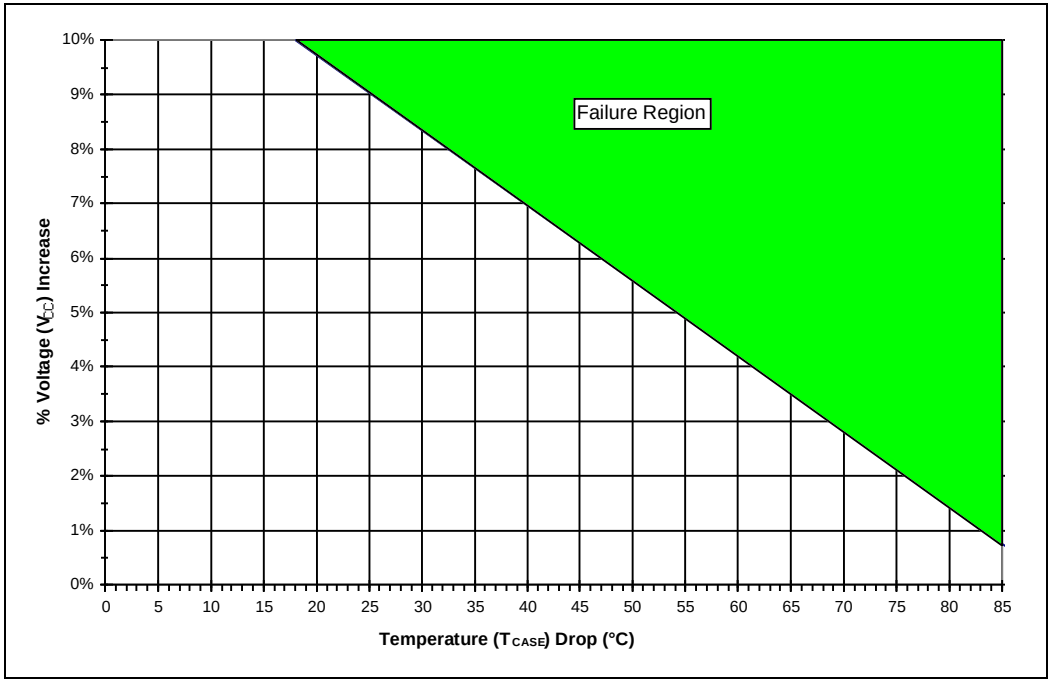


Figure 1. V_{CC} Increase vs. T_{CASE} Drop for DPLL Failure (Worst Case)

IMPLICATION: If the T_{CASE} of any Intel 450KX PCIset component is allowed to decrease by more than 18°C after the point at which DPLL lock is obtained after a DPLL hard reset, a positive voltage swing may cause the component to lose its internal clock for 2 - 500 processor bus clocks. This may result in a system hang, lost data, or other unpredictable system failure (note that if the component is not processing commands or data for the time during which the internal clock is lost, no failure will be observed). The larger the temperature drop and/or voltage swing, the more likely the failure.

If V_{CC} swings from 3.3 V -5% to 3.3 V +5%, and T_{CASE} does drop more than 18 °C past the temperature at which the DPLL was reset, this erratum may occur. Similarly, if T_{CASE} transitions from 85 °C (at DPLL reset time) to 0 °C, a swing in V_{CC} of more than 0.5% may cause this erratum. Thus, maintaining a moderately constant T_{CASE} and V_{CC} will prevent this erratum, as per the graph above.

WORKAROUND: Ensure that the DPLL reset occurs during a period where the T_{CASE} is low and/or the V_{CC} is high relative to normal operational conditions (e.g., if the system is running at a high temperature and is powered down, allow it to cool before powering up again). Alternately, ensure that the system meets a restricted specification for changes in T_{CASE} and V_{CC}.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

37. Memory Gap Reclaiming May Corrupt Data

PROBLEM: If the memory subsystem is configured using the Memory Gap Register (MG), Low Memory Gap Register (LMG), or High Memory Gap Start Address and End Address registers (HMGSA, HMGEA) to allow a gap in the address map of the 82453KX MC, and if the memory in these gaps is reclaimed (by setting the appropriate bit in the MG, LMG, or HMGSA registers), the row address strobe (RAS#) signals may be corrupted.

IMPLICATION: An incorrect address may be generated for a memory access if any of these three memory gaps are enabled with the memory reclaimed. This would result in data corruption and unpredictable system failure.

WORKAROUND: If these memory gaps are used, do not reclaim the memory in the gaps.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

38. RAW May Corrupt Write Data in 1:1 Interleaving

PROBLEM: If a memory subsystem is configured for 1:1 interleaving (i.e., only using one memory interleave, also known as noninterleaved), and read-around-write (RAW) is enabled, a partial write transaction to a memory location marked as Modified in the L2 cache followed by a line read transaction which is reordered around the partial write may result in the write data being corrupted.

IMPLICATION: With RAW enabled and the memory subsystem 1:1 interleaved, data corruption may occur, resulting in unpredictable system failure.

WORKAROUND: Do not enable RAW if the system is configured in 1:1 interleaving.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

39. BINIT# Assertion May Cause Active RAS# Negation

PROBLEM: BINIT# is asserted on the Pentium Pro processor system bus to indicate the occurrence of a catastrophic system error condition or a situation that prevents reliable future operation. When the 82453GX MC component of the 450GX PCIset recognizes the assertion of BINIT# on the system bus, it prepares to clear certain internal state. In the process, a currently active RAS# signal associated with a read, write or refresh

operation in progress may also be negated. If this negation causes the minimum RAS# pulse width timing to be violated then spurious bits may appear in one page of the memory array.

IMPLICATION: The catastrophic system error conditions that led to BINIT# assertion may in turn lead to a page of memory being incompletely written or improperly refreshed before potentially recovering from BINIT#.

WORKAROUND: Recovery from BINIT# assertion may be aided by a Machine Check Exception (MCE) or System Management Interrupt (SMI) handler. MCE or SMI handlers resident in nonvolatile memory can protect recovery routines from encountering this situation, allowing them to be reliably executed after BINIT# assertion.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

SPECIFICATION CLARIFICATIONS

1. Explicit Writebacks Claimed by 82454KX PB

Note 2 in Section 3.2 of the *Intel 450KX/GX PCIset* datasheet states that writebacks initiated by other agents are ignored by the PB. It should be noted that while this is true with respect to PCI bus transactions (i.e., no PCI bus cycles will be generated due to any writeback transaction), if a writeback occurs to memory behind the 82454KX PB, the data will be lost or a violation of processor bus protocol will occur. The 82454KX PB is not a caching agent, and no writeback transactions should be targeted to devices on the PCI bus. Memory behind the 82454KX PB may not be mapped as cacheable (WB type) memory.

DOCUMENTATION CHANGES

1. Register Offset and Default Value Correction

Some configuration registers are documented unclearly or inconsistently in the *Intel 450KX/GX PCIset* datasheet. A table of the correct offsets and values is given below with the changes in bold (note that this list only contains registers with changes):

Configuration Register	Address Offset	Default Value	Notes
82454KX			
Top of System Memory	40-43h	**0000** 0000h	
Bridge Device Number	49h	0001 1001**b**	
PB Configuration	4Ch	**1**9h	
PCI Read/Write Control	54-55h	**00**00h	
Memory Gap Range	78-79h	**00**00h	
Memory Gap Upper Address	7A-7Bh	**00**00h	
PCI Frame Buffer	7C-7Fh	**0000 00**00h	
High Memory Gap Range Start Address	88-8Bh	**0000 00**00h	
High Memory Gap End Address	8C-8Fh	**0000 00**00h	
Configuration Values Driven on Reset	B0-B1h	**00**00h	Bit 7: 1 = Depth of **1**. 0 = Depth of **8**. Pentium® Pro processors use an in-order depth of **1** if this bit is 1.
Captured System Configuration Values	B4-B5h	**000X XXXX XXX0 0000b**	X = captured during hard reset. Bit 7: 1 = Depth of **1**. 0 = Depth of **8**. Pentium Pro processors use an in-order depth of **1** if this bit is 1.
SMRAM Range	B8-BBh	0000 0005h	Bits [15:0] correspond to A[31:**16**]#. The default starting address is **5**0000h and ranges to **5**FFFFh.
PB Retry Timers	C8-**CB**h	0000 0003h	

Configuration Register	Address Offset	Default Value	Notes
82453KX			
Controller Device Number	49h	0001010X**b**	X = loaded at reset
Single Bit Correctable Error Address	74-77h	**0000** 0000h	
Low Memory Gap Register	7C-7Fh	0010 0000h	**Bits [9:5]: Reserved.** Bits [4:0]: **Low Memory Gap Size.** This field defines the memory gap size as follows: **Bits [4:0] Size** **Bits [4:0] Size** 00000 1 MB **00111** 8 MB **00001** 2 MB **01111** 16 MB **00011** 4 MB **11111** 32 MB
High Memory Gap Start Address	88-8Bh	**0000** 0000h	**Bit 30: Reclaim Enable.** 1 = Enable. 0 = Disable (default). When enabled, the physical memory in this gap is reclaimed.
High Memory Gap End Address	8C-8Fh	**0000** 0000h	
Memory Timing Register	AC-AFh	30DF3516h	Bit 15: 1 = **2** Cycles. 0 = **1** Cycle (default).
SMRAM Range	B8-BBh	**0000** 000Ah	

2. CMOS Definition Should be 3.3 V or 5 V

In Section 1.0. of both Chapter 2 and Chapter 3 of the *Intel 450KX/GX PCIset* datasheet, CMOS signals are defined as follows:

CMOS Rail-to-rail CMOS tolerant to 5 V levels.

This should read:

CMOS Rail-to-rail CMOS tolerant to 3.3 V or 5 V levels. See Chapter 4, Section 1.2, “Signal Groups.”

3. Pull-up Resistor Required on PCLK

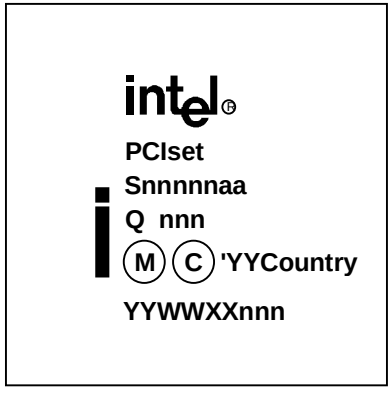
In Chapter 2, Table 4 of the *Intel 450KX/GX PCIset* datasheet, it is incorrectly stated that a pull-down resistor is required on the PCLK signal. This should be specified as a **pull-up** resistor, as is stated in Section 3.7.1.2 of Chapter 2.

Part II: Specification Update for the Intel 450GX PCIset

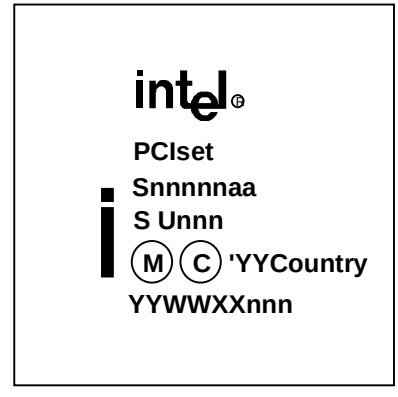
GENERAL INFORMATION

Top Markings

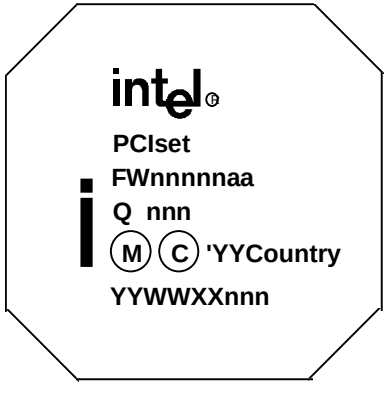
B- and C-Step Sample Units, QFP:



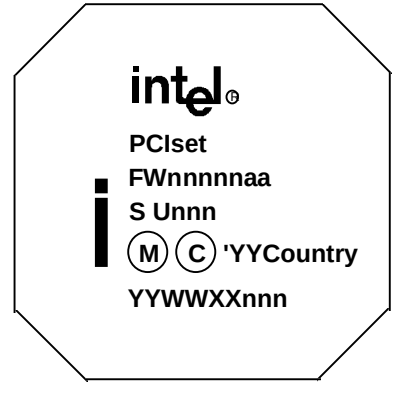
B- and C-step Production Units, QFP:



B- and C-step Sample Units, BGA:



B- and C-step Production Units, BGA:



NOTES:

- nnnnnaa = Product Number
- Q nnn = Sample Specification Number
- S Unnn = S-spec Number
- 'YY Country = Copyright Dates and Country of Origin
- YYWWXXnnn = Alternative Identification Number

Basic Intel 450GX PCIset Identification Information

Product Number	Vendor ID	Device ID	Revision ID	Product Stepping	Kit Steppings	S-Spec	V_{CC}	T_{CASE}	Notes
S82451GX	n/a[1]	n/a[1]	n/a[1]	A1	B0	Q 300	3.3 V ± 5%	0 °C – 85 °C	3
S82451GX	n/a[1]	n/a[1]	n/a[1]	A1	B0	Q 405	3.3 V ± 5%	0 °C – 85 °C	3
S82451GX	n/a[1]	n/a[1]	n/a[1]	A1	B0	S U019	3.3 V ± 5%	0 °C – 85 °C	
S82451GX	n/a[1]	n/a[1]	n/a[1]	A1	C0	Q 300	3.3 V ± 5%	0 °C – 85 °C	3
S82451GX	n/a[1]	n/a[1]	n/a[1]	A1	C0	Q 405	3.3 V ± 5%	0 °C – 85 °C	3
S82451GX	n/a[1]	n/a[1]	n/a[1]	A1	C0	S U055	3.3 V ± 5%	0 °C – 85 °C	
S82452GX	n/a[1]	n/a[1]	n/a[1]	A3	B0	Q 395	3.3 V ± 5%	0 °C – 85 °C	3
FW82452GX	n/a[1]	n/a[1]	n/a[1]	A3	B0	Q 398	3.3 V ± 5%	0 °C – 85 °C	2,3
S82452GX	n/a[1]	n/a[1]	n/a[1]	A3	B0	Q 406	3.3 V ± 5%	0 °C – 85 °C	3
FW82452GX	n/a[1]	n/a[1]	n/a[1]	A3	B0	Q 409	3.3 V ± 5%	0 °C – 85 °C	2,3
S82452GX	n/a[1]	n/a[1]	n/a[1]	A3	B0	S U056	3.3 V ± 5%	0 °C – 85 °C	
FW82452GX	n/a[1]	n/a[1]	n/a[1]	A3	B0	S U057	3.3 V ± 5%	0 °C – 85 °C	2
S82452GX	n/a[1]	n/a[1]	n/a[1]	A4	C0	Q 987	3.3 V ± 5%	0 °C – 85 °C	3
FW82452GX	n/a[1]	n/a[1]	n/a[1]	A4	C0	Q 990	3.3 V ± 5%	0 °C – 85 °C	2,3
S82452GX	n/a[1]	n/a[1]	n/a[1]	A4	C0	Q 992	3.3 V ± 5%	0 °C – 85 °C	3
FW82452GX	n/a[1]	n/a[1]	n/a[1]	A4	C0	Q 995	3.3 V ± 5%	0 °C – 85 °C	2,3
FW82452GX	n/a[1]	n/a[1]	n/a[1]	A4	C0	Q 065	3.3 V ± 5%	0 °C – 85 °C	2,3
S82452GX	n/a[1]	n/a[1]	n/a[1]	A4	C0	SY050	3.3 V ± 5%	0 °C – 85 °C	
FW82452GX	n/a[1]	n/a[1]	n/a[1]	A4	C0	SY053	3.3 V ± 5%	0 °C – 85 °C	2
S82453GX	8086h	84C5h	4	A4	B0	Q 396	3.3 V ± 5%	0 °C – 85 °C	3
S82453GX	8086h	84C5h	4	A4	B0	Q 407	3.3 V ± 5%	0 °C – 85 °C	3
S82453GX	8086h	84C5h	4	A4	B0	S U058	3.3 V ± 5%	0 °C – 85 °C	
S82453GX	8086h	84C5h	5	A5	C0	Q 988	3.3 V ± 5%	0 °C – 85 °C	3

Basic Intel 450GX PCIset Identification Information (Continued)

Product Number	Vendor ID	Device ID	Revision ID	Product Stepping	Kit Steppings	S-Spec	V_{CC}	T_{CASE}	Notes
S82453GX	8086h	84C5h	5	A5	C0	Q 993	3.3 V ± 5%	0 °C – 85 °C	3
S82453GX	8086h	84C5h	5	A5	C0	SY051	3.3 V ± 5%	0 °C – 85 °C	
S82454GX	8086h	84C4h	4	A4	B0	Q 397	3.3 V ± 5%	0 °C – 85 °C	3
FW82454GX	8086h	84C4h	4	A4	B0	Q 399	3.3 V ± 5%	0 °C – 85 °C	2,3
S82454GX	8086h	84C4h	4	A4	B0	Q 408	3.3 V ± 5%	0 °C – 85 °C	3
FW82454GX	8086h	84C4h	4	A4	B0	Q 410	3.3 V ± 5%	0 °C – 85 °C	2,3
S82454GX	8086h	84C4h	4	A4	B0	S U059	3.3 V ± 5%	0 °C – 85 °C	
FW82454GX	8086h	84C4h	4	A4	B0	S U063	3.3 V ± 5%	0 °C – 85 °C	2
S82454GX	8086h	84C4h	6	A6	C0	Q 989	3.3 V ± 5%	0 °C – 85 °C	3
FW82454GX	8086h	84C4h	6	A6	C0	Q 991	3.3 V ± 5%	0 °C – 85 °C	2,3
S82454GX	8086h	84C4h	6	A6	C0	Q 994	3.3 V ± 5%	0 °C – 85 °C	3
FW82454GX	8086h	84C4h	6	A6	C0	Q 996	3.3 V ± 5%	0 °C – 85 °C	2,3
FW82454GX	8086h	84C4h	6	A6	C0	Q 066	3.3 V ± 5%	0 °C – 85 °C	2,3
S82454GX	8086h	84C4h	6	A6	C0	SY052	3.3 V ± 5%	0 °C – 85 °C	
FW82454GX	8086h	84C4h	6	A6	C0	SY054	3.3 V ± 5%	0 °C – 85 °C	2

NOTES:

1. These components are not visible from the PCI bus, and so do not have Vendor, Device, or Revision ID registers.
2. These components have BGA (Ball Grid Array) packaging.
3. These are engineering samples only, provided under an Intel 450GX PCIset loan agreement.

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the Intel 450GX PCIset. Intel intends to fix some of the errata in future steppings of the component(s), and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

X:	Specification Change, Erratum, Specification Clarification, or Documentation Change applies to the given stepping.
Doc:	Intel intends to update the appropriate documentation in a future revision.
Fix:	Intel is investigating the possibility of fixing this erratum in a future stepping of the component(s).
Fixed:	This erratum has been previously fixed.
NoFix:	Intel is currently not investigating a fix for this erratum.
(No mark) or (blank box):	This item is fixed in or does not apply to the given kit stepping.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	B0	C0	Plans	SPECIFICATION CHANGES
1	X	X	Doc	PLLRST pin added
2	X	X	Doc	Valid memory timing parameters
3	X	X	Doc	CMOS overshoot/undershoot specification
4		X	Doc	New features added to PDM register
5		X	Doc	Unused Pentium® Pro Processor Device Log register added
6		X	Doc	Locks to in-line shadowed BIOS not supported in Aliased GAT mode
7		X	Doc	AERR# to BERR# Conversion Enable bit added
NO.	**B0**	**C0**	**Plans**	**ERRATA**
1	X		Fixed	SMRAM addresses may not be decoded correctly
2	X		Fixed	Processor bus ECC error reporting may not record error information for one error
3	X		Fixed	RAW may hang 1:1 or 2:1 interleaved MP systems
4	X		Fixed	Mixed interleave increments may cause data corruption
5	X	X	NoFix	Parity error may occur for ADS# during BINIT#
6	X		Fixed	Configuration cycle to noncompatibility bridge may collide with inbound posted write
7	X		Fixed	Hang with PCI-to-PCI bridges in MP systems
8	X		Fixed	PCI_RST# not asserted asynchronously
9	X		Fixed	Combination of ECC errors may cause one error to be undetected
10	X		Fixed	BERR# to BINIT# conversion may prevent recovery from BINIT#
11	X	X	NoFix	16-Byte read with two ECC errors may not be reported correctly

NO.	B0	C0	Plans	ERRATA
12	X		Fixed	Inbound locked PCI transactions may hang system
13	X		Fixed	Retry on inbound read may corrupt outbound data
14	X		Fixed	ADS# in last clock of BINIT# prevents recovery
15	X		Fixed	Some signals indeterminate after RESET# deassertion
16	X		Fixed	Delayed read from PCI-to-PCI bridge may corrupt data
17	X		Fixed	Page Open Policy of “hold page open” may corrupt write data
18	X	X	NoFix	T_{CASE} drop plus voltage swing may cause DPLL failure
19	X		Fixed	Processor bus ECC signals may be corrupted
20	X		Fixed	IO_REQ# may not be deasserted for BPRI# during GAT, Non-GAT, or APIC Flush mode request
21	X		Fixed	Memory gap reclaiming may corrupt data
22	X		Fixed	RAW may corrupt write data in 1:1 interleaving
23		X	NoFix	Inbound write may be posted too soon after misaligned or multi-Dword cycle
24	X	X	NoFix	IO_REQ# may not be deasserted for BPRI# during GAT mode request
25	X	X	NoFix	BINIT# assertion may cause active RAS# negation
26	X	X	NoFix	SMM address decode limitation for systems supporting greater than 4 Gbytes
27	X	X	NoFix	Mixed configuration and memory accesses may cause system hang
28	X	X	NoFix	Inbound read retry near configuration write can disrupt PCI cycles
29	X	X	NoFix	Hang with zero-byte write followed by a nonzero byte write
NO.	**B0**	**C0**	**Plans**	**SPECIFICATION CLARIFICATIONS**
1	X	X	Doc	Explicit writebacks claimed by 82454GX PB
2	X	X	Doc	Supported configurations for MC row limit register programming
NO.	**B0**	**C0**	**Plans**	**DOCUMENTATION CHANGES**
1	X	X	Doc	Register offset and default value correction
2	X	X	Doc	CMOS definition should be 3.3 V or 5 V
3	X	X	Doc	Pull-up resistor required on PCLK

SPECIFICATION CHANGES

1. PLLRST Pin Added

A PLLRST pin will be added to the definition of each device in the Intel 450GX PCIset. The pin numbers will be assigned as follows:

Device	Pin Number
82454GX PB QFP	301
82454GX PB BGA	A5
82453GX DC QFP	81
82452GX DP QFP	202
82452GX DP BGA	B12
82451GX MIC QFP	42

This signal will be added to the block diagram in Figure 1 of both Chapter 2 and Chapter 3.

Each of the specified PLLRST pins are 5 V tolerant signals.

The signal will be added to Chapter 2, Section 1.4 and to Chapter 3, Sections 1.1, 1.2 and 1.3 as signal "PLLRST", type "I, CMOS", and described as "This pin must be driven high for at least 2 clocks to reset the internal DPLL (Digital Phase Lock Loop). The DPLL should be reset after (or until) the clock input pins are stable at their final operating frequency. This pin does not have an edge rate requirement."

The following sentences will be added to Chapter 2, Section 3.7.2 and Chapter 3, Section 3.4: "The PLLRST pin must be driven high for at least 2 clocks to reset the internal DPLL. The DPLL should be reset after (or until) the clock input pins are stable at their final operating frequency."

Chapter 4 will be updated to include this pin information throughout.

2. Valid Memory Timing Parameters

The following is a list of timing values which have been validated by Intel. The list is the result of applying the rules set forth in the *Intel 450KX/GX PCIset* datasheet plus a set of filters to eliminate settings that Intel believes would not or could not be used in practice. Note that OEMs must still ensure that the timing parameters used meet the timing constraints for their system design, applicable clock rates, and supported DRAM speeds. See below for a list of acronyms used in the table.

RCD = 3, RCAD = 2, and CSR = 1 for all setting options listed below.

						1:1			2:1			4:1		
LWC	**RASPW**	**CAH**	**RCAS**	**WCAS**	**RP**	**CP**	**RBD**	**ACh**	**CP**	**RBD**	**ACh**	**CP**	**RBD**	**ACh**
2	5	1	2	2	3	1	2	2814	2	1	2834	1	0	2814
2	5	1	3	2	3	1	3	2914	1	1	2914	1	0	2914
2	5	1	3	3	3	1	3	2954	1	1	2954	1	0	2954
2	6	1	2	2	3	1	2	3014	2	1	3034	1	0	3014
2	6	1	3	2	3	1	3	3114	1	1	3114	1	0	3114
2	6	1	3	2	4	1	3	3115	1	1	3115	1	0	3115
2	6	1	3	3	3	1	3	3154	1	1	3154	1	0	3154
2	6	1	3	3	4	1	3	3155	1	1	3155	1	0	3155
2	6	2	3	2	3	1	3	3514	1	1	3514	1	0	3514
2	6	2	3	2	4	1	3	3515	1	1	3515	1	0	3515
2	6	2	3	3	3	1	3	3554	1	1	3554	1	0	3554
2	6	2	3	3	4	1	3	3555	1	1	3555	1	0	3555
2	6	2	4	3	3	1	4	3654	2	2	3674	1	0	3654
2	6	2	4	3	4	1	4	3655	2	2	3675	1	0	3655
3	5	1	2	2	3	2	3	4834	2	1	4834	1	0	4814
3	5	1	3	2	3	2	4	4934				1	0	4914
3	5	1	3	3	3	2	4	4974				1	0	4954
3	6	2	3	2	3	2	4	5534				1	0	5514
3	6	2	3	2	4	2	4	5535				1	0	5515
3	6	2	3	3	3	2	4	5574				1	0	5554
3	6	2	3	3	4	2	4	5575				1	0	5555
3	6	2	4	3	3	2	5	5674	2	2	5674	1	0	5654
3	6	2	4	3	4	2	5	5675	2	2	5675	1	0	5655
3	6	2	4	4	4	1	4	5695	2	2	56B5	1	0	5695

RCD = 3, RCAD = 2, and CSR = 2 for all setting options listed below.

						1:1			2:1			4:1		
LWC	**RASPW**	**CAH**	**RCAS**	**WCAS**	**RP**	**CP**	**RBD**	**ACh**	**CP**	**RBD**	**ACh**	**CP**	**RBD**	**ACh**
3	6	2	3	4	3	1	3	D594	1	1	D594	1	0	D594
3	6	2	4	3	4	2	5	D675	2	2	D675	1	0	D655
2	6	2	3	3	3	1	3	B554	1	1	B554	1	0	B554

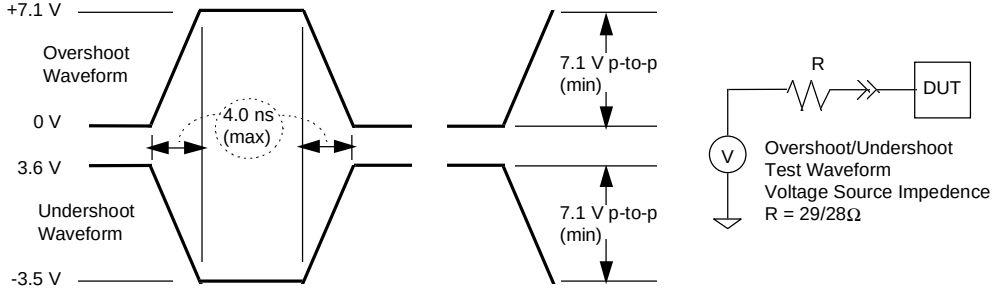
NOTE:
All above values are in number of cycles, not actual bit settings, except ACh (which is the actual bit setting, in hexadecimal).

RCD: RAS# to CAS# Delay: bits 3:2 of the Memory Timing Register (AC-AFh).
RCAD: RAS# to Column Address Delay: bit 4 of the Memory Timing Register (AC-AFh).
CSR: CAS# Setup to RAS# for CAS# before RAS# refresh: bit 15 of the Memory Timing Register (AC-AFh).
LWC: Last Write to CAS#: bits 14:13 of the Memory Timing Register (AC-AFh).
RASPW: RAS# Pulse Width: bits 12:11 of the Memory Timing Register (AC-AFh).
CAH: Column Address Hold Time: bit 10 of the Memory Timing Register (AC-AFh).
RCAS: Read CAS# Pulse Width: bits 9:8 of the Memory Timing Register (AC-AFh).
WCAS: Write CAS# Pulse Width: bits 7:6 of the Memory Timing Register (AC-AFh).
RP: RAS# Precharge Time: bits 1:0 of the Memory Timing Register (AC-AFh).
CP: CAS# Precharge Time: bit 5 of the Memory Timing Register (AC-AFh).
RBD: Read Burst Delay: bits 2:0 of the Command Register (4C-4Fh).
ACh: Actual hexadecimal value programmed into bits 15:0 of the Memory Timing Register (AC-AFh).

3. CMOS Overshoot/Undershoot Specification

The following will be added to Chapter 4, Section 2.4, “Intel 450KX/GX Undershoot Specification,” in the *Intel 450KX/GX PCIset* datasheet, and the section will be retitled “Intel 450KX/GX Overshoot/Undershoot Specifications.”

The 3.3 V tolerant CMOS signals of the processor bus allow for the following maximum AC waveforms:



Average duty cycle of 17.6%

Note: This test covers the AC operating conditions only.

4. New Features Added to PDM Register

- GAT/non-GAT Optimization Changes: the optimizations previously associated with non-GAT mode (e.g., less frequent dynamic disabling of inbound write posting) have been added to GAT mode. Thus, EISA performance should see non-GAT-like performance while running in full GAT mode. In addition, support was added for Aliased GAT mode (i.e., putting the 82454 PB in non-GAT mode with the south bridge in GAT

mode). This mode allows the inbound write posting optimization to take effect, in addition to allowing the deassertion of BPRI# between requests. Bit 3 of the PCI Decode Mode register at offset 48h is used for this purpose; setting this bit to '1' enables Aliased GAT mode. Table 1 details the optimizations.

Table 1. GAT/Non-GAT Optimization Changes in C0 82454GX PB Silicon

Operation	A2 and B0 Steppings	C0 Stepping
82454GX PB receiving GAT mode requests, South bridge in GAT mode	Inbound write posting dynamically disabled, BPRI# held asserted	Inbound write posting kept enabled, BPRI# held asserted
82454GX PB receiving non-GAT mode requests (Aliased GAT mode), South bridge in GAT mode, Both sideband signals aliased to FLUSHBUF	Inbound write posting kept enabled, BPRI# held asserted	Inbound write posting kept enabled, BPRI# deasserted after MEMACK# Locks to shadowed BIOS not supported
82454GX PB receiving any sideband requests, South bridge in non-GAT mode	Not supported	Not supported

- BPRI# Optimization Disable: By setting bit 4 of the PCI Decode Mode register to a "0", this optimization is enabled, allowing BPRI# to be deasserted prior to the response phase of a PB initiated cycle. This is the default state. Writing a "1" to this register bit disables the optimization, ensuring that the PB will keep BPRI# asserted until the response phase for its previous cycle. This forces serialization of inbound requests, which is necessary in systems where inbound read prefetching can occur to a device that can issue a retry or hard fail response. Note that another PB device can issue such a response.
- Livelock Prevention Disable: The workaround for Intel 450GX Erratum 7 has been incorporated internally into the C0 stepping of the 82454GX PB. A mechanism is provided to disable this workaround, by setting bit 5 of the PCI Decode Mode register at offset 48h to a '1'.
- Traffic Priority Mode: This bit can be asserted to override the priority normally given to outbound requests. If this bit is zero (the default state), then non-GAT mode is entered for 64 clocks after an inbound request is retried eight times. Setting bit 6 of the PCI Decode Mode register at offset 48h to '1' disables this new feature. Intel recommends that BIOS override the default value and set this bit to '1' in systems with PCI Local Bus Specification 2.1 compliant PCI-to-PCI bridges which may experience extremely heavy inbound traffic; otherwise, temporary processor read starvation could result, reducing performance. Note that in other systems, especially those which experience heavy outbound traffic, this bit should remain at the default setting of '0'; otherwise, inbound read starvation may result, also impacting performance.

Configuration Register	Address Offset	Default Value	Notes
82454GX			
PCI Decode Mode	48h	06h	Bit 6: Traffic priority mode Bit 5: Livelock prevention disable Bit 4: BPRI# optimization disable Bit 3: Aliased GAT mode enable

5. Unused Pentium® Pro Processor Device Log Register Added

A new 16-bit register, called the “Unused Pentium Pro Processor Device Log,” has been added to the 82454GX PB at address offset CCh. This register should be programmed by BIOS to reflect the populated and unpopulated device IDs between 16 and 31 on the host bus (bus 0). The BIOS algorithm should perform a scan of the range from 16 to 31 on bus 0, detect each location that returns all 1’s (indicating an unpopulated device ID) from offset 00h in their configuration space, and set the corresponding bit in 82454GX PB configuration register CCh. (Bits corresponding to populated device ID's must remain “0” (deasserted). Bit *n* of this register corresponds to device ID *n* + 16.) Previously, all reads to locations which return all 1’s from offset 00h generated by further PCI scans would have timed-out (been claimed by the watchdog timer in the 82454GX PB); the new register will force the 82454GX PB to claim these transactions via positive decode and forward them to the PCI bus, where they will result in a PCI master abort. This will provide much faster missing device access handling than the previous watchdog timer mechanism in the 82454GX PB (which will still be used if this register is left with its default value of 00h). The new treatment of these cycles is necessary to avoid a potential for loss of read data in the presence of PCI 2.1 compliant PCI-to-PCI bridges during PCI device scans (see Intel 450GX Erratum 16).

Configuration Register	Address Offset	Default Value	Notes
82454GX			
Unused Pentium® Pro Processor Device Log	CCh	00h	Bit *n* corresponds to device ID *n* + 16. 1 = device ID is unpopulated (as determined by a scan of bus 0). 0 = device present at ID *n* + 16.

6. Locks to In-Line Shadowed BIOS Not Supported in Aliased GAT Mode

As described in Intel 450GX Specification Change 4, *New Features Added to PCM Register*, bit 3 of the PCI Decode Mode register in the 82454GX PB is used to put the PCI Bridge into Aliased GAT mode. Section 3.3, “PCI Bus Interface,” of the *Intel 450KX/GX PCIset* datasheet describes the 82454GX PB’s support for host bus locks. The following information will be added to this section:

Locked transactions targeting in-line shadowed BIOS regions using conventional write protection (i.e., read-only to memory and write only to the PB) are not supported if Aliased GAT mode is enabled. If locked transactions must be issued to BIOS with Aliased GAT mode enabled, then the relevant BIOS region must be either:

- Mapped read/write in memory (forgoing write protection),
- Read only in memory, write only to a third party device, or
- Read only in memory, allowing the PB watchdog timer to time out write transactions.

7. AERR# to BERR# Conversion Enable Bit Added

Bit 1 of the PB Extended Error Reporting Command register (EXERRCMD) at offset C0h is Reserved for Intel 450GX PCIsets of B0 stepping; for the C0 stepping of the Intel 450GX PCIset, this bit can be set to ‘1’ to enable the assertion of the BERR# signal upon detection of an assertion of AERR#.

Configuration Register	Address Offset	Default Value	Notes
82454GX			
PB Extended Error Reporting Command	C0h	0000 0010h	Bit 1: AERR# to BERR# enable.

ERRATA

1. SMRAM Addresses May Not Be Decoded Correctly

PROBLEM: While executing in SMM (System Management Mode), certain sequences of transactions may allow the CAS# signal to be asserted without a corresponding RAS# signal during a memory access to SMRAM. The sequences must be pipelined SMRAM requests (with the IOQ depth set to 8) as follows:

- An SMRAM request which opens a page (i.e., the transaction address accesses a block of DRAM with a new row address).
- An SMRAM request which is a page hit.
- Another SMRAM request which is a page hit.

The address phase of the third request must occur during the first clock of CAS# assertion for the second request to encounter this erratum. A second sequence is:

- An SMRAM request which is a page hit.
- Another SMRAM request whose ADS# assertion comes 5 or 6 clocks later than the ADS# assertion for the previous transaction, and which is also a page hit.

IMPLICATION: If these sequences occur while in SMM, data corruption may result.

WORKAROUND: This erratum can be avoided in the Intel 450GX PCIset by setting the IOQ depth to 1, thus preventing transactions from being pipelined together.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

2. Processor Bus ECC Error Reporting May Not Record Error Information for One Error

PROBLEM: If a line transaction returns data to the processor bus with an UNC or SBC ECC error detected on chunk 0, it will be reported correctly. If, however, an error of the opposite type (SBC vs. UNC) is detected on chunk 1 or chunk 2, this error will not be reported in the error reporting registers. However, an SBC error will be detected and corrected appropriately by the 82452GX DP, and an UNC error will cause BERR# to be driven (assuming this feature is enabled).

IMPLICATION: After this specific sequence of errors, one error will not be reported properly when detected in combination with other errors. This will result in an error not being logged into the error reporting registers of the 82453GX MC. However, this erratum does not affect the detection and correction of SBC errors or the detection of UNC errors.

WORKAROUND: None identified.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

3. RAW May Hang 1:1 or 2:1 Interleaved MP Systems

PROBLEM: If Read-Around-Write (RAW) is enabled in the 82453GX MC, there is a potential for two reads being assigned to the same internal data buffer, causing the system to hang. The following transactions must be issued during a snoop stall for a previous read for this erratum to occur:

1. A line read transaction
2. A 0-byte length read transaction
3. An explicit writeback transaction
4. A line read transaction

Transactions 1 and 4 may target the same buffer in this situation.

IMPLICATION: Systems which use 4:1 interleaving and uniprocessor systems will not be affected by this erratum. Other systems will hang if this sequence occurs during a snoop stall.

WORKAROUND: Do not enable RAW in the 82453GX MC in a 1:1 or 2:1 interleaved MP configuration.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

4. Mixed Interleave Increments May Cause Data Corruption

PROBLEM: If some DRAM module sizes are mixed together, some Intel 450GX PCIset-based systems may corrupt user or system data, resulting in incorrect calculations and/or system failure. This can only occur if:

- Interleave increments containing 8-Mbytes or 32-Mbytes of memory exist in conjunction with interleave increments which contain other amounts of memory, or
- One or more interleave increments have 8- or 32-Mbytes of memory, and there are no DRAM modules in the first row (row 0) of the memory subsystem.

Note that in systems with only one row of memory in use (i.e., 2 SIMMs in 1:1 interleave, 4 SIMMs in 2:1 interleave, or 8 SIMMs in 4:1 interleave), or with all SIMMs or DIMMs the same size and configuration, only one interleave increment size is possible (since all memory in the same row must be the same size), so this erratum will not affect the system.

Also note that the BIOS of some (usually server) platforms may automatically downsize or eliminate a row of memory if a bad DRAM module is detected in that row. It is possible for this alteration of memory sizes to result in the system entering a vulnerable configuration (if memory is downsized to interleave increments of 8 or 32 Mbytes, or if row 0 is removed from the configuration). This can occur even with logically double-sided DRAM modules, which otherwise always have the same size interleave increments across their two rows.

IMPLICATION: Some systems only support one row of memory (i.e., 1:1 interleaving with 2 SIMMs, 2:1 interleaving with 4 SIMMs, or 4:1 interleaving with 8 SIMMs). In these systems, only one interleave increment size is possible (since all memory in the same row must be the same size), so they are not affected by this erratum. In systems which support two or more rows of memory (other than systems which support two rows of double-sided SIMM DRAM only), one must be careful not to mix DRAM of certain sizes. If there are 8 or 32 Mbytes of DRAM in any interleave increment, all other interleave increments must have the same amount of DRAM, and row 0 must be populated with DRAM modules to avoid data corruption due to this erratum.

The chart below gives the interleave increments for some common memory technologies:

SIMMs	DRAM	Technology	Interleave Increment
Two 4-Mbyte, single-sided	1-Mbit x 4	4-Mbit	8 Mbytes*
Two 8-Mbyte, double-sided	1-Mbit x 4	4-Mbit	8 Mbytes*
Two 8-Mbyte, single-sided	2-Mbit x 8	16-Mbit	16 Mbytes
Two 16-Mbyte, double-sided	2-Mbit x 8	16-Mbit	16 Mbytes
Two 16-Mbyte, single-sided	4-Mbit x 4	16-Mbit	32 Mbytes*
Two 32-Mbyte, double-sided	4-Mbit x 4	16-Mbit	32 Mbytes*
Two 32-Mbyte, single-sided	8-Mbit x 8	64-Mbit	64 Mbytes
Two 64-Mbyte, double-sided	8-Mbit x 8	64-Mbit	64 Mbytes
Two 64-Mbyte, single-sided	16-Mbit x 4	64-Mbit	128 Mbytes
Two 128-Mbyte, double-sided	16-Mbit x 4	64-Mbit	128 Mbytes

DIMMs	DRAM	Technology	Interleave Increment
One 8-Mbyte, single-sided	1-Mbit x 4	4-Mbit	8 Mbytes*
One 16-Mbyte, double-sided	1-Mbit x 16	16-Mbit	8 Mbytes*
One 16-Mbyte, single-sided	2-Mbit x 8	16-Mbit	16 Mbytes
One 32-Mbyte, double-sided	2-Mbit x 8	16-Mbit	16 Mbytes
One 32-Mbyte, single-sided	4-Mbit x 4	16-Mbit	32 Mbytes*
One 64-Mbyte, double-sided	4-Mbit x16	64-Mbit	32 Mbytes*
One 64-Mbyte, single-sided	8-Mbit x 8	64-Mbit	64 Mbytes
One 128-Mbyte, double-sided	8-Mbit x 8	64-Mbit	64 Mbytes
One 128-Mbyte, single-sided	16-Mbit x 4	64-Mbit	128 Mbytes

NOTE:
*To avoid corruption of data, do not mix 8-Mbyte or 32-Mbyte interleave increments with other increment sizes (including each other). If 8-Mbyte or 32-Mbyte interleave increments are used (exclusively), ensure that row 0 is populated with DRAM modules.

WORKAROUND: When upgrading memory:

- In systems which support multiple rows of memory, always populate row 0 with DRAM modules.
- Exercise caution when using 4-Mbyte or 16-Mbyte SIMMs (single- or double- sided), or when using 8-Mbyte or 32-Mbyte DIMMs. Note that exclusively using DRAM modules which are all the same size will always avoid this erratum.
- When writing a BIOS for an Intel 450GX-based system, the memory configurations susceptible to this erratum should be detected and flagged to alert the user of the problem. Ensure that such detection mechanisms are placed after any bad DRAM detection mechanisms so that vulnerable configurations are detected after memory downsizing has occurred.
- Refer to your system documentation, or contact your system vendor, for details on your system's support for the various interleaving modes and DRAM styles.

See the white paper *Mixing DRAM Sizes with the 82450KX/GX PCIset* on Intel's World Wide Web site at URL http://www.intel.com/procs/support/ppro/450kxgx.htm for more information.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

5. Parity Error May Occur for ADS# During BINIT#

PROBLEM: If BINIT# is asserted due to some catastrophic system event, the system will reset the bus and attempt to recover. If, however, ADS# is asserted for a request during the BINIT#, some of the signals associated with the request may not be driven when they should be. This results in an incorrect request parity and an assertion of AERR# 2 clocks after the BINIT# is complete, which is not a valid error phase.

IMPLICATION: A second (spurious) AERR# will be observed, resulting in a spurious SERR#. No data loss or hang is associated with this erratum, just an extra assertion of AERR# after detection of a catastrophic bus condition.

WORKAROUND: None identified.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

6. Configuration Cycle to Noncompatibility Bridge May Collide with Inbound Posted Write

PROBLEM: It is possible for a noncompatibility 82454GX PB (nc82454) in a dual-bridge system to respond incorrectly to a CONFDATA cycle. This is due to a boundary condition in the 82454GX PB which may result in the nc82454's CONFADDR register not being updated for a previous CONFADDR cycle. This, in turn, may result in the nc82454 either claiming a subsequent CONFDATA cycle intended for another PCI device, or not responding to a subsequent CONFDATA cycle intended for it. This boundary condition arises only when configuration cycles are directed at the nc82454 during inbound posted write traffic.

IMPLICATION: This erratum may result in corrupted configuration space of bridges or PCI devices in dual-82454GX PB systems, possibly resulting in assertion of BINIT#.

WORKAROUND: Use an IOQ depth of 1 on dual-82454GX PB systems. This will prevent the pipelining necessary for the inbound posted write and outbound configuration cycle to collide. If an IOQ depth of 8 is desired, do not enable inbound write posting in the noncompatibility 82454GX PB. In this case, BIOS level and operating-system level workarounds (if present) will reenable inbound posting in the noncompatibility 82454GX PB and work around the erratum via BIOS code and OS software. The OS workaround will be incorporated into future revisions of some operating systems; contact your OS vendor for release details. These workarounds require that:

1. There are two 82454GX PB's in the system of stepping B0 or earlier.
2. Inbound write posting is enabled in the compatibility 82454GX PB.

If these conditions are met, the operating system and BIOS must do the following whenever configuration cycles are issued:

1. In a loop, read the Vendor ID from the nc82454's configuration space, until it matches the known value. When this occurs, the OS is pointing at the nc82454's configuration space.
2. In a loop, read the PCI Read/Write Control register. When this value no longer matches the Vendor ID, the OS is pointing at the correct register in configuration space.
3. Write a value into the PCI Read/Write Control register which disables inbound write posting.
4. Issue the configuration cycles as originally intended.
5. Write a value into the nc82454's PCI Read/Write Control register to reenable inbound write posting.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

7. Hang with PCI-to-PCI Bridges in MP Systems

PROBLEM: If a PCI-to-PCI bridge is present in a system, either on a card or native on the motherboard, a "livelock" hang condition may be possible if pipelined transactions are allowed (i.e., the IOQ depth is set to 8). This may happen if the following events occur:

1. An ordering event (such as I/O reads, and I/O writes for some components) from one processor is followed by a second such event from another processor. These outbound events are directed through the 82454GX PB, and dynamically disable inbound write posting.
2. The PCI-to-PCI bridge is attempting to perform an inbound write through the 82454GX PB.

If this situation arises, the PCI-to-PCI bridge will retry the outbound transactions, but must follow ordering constraints on the I/O operations. The outbound transactions are then reissued on the processor bus faster than the 82454GX PB can prepare to service the inbound write request from the PCI-to-PCI bridge. Consequently, the inbound write cannot complete, and the I/O transactions are continuously retried and reissued on the processor bus, resulting in a "livelock" hang with neither side making forward progress.

IMPLICATION: PCI-to-PCI bridges present in an MP system may cause the system to hang.

WORKAROUND: Set the IOQ depth to 1. If this is not acceptable (multiprocessor systems may see significant performance degradation with this setting), a hardware workaround may be implemented using a programmable logic component. This workaround allows the outbound transactions to complete after they are retried by the PCI-to-PCI bridge, by putting the 82454GX PB in non-GAT (as opposed to GAT, or Guaranteed Access Time, mode) for 64 processor clocks after an outbound request is retried once, or after an inbound request is retried 8 times.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

8. PCI_RST# Not Asserted Asynchronously

PROBLEM: The 82454GX PB requires a valid BCLK to assert the PCI_RST# signal, due to clocked logic in the assertion paths of these signals.

IMPLICATION: This signal is not asynchronous, as was intended.

WORKAROUND: Ensure a valid BCLK is provided before attempting to reset the PCI bus.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

9. Combination of ECC Errors May Cause One Error to Be Undetected

PROBLEM: The 82452GX DP may not detect a memory ECC error during pipelined line reads, when there are multiple SBC and/or UNC errors across cache line boundaries. The error combinations which are affected are as follows:

1. An SBC error will detected and corrected, but not reported to the 82453GX MC, if it occurs on chunk 3 of the first line read when there is an UNC error on chunk 2 of the first line read and an SBC on chunk 0 of the second line read. In this case, no error record will exist for the first SBC, but data will not be corrupted.
2. An UNC error will be detected by the 82452GX DP but not reported to the 82453GX MC, if it occurs on chunk 3 of the first line read when there is an SBC error on chunk 2 of the first line read and either type of error on chunk 0 of the second line read. In this case, no error record will exist for the first UNC, and BERR# will not be driven if the third error is an SBC.

Note that these are the only combinations of errors affected by this erratum; other combinations of errors will all be detected (including cache lines with **more** errors than specified), and any subsequent UNC errors which occur will cause BERR# to be driven by the 82453GX MC (assuming this feature is enabled).

IMPLICATION: An error will not be detected if it occurs with these very specific combinations, possibly resulting in corrupted data. The other errors in these combinations, as well as all other errors which occur on other transactions which do not fall within this pattern, will be detected correctly.

WORKAROUND: None identified.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

10. BERR# to BINIT# Conversion May Prevent Recovery From BINIT#

PROBLEM: If an error on a bus split operation occurs which causes an assertion of both BERR# and BINIT#, and BERR# to BINIT# conversion is enabled in the 82454GX PB, BINIT# will be driven a second time, 2 bus clocks after the first completes. At this time, another 450GX agent may still be driving BNR# for the first BINIT#, and other devices may then try to drive BNR# for the second BINIT#. This results in the system being unable to recover successfully from the BINIT#, hanging the system.

IMPLICATION: After a double assertion of BINIT# due to detection of a catastrophic error, the bus may not be reset properly, resulting in a system hang.

WORKAROUND: Do not enable BERR#-to-BINIT# conversion in the 82454GX PB. BERR#-to-SERR# conversion can be used instead.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

11. 16-Byte Read with Two ECC Errors May Not Be Reported Correctly

PROBLEM: If a line read contains either type of error in chunk 3, and the line read is followed by a 16-byte read which has either an SBC error in chunk 0 and an UNC error in chunk 1 or an UNC error in chunk 1 and an SBC in chunk 0, a stale error record will be left in the error reporting registers which does not correspond to the last errors detected. All errors in this combination will be detected, however, and BERR# will be driven for UNC errors (assuming this feature is enabled). Note that neither the Pentium Pro processor nor any 450GX PCIset agent will generate 16-byte reads; only systems containing third-party bus agents may be affected by this case.

IMPLICATION: Under some circumstances, some errors will not be reported properly when detected in combination with other errors. This may result in an error not being logged into the error reporting registers of the 82453GX MC at all, or it may result in incorrect error information being logged. This erratum does not affect the detection and correction of SBC errors or the detection of UNC errors.

WORKAROUND: Do not use third-party agents which issue 16-byte reads.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

12. Inbound Locked PCI Transactions May Hang System

PROBLEM: This erratum manifests itself in the following sequence:

1. A locked read request is issued on the PCI bus, and targets the processor bus. The 82454KX PB asserts DEVSEL#.
2. The transaction is entered into the 82454GX PB's request queue, which then asserts BPRI#.
3. Before the ADS# for this transaction occurs, a pipelined retry response is received for the previous request.
4. ADS# is asserted on the processor bus for the locked read. In the sequence which causes the system to hang, the 82454GX PB confuses the retry for the previous transaction with a retry for this locked read. LOCK# is then asserted for only one clock, but the PCI LOCK# signal remains asserted.
5. The locked read's response phase completes on the processor bus and TRDY# is asserted on the PCI bus, completing the first part of the lock. Note that BPRI# is still asserted.
6. The locked write which is the second half of the inbound lock is issued on the PCI bus, and the 82454KX PB asserts DEVSEL#.
7. The locked write transaction is entered into the queue. However, the 82454GX PB cannot issue the transaction on the processor bus until PCI LOCK# is deasserted. The PCI bus cannot deassert PCI LOCK# until the write completes. This deadlock results in the system hanging.

IMPLICATION: If a PCI device driver allows the device to issue a locked transaction targeting the processor bus, and the IOQ depth is set to 8, a retry response for a transaction may cause the system to hang.

WORKAROUND: Drivers that are capable of issuing inbound locked PCI transactions are very rare. When using these drivers in a system, use an IOQ depth of 1.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

13. Retry on Inbound Read May Corrupt Outbound Data

PROBLEM: If an inbound read is retried by a third-party agent or second 82454GX PB (in a peer-to-peer PCI transaction), and DBSY# is still asserted from a normal data response for a pipelined read directed through the 82453GX MC, an outbound write can be issued while the outbound data buffer and status pointer are out of synch. This results in incorrect data being used for the outbound write.

IMPLICATION: Using third-party devices which issue pipelined retry responses or drivers which cause PB-to-PB traffic may result in data corruption. Intel has not currently identified any software which is capable of causing PB-to-PB traffic in a dual-82454GX PB system.

WORKAROUND: If third-party devices which issue retry responses are used in the system, or if drivers are used in a dual-82454GX PB system which allow PB-to-PB traffic, use an IOQ depth of 1. Alternatively, a third-party device can delay its retry response until DBSY# is deasserted from the previous response. Also, ensure that drivers which support peer-to-peer PCI transactions only do so for devices under the same 82454GX PB.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

14. ADS# in Last Clock of BINIT# Prevents Recovery

PROBLEM: If an ADS# assertion for a transaction targeting the 82453GX MC occurs during the last clock of an assertion of BINIT#, the ADS# will not be canceled correctly. The system will hang instead of recovering from the catastrophic condition which resulted in the BINIT# assertion.

IMPLICATION: BINIT# is only asserted upon detection of a catastrophic bus condition. If this occurs, the system may not generally be able to recover. This erratum decreases the possibility of being able to recover from this condition, but does not cause any additional incorrect behavior.

WORKAROUND: None identified.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

15. Some Signals Indeterminate After RESET# Deassertion

PROBLEM: There exists a window of a single bus clock after RESET# has been deasserted where simulation has shown a possibility of the 82453GX MC sending a spurious command via the MEM_CMD# and/or MIC_CMD# signals to the 82452GX DP and/or 82451GX MICs.

IMPLICATION: If this were to occur, it might result in the 82452GX DP and/or 82451GX MICs attempting to execute a false command, most likely resulting in a system hang on startup. However, Intel has not identified any silicon 450GX component that has ever exhibited this condition, either under test or in actual systems; the MEM_CMD# and MIC_CMD# signals have always been observed to come up in a deterministic fashion.

WORKAROUND: None identified.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

16. Delayed Read from PCI-to-PCI Bridge May Corrupt Data

PROBLEM: There exists a boundary condition in the 82454GX PB which may cause corruption of read data in an MP system, if the following sequence of events occurs:

1. A processor performs a destructive read directed towards a device below a PCI 2.1 Local Bus Specification compliant PCI-to-PCI bridge. The bridge delays the read and the 82454GX PB gives a retry response to the transaction. When this occurs, the PCI-to-PCI bridge starts a timer. The PCI-to-PCI bridge discards the read data from the target device if this timer expires.
2. A different processor initiates a configuration access (read or write) to a nonexistent device with a device ID of greater than 15. These accesses are allowed to time out on the processor bus (and are claimed by the 82454GX PB's watchdog timer), and are not forwarded to the PCI bus by the 82454GX PB.
3. Another processor issues a nonposted write to the 82454GX PB, or an inbound request targets the 82454GX PB before the first processor can retry the destructive read. If this occurs, the read cannot be forwarded to the PCI bus until the 82454GX PB's watchdog timer expires.

The PCI-to-PCI bridge's timer will expire after 2^{15} PCI bus clocks (which is less than the 82454GX PB's minimum watchdog timer value of 1.5 ms). After this, it will discard the data, as required by the PCI 2.1 Local Bus Specification. Since the read was destructive, the data is lost.

IMPLICATION: This erratum would typically occur when a driver is scanning for populated PCI device numbers in the system. If delayed reads are enabled in the PCI-to-PCI bridge, data corruption may result.

WORKAROUND: Do not enable delayed reads in PCI 2.1 Local Bus Specification compliant PCI-to-PCI bridge devices.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

17. Page Open Policy of "Hold Page Open" May Corrupt Write Data

PROBLEM: If Read-Around-Write (RAW) is enabled, the Page Open Policy is set to "hold page open," and the IOQ depth is set to 8, there is a potential for data corruption after a configuration cycle is issued during a sequence of memory transactions, as follows:

1. A read from memory.
2. A write to the Configuration Address register.
3. A write to memory which is a page miss.
4. A read from memory which is a page hit (relative to transaction #1).

Or,

1. A read from memory with an ECC error logged.
2. A write to memory which is a page miss.
3. A read from memory which is a page hit (relative to transaction #1).

These sequences, with the configuration detailed above, will cause the data for the write to memory to be corrupted.

IMPLICATION: With all of these features enabled, data corruption may occur, resulting in unpredictable system failure.

WORKAROUND: Use the default Page Open Policy (close page). Disabling RAW and ERAW or using an IOQ depth of 1 will also prevent this erratum, but may have a larger impact on performance.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

18. T_{CASE} Drop Plus Voltage Swing May Cause DPLL Failure

PROBLEM: Analysis of the DPLL (Digital Phase Lock Loop) units of the Intel 450GX PCIset components has shown that a DPLL failure can occur during certain changes in temperature and/or voltage within the Intel 450GX PCIset component specification, resulting in a loss of DPLL functionality for between 2 and 500 bus clocks.

The current specification states that the Intel 450GX PCIset is operational over a T_{CASE} range of 0 - 85 °C and a V_{CC} range of 3.3 V ± 5%.

After a device has undergone a hard reset of the DPLL (via the PLLRST pin), a drop in T_{CASE} accompanied by an increase in V_{CC} may cause this erratum to occur. The magnitude of the temperature drop and supply voltage increase required to cause this failure is graphed below:

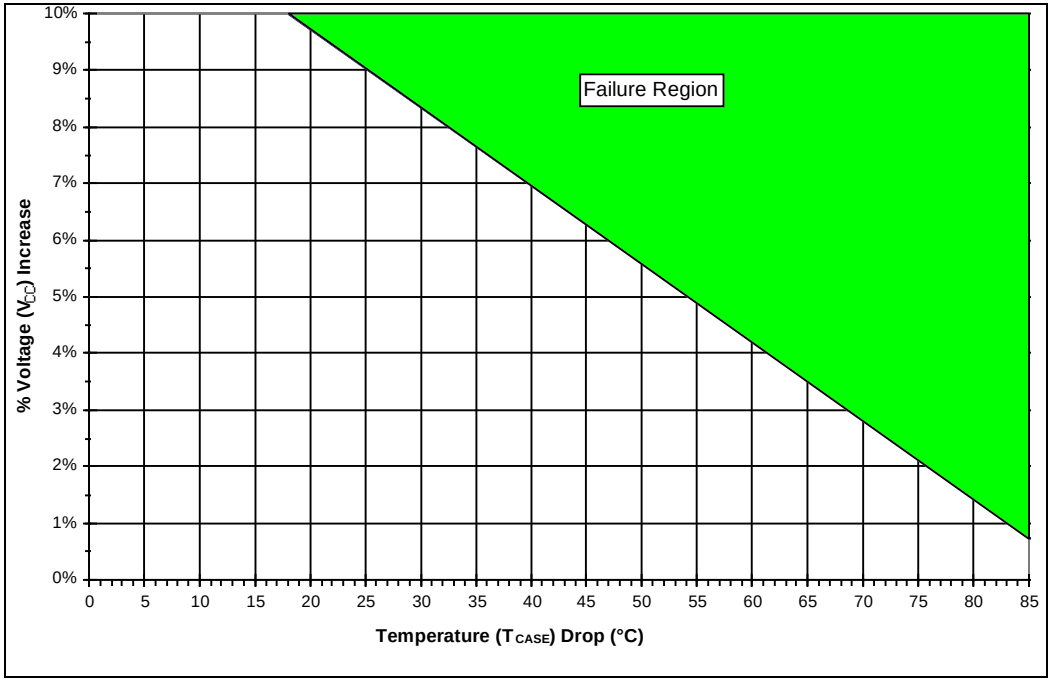


Figure 1. V_{CC} Increase vs. T_{CASE} Drop for DPLL Failure (Worst Case)

IMPLICATION: If the T_{CASE} of any Intel 450GX PCIset component is allowed to decrease by more than 18 °C after the point at which DPLL lock is obtained after a DPLL hard reset, a positive voltage swing may cause the component to lose its internal clock for 2 - 500 processor bus clocks. This may result in a system hang, lost data, or other unpredictable system failure (note that if the component is not processing commands or data for the time during which the internal clock is lost, no failure will be observed). The larger the temperature drop and/or voltage swing, the more likely the failure.

If V_{CC} swings from 3.3 V -5% to 3.3 V +5%, and T_{CASE} does drop more than 18 °C past the temperature at which the DPLL was reset, this erratum may occur. Similarly, if T_{CASE} transitions from 85 °C (at DPLL reset time) to 0 °C, a swing in V_{CC} of more than 0.5% may cause this erratum. Thus, maintaining a moderately constant T_{CASE} and V_{CC} will prevent this erratum, as per the graph above.

WORKAROUND: Ensure that the DPLL reset occurs during a period where the T_{CASE} is low and/or the V_{CC} is high relative to normal operational conditions (e.g., if the system is running at a high temperature and is powered down, allow it to cool before powering up again). Alternately, ensure that the system meets a restricted specification for changes in T_{CASE} and V_{CC}.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

19. Processor Bus ECC Signals May Be Corrupted

PROBLEM: The processor bus ECC signals issued by the 82454GX PB may not contain correct ECC information, when processor bus ECC is enabled, the IOQ depth is 8, and inbound posting (PCI bus to processor bus) is enabled. This erratum occurs on all Intel 450GX components; Intel has observed it more frequently at low voltage and high temperature.

IMPLICATION: With an IOQ depth of 8 and inbound posting enabled, processor bus ECC will not be reliable.

WORKAROUND: Any one of the following three workarounds may be implemented to prevent this erratum:

1. Disable processor bus ECC in all processor bus agents. Memory bus ECC is not affected and can remain enabled. To disable processor bus ECC and keep memory bus ECC enabled, use the following processor bus ECC settings:
   - Data Error Checking Enable:
     Pentium® Pro processor, EBL_CR_POWERON MSR, bit 1 = 0 (disabled).
   - Logging Uncorrectable Errors on the Host Data Bus Enable:
     82453GX MC, register offset C4-C5h, bit 7 = 0 (disabled).
   - Logging Correctable Errors on the Host Data Bus Enable:
     82453GX MC, register offset C4-C5h, bit 8 = 1 (enabled).
   - Single-bit Error Correcting of Host Data Bus Enable:
     82453GX MC, register offset C4-C5h, bit 9 = 0 (disabled).
   - Single-bit ECC Error Correcting of Host Data Bus Enable:
     82454GX PB, register offset C0h, bit 10 = 0 (disabled).
   - Report Uncorrectable Host Data Bus ECC Errors:
     82454GX PB, register offset C0h, bit 11 = 0 (disabled).
2. Use an IOQ depth of 1.
3. Disable inbound write posting in the 82454GX PB.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

20. IO_REQ# May Not Be Deasserted for BPRI# During GAT, Non-GAT, or APIC Flush Mode Request

PROBLEM: During a GAT, non-GAT, or APIC Flush mode sideband request after the reception of inbound posted writes, the 82454GX PB goes into a state where all inbound posted writes are then drained. IO_REQ# is kept asserted during this process. However, if a retry occurs, IO_REQ# should be deasserted soon after BPRI# is asserted, instead of remaining asserted until all inbound posted writes are drained. If inbound writes target a cluster bridge and cannot make progress (due to retries from the cluster bridge), a deadlock occurs. After MEMACK# assertion for a sideband request, if a posted write is retried, the 82454GX PB does not rearbitrate for BPRI# before reissuing the write, and contention on the BPRI# signal may result. It is also possible for traffic originating behind the compatibility 82454GX PB and targeting the noncompatibility 82454GX PB to encounter this boundary condition. However, Intel has not currently identified any software which generates such traffic.

IMPLICATION: Handling of all GAT mode (FLUSHBUF# and MEMREQ# asserted), non-GAT mode (only FLUSHBUF# asserted), and APIC Flush (only MEMREQ# asserted) sideband requests are affected, whether from a EISA master/south bridge or other logic on the board (including the logic workaround for 450GX Erratum 7 or for GAT mode transaction aliasing).

WORKAROUND: Ensure that drivers which support peer-to-peer PCI transactions only do so for PCI devices under the same 82454GX PB. No workaround has been identified for third-party clustering agents.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

21. Memory Gap Reclaiming May Corrupt Data

PROBLEM: If the memory subsystem is configured using the Memory Gap Register (MG), Low Memory Gap Register (LMG), or High Memory Gap Start Address and End Address registers (HMGSA, HMGEA) to allow a gap in the address map of the 82453GX MC, and if the memory in these gaps is reclaimed (by setting the appropriate bit in the MG, LMG, or HMGSA registers), the row address signals may be corrupted during the row address strobe (RAS#) signal assertion.

IMPLICATION: An incorrect address may be generated for a memory access if any of these three memory gaps are enabled with the memory reclaimed. This would result in data corruption and unpredictable system failure.

WORKAROUND: If these memory gaps are used, do not reclaim the memory in the gaps.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

22. RAW May Corrupt Write Data in 1:1 Interleaving

PROBLEM: If a memory subsystem is configured for 1:1 interleaving (i.e., only using one memory interleave, also known as noninterleaved), and read-around-write (RAW) is enabled, a partial write transaction to a memory location marked as Modified in the L2 cache followed by a line read transaction which is reordered around the partial write may result in the write data being corrupted.

IMPLICATION: With RAW enabled and the memory subsystem 1:1 interleaved, data corruption may occur, resulting in unpredictable system failure.

WORKAROUND: Do not enable RAW if the system is configured in 1:1 interleaving.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

23. Inbound Write May be Posted Too Soon After Misaligned or Multi-Dword Cycle

PROBLEM: Inbound writes should not be posted by the 82454GX PB between the time an outbound memory read, I/O write, or I/O read cycle is taken from the request queue until it completes on the PCI bus. If such a cycle required multiple transfers on the PCI bus (i.e., is misaligned across a Dword boundary or is a multi-Dword request) and the last transfer of the request receives a retry response from the PCI bus, then a write may be posted before the cycle completes.

IMPLICATION: Misaligned or multi-Dword memory reads, I/O reads, and I/O writes may cause a subsequent inbound write transaction to be posted improperly, resulting in an ordering violation and system hang.

WORKAROUND: Ensure that:

1. The Lock Atomic Reads feature in the 82454GX PB's PB Configuration Register (bit 6 of register offset 4Ch) is set, and that the arbiter uses full PCI bus locks. This will prevent another PCI master from acquiring the PCI bus after a retry on the last transfer of a misaligned or multi-Dword memory or I/O read.
2. Ensure that misaligned I/O writes do not occur. Intel has not currently identified any commercial operating system or application software which contains misaligned I/O writes.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

24. IO_REQ# May Not Be Deasserted for BPRI# During GAT Mode Request

PROBLEM: During a GAT mode sideband request after the reception of inbound posted writes, the 82454GX PB goes into a state where all inbound posted writes are then drained. IO_REQ# is kept asserted during this process. However, if a retry occurs, IO_REQ# should be deasserted soon after BPRI# is asserted, instead of remaining asserted until all inbound posted writes are drained. If inbound writes target a cluster bridge and cannot make progress (due to retries from the cluster bridge), a deadlock occurs. After MEMACK# assertion for a GAT mode sideband request, if a posted write is retried, the 82454GX PB does not rearbitrate for BPRI# before reissuing the write, and contention on the BPRI# signal may result. It is also possible for traffic originating behind the compatibility 82454GX PB and targeting the noncompatibility 82454GX PB to encounter this boundary condition. However, Intel has not currently identified any software which generates such traffic.

IMPLICATION: Handling of all GAT mode (FLUSHBUF# and MEMREQ# asserted) sideband requests are affected. Such requests may result in a deadlock if peer-to-peer transactions or third-party clustering agents are used.

WORKAROUND: Ensure that drivers which support peer-to-peer PCI transactions only do so for PCI devices under the same 82454GX PB. Systems with third-party clustering agents must use Aliased GAT mode to avoid this erratum.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

25. BINIT# Assertion May Cause Active RAS# Negation

PROBLEM: BINIT# is asserted on the Pentium Pro processor system bus to indicate the occurrence of a catastrophic system error condition or a situation that prevents reliable future operation. When the 82453GX MC component of the 450GX PCIset recognizes the assertion of BINIT# on the system bus, it prepares to clear certain internal state. In the process, a currently active RAS# signal associated with a read, write or refresh operation in progress may also be negated. If this negation causes the minimum RAS# pulse width timing to be violated then spurious bits may appear in one page of the memory array.

IMPLICATION: The catastrophic system error conditions that led to BINIT# assertion may in turn lead to a page of memory being incompletely written or improperly refreshed before potentially recovering from BINIT#.

WORKAROUND: Recovery from BINIT# assertion may be aided by a Machine Check Exception (MCE) or System Management Interrupt (SMI) handler. MCE or SMI handlers resident in nonvolatile memory can protect recovery routines from encountering this situation, allowing them to be reliably executed after BINIT# assertion.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

26. SMM Address Decode Limitation for Systems Supporting Greater Than 4 Gbytes

PROBLEM: If a System Management Mode (SMM) range is enabled in the 82453GX Memory Controller, and if the system supports a memory range greater than 4 Gbytes, then the SMM region allocation causes a gap to appear at each SMM base address per 4-Gbyte multiple. This gap will appear at {(4 Gbytes * n) + SMM Base}.

IMPLICATION: Due to the gap introduced by the allocation of an SMM region, there is a loss of supported memory equal to the SMM range size per 4-Gbyte segment of memory.

WORKAROUND: Possible workarounds include avoiding the usage of SMM or if SMM is required, to deallocate the extra gap in memory if the system is intended to support greater than 4 Gbytes of memory.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

27. Mixed Configuration and Memory Accesses May Cause System Hang

PROBLEM: The 82453GX Memory Controller, under specific traffic conditions, can cause the system to hang. The traffic required to cause this erratum is as follows:

1. At least one request on the Pentium® Pro processor system bus to an agent other than the 82453 Memory Controller must occur for which the snoop results are immediately resolved, but the data transfer is delayed. This erratum is more likely to occur if there are many such outstanding requests, all of which resolve their snoop results immediately, and each of which delay the data bus for a portion of the total delay.
2. Three read requests must be generated on the bus, directed to addresses claimed by the 82453 Memory Controller. All three requests must have snoop results which resolve immediately. The data transfers for all three of these reads must be delayed until step 3 completes.
3. A configuration read must occur, directed to the 82453 Memory Controller. This must occur significantly before the delayed data transfer in step 1 above.

The request traffic above may cause the 82453 Memory Controller to assert DBSY# and “hang” in that state.

IMPLICATION: When this erratum occurs, the configuration read is processed immediately and the data is transferred to the data buffers, overwriting the data from the first memory read. The subsequent deallocation of the buffers results in the 82453 Memory Controller asserting DBSY#, and waiting for valid data (which was already delivered and erroneously deallocated). If this occurs, the 82453 Memory Controller will not make forward progress; an assertion of BINIT# or RESET# is required to clear the component’s state and proceed.

Because the 82454 PCI Bridge will not delay a data transfer without also delaying the snoop portion of the transaction, a system with only Intel 450GX PCIset components and Pentium Pro processors will not encounter this erratum. Only third-party system bus agents with the following characteristics can encounter this erratum:

1. The third-party agent does not delay the snoop portion of outstanding data transfers when delaying a data transfer.
2. The third-party agent is capable of supporting more than two outstanding transactions active on the system bus at one time.

WORKAROUND: The Intel 450KX/GX PCIset specification states that configuration space accesses to the 82453 Memory Controller should only be performed by one processor at a time. Additionally, if third-party system bus agents with the characteristics above are used, no other agent in the system (including the 82454 PCI Bridge and third-party agents) should access a system bus agent other than the 82454 PCI Bridge during configuration accesses. This can be achieved through the use of a cached semaphore for configuration space accesses, where one processor locks the resource, and the other agents wait for the lock to be relinquished before continuing with their normal memory accesses.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

28. Inbound Read Retry Near Configuration Write Can Disrupt PCI Cycles

PROBLEM: There is a one clock window, immediately after the ADS# assertion for an I/O write to the Configuration Address register (address CF8h), where the retry of a read initiated by the auxiliary PB can result in an error. This error will not occur in a compatibility PB, and therefore cannot occur in single PB systems. If the auxiliary PB receives a read retry in this clock, it will internally drop its "write command" for the CF8 update. This can result in one of two failures:

1. The data in the Configuration Address register for the auxiliary PB becomes stale (which may or may not have observable effects).
2. The data buffer pointers are temporarily confused when DBSY# for the Configuration Address register is received without the corresponding internal write command. Therefore, if a PCI cycle propagates to the system bus before the I/O write completes, the data for this read or write cycle may be pulled from the wrong data buffer.

IMPLICATION: If the previous value of the Configuration Address register selected the auxiliary PB, then depending on the new value of the register, either bus contention or a register update failure will occur. Bus contention will occur if the register data is changed to point to a device that is not below the auxiliary PB. Usage of stale data will occur if the register data is changed to point to another register internal to or below the auxiliary PB. If the previous value of the register did not select the auxiliary PB, and it is then changed to point to the auxiliary PB, a bus time-out will occur. Regardless of the values in the Configuration Address register, if a PCI cycle propagates to the system bus before the write to the register completes, the read or write data may be incorrect.

WORKAROUND: Prevent the auxiliary PB from receiving a retry for an inbound read in the clock after an ADS# assertion to address CF8h. There are several ways this can be accomplished through specialized code and/or external logic. To accomplish this without external hardware, BPRI# Optimization (register 48h, bit 4) can be disabled in the auxiliary PB. When the BPRI# Optimization is disabled, the PB will keep BPRI# asserted until the response phase for its inbound read is received. Therefore, the ADS# assertion for the Configuration Address register cannot occur until after the inbound read is retried. The BPRI# Optimization for the compatibility PB can remain active and does not need to be disabled.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

29. Hang with Zero-Byte Write Followed by a Nonzero Byte Write

PROBLEM: If an inbound PCI zero-byte write is followed by a PCI nonzero byte write, and a specific set of timing circumstances exist, the chipset can become out of sync. This will cause DBSY# to remain asserted infinitely while awaiting data that will not be delivered.

IMPLICATION: When the above criteria are met, the system will hang. A hard reset or power cycle is required to recover from this condition.

WORKAROUND: There are two workarounds for this issue. Either set the In-Order-Queue (IOQ) depth to 1 or do not issue zero-byte transactions to the PCI bus of an 82454KX/GX PCI Bridge.

STATUS: For the steppings affected see the Summary Table of Changes at the beginning of this section.

SPECIFICATION CLARIFICATIONS

1. Explicit Writebacks Claimed by 82454GX PB

Note 2 in Section 3.2 of the *Intel 450KX/GX PCIset* datasheet states that writebacks initiated by other agents are ignored by the PB. It should be noted that while this is true with respect to PCI bus transactions (i.e., no PCI bus cycles will be generated due to any writeback transaction), if a writeback occurs to memory behind the 82454GX PB, the data will be lost or a violation of processor bus protocol will occur. The 82454GX PB is not a caching agent, and no writeback transactions should be targeted to devices on the PCI bus. Memory behind the 82454GX PB may not be mapped as cacheable (WB type) memory.

2. Supported Configurations For MC Row Limit Register Programming

The following text will be added to the paragraph describing the DRL DRAM Row Limit Register in Section 2.3.13. of Chapter 3, “Memory Controller,” of the Intel 450GX PCIset databook.

“The DRAM Row Limit registers may only be programmed in such a fashion that they do not violate the supported memory configurations outlined in Table 22, “Minimum and Maximum Memory Sizes for Each Configuration.” Other configurations of the row limit registers using increments other than those described are not supported.”

DOCUMENTATION CHANGES

1. Register Offset and Default Value Correction

Some configuration registers are documented unclearly or inconsistently in the *Intel 450KX/GX PCIset* datasheet. A table of the correct offsets and values is given below with the changes in bold (note that this list only contains registers with changes):

Configuration Register	Address Offset	Default Value	Notes
82454GX			
Top of System Memory	40-43h	**0000** 0000h	
Bridge Device Number	49h	0001 1001**b** 0001 1010**b**	Compatibility 82454GX Auxiliary 82454GX
PB Configuration	4Ch	**1**9h **1**Ah	Compatibility 82454GX Auxiliary 82454GX
PCI Read/Write Control	54-55h	**00**00h	
Memory Gap Range	78-79h	**00**00h	
Memory Gap Upper Address	7A-7Bh	**00**00h	
PCI Frame Buffer	7C-7Fh	**0000 00**00h	
High Memory Gap Range Start Address	88-8Bh	**0000 00**00h	
High Memory Gap End Address	8C-8Fh	**0000 00**00h	
Configuration Values Driven on Reset	B0-B1h	**00**00h	Bit 7: 1 = Depth of **1**. 0 = Depth of **8**. Pentium® Pro processors use an in-order depth of **1** if this bit is 1.
Captured System Configuration Values	B4-B5h	**000X XXXX XXX0 0000b**	X = captured during hard reset. Bit 7: 1 = Depth of **1**. 0 = Depth of **8**. Pentium Pro processors use an in-order depth of **1** if this bit is 1.
SMRAM Range	B8-BBh	0000 0005h	Bits [15:0] correspond to A[31:**16**]**#**. The default starting address is **5**0000h and ranges to **5**FFFFh.
PB Retry Timers	C8-**CB**h	0000 0003h	

Configuration Register	Address Offset	Default Value	Notes
82453GX			
Controller Device Number	49h	0001010X**b**	X = loaded at reset
Single Bit Correctable Error Address	74-77h	**0000** 0000h	
Low Memory Gap Register	7C-7Fh	0010 0000h	**Bits [9:5]: Reserved.** Bits [4:0]: **Low Memory Gap Size.** This field defines the memory gap size as follows: **Bits [4:0] Size** **Bits [4:0] Size** 00000 1 MB **00111** 8 MB **00001** 2 MB **01111** 16 MB **00011** 4 MB **11111** 32 MB
High Memory Gap Start Address	88-8Bh	**0000** 0000h	**Bit 30: Reclaim Enable.** 1 = Enable. 0 = Disable (default). When enabled, the physical memory in this gap is reclaimed.
High Memory Gap End Address	8C-8Fh	**0000** 0000h	
Memory Timing Register	AC-AFh	30DF3516h	Bit 15: 1 = **2** Cycles. 0 = **1** Cycle (default).
SMRAM Range	B8-BBh	**0000** 000Ah	

2. CMOS Definition Should be 3.3 V or 5 V

In Section 1.0. of both Chapter 2 and Chapter 3 of the *Intel 450KX/GX PCIset* datasheet, CMOS signals are defined as follows:

CMOS Rail-to-rail CMOS tolerant to 5 V levels.

This should read:

CMOS Rail-to-rail CMOS tolerant to 3.3 V or 5 V levels. See Chapter 4, Section 1.2, “Signal Groups.”

3. Pull-up Resistor Required on PCLK

In Chapter 2, Table 4 of the *Intel 450KX/GX PCIset* datasheet, it is incorrectly stated that a pull-down resistor is required on the PCLK signal. This should be specified as a **pull-up** resistor, as is stated in Section 3.7.1.2 of Chapter 2.