INTEL 430MX PCISET 82437MX MOBILE SYSTEM CONTROLLER (MTSC) AND 82438MX MOBILE DATA PATH (MTDP)

- **Supports the Pentium® Processor at iCOMP® Index 815\100 MHz, iCOMP Index 735/90 MHz, iCOMP Index 1000/120, and the 75 MHz Pentium Processor**
- **Integrated Second Level Cache Controller**
  - **Direct Mapped Organization**
  - **Write-Back Cache Policy**
  - **Cacheless, 256 Kbytes, and 512 Kbytes**
  - **Standard, Burst and Pipelined Burst SRAMs**
  - **Cache Hit Read/Write Cycle Timings at 3-1-1-1 with Burst or Pipelined Burst SRAMs**
  - **Back-to-Back Read Cycles at 3-1-1-1-1-1-1-1 with Burst or Pipelined Burst SRAMs**
  - **Integrated Tag/Valid Status Bits for Cost Savings and Performance**
  - **Supports 3.3V SRAMs for Tag Address**
- **Integrated DRAM Controller**
  - **64-Bit Data Path to Memory**
  - **4 Mbytes to 128 Mbytes Main Memory**
  - **EDO/Hyper Page Mode DRAM (x-2-2-2 Reads) Provides Superior Cacheless Designs**
  - **Standard Page Mode DRAMs**
  - **4 RAS Lines**
  - **4-Qword Deep Buffer for 3-1-1-1 Posted Write Cycles**
  - **Symmetrical and Asymmetrical DRAMs**
  - **3V or 5V DRAMs**
- **Fully Synchronous 25/30/33 MHz PCI Bus Interface**
  - **100 MB/s Instant Access Enables Native Signal Processing on Pentium Processors**
  - **Synchronized CPU-to-PCI Interface for High Performance Graphics**
  - **PCI Bus Arbiter: MPIIX and Three PCI Bus Masters Supported**
  - **CPU-to-PCI Memory Write Posting with 4-Dword Deep Buffers**
  - **Converts Back-to-Back Sequential CPU to PCI Memory Writes to PCI Burst Writes**
  - **PCI-to-DRAM Posting of 12 Dwords**
  - **PCI-to-DRAM up to 120 MB/s Bandwidth Utilizing Snoop Ahead Feature**
- **NAND Tree for Board-Level ATE Testing**
- **208-Pin QFP for the 82437MX System Controller (MTSC); 100-Pin TQFP for Each 82438MX Data Path (MTDP)**

The Intel 430MX PCIset consists of the 82437MX System Controller (MTSC), two 82438MX Data Paths (MTDP), and the 82371MX PCI I/O IDE Xcelerator (MPIIX). The PCIset forms a Host-to-PCI bridge and provides the second level cache control and a full function 64-bit data path to main memory. The MTSC integrates the cache and main memory DRAM control functions and provides bus control for transfers between the CPU, cache, main memory, and the PCI Bus. The second level (L2) cache controller supports a write-back cache policy for cache sizes of 256 Kbytes and 512 Kbytes. Cacheless designs are also supported. The cache memory can be implemented with either standard, burst, or pipelined burst SRAMs. An external Tag RAM is used for the address tag and an internal Tag RAM for the cache line status bits. For the MTSC DRAM controller, four rows are supported for up to 128 Mbytes of main memory. The MTSC optimized PCI interface allows the CPU to sustain the highest possible bandwidth to the graphics frame buffer at all frequencies. Using the snoop ahead feature, the MTSC allows PCI masters to achieve full PCI bandwidth. The MTDPs provide the data paths between the CPU/cache, main memory, and PCI. For increased system performance, the MTDPs contain read prefetch and posted write buffers.

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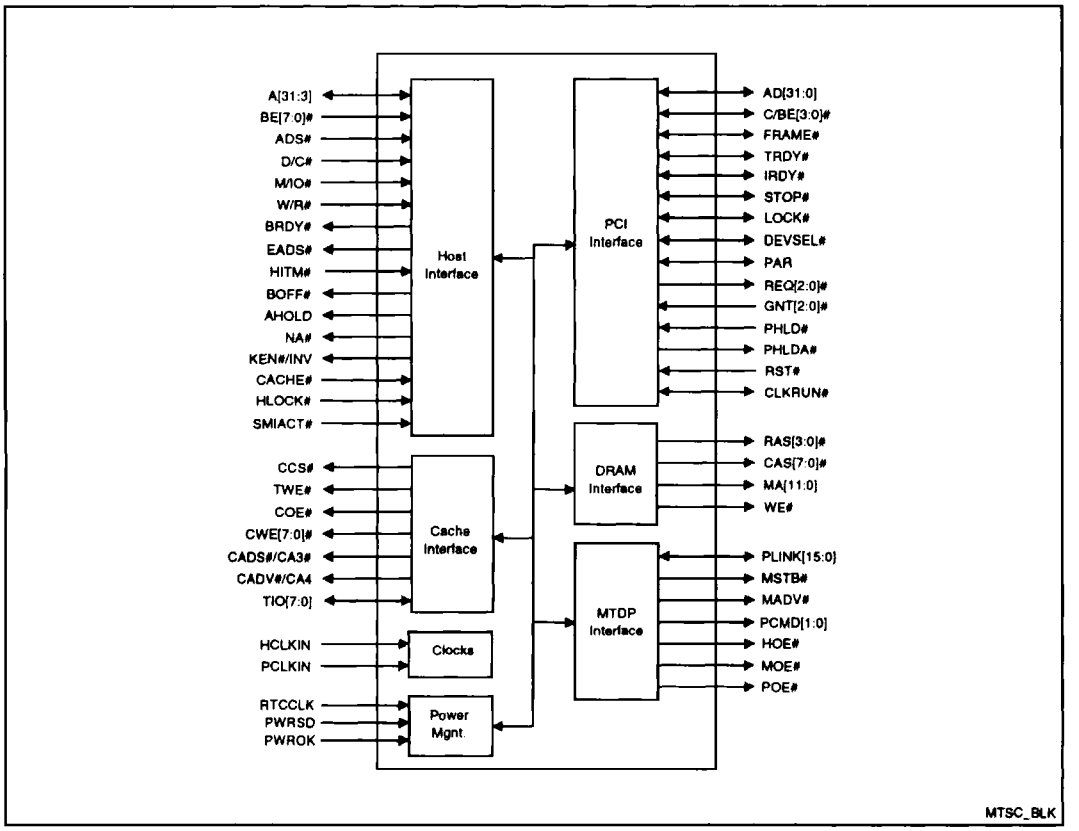
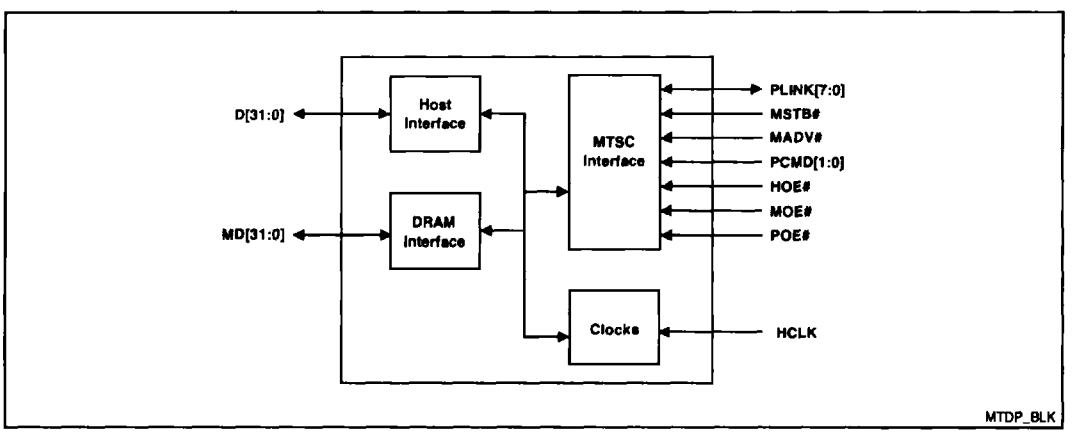


82437MX MTSC Block Diagram



82438MX MTDP Block Diagram