

82352/82352DT EISA BUS BUFFER (EBB)

- **Designed Specifically for EISA Bus Requirements**
- **Provides Three Modes of Operation**
 - Data Latch and Swap Functions Allow Swapping and Assembly of Data between the Host and EISA/ISA Buses on a Byte by Byte Basis (Mode 0)
 - Provides a Buffered Path with Parity Generation/Check between the Host Data Bus and DRAM (Mode 1)
 - Address Latch Functions Provide Latching between the Host and EISA/ISA Buses (LA and SA Addresses) (Mode 3)
- **120-Pin Quad Flat Pack (QFP)**
- **Similar in Function to Discrete Implementation Using 74F543s/544, 74180s, and 74ALS245s**
- **Replaces 19 Discrete Components**
 - Three 82352s are Used Per 82350 EISA System
 - One 82352 is Used Per 82350DT EISA System
- **The 82352 Interfaces Easily to the System**
 - Buffer Control for the 32-Bit Mode W/O Parity and the EISA Address Mode is Provided by the 82358 (EISA Bus Controller)
- **The 82352 and 82352DT are Socket Compatible**
- **The 82352DT is Designed to Meet All of the 82352 Specifications**
(See Packaging Specification Order Number 240800, Package Type S)

The 82352/82352DT design allows it to replace the multiple address and data latch-buffer/driver ICs used in EISA applications. The EBB provides three modes of operation: a 32-bit mode without parity to replace the EISA data swap buffers, a 32-bit mode with parity to replace the EISA DRAM data parity buffers, and an EISA address mode to replace the host to EISA/ISA address buffers. Mode 2 on the EBB is reserved. The same chip is strapped in three different ways to obtain the three configurations.

82352 is manufactured and tested for Intel by Texas Instruments and IC Solutions in accordance with their respective internal standards.

82352DT is manufactured and tested for Intel by LSI Logic in accordance with their internal standards.

82352 EISA BUS BUFFER (EBB)

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1.0 INTRODUCTION

1.1 Bus Description/EISA System Interface

The EBB supports up to three buses when used in an EISA system. Each bus is broken down into groups; usually one byte in width. Each group is identified by a letter/number combination which identifies the associated bus and relative group location in the bus. The following identifies the various bus/group relationships on a per mode basis.

Mode 0: 32-Bit Data Mode without Parity

A-BUS = A-BUS <31..0> = **A0** + **A1** + **A2** + **A3**

A0 = A0 <7..0> = HOST DATA BUS <7..0>

A1 = A1 <7..0> = HOST DATA BUS <15..8>

A2 = A2 <7..0> = HOST DATA BUS
<23..16>

A3 = A3 <7..0> = HOST DATA BUS
<31..24>

B-BUS B-BUS <31..0> = **B0** + **B1** + **B2** + **B3**

B0 = B0 <7..0> = EISA/ISA DATA BUS
<7..0>

B1 = B1 <7..0> = EISA/ISA DATA BUS
<15..8>

B2 = B2 <7..0> = EISA/ISA DATA BUS
<23..16>

B3 = B3 <7..0> = EISA/ISA DATA BUS
<31..24>

Mode 1: 32-Bit Data Mode with Parity

A-BUS = A-BUS <31..0> = **A0** + **A1** + **A2** + **A3**

A0 = A0 <7..0> = DRAM DATA BUS <7..0>

A1 = A1 <7..0> = DRAM DATA BUS
<15..8>

A2 = A2 <7..0> = DRAM DATA BUS
<23..16>

A3 = A3 <7..0> = DRAM DATA BUS
<31..24>

B-BUS B-BUS <31..0> = **B0** + **B1** + **B2** + **B3**

B0 = B0 <7..0> = HOST DATA BUS <7..0>

B1 = B1 <7..0> = HOST DATA BUS <15..8>

B2 = B2 <7..0> = HOST DATA BUS
<23..16>

B3 = B3 <7..0> = HOST DATA BUS
<31..24>

Mode 3: EISA Address Mode

A-BUS = A-BUS <31..2> = **A0** + **A1** + **A2** + **A3**

A0 = A0 <6..0> = HOST ADDRESS BUS
<8..2>

A1 = A1 <7..0> = HOST ADDRESS BUS
<16..9>

A2 = A2 <6..0> = HOST ADDRESS BUS
<23..17>

A2 = A2 <7> = HOST (HM/IO#)

A3 = A3 <7..0> = HOST ADDRESS BUS
<31..24>

B-BUS = B-BUS <31..2> = **B0** + **B1** + **B2** + **B3#**

B0 = B0 <6..0> = EISA ADDRESS BUS LA
<8..2>

B1 = B1 <7..0> = EISA ADDRESS BUS LA
<16..9>

B2 = B2 <6..0> = EISA/ISA ADDRESS BUS
LA <23..17>

B3 = B3# <7..0> = EISA ADDRESS BUS B-
BUS <31..24>

S-BUS = B-BUS <19..2> = **S0** + **S1** + **S2**

S0 S0 <6..0> = ISA ADDRESS BUS SA
<8..2>

S1 S1 <7..0> = ISA ADDRESS BUS SA
<16..9>

S2 S2 <2..0> = ISA ADDRESS BUS SA
<19..17>

NOTE:

The **B3#** (LA# <31..24>) bus group is allowed to float high during ISA bus master operation. These high bits are inverted by the 74F544 style latch/buffer and driven onto **A3** as zeros. This allows correct 32-bit addresses to be transferred to the system during ISA bus master operation.

SUMMARY:

Mode 0 is connected to the EISA System as follows:

AX— Host Data Bus

BX— EISA/ISA Data Bus

Mode 1 is connected to the EISA System as follows:

AX— DRAM Memory lines

BX— Host Data Bus

Mode 2 is reserved.

Mode 3 is connected to the EISA System as follows:

AX— Host Address Bus

BX— LA Address Bus (EISA/ISA Bus)

SX— SA Address Bus (ISA Bus)

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2.0 FUNCTIONAL DESCRIPTION

The EBB's functional description is broken down into three discrete descriptions along with one integrated description. Each of the three discrete descriptions view the EBB's functional logic in terms of the ICs it is replacing.

Unless otherwise noted, each functional description assumes the Master Output Enable (MOE#) and the A-BUS Latch Enable (A_LE#) signals are asserted (low).

NOTE:

Mode 2 is reserved.

2.1 Mode 0: 32-Bit Data Mode without Parity

2.1.1 MODE 0 DESCRIPTION

Functionally, this 32-bit data mode is similar to using 74F543s and 74ALS245s. Each of the four latch/buffer modules in Figure 2 can be replaced by a 74F543 with their "chip enable" lines tied to ground. A 74ALS245 can replace each bidirectional transceiver module also found in Figure 2.

The latch/buffer modules, when operated together, will allow bidirectional data transfers and latching between the 32-bit A-BUS and 32-bit B-BUS. Control of the buses on both 16-bit and 8-bit increments is also possible within the defined constraints of the control signals (REFER TO SECTIONS 3.1, 4.1 and 5.1).

The bidirectional transceiver modules allow 8-bit data transfers to occur between the four bytes comprising the B-BUS. If the B-BUS is viewed as a four-byte data word, these buffers will allow the lowest order byte, B0, to transfer data to or from the remaining three bytes. Also 16-bit data transfers can be supported between the low order bytes (B0, B1) and the high order bytes (B2, B3). The Ax D-Latch inputs will also have access to the data during transfer.

The bidirectional transceiver modules are enabled by asserting the corresponding BxxCPYE# line low. The direction of the copy is determined by the logic level of the CPY_DN# line.

The A_LE# control signal is OR'ed with all the individual Ax latch enable control signals. If all Ax lines are asserted, this line will act as a global A-BUS latch enable.

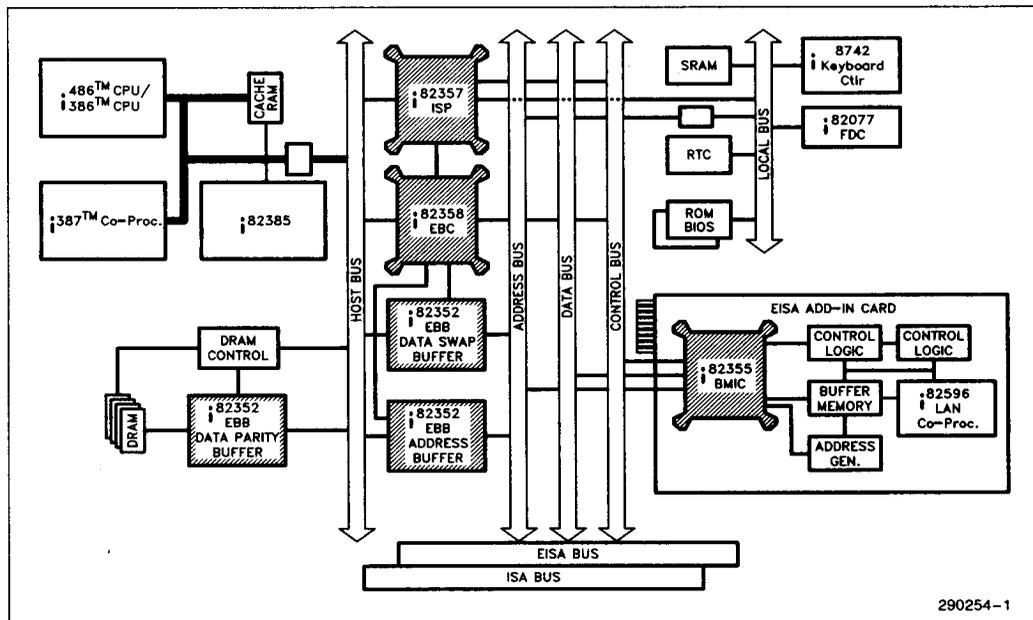


Figure 1. 82350 EISA Chip Set

2.1.2 MODE 0: BLOCK DIAGRAM

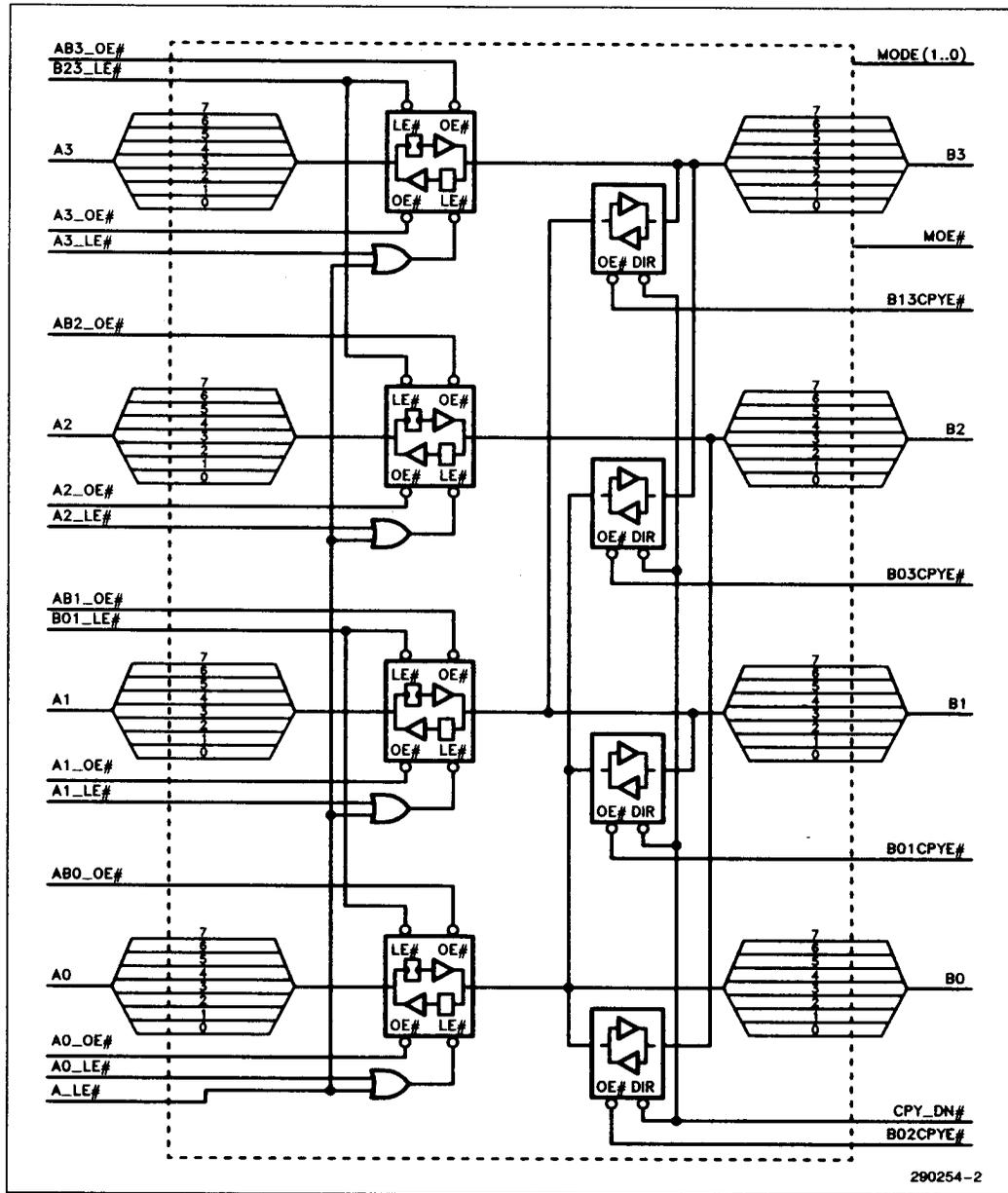


Figure 2. Mode 0: 32-Bit Mode without Parity

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2.2 Mode 1: 32-Bit Data Mode with Parity

2.2.1 MODE 1 DESCRIPTION

This data mode is similar to the mode discussed in 2.1 except for the addition of even-parity generation/detection circuits (see Figure 3). Parity support is available for each byte in both the **A-BUS** and **B-BUS**.

The parity generation and detection is functionally similar to the 74180. Each **Ax** and **Bx** is serviced by a separate parity module.

During data transfers from the **B-BUS** to the **A-BUS**, four independent even-parity signals are generated. These parity signals are routed through the same 74F543 style latch/buffer modules that supports the byte used in their generation. This will allow each parity signal to be latched with its associated **Bx** byte.

2.2.2 MODE 1: BLOCK DIAGRAM

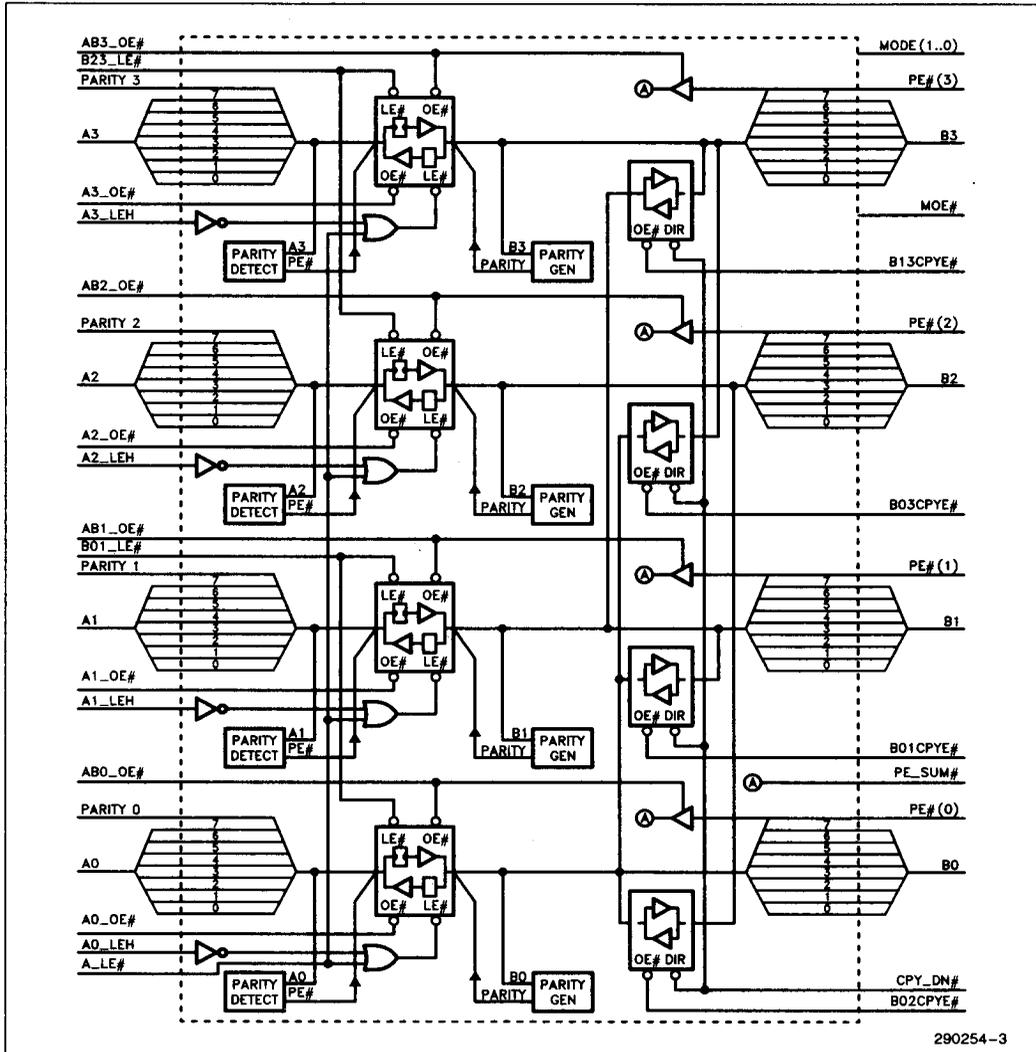


Figure 3. Mode 1: 32-Bit Mode with Parity

During data transfers from the **A-BUS** to the **B-BUS**, incoming **Ax** byte parity is compared with the parity generated in the parity detection modules. If the parities differ and if the output enable for that byte is active, the parity error signal for that byte, along with the parity-sum signal will go active.

The parity-sum signal will not respond to errors for bytes that do not have asserted output enables.

Parity support is not available for any **Bx** to **Bx** data transfer using the bidirectional transceiver modules.

Note that the latch enable signals for the **A0, A1, A2** and **A3** bus groups are inverted in this mode.

2.3 Mode 3: EISA Address Mode

2.3.1 MODE 3 DESCRIPTION

The EISA Address Mode is similar to a discrete implementation using six 74F543s and a 74F544. Each of the six non-inverting latch/buffer modules in Figure 4 can be replaced by a 74F543. The 74F544 can replace the single inverting latch/buffer. Each of the seven chips would have their "chip enable" lines tied low.

2.3.1.1 EBB-EISA Bus Relationships

The EISA Address Mode is required to support three separate address buses (**A-BUS**, **B-BUS**, **S-BUS**) along with two control signals (HM/IO#, M-IO#). When this mode is operating in an EISA system, the following relationships must exist for proper operation:

EBB Bus	EISA Bus	
A3<7..0>	HA<31..24>	System Specific
A2<6..0>	HA<23..17>	System Specific
A2<7>	HM/IO#	System Specific
A1<7..0>	HA<16..9>	System Specific
A0<6..0>	HA<8..2>	System Specific
B3#<7..0>	LA#<31..24>	EISA Defined
B2<6..0>	LA<23..17>	EISA Defined

EBB Bus	M-IO#	EISA Bus
B2<7>	M-IO#	EISA Defined
B1<7..0>	LA<16..9>	EISA Defined
B0<6..0>	LA<8..2>	EISA Defined
S2<2..0>	SA<19..17>	EISA Defined
S1<7..0>	SA<16..9>	EISA Defined
S0<6..0>	SA<8..2>	EISA Defined

2.3.1.2 Host System as Bus Master

The host system will present system (HA) address data along with the HM/IO# command signal to the EBB using the **A-BUS**. This data will immediately update the **B-BUS** (LA) and M-IO# if the **B-BUS** latch enable is asserted. When the **B-BUS** data is considered valid, the S-BUS__LE# signal will unlatch the **S-BUS** (SA).

2.3.1.3 ISA Bus Master

The ISA bus master will present address data to the EBB using the **S1, S0 (SA<16..2>)** and **B2(LA<23..17>)** bus groups. If both A-BUS__LE# and S-BUS__OE# are asserted, this data will immediately update the **A2, A1, A0 (HA<23..2>)** and **B1, B0 (LA<16..2>)** bus groups.

The **B3# (LA#<31..24>)** bus group is allowed to float high during ISA bus master operation. These high bits are inverted by the 74F544 style latch/buffer and driven onto **A3** as zeroes. This allows correct 32-bit addresses to be transferred to the system during ISA bus master operation.

2.3.1.4 EISA Bus Master

The EISA bus master presents the LA<31..2> address data along with M-IO# to the EBB using the **B-BUS**. This data will immediately update the **A-BUS** and HM/IO# if the A-BUS__LE signal is asserted. When the **B-BUS** data is considered valid, the S-BUS__LE# signal will unlatch the **S-BUS**.

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2.3.2 MODE 3: BLOCK DIAGRAM

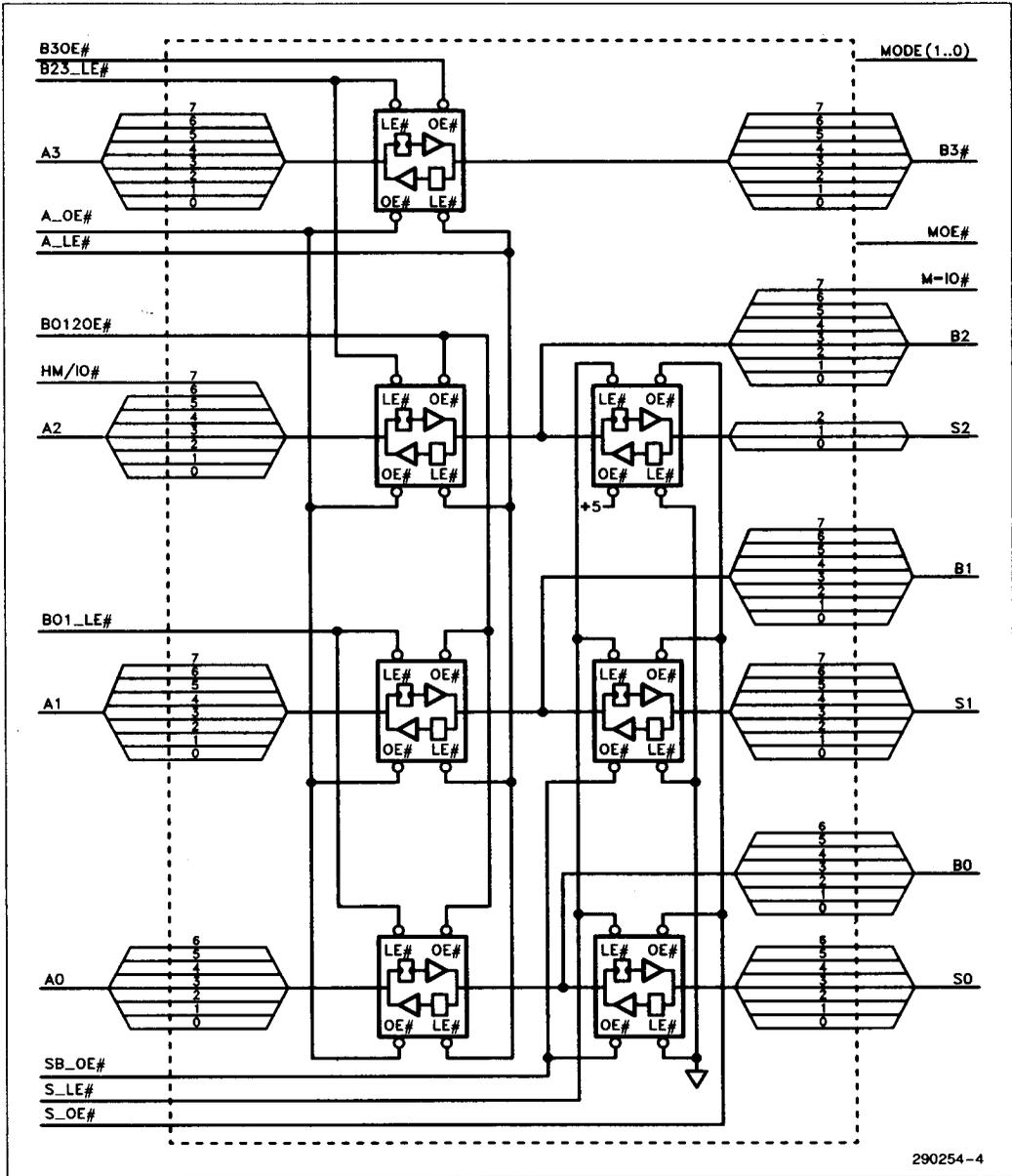


Figure 4 Mode 3: EISA Address Mode

3.0 MODE 0: 32-BIT DATA MODE WITHOUT PARITY DETAILED DESCRIPTION

3.1 Detailed Pin Description

The following table contains detailed descriptions of each signal while the EBB is in its non-parity 32-bit data mode. Note: For all "N/C" pins, use an 8.2K pullup resistor.

Symbol	# Pins	Type	Function
A-BUS	32	B	<p>One of the two 32-bit buses manipulated by the EBB. Each of the four bytes in A-BUS (A0<7..0>, A1<7..0>, A2<7..0> and A3<7..0>) can be independently controlled. During non-copy transfers, the signal associations are:</p> <p style="text-align: center;"> A0 B0 A1 B1 A2 B2 A3 B3 </p>
B-BUS	32	HCB	<p>One of the two 32-bit buses manipulated by the EBB. Each of the four bytes in B-BUS (B0<7..0>, B1<7..0>, B2<7..0> and B3<7..0>) can be independently controlled. During non-copy transfers, the signal associations are:</p> <p style="text-align: center;"> B0 A0 B1 A1 B2 A2 B3 A3 </p>
MOE#	1	I	Master Output Enable. This signal is ORed together with all other output enables used in this mode of operation. When asserted (low), this signal will allow the other output enables to function. When negated (high), all EBB outputs will go into their High-Z states.
Ax_OE#	4	I	<p>Ax Output Enables. When MOE# is low, these signals enable the output of the Ax. The signal associations are:</p> <p style="text-align: center;"> A0_OE# A0 A1_OE# A1 A2_OE# A2 A3_OE# A3 </p>
ABx_OE#	4	I	<p>Ax to Bx Output Enables. When MOE# is low, these signals enable the outputs of the Bx buffers during data transfers from the A-BUS to the B-BUS. The signal associations are:</p> <p style="text-align: center;"> AB0_OE# A0 B0 AB1_OE# A1 B1 AB2_OE# A2 B2 AB3_OE# A3 B3 </p>
A_LE#	1	I	<p>A-BUS Latch Enable. This signal is "ORed" with the Ax_LE# latch enables. When asserted (low), this signal will allow all the Ax latch enables to function. When negated (high), all the A-BUS latches will latch the input data present at the time of the low to high transition if the individual Ax latch enable is asserted (low) at the time of this transition.</p>

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Symbol	# Pins	Type	Function																
Ax_LE #	4	I	<p>Ax Latch Enables. When A__LE # is low, these signals can be used to individually control the latching of B-BUS data to the A-BUS. For non-copy transfers, the signal associations are:</p> <table style="margin-left: 40px;"> <tr> <td>A0_LE #</td> <td>B0</td> <td>A0</td> </tr> <tr> <td>A1_LE #</td> <td>B1</td> <td>A1</td> </tr> <tr> <td>A2_LE #</td> <td>B2</td> <td>A2</td> </tr> <tr> <td>A3_LE #</td> <td>B3</td> <td>A3</td> </tr> </table>	A0_LE #	B0	A0	A1_LE #	B1	A1	A2_LE #	B2	A2	A3_LE #	B3	A3				
A0_LE #	B0	A0																	
A1_LE #	B1	A1																	
A2_LE #	B2	A2																	
A3_LE #	B3	A3																	
B01_LE #	1	I	B01 and B1 Latch Enable. This signal is used to control the latching of A0 and A1 bus groups to the B0 and B1 bus groups respectively. On the asserted to negated (low to high) transition, data present at the latch inputs will be latched onto the latch output.																
B23_LE #	1	I	B2 and B3 Latch Enable. This signal is used to control the latching of A2 and A3 bus groups to the B2 and B3 bus groups respectively. On the asserted to negated (low to high) transition, data present at the latch inputs will be latched onto the latch output.																
CPY_DN #	1	I	<p>Bus Group Copy Down. This signal determines the direction of data flow for data appearing on the four Bx copy transceivers. When asserted (low), the transceivers will allow the following potential data transfers:</p> <table style="margin-left: 40px;"> <tr> <td>Transceiver-1:</td> <td>From B1 to B0, A0 D-Latch</td> </tr> <tr> <td>Transceiver-2:</td> <td>From B2 to B0, A0 D-Latch</td> </tr> <tr> <td>Transceiver-3:</td> <td>From B3 to B0, A0 D-Latch</td> </tr> <tr> <td>Transceiver-4:</td> <td>From B3 to B1, A0 D-Latch</td> </tr> </table> <p>When negated (high), the transceivers will allow the following potential data transfers:</p> <table style="margin-left: 40px;"> <tr> <td>Transceiver-1:</td> <td>From B0 to B1, A1 D-Latch</td> </tr> <tr> <td>Transceiver-2:</td> <td>From B0 to B2, A2 D-Latch</td> </tr> <tr> <td>Transceiver-3:</td> <td>From B0 to B3, A3 D-Latch</td> </tr> <tr> <td>Transceiver-4:</td> <td>From B1 to B3, A3 D-Latch</td> </tr> </table> <p>It is recommended that only these combinations be used to swap data between the A-bus and the B-bus.</p>	Transceiver-1:	From B1 to B0 , A0 D-Latch	Transceiver-2:	From B2 to B0 , A0 D-Latch	Transceiver-3:	From B3 to B0 , A0 D-Latch	Transceiver-4:	From B3 to B1 , A0 D-Latch	Transceiver-1:	From B0 to B1 , A1 D-Latch	Transceiver-2:	From B0 to B2 , A2 D-Latch	Transceiver-3:	From B0 to B3 , A3 D-Latch	Transceiver-4:	From B1 to B3 , A3 D-Latch
Transceiver-1:	From B1 to B0 , A0 D-Latch																		
Transceiver-2:	From B2 to B0 , A0 D-Latch																		
Transceiver-3:	From B3 to B0 , A0 D-Latch																		
Transceiver-4:	From B3 to B1 , A0 D-Latch																		
Transceiver-1:	From B0 to B1 , A1 D-Latch																		
Transceiver-2:	From B0 to B2 , A2 D-Latch																		
Transceiver-3:	From B0 to B3 , A3 D-Latch																		
Transceiver-4:	From B1 to B3 , A3 D-Latch																		
B01CPYE #	1	I	B-BUS Copy Enable 01. When MOE # is low, this signal enables copy Transceiver-1 to transfer data between B0 and B1 . The data direction is determined by the logic value of CPY_DN #.																
B02CPYE #	1	I	B-BUS Copy Enable 02. When MOE # is low, this signal enables copy Transceiver-2 to transfer data between B0 and B2 . The data direction is determined by the logic value of CPY_DN #.																
B03CPYE #	1	I	B-BUS Copy Enable 03. When MOE # is low, this signal enables copy Transceiver-3 to transfer data between B0 and B3 . The data direction is determined by the logic value of CPY_DN #.																
B13CPYE #	1	I	B-BUS Copy Enable 13. When MOE # is low, this signal enables copy Transceiver-4 to transfer data between B1 and B3 . The data direction is determined by the logic value of CPY_DN #.																
SLEW	1	I	<p>Output Buffer Slew Rate Control. This signal will provide slew rate control for all external output buffers used in the EBB. When this signal is negated (low), all output buffers will switch at their non-compensated slew rate. When this signal is asserted (high), the output buffers will switch at a slower (> 2 ns) slew rate.</p> <p style="text-align: center;">NOTE:</p> <p>When the Slew signal is asserted (high), add 1.5 ns to all A.C. timings.</p>																

Symbol	# Pins	Type	Function															
MODE <1..0>	2	I	Operating Mode Pins. These signals determine the mode of operation for the EBB. They are intended to be hardwired to the proper value. Operating mode determination: <table border="0" style="margin-left: 20px;"> <tr> <td>Mode <1></td> <td>Mode <0></td> <td>Operating Mode</td> </tr> <tr> <td># L</td> <td>L</td> <td>32-Bit Wide Data Mode w/o Parity</td> </tr> <tr> <td>L</td> <td>H</td> <td>32-Bit Wide Data Mode with Parity</td> </tr> <tr> <td>H</td> <td>L</td> <td>RESERVED</td> </tr> <tr> <td>H</td> <td>H</td> <td>EISA Address Mode</td> </tr> </table> # Mode described in this section	Mode <1>	Mode <0>	Operating Mode	# L	L	32-Bit Wide Data Mode w/o Parity	L	H	32-Bit Wide Data Mode with Parity	H	L	RESERVED	H	H	EISA Address Mode
Mode <1>	Mode <0>	Operating Mode																
# L	L	32-Bit Wide Data Mode w/o Parity																
L	H	32-Bit Wide Data Mode with Parity																
H	L	RESERVED																
H	H	EISA Address Mode																

3.2 D.C. Specifications

3.2.1 MAXIMUM RATINGS

Temperature Under Bias	-65° to +110°C
Storage Temperature	-65°C to +150°C
Supply Voltage with Respect to Ground	-0.5V to +7V
Voltage on Any Pin	-0.5V to +7V

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

3.2.2 D.C. SPECIFICATION TABLE

The following is a table of load capacitances, input voltage levels, current levels, and input leakage currents for the 32-bit non-parity mode:

T_A = 0°C to +70°C, V_{CC} = 5V ±5%, I_{CC} Max = 160 mA⁽⁸⁾

Signal Name	Pins	Type	I _{OL} Max (mA)	I _{OH} Max (mA)	I _I Max μA	V _I Max (V)	V _H Min (V)	C _{IN} ⁽⁷⁾ (pF)	C _{LOAD} (pF)
A-BUS <31..0>	8	B	12	-3	10	0.8/0.5	2.0/2.4	27	100
B-BUS <31..0>	8	HC B	24	-3	10	0.8/0.5	2.0/2.4	27	240
MOE #	1	I	N/A	N/A	10	0.8	2.0	27	N/A
Ax_OE #	4	I	N/A	N/A	10	0.8	2.0	27	N/A
ABx_OE #	4	I	N/A	N/A	10	0.8	2.0	27	N/A
A_LE #	1	I	N/A	N/A	10	0.8	2.0	27	N/A
Ax_LE #	4	I	N/A	N/A	10	0.8	2.0	27	N/A
B01_LE #	1	I	N/A	N/A	10	0.8	2.0	27	N/A
B23_LE #	1	I	N/A	N/A	10	0.8	2.0	27	N/A
CPY_DN #	1	I	N/A	N/A	10	0.8	2.0	27	N/A
B01CPYE #	1	I	N/A	N/A	10	0.8	2.0	27	N/A
B02CPYE #	1	I	N/A	N/A	10	0.8	2.0	27	N/A
B03CPYE #	1	I	N/A	N/A	10	0.8	2.0	27	N/A
B13CPYE #	1	I	N/A	N/A	10	0.8	2.0	27	N/A
MODE <1..0>	2	I	N/A	N/A	10	0.8	2.0	27	N/A

NOTES:

1. I_I Max = I_I for inputs, I_{LO} for outputs (or I/O).
2. V_I Max = V_{IL} for inputs, V_{IL}/V_{OL} for I/O.
3. V_H Min = V_{IH} for inputs, V_{IH}/V_{OH} for I/O.
4. V_{IN} for leakage = 0.45V to V_{CC}.
5. V_{OL} is tested while sinking I_{OL} (24 mA).
6. V_{OH} is tested while sourcing I_{OH} (-3 mA).
7. C_{IN} is maximum capacitance value.
8. Tested with no loads.



3.3 A.C. Specifications

3.3.1 A.C. SPECIFICATION TABLE

Parameter	From	To	Waveform	Parameter Value	C _L Loading
t _{PLH} or t _{PHL}	A-BUS	B-BUS	1	15.00 ns Max	240 pF
t _{PLH} or t _{PHL}	B-BUS	A-BUS	1	15.00 ns Max	100 pF
t _{PLH} or t _{PHL}	B-BUS	B-BUS	1	16.00 ns Max	240 pF
t _{PLH} or t _{PHL}	BxxCPYE #	B-BUS	1, 2	15.00 ns Max	*240 pF
t _{PLH} or t _{PHL}	BxxCPYE #	A-BUS	1, 2	17.00 ns Max	**100 pF
t _{PLH} or t _{PHL}	CPY_DN #	B-BUS	1, 2	15.00 ns Max	*240 pF
t _{PLH} or t _{PHL}	CPY_DN #	A-BUS	1, 2	17.00 ns Max	**100 pF
t _{PLH} or t _{PHL}	LE # / A_LE #	A-BUS	1, 2	15.00 ns Max	100 pF
t _{PLH} or t _{PHL}	LE #	B-BUS	1, 2	15.00 ns Max	240 pF
t _{PZH} or t _{PZL}	OE # or MOE #	A-BUS	3, 4	16.00 ns Max	100 pF
t _{PHZ} or t _{PLZ}	OE # or MOE #	A-BUS	3, 4	15.00 ns Max	100 pF
t _{PZH} or t _{PZL}	OE # or MOE #	B-BUS	3, 4	15.00 ns Max	240 pF
t _{PHZ} or t _{PLZ}	OE # or MOE #	B-BUS	3, 4	15.00 ns Max	240 pF
t _{SU}	A or B-BUS Data before LE		5	3.50 ns Min	
t _H			5	3.50 ns Min	
t _W	LE # Pulse Width (Low)		5	4.00 ns Min	

*Data originating from the A-Bus or B-Bus going to the B-Bus.

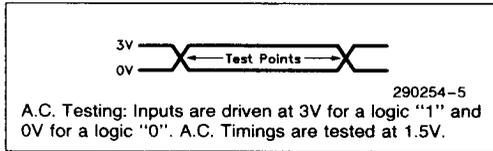
**Data originating from the B-Bus going to the A-Bus.

NOTES:

1. Increase the above A.C. timings by a maximum of 1.5 ns when the slew rate control pin is asserted high.
2. The EBB outputs driving the EISA bus, identified by a 240 pF load, are guaranteed using a distributed load (refer to Section 10.0).

3.3.2 A.C. CHARACTERISTIC WAVEFORMS

A.C. TESTING INPUT, OUTPUT WAVEFORM



NOTE:

1. The input waveforms have $t_r \leq 2.5$ ns from 0V to 3V.

1

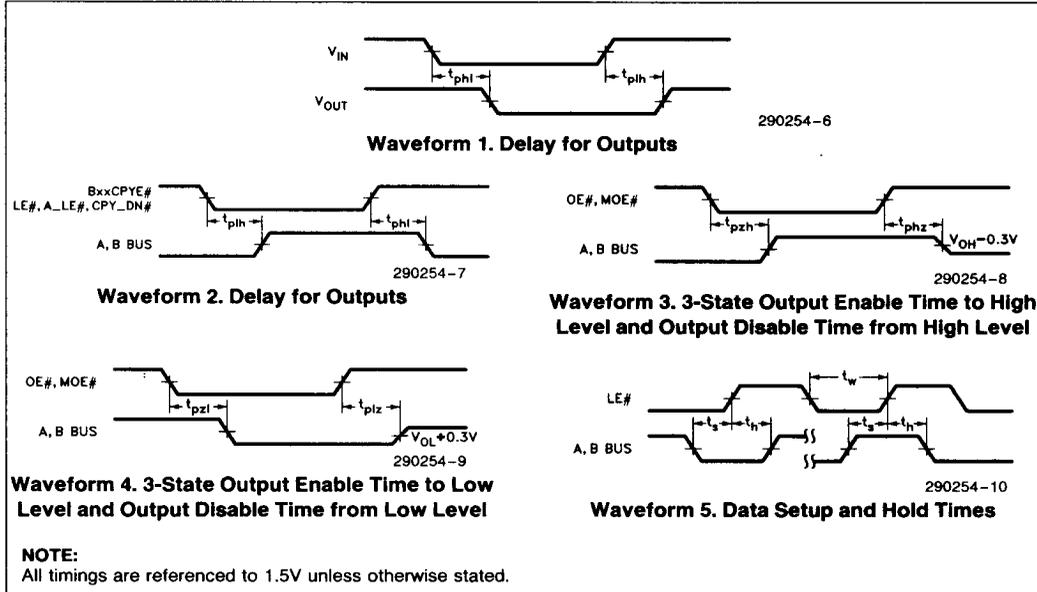


Figure 5. Mode 0

3.4 Pin Summary

The following table identifies the signals required for the EBB to operate in its non-parity 32-bit data mode:

Signal Name	No. of Pins	Signal Type
A-BUS	32	B
B-BUS	32	HCB
MOE#	1	I
Ax_OE#	4	I
ABx_OE#	4	I
A_LE#	1	I
Ax_LE#	4	I
B01_LE#	1	I
B23_LE#	1	I
CPY_DN#	1	I
B01CPYE#	1	I
B02CPYE#	1	I

Signal Name	No. of Pins	Signal Type
B03CPYE#	1	I
B13CPYE#	1	I
SLEW	1	I
MODE <1..0>	2	I
GND	14	Ground
V _{CC}	7	Power
N/C	11	
	120	
Pin Summary:	88	Signals Power & Ground N/C
	21	
	11	

3.5 Mode 0: 120-Pin Package Pinout

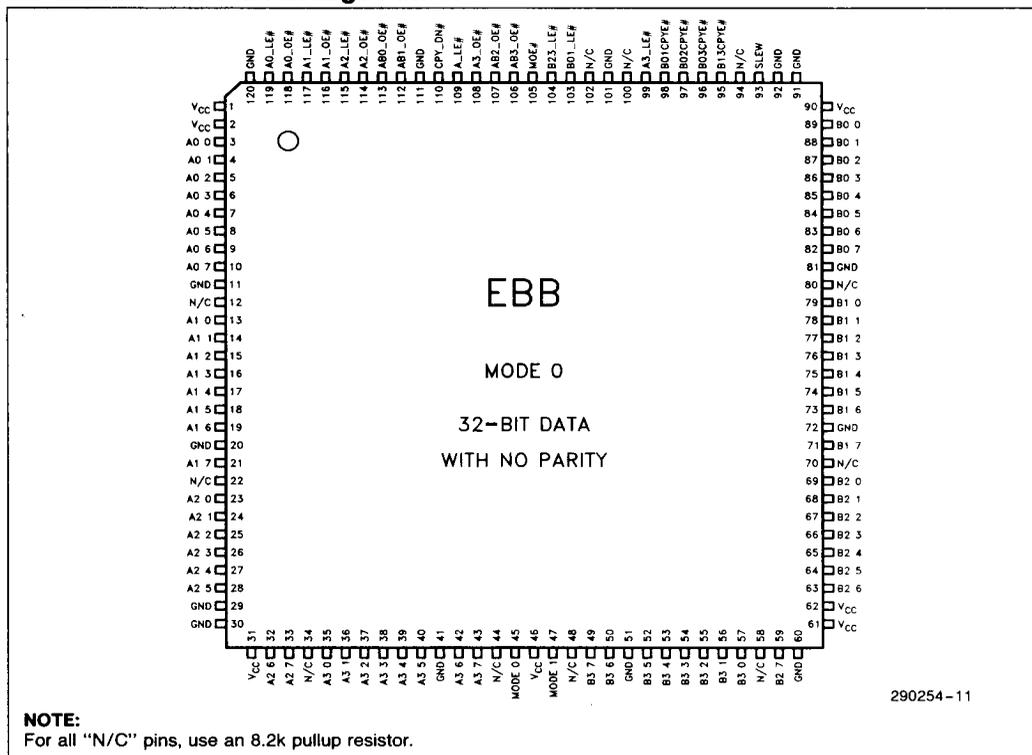


Figure 6. 120-Pin Package Pinout

4.0 MODE 1: 32-BIT DATA MODE WITH PARITY DETAILED PIN DESCRIPTION

4.1 Detailed Pin Description

The following table contains detailed descriptions of each signal while the EBB is in its 32-bit data mode with parity support. Note: For all "N/C" pins, use an 8.2K pullup resistor.

Symbol	# Pins	Type	Function												
A-BUS	32	B	<p>One of the two 32-bit buses manipulated by the EBB. Each of the four bytes in A-BUS (A0<7..0>, A1<7..0>, A2<7..0> and A3<7..0>) can be independently controlled. During non-copy transfers, the signal associations are:</p> <table style="margin-left: auto; margin-right: auto;"> <tr> <td>A0</td> <td>B0</td> </tr> <tr> <td>A1</td> <td>B1</td> </tr> <tr> <td>A2</td> <td>B2</td> </tr> <tr> <td>A3</td> <td>B3</td> </tr> </table>	A0	B0	A1	B1	A2	B2	A3	B3				
A0	B0														
A1	B1														
A2	B2														
A3	B3														
B-BUS	32	HCB	<p>One of the two 32-bit buses manipulated by the EBB. Each of the four bytes in B-BUS (B0<7..0>, B1<7..0>, B2<7..0> and B3<7..0>) can be independently controlled. During non-copy transfers, the signal associations are:</p> <table style="margin-left: auto; margin-right: auto;"> <tr> <td>B0</td> <td>A0</td> </tr> <tr> <td>B1</td> <td>A1</td> </tr> <tr> <td>B2</td> <td>A2</td> </tr> <tr> <td>B3</td> <td>A3</td> </tr> </table>	B0	A0	B1	A1	B2	A2	B3	A3				
B0	A0														
B1	A1														
B2	A2														
B3	A3														
MOE #	1	I	<p>Master Output Enable. This signal is "ORed" with all other output enables used in this mode of operation. When asserted (low), this signal will allow the other output enables to function. When negated (high), all EBB outputs will go into their High-Z states.</p>												
Ax_OE #	4	I	<p>Ax Output Enables. When MOE # is low, these signals enable the output of the Ax. The signal associations are:</p> <table style="margin-left: auto; margin-right: auto;"> <tr> <td>A0_OE #</td> <td>A0</td> </tr> <tr> <td>A1_OE #</td> <td>A1</td> </tr> <tr> <td>A2_OE #</td> <td>A2</td> </tr> <tr> <td>A3_OE #</td> <td>A3</td> </tr> </table>	A0_OE #	A0	A1_OE #	A1	A2_OE #	A2	A3_OE #	A3				
A0_OE #	A0														
A1_OE #	A1														
A2_OE #	A2														
A3_OE #	A3														
ABx_OE #	4	I	<p>Ax to Bx Output Enables. When MOE # is low, these signals enable the outputs of the Bx buffers during data transfers from the A-BUS to the B-BUS. The signal associations are:</p> <table style="margin-left: auto; margin-right: auto;"> <tr> <td>AB0_OE #</td> <td>A0</td> <td>B0</td> </tr> <tr> <td>AB1_OE #</td> <td>A1</td> <td>B1</td> </tr> <tr> <td>AB2_OE #</td> <td>A2</td> <td>B2</td> </tr> <tr> <td>AB3_OE #</td> <td>A3</td> <td>B3</td> </tr> </table>	AB0_OE #	A0	B0	AB1_OE #	A1	B1	AB2_OE #	A2	B2	AB3_OE #	A3	B3
AB0_OE #	A0	B0													
AB1_OE #	A1	B1													
AB2_OE #	A2	B2													
AB3_OE #	A3	B3													
A_LE #	1	I	<p>A-BUS Latch Enable. This signal is "ORed" with the Ax_LEH # latch enables. When asserted (low), this signal will allow all the Ax latch enables to function. When negated (high), all the A-BUS latches will latch the input data present at the time of the low to high transition if the individual Ax_LEH latch enable is asserted (high) at the time of this transition.</p> <p style="text-align: center;">NOTE:</p> <p>The Ax latch enables are inverted in this mode. (Refer to Figure 2.)</p>												

Symbol	# Pins	Type	Function																
Ax_LEH	4	I	<p>Ax Latch Enables. When A__LE# is low, these signals are used to control the latching of B-BUS data to the A-BUS. For non-copy transfers, the signal associations are:</p> <p style="text-align: center;">NOTE:</p> <p>The Ax latch enables are inverted in this mode. (Refer to Figure 2.)</p> <table style="margin-left: auto; margin-right: auto;"> <tr> <td>A0_LEH</td> <td>B0</td> <td>A0</td> </tr> <tr> <td>A1_LEH</td> <td>B1</td> <td>A1</td> </tr> <tr> <td>A2_LEH</td> <td>B2</td> <td>A2</td> </tr> <tr> <td>A3_LEH</td> <td>B3</td> <td>A3</td> </tr> </table>	A0_LEH	B0	A0	A1_LEH	B1	A1	A2_LEH	B2	A2	A3_LEH	B3	A3				
A0_LEH	B0	A0																	
A1_LEH	B1	A1																	
A2_LEH	B2	A2																	
A3_LEH	B3	A3																	
B01_LE#	1	I	<p>B01 and B1 Latch Enable. This signal is used to control the latching of A0 and A1 bus groups to the B0 and B1 bus groups respectively. On the asserted to negated (low to high) transition, data present at the latch inputs will be latched onto the latch output.</p>																
B23_LE#	1	I	<p>B2 and B3 Latch Enable. This signal is used to control the latching of A2 and A3 bus groups to the B2 and B3 bus groups respectively. On the asserted to negated (low to high) transition, data present at the latch inputs will be latched onto the latch output.</p>																
CPY_DN#	1	I	<p>Bus Group Copy Down. This signal determines the direction of data flow for data appearing on the four Bx copy transceivers. When asserted (low), the transceivers will allow the following potential data transfers:</p> <table style="margin-left: auto; margin-right: auto;"> <tr> <td>Transceiver-1:</td> <td>From B1 to B0, A0 D-Latch</td> </tr> <tr> <td>Transceiver-2:</td> <td>From B2 to B0, A0 D-Latch</td> </tr> <tr> <td>Transceiver-3:</td> <td>From B3 to B0, A0 D-Latch</td> </tr> <tr> <td>Transceiver-4:</td> <td>From B3 to B1, A1 D-Latch</td> </tr> </table> <p>When negated (high), the transceivers will allow the following potential data transfers:</p> <table style="margin-left: auto; margin-right: auto;"> <tr> <td>Transceiver-1:</td> <td>From B0 to B1, A1 D-Latch</td> </tr> <tr> <td>Transceiver-2:</td> <td>From B0 to B2, A2 D-Latch</td> </tr> <tr> <td>Transceiver-3:</td> <td>From B0 to B3, A3 D-Latch</td> </tr> <tr> <td>Transceiver-4:</td> <td>From B1 to B3, A3 D-Latch</td> </tr> </table> <p>It is recommended that only these combinations be used to swap data between the A-bus and the B-bus.</p>	Transceiver-1:	From B1 to B0 , A0 D-Latch	Transceiver-2:	From B2 to B0 , A0 D-Latch	Transceiver-3:	From B3 to B0 , A0 D-Latch	Transceiver-4:	From B3 to B1 , A1 D-Latch	Transceiver-1:	From B0 to B1 , A1 D-Latch	Transceiver-2:	From B0 to B2 , A2 D-Latch	Transceiver-3:	From B0 to B3 , A3 D-Latch	Transceiver-4:	From B1 to B3 , A3 D-Latch
Transceiver-1:	From B1 to B0 , A0 D-Latch																		
Transceiver-2:	From B2 to B0 , A0 D-Latch																		
Transceiver-3:	From B3 to B0 , A0 D-Latch																		
Transceiver-4:	From B3 to B1 , A1 D-Latch																		
Transceiver-1:	From B0 to B1 , A1 D-Latch																		
Transceiver-2:	From B0 to B2 , A2 D-Latch																		
Transceiver-3:	From B0 to B3 , A3 D-Latch																		
Transceiver-4:	From B1 to B3 , A3 D-Latch																		
B01CPYE#	1	I	<p>B-BUS Copy Enable 01. When MOE# is low, this signal enables copy Transceiver-1 to transfer data between B0 and B1. The data direction is determined by the logic value of CPY_DN#.</p>																
B02CPYE#	1	I	<p>B-BUS Copy Enable 02. When MOE# is low, this signal enables copy Transceiver-2 to transfer data between B0 and B2. The data direction is determined by the logic value of CPY_DN#.</p>																
B03CPYE#	1	I	<p>B-BUS Copy Enable 03. When MOE# is low, this signal enables copy Transceiver-3 to transfer data between B0 and B3. The data direction is determined by the logic value of CPY_DN#.</p>																
B13CPYE#	1	I	<p>B-BUS Copy Enable 13. When MOE# is low, this signal enables copy Transceiver-4 to transfer data between B1 and B3. The data direction is determined by the logic value of CPY_DN#.</p>																
SLEW	1	I	<p>Output Buffer Slew Rate Control. This signal will provide slew rate control for all external output buffers used in the EBB. When this signal is negated (low), all output buffers will switch at their non-compensated slew rate. When this signal is asserted (high), the output buffers will switch at a slower (> 2 ns) slew rate.</p> <p style="text-align: center;">NOTE:</p> <p>When the Slew signal is asserted (high), add 1.5 ns to all A.C. timings.</p>																

Symbol	# Pins	Type	Function															
MODE<1..0>	2	I	<p>Operating Mode Pins. These signals determine the mode of operation for the EBB. They are intended to be hardwired to the proper value. Operating mode determination:</p> <table> <thead> <tr> <th>Mode<1></th> <th>Mode<0></th> <th>Operating Mode</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>32-Bit Wide Data Mode w/o Parity</td> </tr> <tr> <td>#L</td> <td>H</td> <td>32-Bit Wide Data Mode with Parity</td> </tr> <tr> <td>H</td> <td>L</td> <td>RESERVED</td> </tr> <tr> <td>H</td> <td>H</td> <td>EISA Address Mode</td> </tr> </tbody> </table> <p># Mode described in this section</p>	Mode<1>	Mode<0>	Operating Mode	L	L	32-Bit Wide Data Mode w/o Parity	#L	H	32-Bit Wide Data Mode with Parity	H	L	RESERVED	H	H	EISA Address Mode
Mode<1>	Mode<0>	Operating Mode																
L	L	32-Bit Wide Data Mode w/o Parity																
#L	H	32-Bit Wide Data Mode with Parity																
H	L	RESERVED																
H	H	EISA Address Mode																
PARITY<3..0>	4	HCB	<p>During data transfers from the B-BUS to the A-BUS, these signals are generated within the EBB to provide even byte parity information. During data transfers from the A-BUS to the B-BUS, these signals are EBB inputs and are used to determine if even byte parity is received by the EBB. During non-copy transfers, the signal associations are:</p> <table> <tbody> <tr> <td>PARITY<0></td> <td>A0</td> <td>B0</td> </tr> <tr> <td>PARITY<1></td> <td>A1</td> <td>B1</td> </tr> <tr> <td>PARITY<2></td> <td>A2</td> <td>B2</td> </tr> <tr> <td>PARITY<3></td> <td>A3</td> <td>B3</td> </tr> </tbody> </table> <p>NOTE: Parity is not supported during Bx to Bx byte copies.</p>	PARITY<0>	A0	B0	PARITY<1>	A1	B1	PARITY<2>	A2	B2	PARITY<3>	A3	B3			
PARITY<0>	A0	B0																
PARITY<1>	A1	B1																
PARITY<2>	A2	B2																
PARITY<3>	A3	B3																
PE#<3..0>	4	O	<p>Parity Error. When active (low), these signals will identify incorrect parity for any of the Ax bus groups. PE#<3..0> are valid when the associated ABx__OE# are active. The signal associations are:</p> <table> <tbody> <tr> <td>PE#<0></td> <td>A0</td> <td>AB0__OE#</td> </tr> <tr> <td>PE#<1></td> <td>A1</td> <td>AB1__OE#</td> </tr> <tr> <td>PE#<2></td> <td>A2</td> <td>AB2__OE#</td> </tr> <tr> <td>PE#<3></td> <td>A3</td> <td>AB3__OE#</td> </tr> </tbody> </table>	PE#<0>	A0	AB0__OE#	PE#<1>	A1	AB1__OE#	PE#<2>	A2	AB2__OE#	PE#<3>	A3	AB3__OE#			
PE#<0>	A0	AB0__OE#																
PE#<1>	A1	AB1__OE#																
PE#<2>	A2	AB2__OE#																
PE#<3>	A3	AB3__OE#																
PE__SUM#	1	O	<p>Parity Error Sum. This signal will go active (low) when any valid PE#<3..0> signals goes active (low).</p>															

1

4.2 D.C. Specifications

4.2.1 MAXIMUM RATINGS

Temperature Under Bias -65° to +110°C
 Storage Temperature -65°C to +150°C
 Supply Voltage
 with Respect to Ground..... -0.5V to +7V
 Voltage on Any Pin -0.5V to +7V

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.2.2 D.C. SPECIFICATION TABLE

The following is a table of load capacitances, input voltage levels, current levels, and input leakage currents for the 32-bit parity mode:

T_A = 0°C to +70°C, V_{CC} = 5V ±5%, I_{CC} Max = 190 mA⁽⁸⁾

Signal Name	Pins	Type	I _{OL} Max (mA)	I _{OH} Max (mA)	I _I Max μA	V _I Max (V)	V _H Min (V)	C _{IN} ⁽⁷⁾ (pF)	C _{LOAD} (pF)
A-BUS<31..0>	8	B	12	-3	10	0.8/0.5	2.0/2.4	27	150
B-BUS<31..0>	8	HCB	24	-3	10	0.8/0.5	2.0/2.4	27	100
MOE#	1	I	N/A	N/A	10	0.8	2.0	27	N/A
Ax_OE#	4	I	N/A	N/A	10	0.8	2.0	27	N/A
ABx_OE#	4	I	N/A	N/A	10	0.8	2.0	27	N/A
A_LE#	1	I	N/A	N/A	N/A	0.8	2.0	27	N/A
Ax_LEH	4	I	N/A	N/A	10	0.8	2.0	27	N/A
B01_LE#	1	I	N/A	N/A	10	0.8	2.0	27	N/A
B23_LE#	1	I	N/A	N/A	10	0.8	2.0	27	N/A
CPY_DN#	1	I	N/A	N/A	10	0.8	2.0	27	N/A
B01CPYE#	1	I	N/A	N/A	10	0.8	2.0	27	N/A
B02CPYE#	1	I	N/A	N/A	10	0.8	2.0	27	N/A
B03CPYE#	1	I	N/A	N/A	10	0.8	2.0	27	N/A
B13CPYE#	1	I	N/A	N/A	10	0.8	2.0	27	N/A
MODE<1..0>	2	I	N/A	N/A	10	0.8	2.0	27	N/A
PARITY<3..0>	4	B	12	-3	10	0.8/0.5	2.0/2.4	27	150
PE#<3..0>	4	O	12	-3	10	0.5	2.4	N/A	100
PE_SUM#	1	O	12	-3	10	0.5	2.4	N/A	100

NOTES:

- I_I Max = I_{LI} for inputs, I_{LO} for outputs (or I/O).
- V_I Max = V_{IL} for inputs, V_{IL}/V_{OL} for I/O.
- V_H Min = V_{IH} for inputs, V_{IH}/V_{OH} for I/O.
- V_{IN} for leakage = 0.45V to V_{CC}.
- V_{OL} is tested while sinking I_{OL} (24 mA).
- V_{OH} is tested while sourcing I_{OH} (-3 mA).
- C_{IN} is Maximum Capacitance Value.
- Test with no loads.

4.3 A.C. Specifications

4.3.1 A.C. SPECIFICATION TABLE

Parameter	From	To	Waveform	Parameter Value	C _L Loading
t _{PLH} or t _{PHL}	A-BUS	B-BUS	1	12.5 ns Max	100 pF
t _{PLH} or t _{PHL}	B-BUS	A-BUS	1	16.00 ns Max	150 pF
t _{PLH} or t _{PHL}	B-BUS	B-BUS	1	16.00 ns Max	100 pF
t _{PLH} or t _{PHL}	BxxCPYE #	B-BUS	1, 2	16.00 ns Max	*100 pF
T _{PLH} or T _{PHL}	BxxCPYE #	A-BUS	1, 2	18.00 ns Max	**150 pF
t _{PLH} or t _{PHL}	CPY_DN #	B-BUS	1, 2	16.00 ns Max	*100 pF
T _{PLH} or T _{PHL}	CPY_DN #	A-BUS	1, 2	18.00 ns Max	**150 pF
t _{PLH} or t _{PHL}	LEH/A_LE #	A-BUS	1, 2	15.00 ns Max	150 pF
t _{PLH} or t _{PHL}	LE #	B-BUS	1, 2	15.00 ns Max	100 pF
t _{PLH} or t _{PHL}	A-BUS	PE #	3	16.00 ns Max	100 pF
t _{PLH} or t _{PHL}	A-BUS	PE_SUM #	3	20.00 ns Max	100 pF
t _{PLH} or t _{PHL}	B-BUS	PARITY	3	19.00 ns Max	150 pF
t _{PZH} or t _{PZL}	OE # or MOE #	A-BUS	4, 5	16.00 ns Max	150 pF
t _{PHZ} or t _{PLZ}	OE # or MOE #	A-BUS	4, 5	16.00 ns Max	150 pF
t _{PZH} or t _{PZL}	OE # or MOE #	B-BUS	4, 5	15.00 ns Max	100 pF
t _{PHZ} or t _{PLZ}	OE # or MOE #	B-BUS	4, 5	15.00 ns Max	100 pF
t _{SU}	A or B-BUS Data before LE		6	3.50 ns Min	
t _{SU-PE #}	Ax Data before LE		6	3.50 ns Min	
t _H			6	3.50 ns Min	
t _w	LE # Pulse Width (Low)		6	4.00 ns Min	

*Data originating from the A-Bus or B-Bus going to the B-Bus.

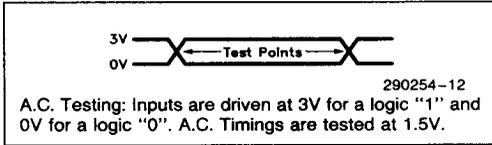
**Data originating from the B-Bus going to the A-Bus.

NOTE:

1. Increase the above A.C. timings by a maximum of 1.5 ns when slew rate control pin is asserted high.

4.3.2 A.C. CHARACTERISTIC WAVEFORMS

A.C. TESTING INPUT, OUTPUT WAVEFORM



NOTE:

1. The input waveforms have $t_r \leq 2.5$ ns from 0V to 3V.

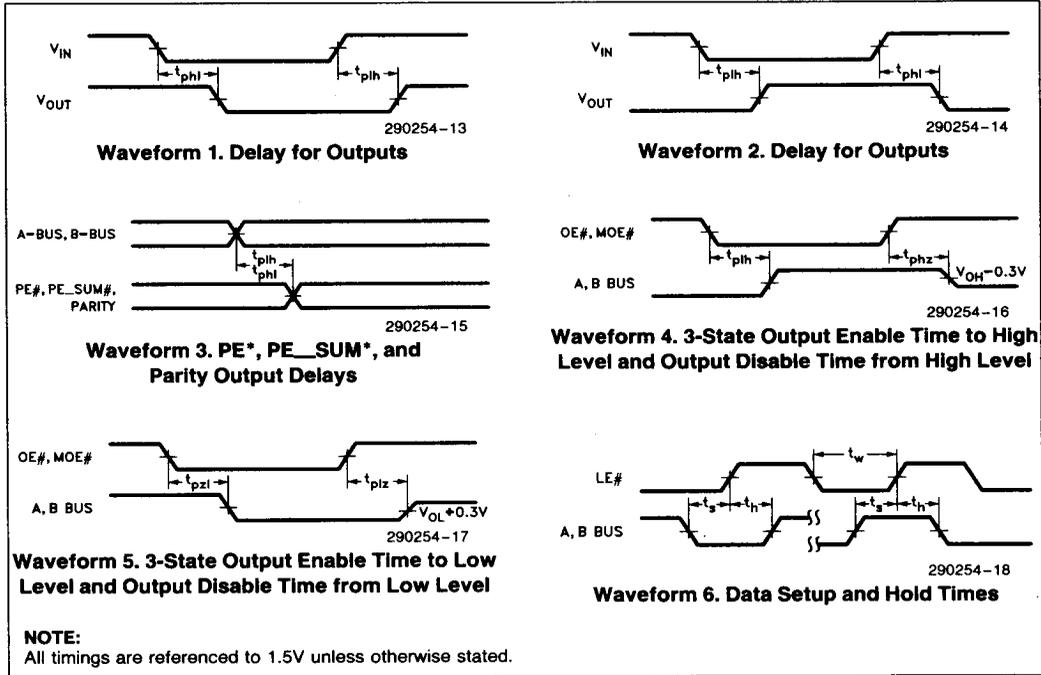


Figure 7. Mode 1

4.4 Pin Summary

The following table identifies the signals required for the EBB to operate in its 32-bit data mode with parity support:

Signal Name	No. of Pins	Signal Type
A-BUS	32	B
B-BUS	32	HCB
MOE#	1	I
Ax_OE#	4	I
ABx_OE#	4	I
A_LE#	1	I
Ax_LEH	4	I
B01_LE#	1	I
B23_LE#	1	I
CPY_DN#	1	I
B01CPYE#	1	I
B02CPYE#	1	I
B03CPYE#	1	I
B13CPYE#	1	I

Signal Name	No. of Pins	Signal Type
SLEW	1	I
MODE<1..0>	2	I
PARITY<3..0>	4	B
PE#<3..0>	4	O
PE_SUM#	1	O
GND	14	Ground
V _{CC}	7	Power
N/C	2	Signals Power & Ground N/C
Pin Summary:	120	
	97	
	21	
	2	

1

4.5 Mode 1: 120-Pin Package Pinout

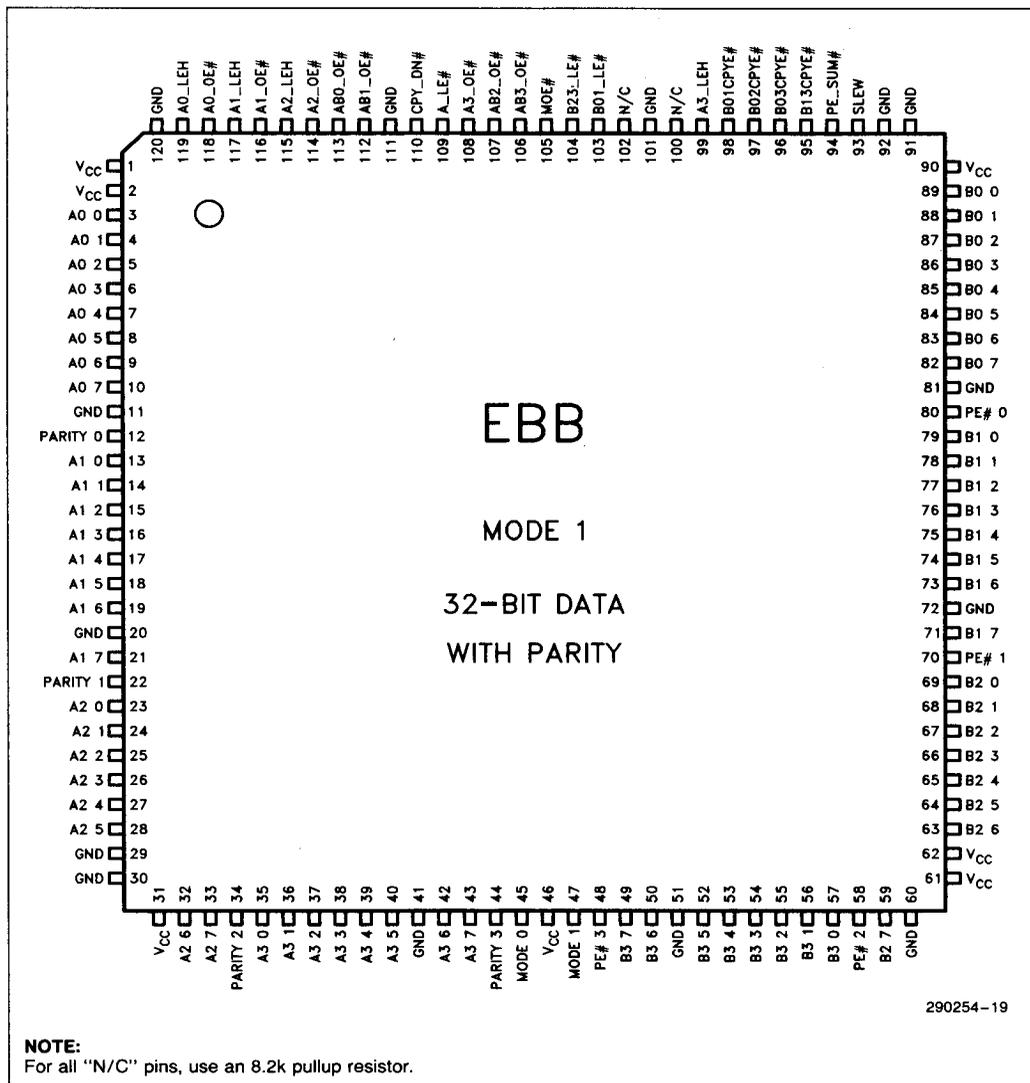


Figure 8. 120-Pin Package Pinout

5.0 MODE 3 DETAILED DESCRIPTION

5.1 Detailed Signal Description

The following table contains detailed descriptions of each signal while the EBB is in its EISA Address operating mode. Note: For all "N/C" pins, use an 8.2k pullup resistor.

Symbol	# Pins	Type	Function
A-BUS	31	B	One of three buses manipulated by the EBB in this mode. This bus is intended to interface with the host system bus as discussed in Section 2.3.1.
B-BUS	31	HCB	One of three buses manipulated by the EBB in this mode. This bus is intended to interface with the EISA LA bus as discussed in Section 2.3.1.
S-BUS	18	HCB	One of three buses manipulated by the EBB in this mode. This bus is intended to interface with the EISA SA bus as discussed in Section 2.3.1.
MOE #	1	I	Master Output Enable. This signal is "ORed" with all other output enables used in this mode of operation. When asserted (low), this signal will allow the other output enables to function. When negated (high), all EBB outputs will go into their high-Z states.
A__OE #	1	I	A-BUS Output Enable. This signal is used with MOE # to transfer address data onto the Host HA <31..2> address lines. When both MOE # and A__OE # are asserted (low), data present on the outputs of the A-BUS D-Latches is driven onto the external A-BUS pins. When either MOE # or A__OE # switch to their negated (high) state, the A-BUS drivers will transition to a high-Z state.
AB3__OE #	1	I	A3 to B3 # Output Enable. This signal is used with MOE # to transfer inverted Host HA <31..24> address data onto the EISA LA # <31..24> address bus. When both MOE # and AB3__OE # are asserted (low), A3 data present on the B3 # D-Latch outputs is driven onto the external B3 # pins. When either MOE # or AB3__OE # switch to their negated (high) state, the B3 # drivers will transition to a high-Z state.
B012OE #	1	I	A0, A1 and A2 to B0, B1 and B2 Output Enable. This signal is used with MOE # to: (1) transfer Host HA <23..2> address data onto the EISA LA <23..2> address pins and (2) make the HA <19..2> address data available to the inputs of the EISA SA <19..2> D-Latches. When both MOE # and B012OE # are asserted (low), the B0-B2 output buffers will drive data present on the B0-B2 D-Latch outputs onto the external B0-B2 pins. Simultaneously, the same data is presented to the S-BUS D-Latch inputs. When either MOE # or B012OE # are negated, B0-B2 buffer data is not available on the B0-B2 pins but B0-B2 external data will remain on the S-BUS latch inputs unless SB__OE # is asserted. (The external pins will typically assume a high-Z state.)

1

Symbol	# Pins	Type	Function															
S_OE#	1	I	S-BUS Output Enable. This signal is used with MOE# to transfer address data onto the EISA SA <19..2> address pins. When both MOE# and S_OE# are asserted (low), S-BUS output buffers will drive S-BUS D-Latch data to the respective S-BUS pins. When either MOE# or S_OE# switch to their deasserted (high) state, the S-BUS drivers will transition to a high-Z state.															
SB_OE#	1	I	S-BUS to B-BUS Output Enable. This signal is used with MOE# to: (1) transfer S-BUS address data onto the EISA LA <19..2> address pins and (2) make the S-BUS available to the inputs of the Host HA <19..2> D-Latches. When both MOE# and SB_OE# are asserted (low), the data present on the S-BUS is driven onto the B-BUS <19..2> external pins. Simultaneously, the same data is presented to the A-BUS <19..2> D-Latch inputs. When either MOE# or SB_OE# are negated, S-BUS data is not available on the B-BUS <19..2> pins and B-BUS data will appear on the A-BUS latch inputs unless B0123OE# is asserted. (The external pins will typically assume a high-Z state.)															
A_LE#	1	I	A-BUS Latch Enable. This signal is used to latch EISA LA <31..2> address data into the Host HA D-Latches. When A_LE# transitions from asserted to negated (low to high), B-BUS data is latched into the A-BUS D-Latches. This data will remain latched until A_LE# is reasserted.															
B01_LE#	1	I	B01 and B1 Latch Enable. This signal is used to control the latching of A0 and A1 bus groups to the B0 and B1 bus groups respectively. On the asserted to negated (low to high) transition, data present at the latch inputs will be latched onto the latch output.															
B23_LE#	1	I	B2 and B3 Latch Enable. This signal is used to control the latching of A2 and A3 bus groups to the B2 and B3 bus groups respectively. On the asserted to negated (low to high) transition, data present at the latch inputs will be latched onto the latch output.															
S_LE#	1	I	S-BUS Latch Enable. This signal is used to latch EISA LA <19..2> address data into the EISA SA D-Latches. When S_LE# transitions from asserted to negated (low to high), B-BUS data is latched into the S-BUS D-Latches. This data will remain latched until S_LE# is reasserted.															
SLEW	1	I	Output Buffer Slew Rate Control. This signal will provide slew rate control for all external output buffers used in the EBB. When this signal is negated (low), all output buffers will switch at their non-compensated slew rate. When this signal is asserted (high), the output buffers will switch at a slower (> 2 ns) slew rate. NOTE: When the Slew signal is asserted (high), add 1.5 ns to all A.C. timings.															
MODE <1..0>	2	I	Operating Mode Pins. These signals determine the mode of operation for the EBB. They are intended to be hardwired to the proper value. Operating mode determination: <table style="margin-left: 40px; border: none;"> <thead> <tr> <th>Mode <1></th> <th>Mode <0></th> <th>Operating Mode</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>32-Bit Wide Data Mode w/o Parity</td> </tr> <tr> <td>L</td> <td>H</td> <td>32-Bit Wide Data Mode with Parity</td> </tr> <tr> <td>H</td> <td>L</td> <td>RESERVED</td> </tr> <tr> <td>#H</td> <td>H</td> <td>EISA Address Mode</td> </tr> </tbody> </table> # Mode described in this section	Mode <1>	Mode <0>	Operating Mode	L	L	32-Bit Wide Data Mode w/o Parity	L	H	32-Bit Wide Data Mode with Parity	H	L	RESERVED	#H	H	EISA Address Mode
Mode <1>	Mode <0>	Operating Mode																
L	L	32-Bit Wide Data Mode w/o Parity																
L	H	32-Bit Wide Data Mode with Parity																
H	L	RESERVED																
#H	H	EISA Address Mode																

5.2 D.C. Specifications

5.2.1 MAXIMUM RATINGS

Temperature Under Bias -65° to +110°C
 Storage Temperature -65°C to +150°C
 Supply Voltage
 with Respect to Ground -0.5V to +7V
 Voltage on Any Pin -0.5V to +7V

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

5.2.2 D.C. SPECIFICATION TABLE

The following is a table of load capacitances, input voltage levels, current levels, and input leakage currents.

T_A = 0°C to +70°C, V_{CC} = 5V ±5%, I_{CC} Max = 115 mA⁽⁸⁾

Signal Name	Pins	Type	I _{OL} Max (mA)	I _{OH} Max (mA)	I _I Max μA	V _I Max (V)	V _H Min (V)	C _{IN} ⁽⁷⁾ (pF)	C _{LOAD} (pF)
A-BUS	30	B	12	-3	10	0.8/0.5	2.0/2.4	27	100
B-BUS	30	HCB	24	-3	10	0.8/0.5	2.0/2.4	27	240
S-BUS	18	HCB	24	-3	10	0.8/0.5	2.0/2.4	27	240
MOE#	1	I	N/A	N/A	10	0.8	2.0	27	N/A
A_OE#	1	I	N/A	N/A	10	0.8	2.0	27	N/A
AB3_OE#	1	I	N/A	N/A	10	0.8	2.0	27	N/A
AB012OE#	1	I	N/A	N/A	10	0.8	2.0	27	N/A
SB_OE#	1	I	N/A	N/A	10	0.8	2.0	27	N/A
S_OE#	1	I	N/A	N/A	10	0.8	2.0	27	N/A
B01_LE#	1	I	N/A	N/A	10	0.8	2.0	27	N/A
B23_LE#	1	I	N/A	N/A	10	0.8	2.0	27	N/A
A_LE#	1	I	N/A	N/A	10	0.8	2.0	27	N/A
S_LE#	1	I	N/A	N/A	10	0.8	2.0	27	N/A
MODE<1.0>	2	I	N/A	N/A	10	0.8	2.0	27	N/A

NOTES:

1. I_I Max = I_{LI} for inputs, I_{LO} for outputs (or I/O).
2. V_I Max = V_{IL} for inputs, V_{IL}/V_{OL} for I/O.
3. V_H Min = V_{IH} for inputs, V_{IH}/V_{OH} for I/O.
4. V_{IN} for leakage = 0.45V to V_{CC}.
5. V_{OL} is tested while sinking I_{OL} (24 mA).
6. V_{OH} is tested while sourcing I_{OH} (-3 mA).
7. C_{IN} is Maximum Capacitance Value.
8. Test with no loads.

5.3 A.C. Specifications

5.3.1 A.C. SPECIFICATION TABLE

Parameter	From	To	Waveform	Parameter Value	C _L Loading
t _{PLH} or t _{PHL}	A-BUS	B-BUS	1, 2	15.00 ns Max	240 pF
t _{PLH} or t _{PHL}	A-BUS	S-BUS	2	15.00 ns Max	240 pF
t _{PLH} or t _{PHL}	B-BUS	A-BUS	1, 2	15.00 ns Max	100 pF
t _{PLH} or t _{PHL}	B-BUS	S-BUS	2	15.00 ns Max	240 pF
t _{PLH} or t _{PHL}	S-BUS	A-BUS	2	15.00 ns Max	100 pF
t _{PLH} or t _{PHL}	S-BUS	B-BUS	2	15.00 ns Max	240 pF

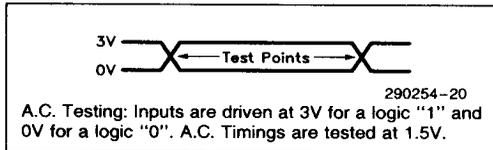


5.3.1 A.C. SPECIFICATION TABLE (Continued)

Parameter	From	To	Waveform	Parameter Value	C _L Loading
t _{PLH} or t _{PHL}	LE #	A-BUS	1, 2	15.00 ns Max	100 pF
t _{PLH} or t _{PHL}	LE #	B-BUS	1, 2	15.00 ns Max	240 pF
t _{PLH} or t _{PHL}	LE #	S-BUS	1, 2	15.00 ns Max	240 pF
t _{PZH} or t _{PZL}	OE # /MOE #	A-BUS	3, 4	16.00 ns Max	100 pF
t _{PHZ} or t _{PLZ}	OE # /MOE #	A-BUS	3, 4	15.00 ns Max	100 pF
t _{PZH} or t _{PZL}	OE # /MOE #	B-BUS	3, 4	15.00 ns Max	240 pF
t _{PHZ} or t _{PLZ}	OE # /MOE #	B-BUS	3, 4	15.00 ns Max	240 pF
t _{PZH} or t _{PZL}	OE # /MOE #	S-BUS	3, 4	15.00 ns Max	240 pF
t _{PHZ} or t _{PLZ}	OE # /MOE #	S-BUS	3, 4	15.00 ns Max	240 pF
t _{SU}	A/B/S-BUS Data before LE		5	3.50 ns Min	
t _H			5	3.50 ns Min	
t _W	All LE #	Pulse Width (Low)	5	4.00 ns Min	

NOTES:

1. Increase the above A.C. timings by a maximum of 1.5 ns when the slew rate control pin is asserted high.
2. The EBB outputs driving the EISA bus, identified by a 240 pF load, are guaranteed using a distributed load (refer to Section 10.0).

5.3.2 A.C. CHARACTERISTIC WAVEFORMS**A.C. TESTING INPUT, OUTPUT WAVEFORM****NOTE:**

1. The input waveforms have $t_r \leq 2.5$ ns from 0V to 3V.

5.3.2 A.C. CHARACTERISTIC WAVEFORMS (Continued)

A.C. TESTING INPUT, OUTPUT WAVEFORM (Continued)

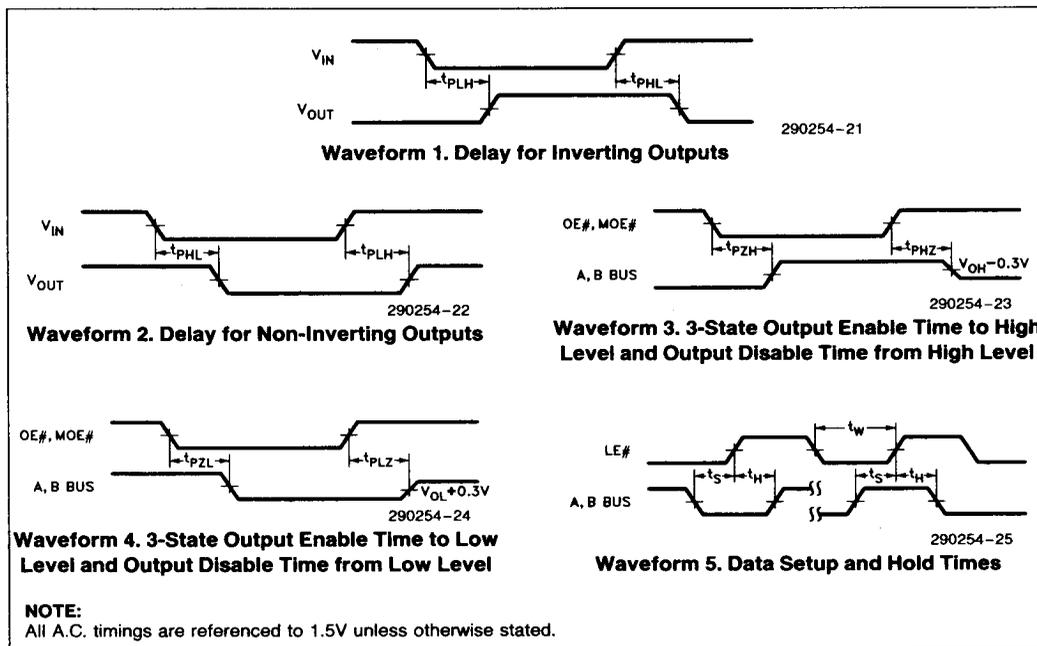


Figure 9. Mode 3

1

5.4 Pin Summary

The following table identifies the signals required for the EBB to operate in its EISA Address Mode of operation.

Signal Name	No. of Pins	Signal Type
A-BUS	31	I/O
B-BUS	31	I/O
S-BUS	18	I/O
MOE#	1	I
A_OE#	1	I
AB3_OE#	1	I
B012OE#	1	I
S_OE#	1	I
SB_OE#	1	I
A_LE#	1	I
B01_LE#	1	I
B23_LE#	1	I

Signal Name	No. of Pins	Signal Type
S_LE#	1	I
SLEW	1	I
MODE <1..0>	2	I
GND	14	Ground
V _{CC}	7	Power
N/C	6	Signals Power & Ground Reserved
Pin Summary:	120	
	91	
	21	
	8	

5.5 Mode 3: 120-Pin Package Pinout

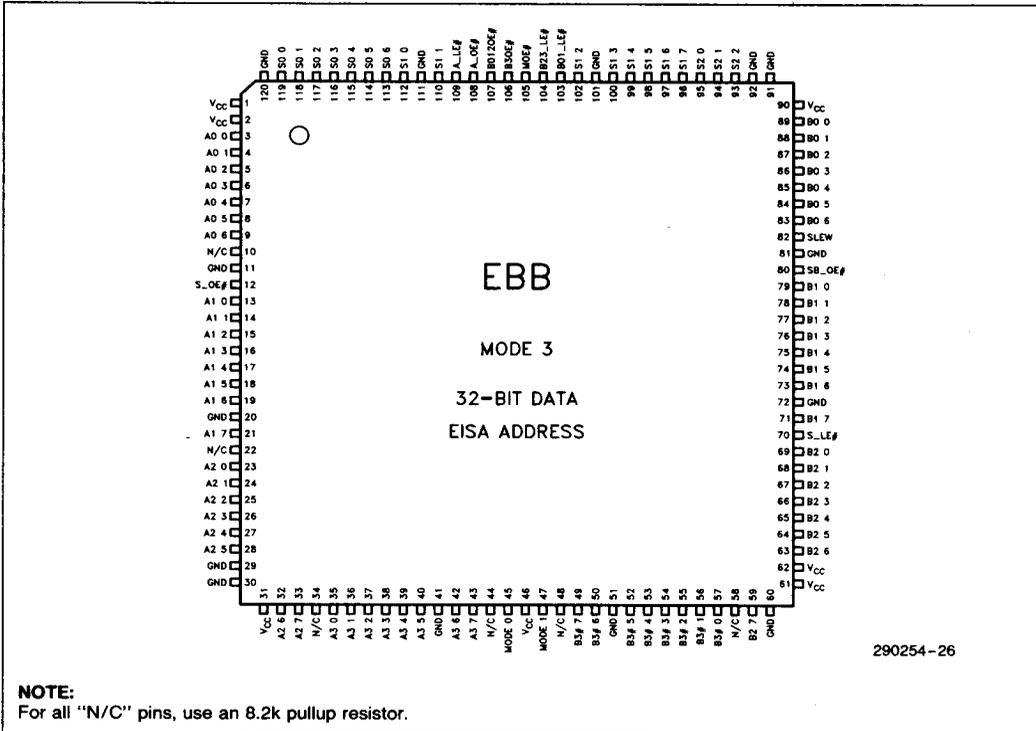


Figure 10. 120-Pin Package Pinout

6.0 82352 CRITICAL FEATURES

6.1 A-BUS Output Buffer Contention (16-Bit Host Application)

The A-BUS is capable of continuous operation where A0 is wired to A2, and A1 is wired to A3. When alternating between driving from A0 and A1 and from A2 and A3 respectively, one output enable is allowed to assert 5 ns before the other output enable negates, at a 4 MHz rate.

6.2 B-BUS Output Buffer Contention (B-Bus to B-Bus re-drive)

The B-Bus is capable of continuous execution of the data-latch and re-drive cycles. For re-drive cycles, the EBB is capable of securing data from the B-Bus and then re-driving it back onto the B-Bus without glitching, while the original data is still driving the B-Bus. This capture and re-drive is accomplished by allowing the data to flow from the B-Bus to the A-Bus and, once the A-Bus has settled, open the A to B latch and assert the A to B output enable. In continuous operation the overlap time with the original data driver will have a 17% duty cycle.

For copy cases, the data is latched in the source byte lane and the copy enable is asserted both before and after the re-drive. No latching is done in the destination byte lanes.

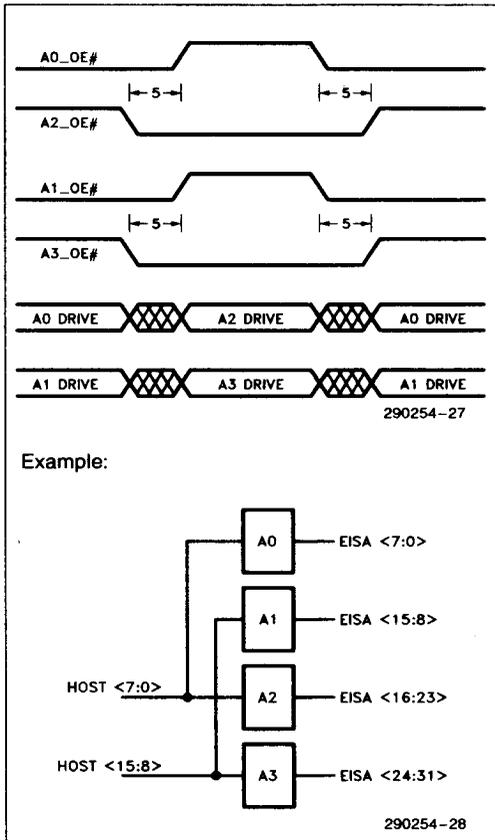


Figure 11. Alternating between Driving from A0 and A1 and from A2 and A3

1

7.0 82352 DEVICE PINOUT

Pin No.	Mode 0 32-Bit Data w/o Parity	Mode 1 32-Bit Data with Parity	Mode 3 Address
1	V _{CC}	V _{CC}	V _{CC}
2	V _{CC}	V _{CC}	V _{CC}
3	A0 0	A0 0	A0 0
4	A0 1	A0 1	A0 1
5	A0 2	A0 2	A0 2
6	A0 3	A0 3	A0 3
7	A0 4	A0 4	A0 4
8	A0 5	A0 5	A0 5
9	A0 6	A0 6	A0 6
10	A0 7	A0 7	N/C
11	GND	GND	GND
12	N/C	PARITY 0	S_OE#
13	A1 0	A1 0	A1 0
14	A1 1	A1 1	A1 1
15	A1 2	A1 2	A1 2
16	A1 3	A1 3	A1 3
17	A1 4	A1 4	A1 4
18	A1 5	A1 5	A1 5
19	A1 6	A1 6	A1 6
20	GND	GND	GND
21	A1 7	A1 7	A1 7
22	N/C	PARITY 1	N/C
23	A2 0	A2 0	A2 0
24	A2 1	A2 1	A2 1
25	A2 2	A2 2	A2 2
26	A2 3	A2 3	A2 3
27	A2 4	A2 4	A2 4
28	A2 5	A2 5	A2 5
29	GND	GND	GND
30	GND	GND	GND
31	V _{CC}	V _{CC}	V _{CC}
32	A2 6	A2 6	A2 6
33	A2 7	A2 7	A2 7
34	N/C	PARITY 2	N/C
35	A3 0	A3 0	A3 0
36	A3 1	A3 1	A3 1
37	A3 2	A3 2	A3 2
38	A3 3	A3 3	A3 3
39	A3 4	A3 4	A3 4
40	A3 5	A3 5	A3 5
41	GND	GND	GND
42	A3 6	A3 6	A3 6
43	A3 7	A3 7	A3 7
44	N/C	PARITY 3	N/C
45	MODE 0	MODE 0	MODE 0
46	V _{CC}	V _{CC}	V _{CC}

7.0 82352 DEVICE PINOUT (Continued)

Pin No.	Mode 0 32-Bit Data w/o Parity	Mode 1 32-Bit Data with Parity	Mode 3 Address
47	MODE 1	MODE 1	MODE 1
48	N/C	PE# 3	N/C
49	B3 7	B3 7	B3 7
50	B3 6	B3 6	B3 6
51	GND	GND	GND
52	B3 5	B3 5	B3 5
53	B3 4	B3 4	B3 4
54	B3 3	B3 3	B3 3
55	B3 2	B3 2	B3 2
56	B3 1	B3 1	B3 1
57	B3 0	B3 0	B3 0
58	N/C	PE# 2	N/C
59	B2 7	B2 7	B2 7
60	GND	GND	GND
61	V _{CC}	V _{CC}	V _{CC}
62	V _{CC}	V _{CC}	V _{CC}
63	B2 6	B2 6	B2 6
64	B2 5	B2 5	B2 5
65	B2 4	B2 4	B2 4
66	B2 3	B2 3	B2 3
67	B2 2	B2 2	B2 2
68	B2 1	B2 1	B2 1
69	B2 0	B2 0	B2 0
70	N/C	PE# 1	S_LE#
71	B1 7	B1 7	B1 7
72	GND	GND	GND
73	B1 6	B1 6	B1 6
74	B1 5	B1 5	B1 5
75	B1 4	B1 4	B1 4
76	B1 3	B1 3	B1 3
77	B1 2	B1 2	B1 2
78	B1 1	B1 1	B1 1
79	B1 0	B1 0	B1 0
80	N/C	PE# 0	SB_OE#
81	GND	GND	GND
82	B0 7	B0 7	SLEW
83	B0 6	B0 6	B0 6
84	B0 5	B0 5	B0 5
85	B0 4	B0 4	B0 4
86	B0 3	B0 3	B0 3
87	B0 2	B0 2	B0 2
88	B0 1	B0 1	B0 1
89	B0 0	B0 0	B0 0
90	V _{CC}	V _{CC}	V _{CC}

1

7.0 82352 DEVICE PINOUT (Continued)

Pin No.	Mode 0 32-Bit Data w/o Parity	Mode 1 32-Bit Data with Parity	Mode 3 Address
91	GND	GND	GND
92	GND	GND	GND
93	SLEW	SLEW	S2 2
94	N/C	PE_SUM#	S2 1
95	B13CPYE#	B13CPYE#	S2 0
96	B03CPYE#	B03CPYE#	S1 7
97	B02CPYE#	B02CPYE#	S1 6
98	B01CPYE#	B01CPYE#	S1 5
99	A3_LE	A3_LEH	S1 4
100	N/C	N/C	S1 3
101	GND	GND	GND
102	N/C	N/C	S1 2
103	B01_LE#	B01_LE#	B01_LE#
104	B23_LE#	B23_LE#	B23_LE#
105	MOE#	MOE#	MOE#
106	AB3_OE#	AB3_OE#	AB3_OE#
107	AB2_OE#	AB2_OE#	B012OE#
108	A3_OE#	A3_OE#	A_OE#
109	A_LE#	A_LE#	A_LE#
110	CPY_DN#	CPY_DN#	S1 1
111	GND	GND	GND
112	AB1_OE#	AB1_OE#	S1 0
113	AB0_OE#	AB0_OE#	S0 6
114	A2_OE#	A2_OE#	S0 5
115	A2_LE#	A2_LEH	S0 4
116	A1_OE#	A1_OE#	S0 3
117	A1_LE#	A1_LEH	S0 2
118	A0_OE#	A0_OE#	S0 1
119	A0_LE#	A0_LEH	S0 0
120	GND	GND	GND

NOTE:

For all "N/C" pins, use an 8.2k pullup resistor.

8.0 82352 PACKAGE DIMENSIONS

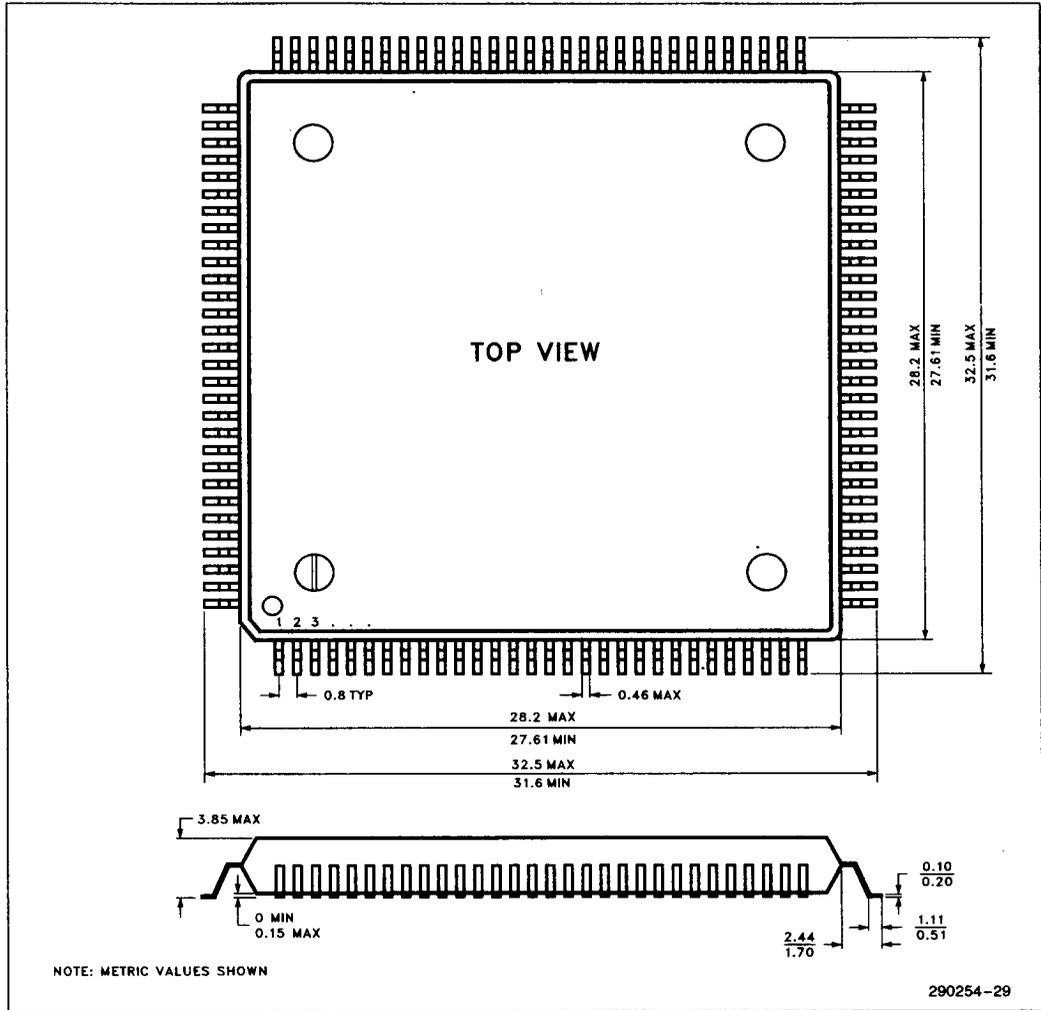


Figure 12. 82352 Package Dimensions

9.0 82352 PACKAGE THERMAL CHARACTERISTICS

Parameter	Air Flow Rate (Ft/Min)			
	0	100	250	500
θ_{JA}	63	48.9	41.9	34.3
θ_{JC}	18			

1

10.0 EISA BUS MODEL

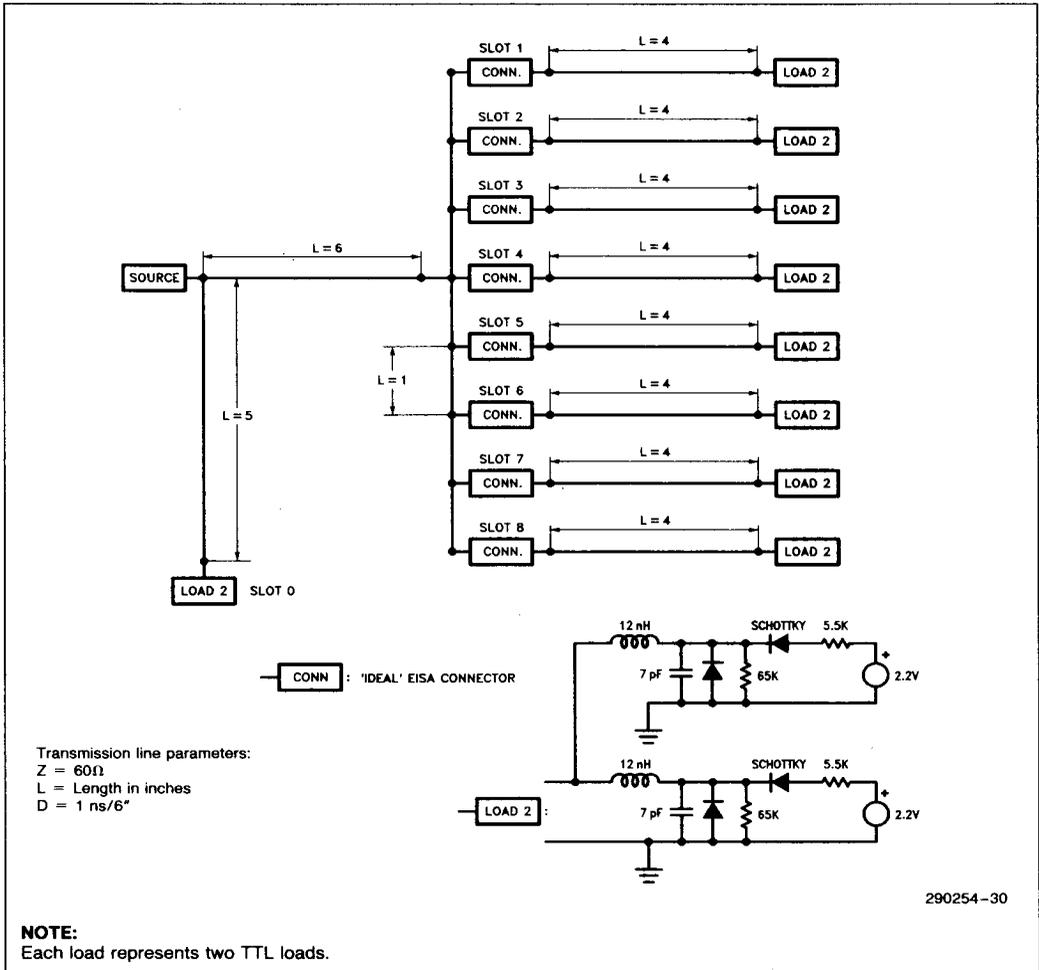


Figure 13. EISA Bus Model

11.0 FREQUENTLY USED ABBREVIATIONS

- I = Input Pin
- O = Output Pin
- B = Bidirectional Pin
- HCB = High Current Bidirectional Pin
- EBB = EISA Bus Buffer
- ISA = Industry Standard Architecture
- EISA = Enhanced Industry Standard Architecture
- QFP = Quad Flat Pack

12.0 82352 REVISION HISTORY

82352 Revision History

Section 3.2.2, Section 4.2.2, Section 5.2.2

Add note "tested with no loads" to I_{CC} Max. Add note "maximum capacitance value" to C_{IN} (pF).

82352 Revision Summary

The following changes have been made since revision 005:

- Section 2.1.1 The words "a discrete implementation" have been deleted from sentence 1. The sentence now reads, "Functionally, this 32-bit data mode is similar to using 74F543s and 74ALS245s."
- Section 3.1 Column heading "Pin No." on pin description table has been corrected to read "# Pins".
On symbol CPY__DN# function, one sentence has been added to the end. This sentence reads, "It is recommended that only these combinations be used to swap data between the A-bus and the B-bus."
- Section 4.1 Column heading "Pin No." on pin description table has been corrected to read "# Pins".
On symbol CPY__DN# function, one sentence has been added to the end. This sentence reads, "It is recommended that only these combinations be used to swap data between the A-bus and the B-bus."
- Section 5.1 Column heading "Pin No." on pin description table has been corrected to read "# Pins".
- Section 9.0 θ_{JC} Was added to the table.

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