82358
EISA BUS CONTROLLER (EBC)

- **Provides EISA/ISA Bus Cycle Compatibility**
  - **— EISA/ISA Standard Memory or I/O Cycle**
  - **— EISA/ISA Wait State Cycles**
  - **— ISA No Wait State Cycle**
  - **— EISA Burst Cycles**
- **Interfaces Host (CPU) Bus to EISA/ISA Bus**
- **Supports 386™ & i486™ Microprocessors**
  - **— 25 MHz & 33 MHz 386 Systems**
  - **— 25 MHz & 33 MHz i486 Systems**
- **Translates Host Bus Cycles to EISA/ISA Bus Cycles**
- **Generates ISA Signals for EISA Masters**
- **Generates EISA Signals for ISA Masters**
- **Supports 8-, 16-, or 32-Bit DMA Cycles**
  - **— Type A, B, or C (Burst) Cycles**
  - **— Compatible Cycles**
- **Supports Host and EISA/ISA Refresh Cycles**
- **Generates Control Signals for Address and Data Buffers**
- **Supports Byte Assembly/Disassembly for 8-, 16-, or 32-Bit Data Transfers**
- **Cache Controller (82385) Interface to Maximize Performance for 386 Based Systems**
- **Supports I/O Recovery Mechanism**
- **Generates 82385, CPU, and System Software Resets**
- **132-Pin PQFP Package**
- **Low Power CHMOS Technology**

The 82358 EISA Bus Controller (EBC) is part of Intel's 82350 EISA chip set. The EBC interfaces either the 386 or i486 microprocessor to the Extended Industry Standard Architecture (EISA) bus. The 82358 (EBC) is designed to facilitate bus cycles between the Host (CPU) and EISA/ISA bus. The EBC generates the appropriate data conversion and alignment control signals to implement an external byte assembly/disassembly mechanism for transferring data of equal or different widths between the Host, Industry Standard Architecture (ISA) and EISA busses. The EBC translates cycles between EISA, ISA and Host busses.

The EBC is tightly coupled with the 82357 DMA controller (ISP) to run 8-, 16-, or 32-bit EISA/ISA DMA transfers between busses. The EBC features special cache hardware interface signals to implement the highest performance 386 based system with the 82385 cache controller.

The EBC features hardware enforced I/O recovery logic to provide I/O recovery time between back to back I/O cycles.

The EBC provides resets to the 82385, 386, i486, and other devices in the system to provide an integrated synchronous system reset.

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October 1990
Order Number: 290252-003