82340DX ISA CHIP SET

- Three Chip ISA (Industry Standard Architecture) Chip Set Capable of Use in 386™ DX-Based System up to 33 MHz
  - — 82346 System Controller,
  - — 82344 ISA Bus Controller,
  - — 82345 Data Buffer
- Two 128-Pin and One 160-Pin (82344) Quad Flatpacks, 1.0- and 1.5-Micron CMOS
- Memory Control of One to Four Banks of 32-Bit DRAM Using 256k, 1M, or 4M Components Allowing 64 Mbytes on System Board
- Page Mode DRAM Operation on Any Number of Banks
- Two/Four-Way Interleaving or Direct Access on System Board Memory
- Programmable Option for Block or Word Interleave
- Programmable DRAM Timing Parameters
- Remap Option Allows Logical Reordering of System Board DRAM Banks
- System Board Refresh Optionally Decoupled from Slot Bus Refresh
- Staggered Refresh Minimizes Power Supply Load Variations
- Built-In "Sleep" Mode Features, Including Use of Slow Refresh DRAMs in Power Critical Operations
- Hardware Supports Full LIM EMS 4.0 Spec over Entire 64 Mbyte Memory Map
- DMA Expanded to Allow Transfers over 64M range
- Shadow RAM Support in 16k Increments over Entire 64k to 1M range
- Support for 387™ DX
- Coprocessor Software Reset Can Be Disabled
- Internal Switching and Programmable CLK2 Support for *PC/AT-Compatible and "Turbo" Modes
- Programmable Drive Reduces the Need for External Buffering on DRAM and Slot Bus Interface Signals
- ISA Bus Control of 386 DX-Based PC/AT-Compatibles. Capable of Asynchronous or Synchronous Bus Operation to 16 MHz
- Compatible with *Lotus 1-2-3 Version 3.0 in 1M Systems
- Bus "Quiet" Mode Assures That Slot Bus Signal Lines Are Driven Only During Slot Accesses
- Integrated Peripheral Functions:
  - — Two 82C37A DMA Controllers with Extended 74LS612 Page Register
  - — Two 82C59A Interrupt Controllers
  - — One 82C54 Timer
  - — One 146818 Real Time Clock
- Additional 64 Bytes of Battery Backed RAM in RTC Provides for Non-Volatile Storage of 82340DX Chip Set Configuration Data and User Specific Information
- Supports 8- or 16-Bit Wide BIOS ROMs
- Cache Support for Posted Writes
- System Memory on MD or D Bus in Non-Cached Systems
- Separate Parity Generation/Checkers for High Speed Operation
- Internal I/O Programmable for 10- or 16-Bit Decode
- Three-State Control Pins Added for Board Level Testability

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Block Diagram