T-49-17-34

ET2000 386/486 WB
Chipset Specifications

Process technology used	0.8μ CMOS
CPUs supported	Intel 80486, 80486SX AMD Am386DX Am486DX Cyrix 486DLC
CPU speed supported	16/20/25/33/40/50 MHz
CPU speed supported in 386 system (No external PALS required)	Intel 80387/ Cyrix/IIT/ULSI/ WEITEK 3167
Coprocessors supported in 486 system (No external PALS required)	WEITEK 4167
AT clock generation	Async/Sync
Programmable AT bus clock	Yes
Hardware/Software turbo switching	Yes
Page Mode DRAM control	Yes
Double word interleave control	Yes
DRAM type supported	256K/1M/4M/16M
Mixing DRAMS	Yes
Concurrent and AT Refresh	Yes
Shadow RAM range maximum size/block size	256 KB/64KB
Support EISA/ISA bus compatibility	Yes
Support Local Bus	Yes
PQFP package:	ETISP - 184 ETCMC, ETEBC, ETEDB -160
Maximum Physical DRAM	256MB

Programmable wait states	Yes
On chip cache controller	Yes
Support 8kx8 and 8kx9 Tag RAM	Yes
Cache update scheme	Write back
Cache organization	Direct mapped
Data cache size	32KB- 1MB
Non-cacheable support	Yes
Each non-cacheable region size	512KB-32MB
Zero wait state cache read hit	Yes
Zero wait state cache write hit	Yes
SRAM Burst mode support 2-1-1-1, 2-2-2-2, 3-1-1-1, 3-2-2-2	Yes
DRAM Burst mode support	Yes
External TTL component	11 ~ 13
SRAM speed required @ 50MHz	20ns
SRAM speed required @ 40MHz	20ns
SRAM speed required @ 33MHz	20ns
SRAM speed required @ 25MHz	35ns
AENx generator	Yes
Fast gate A20	Yes
Fast reset	Yes

1900 McCarthy Boulevard, Suite 110
Milpitas, California 95035 USA
FAX (408) 432-8146 , Tel (408) 432-8147

ETEQ

Microsystems, Inc.