386/AT CHIPSets

CS8230: 386/AT CHIPSet

- 100% IBM PC AT compatible
- Tightly coupled 80386 interface
  - —Designed to interface directly with the 80386
  - —Supports 16, 20 and 25MHz operation
- Operates in page mode, with interleave memory subsystem
- Independent clock to support correct AT bus timing
- Provides flexible processor clock selection
- Supports staggered and non-staggered refresh
- A complete 386/AT requires only 40 IC's plus memory
- Flexible Memory Architecture
  - —Supports memory configuration of up to 16MB
  - —Programmable wait states
  - —Supports 256K and 1MB DRAMs
  - —Supports page mode access with interleaved memory banks
  - —Supports zero wait state read hit operation
  - —Supports shadowing of BIOS EPROMs for efficient BIOS execution

CS8231: TURBO CACHE-BASED 386/AT CHIPSet

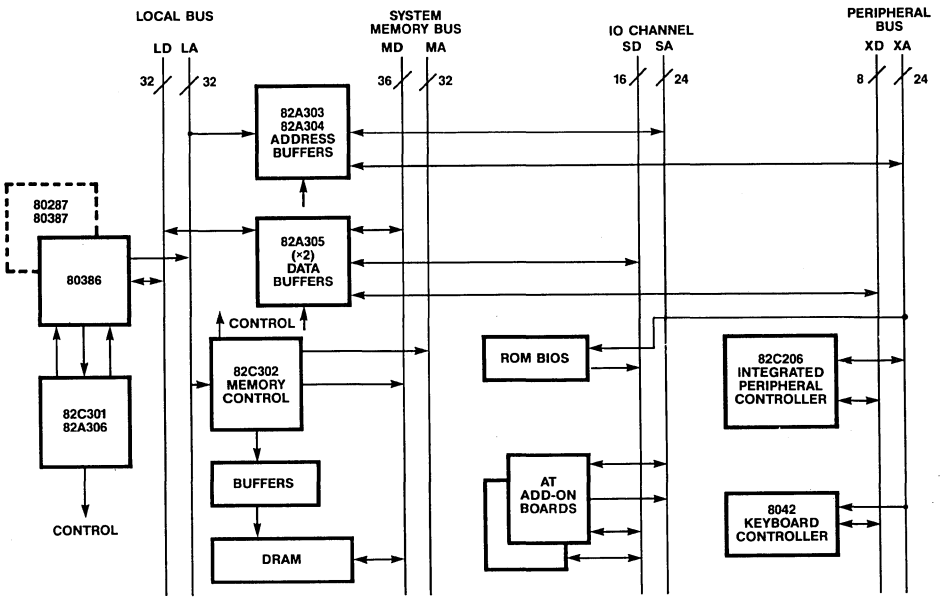
- 100% IBM PC AT compatible
- Tightly coupled 386 interface
  - —Designed to interface directly with the 80386
  - —Supports 16, 20 and 25MHz operation
- Independent clock to support AT bus timing
- A complete 386/AT CACHE BASED PC AT now requires only 40 IC's plus memory
- Integrates Cache Directory and CACHE/DRAM CONTROLLER on single chip to provide higher integration and performance
- Integrated CACHE/DRAM Controller enhances 80386 memory system performance
  - —Averages to nearly zero wait state memory access
  - —Zero wait state non-pipelined/pipelined read hit access
  - —Zero wait state non-pipelined/pipelined write access
  - —Buffered write-through DRAM update scheme to minimize write cycle penalty
- Supports 16KB/32KB two way set associative cache organization
  - —32 byte line size
  - —4 byte sub-lined size with associative valid bid
  - —Supports 4 blocks (of variable size—4KB/4MB) of main memory as non-cacheable address space
  - —Supports caching of data and code
- Supports control mechanism for preventing unnecessary disturbance of cache contents during I/O operation
- Flexible memory architecture
  - —Supports memory configuration up to 64MB
  - —Programmable wait states
  - —Supports 256K and 1MB DRAMs in configuration of up to 4 blocks of 4 banks
  - —Supports parity or Error Detection and Correction (EDC) schemes to provide a highly reliable system
- Supports shadowing of BIOS EPROMs
- Cache hit rate up to 99%

CS8230 386/AT CHIPSet
82C301 BUS CONTROLLER
82C302 PAGE/INTERLEAVE MEMORY CONTROLLER
82A303 HIGH ADDRESS BUFFER
82A304 LOW ADDRESS BUFFER
82B305 DATA BUFFER
82A306 CONTROL BUFFER

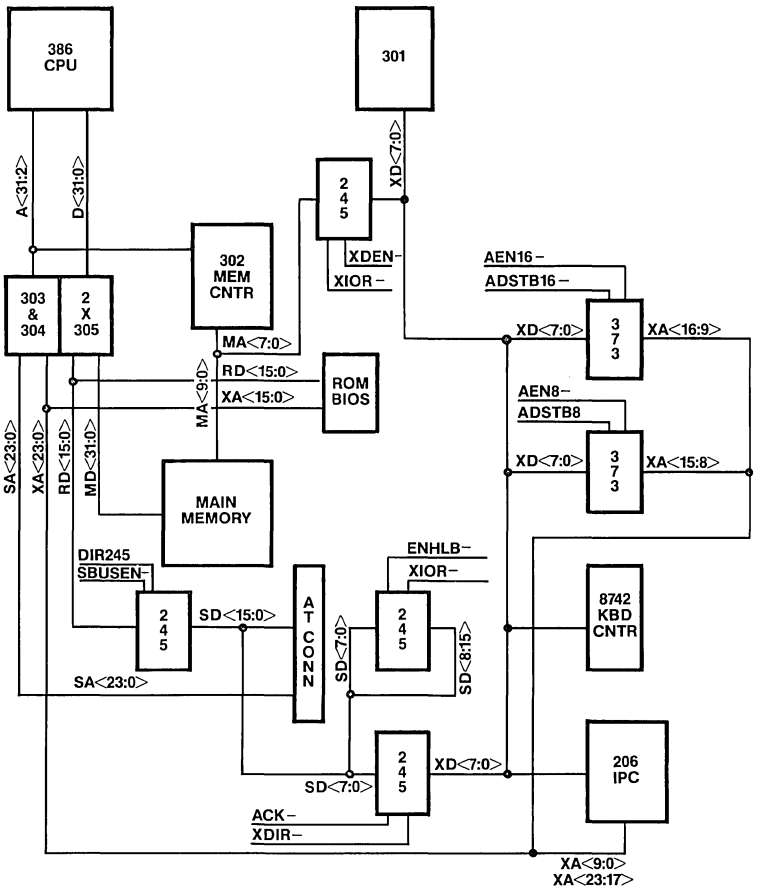
The CS8230-16-20-25 AT/386 CHIPSet™ is a seven chip VLSI implementation of most of the system logic to control an iAPX 386 based system. The CHIPSet is designed to offer a 100% PC AT compatible integrated solution. The flexible architecture of the CHIPSet allows it to be used in any iAPX386 based system design, such as CAD/CAE workstations, office systems, industrial and financial transaction systems.

CS8230 CHIPSet combined with CHIPs 82C206, Integrated Peripherals Controller, provides a complete PC AT compatible system using only 40 components plus memory devices.

The CS8230 CHIPSet™ consists of one 82C301 Bus Controller, one 82C302 Page/Interleave Memory Controller, one each of 82A303 and two 82A304 Address Bus Interfaces, two 82A305 or 82B305 Data Bus Interfaces, and a 82A306 Control Signal Buffer. An all CMOS CS8232-16, and CS8232-20 CHIPSet allow OEM's to reduce the form factor, size and weight of their portable, laptop machines due to the reduced power requirements, the reduced cooling requirements and the reduced buffering requirements of the CHIPSet. In particular, the all CMOS CS8232-16 and CS8232-20 CHIPSet will reduce a system's power consumption requirement by at least half that of an NMOS/BIPOLAR/CMOS based system.



AT/386 System Block Diagram



AT/386 Detailed Block Diagram Using the CS8230 CHIPSet

The only difference between the CS8232 CHIPSet and the CS8230 CHIPSet is that the bipolar parts (82A303, 82A304, 82A305, 82A306) in the CS8230 CHIPSet have been replaced with CMOS parts (82C303, 82C304, 82C305, 83C306). The difference between the new CMOS parts is that the drive capability is 12 mA as opposed to 24 mA in the bipolar parts.

The CHIPSet supports a local CPU bus, a 32-bit system memory bus, and AT buses as shown in the System Block Diagram. The 82C301 and 82A306/82C306 provide the generation and synchronization of control signals for all buses. The 82C301 also supports an independent AT bus clock, and allows for dynamic selection of the processor clock between the 16-20-25MHz clock and the AT bus clock. The 82A306 provides buffers for bus control signal in addition to other miscellaneous logic functions.

The 82C302 Page/Interleave Memory Controller provides an interleaved memory subsystem design with page mode operation. It supports 1 MB to 16 MB of DRAMs with combinations of 256Kbit and 1Mbit DRAMs. The processor can operate at 16-20-25 MHz with zero wait state memory accesses.

The 82A303/82C303 and 82A304/82C304 interface between all address buses and the addresses needed for proper data path conversion. Two 82A305/82C305/82B305 are used to interface between the local, system memory, and AT data buses. In addition to having high current drive, they also perform the conversion necessary between the different sized data paths.

System Overview

The CS8230 is designed for use in 80386-based systems and provides complete support for the IBM PC AT bus. There are four buses supported by the CS8230 as shown in the AT/386 system block diagram: the CPU local bus (A and D), the system memory bus (MA and MD), the IO Channel bus (SA and SD), and the X bus (XA and XD). The system memory bus is used to interface to DRAM's controlled by the 82C302. The IO channel bus refers to the bus supporting the AT bus adapters which could be either 8 bit devices or 16 bit devices. The X bus refers to the peripheral bus to which the DMA controllers and timers are attached in an IBM PC AT. The X bus has only an 8-bit data path. The term "AT bus" is used to refer to the IO channel bus and X bus. Provisions are also made for user extension of the IO channel to a 32 bit bus.

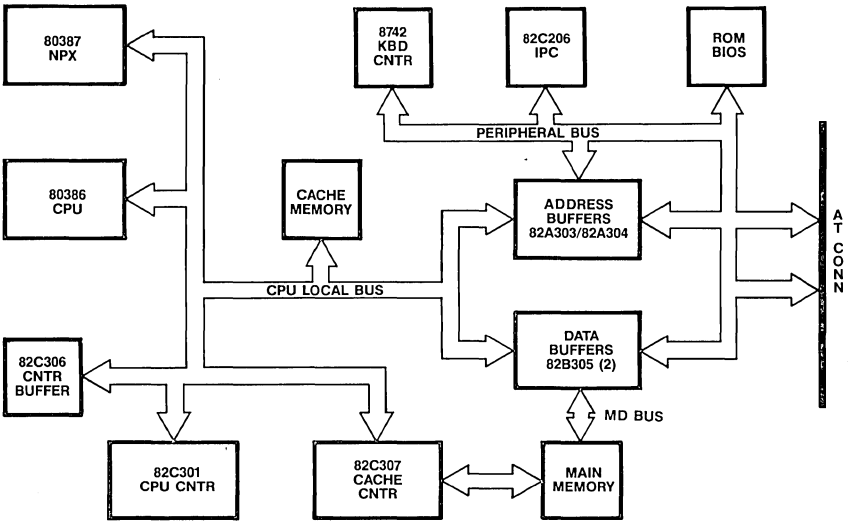
Notations and Glossary

The following notations are used to refer to the configuration and diagnostic registers internal to the 82C301 and 82C302.

REGnH denotes the internal register with the index n in hexadecimal notation.

REGnH<x:y> denotes the bit field from bits y to x of the internal register with the index n in hexadecimal notation.

CS8231: TURBO CACHE-BASED 386/AT CHIPSet
82C301 BUS CONTROLER
82A303 HIGH ORDER ADDRESS BUFFER
82A304 LOW ORDER ADDRESS BUFFER
82B305 DATA BUFFER
82A306 CONTROL BUFFER
82C307 INTEGRATED CACHE/DRAM CONTROLLER



Block Diagram of a Chips Turbo 386/AT Cache Based System

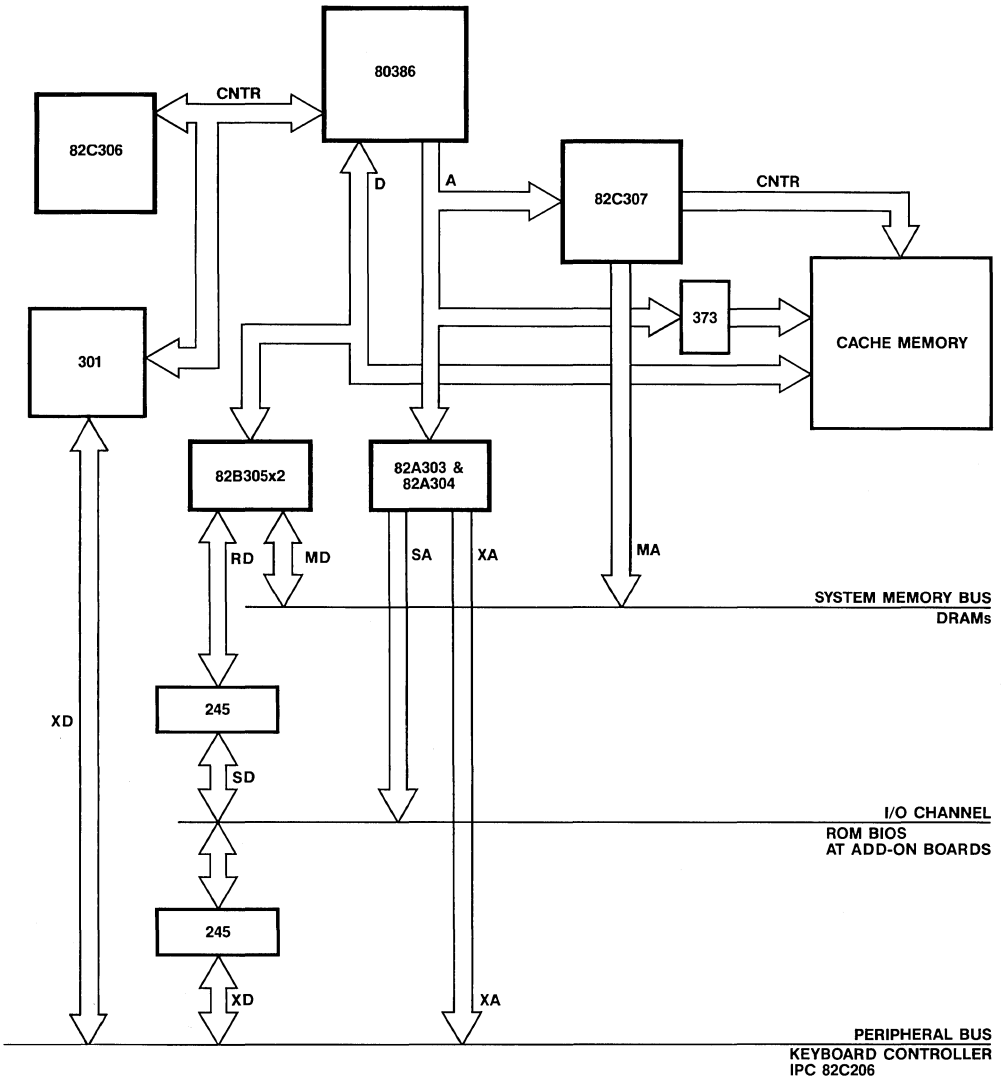
The CS8231 ***TURBO CACHE BASED*** 386/AT CHIPSet is a seven chip VLSI implementation of most of the system logic to implement a ***CACHE BASED*** iAPX 386 based system. The CHIPSet is designed to offer a 100% PC AT compatible integrated solution. The flexible architecture of the CHIPSet allows it to be used in any iAPX386 based system design, such as CAD/CAE workstations, office systems, industrial and financial transaction systems.

The CS8231 CHIPSet combined with CHIP's 82C206, Integrated Peripherals Controller, provides a complete PC AT compatible system using only 40 components plus memory devices.

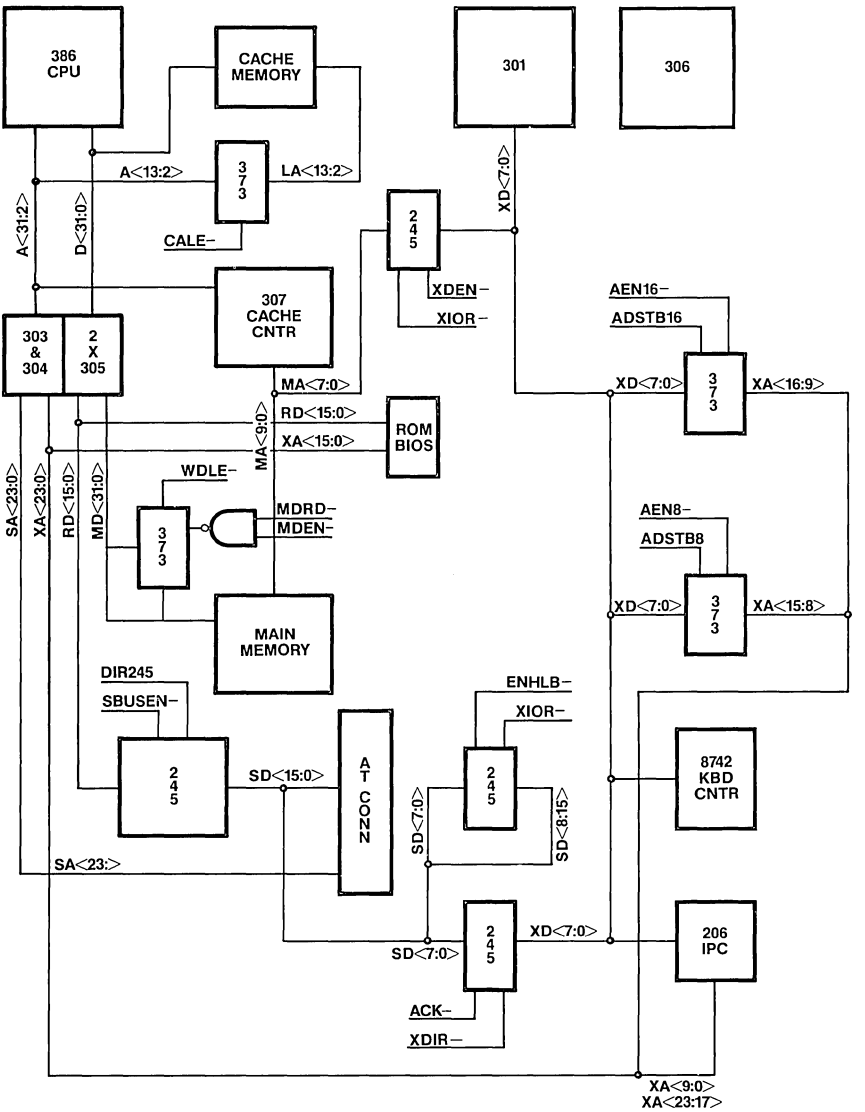
The CS8231 CHIPSet consists of one 82C301 Bus Controller, one 82C307 Integrated CACHE/DRAM controller, one each of 82A303 and 82A304 Address Bus Interfaces, two 82B305 Data Bus Interfaces, and a 82A306 Control Signal Buffer.

The CHIPSet supports a local CPU bus, a 32-bit system memory bus, and AT buses as shown in the system diagram below. The 82C301 and 82A306 provide the generation and synchronization of control signals for all buses. The 82C301 also supports an independent AT bus clock, and allows for dynamic selection of the processor clock between the 16MHz, 20MHz, or 25MHz clocks and the AT bus clock. The 82A306 provides buffers for bus control signals in addition to other miscellaneous logic functions.

The 82C307 is a high performance and high integration CACHE/DRAM controller designed to interface directly to the 80386 microprocessor. It maintains frequently accessed code and data in high speed memory, allowing the 80386 to operate at its maximum rated frequency with near zero waitstates. By



AT/386 Cache Based Block Diagram



AT/386 Cache Based Detailed Block Diagram

integrating DRAM control functions on-chip, it supports simultaneous activation of cache and DRAM access, thereby minimizing the cache miss cycle penalty. It has hardware support to allow the user to designate up to four blocks (of variable size from 2KB to 128KB) of main memory as non-cacheable address space. This feature is important for compatibility issues when operating in a multiprocessing or LAN environment, or where dual-port memory is used, and to designate certain regions of video RAM as non-cacheable. This feature eliminates the need to use very fast PALs externally to decode non-cacheable regions and gives the user much more flexibility. Optional EDC support logic is integrated on to the 82C307 which allows it to interface to any of the generically available 32-bit Error Detection and Correction Circuits to realize a highly reliable memory subsystem.

Cache coherency is maintained during DMA cycles by channeling all accesses through the cache controller logic. During DMA read operations, the cache RAM is not accessed and data is retrieved from the main memory. During DMA write operations, if a cache hit is detected, the cache RAM is updated and the corresponding tag validated. Cache coherency is maintained at all times, with no performance penalty. The 82C307 is available in a 100 pin PFP package.

The 82A303 and 32A304 interface between all address buses, and the addresses needed for proper data path conversion. Two 82B305 are used to interface between the local, system memory, and at data buses. In addition to having high current drive, they also perform the conversion necessary between the different sized data paths.

Following is a list of the parts shipped with each CHIPSet:

CS8230-16	**CS8230-20**	**CS8230-25**
82C301	82C301-20	82C301-25
82C302	82C302-20	82C302-25
82A303	82A303	82A303
82A304	82A304	82A304
82A305	82B305	82B305
82A306	82A306	82A306
CS8232-16	**CS8232-20**	**CS8232-25**
82C301	82C301-20	82C301-25
82C302	82C302-20	82C302-25
82C303	82C303	82C303
82C304	82C304	82C304
82C305	82C305	82B305
82C306	82C306	82C306
CS8236-16	**CS8236-20**	**CS8236-25**
82C301	82C301	82C301
82C302	82C302	82C302
82A303	82A303	82A303
82A304	82A304	82A304
82A305	82B305	82B305
82A306	82A306	82A306
82C206	82C206	82C206
	CS8231-20	**CS8231-25**
	82C301	82C301
	82A303	82A303
	82A304	82A304
	82B305	82B305
	82A306	82A306
	82C307	82C307
	CS8237-20	**CS8237-25**
	82C301	82C301
	82A303	82A303
	82A304	82A304
	82B305	82B305
	82A306	82A306
	82C307	82C307
	82C206	82C206

82C301 Bus Controller

- Optional Independent AT Bus Clock
- Processor Clock Selection
- AT Bus Timing Configuration
- CPU Interface and Bus Control
- Port B Register

Overview

The 82C301 provides a clock generation circuitry to solve two basic problems. One is to provide system designers the choice of a particular AT bus clock most adequate for their applications. The other is to allow the processor to run at the full speed and optionally at a speed to match timing dependent application software. Because many AT adapter boards are designed with built in timing assumptions, independent programmable controls are provided for AT bus command timing and wait state generation for IO accesses and for 8, 16, and 32 bit memory accesses.

The 82C301 interfaces directly with the 80386 and implements the state machines required for controlling all bus accesses. It also features a status register known as Port B register used in a standard IBM PC AT.

Functional Description

The 82C301 has the following function blocks as illustrated in figure 1-1:

- Clock generation and reset control
- CPU bus access state machine
- AT bus access state machine
- Port B register and NMI logic
- Bus Arbitration and refresh logic

Clock Generation and Selection Logic

The 82C301 provides a flexible clock selection scheme as shown in Figure 1.2. It has two inputs; CLK2IN and ATCLK1. CLK2IN is driven from a packaged crystal oscillator circuit, running at twice the processor rated CPU frequency (32 MHz for a 16 MHz 80386). An oscillator circuit is provided for the ATCLK1 signal, so that it can be connected to either a packaged oscillator or a crystal. Typically, the ATCLK1 should be of a lower frequency than CLK2IN.

The 82C301 generates processor clock, CLK2, for driving the 80386 CLK2 input as well as the CPU state machine. SCLK is CLK2/2 and is in phase with the internal states of the 80386. BCLK (internal) is the AT bus state machine clock and is used for the AT bus interface. SYSCLK is the AT bus system clock and is always BCLK/2.

CLK2 can be derived from CLK2IN or from the ATCLK1. In the synchronous mode, both CLK2 and BCLK are derived from CLK2IN, so that the processor state machine and the AT state machine run synchronously. In the asynchronous mode, BCLK is generated from the ATCLK1 and CLK2 is generated from CLK2IN or the ATCLK1. In this case, the processor state machine and the AT state machine run asynchronous to each other. The following clock selections are possible:

Synchronous mode

1. CLK2 = CLK2IN
   BCLK = CLK2IN/2
   SYSCLK = BCLK/2 = CLK2IN/4

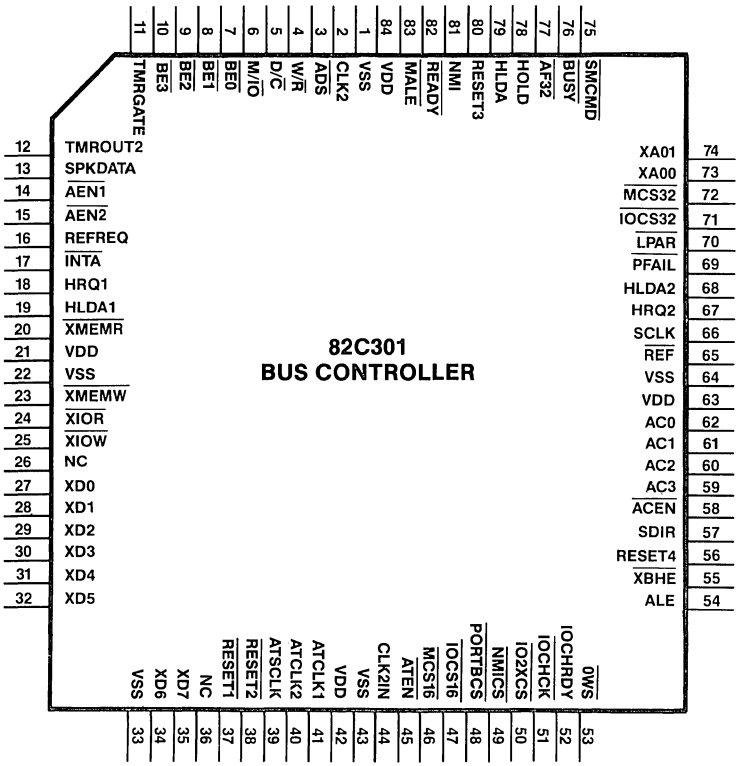
2. CLK2 = CLK2IN
   BCLK = CLK2IN/3
   SYSCLK = BCLK/2 = CLK2IN/6

3. CLK2 = BCLK = CLK2IN/2
   SYSCLK = BCLK/2 = CLK2IN/4

Asynchronous mode

1. CLK2 = CLK2IN
   BCLK = ATCLK1
   SYSCLK = BCLK/2 = ATCLK1/4

Under normal operation, CLK2IN should be selected as the processor clock (CLK2) to allow the processor to operate at the rated maximum speed. BCLK can either be a subdivision of CLK2IN or be derived from the ATCLK1. ATCLK may be selected to generate the CLK2 only when it is desired to slow


82C301
BUS CONTROLLER
1 VSS
2 CLK2
3 ADS
4 W/R
5 D/C
6 M/IO
7 BE0
8 BE1
9 BE2
10 BE3
11 TMRGATE
12 TMROUT2
13 SPKDATA
14 AEN1
15 AEN2
16 REFREQ
17 INTA
18 HRQ1
19 HLDA1
20 XMEMR
21 VDD
22 VSS
23 XMEMW
24 XIOR
25 XIOW
26 NC
27 XD0
28 XD1
29 XD2
30 XD3
31 XD4
32 XD5
33 VSS
34 XD6
35 XD7
36 NC
37 RESET1
38 RESET2
39 ATCLK
40 ATCLK2
41 ATCLK1
42 VDD
43 VSS
44 CLK2IN
45 ATEN
46 MCS16
47 IOCS16
48 PORTBCS
49 NMICS
50 IO2XCS
51 IOCHCK
52 IOCHRDY
53 0WS
54 ALE
55 XBHE
56 RESET4
57 SDIR
58 ACEN
59 AC3
60 AC2
61 AC1
62 AC0
63 VDD
64 VSS
65 REF
66 SCLK
67 HRQ2
68 HLDA2
69 PFAIL
70 LPAR
71 IOCS32
72 MCS32
73 XA00
74 XA01
75 SMCMD
76 BUSY
77 AF32
78 HOLD
79 HLDA
80 RESET3
81 NMI
82 READY
83 MALE
84 VDD

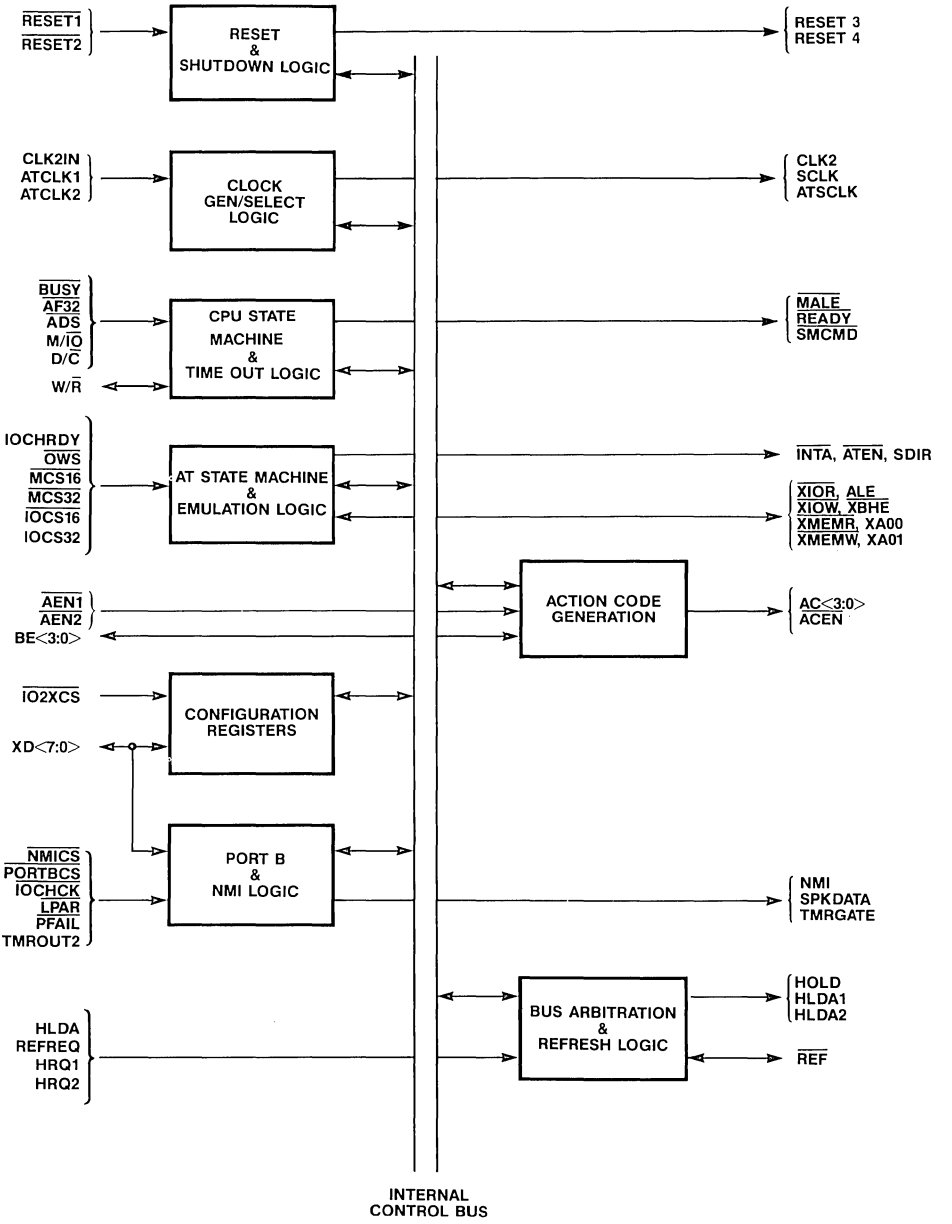


Figure 1-1. 82C301 Functional Block Diagram

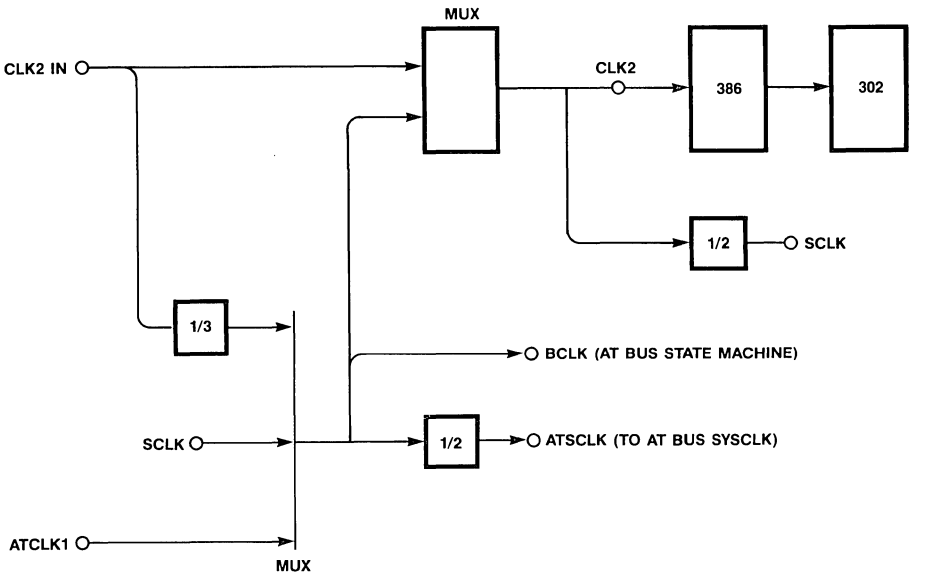


Figure 1-2. CLK2 and ATSCLK Clock Selection

down the processor for timing dependent code execution. Once the options for clock selections are set, the clock switching occurs with clean transition in the synchronous or the asynchronous mode. During clock switching, no phases of CLK2 are less than the minimum value or greater than the maximum value specified for the 80386 CPU. The clock source selection is made by writing to REG 4H<4> and REG 6H<1:0>, which defaults to:

CLK2 = CLK2IN
SYSCLK = CLK2IN/6

Table 1-1. Examples of BCLK and SYSCLK derived from CLK2

CLK2IN	SCLK	Ratio	BCLK	SYSCLK
24	12	/2	12	6
32	16	/2	16	8
32	16	/3	10.7	5.4
40	20	/2	20	10
50	25	/3	16.7	8.4

Reset and Shutdown Logic

Two reset inputs $\overline{\text{RESET1}}$ and $\overline{\text{RESET2}}$ are provided on the 82C301 bus controller. $\overline{\text{RESET1}}$ is the Power Good signal from the power supply. When $\overline{\text{RESET1}}$ is active, the 82C301 asserts RESET3 and RESET4 for a system reset. $\overline{\text{RESET2}}$ is generated from the 8042 (or 8742) keyboard controller when a "warm reset" is required. The warm reset activates RESET3 to reset the 80386 CPU. RESET3 is also activated by the 82C301 when a shutdown condition is detected.

RESET3 is asserted for at least 85 CLK2 cycles during power on reset and for during warm reset. RESET4 is used to reset the AT bus, 82C206 IPC, 8042 keyboard controller, 82C302 page interleaved memory controller, and 82C307 Cache/DRAM controller. It is synchronized with respect to CLK2 and is asserted as long as the power good signal is held low. After a shut down condition is detected, RESET3 is asserted and is held

high for at least 85 CLK2 cycles and then deasserted. RESET3 resulting from a shut down condition is synchronous with respect to CLK2, ensuring proper CPU operation. Both RESET3 and RESET4 meet the setup and hold time requirements of the 80386 CPU.

Bus Arbitration

The 82C301 controls all bus activity and provides arbitration between CPU, DMA/ Master devices, and DRAM refresh logic. It handles HRQ1, HRQ2 and REFREQ by generating a hold request to the CPU and arbitrating among these requests in a non-preemptive manner. The CPU relinquishes the bus by issuing HLDA. The 82C302 or 82C307 responds by issuing HLDA1, HLDA2 or REF depending on the requesting device. During refresh cycles, the refresh logic has control of the bus until REF goes inactive. XMEMR is asserted low during a refresh cycle and the refresh addresses are provided on the MA0-MA9 address lines by the refresh address counter on the 82C302 or 82C307. During a DMA cycle, the DMA controller has control of the bus until HRQ goes inactive. During the HLDA cycle, the 82C301 generates both SMCMD and action code AC<3:0> to control the buffer enable and directions for the address and data buffers. Bus size conversions are not supported by the 82C301 for these bus cycles and if necessary, should be performed by the requesting device.

Action Code Generation Logic

The AT state machine performs the data conversions for CPU accesses to devices not on the local CPU or memory bus. The AT bus conversions are performed for 32, 16 or 8 bit read or write operations. 32 bit transfers are broken down into smaller 8 bit or 16 bit AT bus reads or writes. The action codes are generated as shown in table 5.2 to control the data bus buffers on the 82A305 data buffers. The action codes are in response to IOCS32, MCS32, IOCS16 and MCS16 inputs.

CPU and AT Bus State Machines

In order to extract maximum performance out of the 80386 on the system board, it is desirable to operate the processor at the maximum rated CPU frequency. This frequency may be too fast for the AT bus. In order to overcome this problem, the 82C301 supports two state machines: the CPU state machine which typically runs off CLK2 and the AT bus state machine which runs off the BCLK.

The CPU state machine and AT state machine control CPU accesses to the devices on the local bus and non-local buses respectively. The CPU state machine supports only 32 bit transfers between the 80386 and system memory (or memory mapped IO) and no bus size conversions are done. Thus the BS16 input on the 80386 is not used in CS8230 or CS8231 based systems and should be connected to a HI level. The AT state machine responsible for all non-local bus CPU accesses controls the AT bus and supports bus size matching.

All CPU access cycles are started by 82C301 asserting MALE. The CPU state machine then samples AF32 one SCLK clock cycle later. If AF32 is active, it is assumed to be a local bus cycle and the CPU state machine terminates this cycle when it detects READY signal active. In response to an MALE, if the AF32 is detected inactive the control is passed to AT state machine. At the end of the bus access cycle, the AT state machine generates READY to terminate the processor access cycle as well as the CPU state machine cycle.

CPU State Machine

The interface to the 80386 requires interpretation of the status lines upon assertion of ADS and synchronization and generation of a READY response to the CPU upon completion of the requested operation. By interpreting the CPU status lines and ADS, the 82C301 generates control signals MALE and SMCMD. In response to each ADS generated by the CPU, an MALE is generated by the 82C301 to indicate the start of a new CPU access cycle. In a non-pipelined CPU cycle, MALE is generated in response to ADS being asserted by the 80386. In a pipelined cycle, MALE is generated when the assertion of READY is detected for the previous CPU cycle. If AF32 is not active one cycle after MALE is asserted, control is passed to the AT bus state machine. The CPU state machine then waits for READY

becoming active to terminate the access cycle. In the CS8230 CHIPset, the READY can be generated by 82C302 or 82C307 which controls the system memory access.

SMCMD indicates a memory cycle for both CPU and non-CPU accesses. During CPU cycles it is generated for all memory cycles by decoding M/IO, D/C and W/R signals. During non-CPU cycles it is active when XMEMR or XMEMW is active.

NA Pipeline Control

The 82C301 supports both pipelined and non-pipelined cycles of the 80386. The NA (Next Address) input on the 80386 can be always asserted in a CS8230 system for higher performance.

Bus Timeout

An optional feature allows generation of an NMI if an internal memory cycle does not complete within a certain timeout period. This occurs if AF32 is asserted in response to MALE and READY is not returned to the 82C301 within 128 CLK2 cycles. A control bit in the 82C301 configuration registers enables this feature.

AT Bus State Machine

The AT state machine gains the control of the buses when AF32 is detected inactive by the CPU state machine. It uses BCLK having a frequency twice that of the IO channel clock SYSCLK. When ATCLK1 is selected as the source for BCLK, it also performs the necessary synchronization of control and status signals between the AT bus and the processor. The 82C301 supports 8, 16 or 32 bit transfers between the processor and 8, 16 or 32 bit memory or IO devices located on the IO channel.

An AT bus cycle is initiated by asserting ALE decoded from the CPU status signals and is terminated by asserting READY. On the falling (or trailing) edge of the ALE, MCS16, IOCS16, MCS32, IOCS32 are sampled to determine the bus size conversion required. It then enters the command cycle. The AT bus state machine provides the sequencing and timing controls for status and command phases of different AT bus cycles. These controls provide for timing emulation of lower speed IO channels to maintain compatibility with AT or PC/XT IO adapters and memory cards. The command cycle is terminated by detecting 0WS or IOCHRDY active.

IO Channel Speed Control

The AT state machine can be programmed to insert wait states in units of ATSCLK and to delay the generation of XIOR, XIOW, XMEMR, and XMEMW commands in one half units of ATSCLK (BCLK) within the selected wait states. The command phase delay can be selectively defined for IO cycles and for 8, 16, and 32 bit wide memory cycles by setting the corresponding fields in REG05H. REG06H controls the IO Channel wait state generation for 8, 16, and 32 bit accesses.

The bus clock BCLK is selected by setting REG06H<1:0>. It should be noted that the processor clock source should be set to CLK2IN whenever the BCLK is selected to be SCLK.

Data Conversion

The AT bus access state machine performs data conversion for CPU accesses to devices not on the local bus when AF32 is not asserted. AT bus data conversions are performed for the following types of transfers:

— 32 bit to 8/16 bit,
— 24 bit to 8/16 bit,
— 16 bit to 8/16 bit.

Larger transfers are broken into smaller AT bus reads or writes and the action code AC<3:0> to the 82A305/82B305/82C305 is generated. Byte addresses XA<01:00> are generated to drive the lower two bits of the AT address bus.

The 82C301 responds to IOCS16, MCS16, IOCS32, and MCS32 in determining what size of data the IO channel needs. If none of the above signals are asserted, 8 bit transfers are assumed and the request is converted into 2, 3 or 4 IO channel cycles based on BE<3:0>. For either MCS16 or IOCS16, the AT bus

state machine converts a 32-bit access into two 16 bit AT bus accesses.

The bus state machine also supports 32-bit transfer between the processor and memory and IO devices on the IO channel. IOCS32 and MCS32 inputs allow a device to request a 32-bits transfer. It is assumed that the necessary extensions to the AT bus are made to utilize this feature. IOCS32 and MCS32 override IOCS16 and MCS16.

In performing these data conversions, a 4-bit action code AC<3:0> is generated to control the buffers in 82A305 for the alignment of data path, and direction control between D, MD, and SD data buses. The definition for the action codes is given in the functional description of 82A305.

Port B Register

The 82C301 provides access to Port B defined for a PC AT as shown in figure 1-3. PORTBCS enables the access to Port B register and is provided as an output from 82A304. Table 1-2 gives the Port B register bit definition.

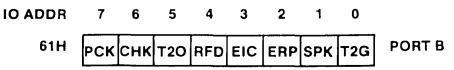


Figure 1-3 Port B register definition

The NMI sub-module performs the latching and enabling of I/O and parity error conditions, which will generate a non-maskable interrupt to the CPU if NMI is enabled. Reading Port B will indicate the source of the error condition (IOCK and PCHK). Enabling and disabling of NMI is accomplished by writing to the I/O address 070H. On the rising edge of XIOW, NMI will be enabled if data bit 7 (XD7) is equal to 1 and will be disabled if XD7 is equal to 0.

CS 8230 Internal Register Access Ports

The CS 8230 have internal registers used for system configuration and for diagnostics. These are accessed through IO ports 22H and 23H normally found in the interrupt controller. An indexing scheme is used to reduce the number of IO addresses required to access all registers needed to configure and control CS 8230 chips. Each access (either read or write) to an internal register is done by first writing its index into port 22H. This index then controls the multiplexers gating the appropriate register data accessible as port 23H. Every access to port 23H must be pre-

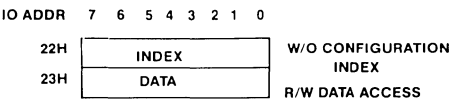


Figure 1-4. Configuration Register Access Ports

Addr	Bits	Function	
61H		Port B Register	
	7	Read only.	PCK - System memory parity check.
	6	Read only.	CHK - IO channel check.
	5	Read only.	T2O - Timer 2 out
	4	Read only.	RFD - Refresh Detect.
	3	Read/write.	EIC - Enable IO channel check.
	2	Read/write.	ERP - Enable system memory parity check.
	1	Read/write.	SPK - Speaker Data
	0	Read/write.	T2G - Timer 2 Gate Speaker

Table 1-2 Port B register definition

ceded by writing the index value to port 22H even if the same data port is being accessed again.

Configuration Registers

There are 3 bytes of configuration and diagnostic registers in 82C301 as shown in figure 1-5. The definitions for these registers are given in table 1-3.

INDEX	7	6	5	4	3	2	1	0	
04H	VERS		—	PC	FE	TE	PF	TO	VERSION/PROCESSOR CLOCK/NMI SOURCES
05H	M32		M15		M8		IO		COMMAND DELAY
06H	32 WS		16 WS		8 WS		B CLK		WAIT STATE/BUS CLOCK

Figure 1-5. 82C301 Internal Configuration Registers

Index	Bits	Function
04H		Version/Processor clock select/NMI source
	7:6	Read only. Version
		0 Initial version
	5	Reserved
	4	Processor Clock Select. If SCLK is selected as the source for BCLK, CLK2 source must not be selected as BCLK.
		0 Use processor oscillator input. Default. 1 Use AT bus state machine clock (SYSCLKx2).
	3	Power Fail Warning Enable
		0 Power Fail NMI not enabled. Default. 1 Power Fail NMI enabled
	2	Local Bus READY timeout NMI Enable
		0 READY timeout NMI not enabled. Default. 1 READY timeout NMI enabled
	1	Read only. Power Fail warning active during last NMI arbitration.
		0 Power Fail warning pin not active. Default. 1 Power Fail warning pin was active.
	0	Read only. Local bus READY timeout
		0 READY timeout has not occurred. Default. 1 READY timeout has occurred

Table 1-3 82C301 Configuration Register Definitions

Table 1-3. 82C301 Configuration Register Definitions (Continued)

Index	Bits	Function
05H		Command delay The value for each one of the command delay fields are defined as: 0 0 cycle delay 1 1 cycle delay 0 2 cycle delay 1 3 cycle delay
	7:6	AT Bus 32 bit memory command delay. Specifies between 0 to 3 BCLK cycles for command delay during an AT bus 32 bit memory cycle. Default is 00.
	5:4	AT Bus 16 bit memory command delay. Specifies between 0 to 3 BCLK cycles for command delay during an AT bus 16 bit memory cycle. Default is 00.
	3:2	AT Bus 8 bit memory command delay. Specifies between 0 to 3 BCLK cycles for command delay during an AT bus 8 bit memory cycle. Default is 01.
	1:0	AT Bus I/O Cycle command delay. Specifies between 0 to 3 BCLK cycles for command delay during an AT bus IO cycle. Default is 01.
06H		Wait State/Bus Clock Source
	7:6	32 bit AT Bus wait state selects 0 to 3 wait states per 32 bit transfer on the AT bus. Each wait state is 2 BCLK or 1 ATSCLK. Default is 3. 00 3 cycle delay 01 2 cycle delay 10 1 cycle delay 11 0 cycle delay
	5:4	16 bit AT Bus wait state selects 0-3 wait states per 16 bit transfer on the AT bus. Each wait state is 2 BCLK cycles. Default is 3. 00 3 cycle delay 01 2 cycle delay 10 1 cycle delay 11 0 cycle delay
	3:2	8 bit AT Bus wait state selects 2-5 wait states per 8 bit transfer on the AT bus. Each wait state is 2 BCLK cycles. Default is 5. 00 5 cycle delay 01 4 cycle delay 10 3 cycle delay 11 2 cycle delay
	1:0	Bus Clock Source Select 00 Use Proc Clock/3 for AT bus state machine. Default. 01 Use Proc Clock/2 for AT bus state machine. 10 Reserved. 11 Use ATCLK input pin for the AT bus state machine.

82C301 Pin Description

Pin No.	Symbol	Pin Type	Description
Clocks			
44	CLK2IN	I	CLOCK 2 INPUT from a packaged TTL crystal oscillator having twice the rated frequency of the processor.
2	CLK2	O	CLK2 output to the Clock 2 input of 80386 and the memory controller. This clock output is derived from 82C302 CLK2IN and has a 50% duty cycle. The clock can also be programmed to be the same as the BCLK.
66	SCLK	O	SCLK is CLK2 divided by two and is an output generated as a reference to verify the phase relationship of the internal clock and CLK2.
41	ATCLK1	I	BUS CLOCK INPUT source from Crystal or Oscillator. This clock input is used for the AT Bus operation and is required only if the AT bus state machine clock (BCLK) will not be derived from the CLK2 input. This signal should be tied low if not used. Its frequency should be lower than CLK2IN.
40	ATCLK2	O	BUS CLOCK CRYSTAL OUTPUT is connected to the crystal oscillator circuit if a packaged oscillator is not used. A series resistor of 10Ω should be used to reduce the amplitude of the resonant circuit. It should be left unconnected if a packaged TTL oscillator is used.
39	ATSCLK	O	AT SYSTEM CLOCK is buffered to drive the clock signal SYSCLK on the AT bus I/O channel. It is half the frequency of BCLK and should have a nominal value in the range of 6 to 8 MHz for maintaining correct AT I/O bus timing with IBM PC AT.
Control			
37	$\overline{\text{RESET1}}$	I	$\overline{\text{RESET1}}$ is an active low input generated by the POWER GOOD signal of the power supply. When low, it activates RESET3 and RESET4. $\overline{\text{RESET1}}$ is latched internally.
38	$\overline{\text{RESET2}}$	I	Active low. $\overline{\text{RESET2}}$ (8042RC) is an active low signal generated from the keyboard controller 8042 for a "warm reset" not requiring the system power to be shut off. It forces a CPU reset by activating the RESET3 signal.
56	RESET4	O	RESET4 is an active high output used to reset the AT Bus, the 82C206 IPC, the 8042 keyboard controller and the 82C302 or 82C307 memory controller. RESET4 is synchronized with the processor clock.

82C301 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
CPU Interface			
80	RESET3	O	RESET3 is an active high output to the 80386 and the 80387 when either RESET1 or RESET2 is active. It is also activated when a shutdown condition in the CPU is detected. RESET3 will stay active for at least 78 CLK2 cycles.
82	READY	I/O	READY is an output during AT bus cycles (AF32 high), and is driven low to terminate the current CPU cycle after detecting IOCHRDY high and 0WS high or if a "time out" condition is detected. It is an open collector output requiring an external pull-up resistor of 10 KOhm. During all other cycles (AF32 low), it is an input (from the 82C302 and any other 32 bit memory controller), and has to be driven low to terminate the current CPU access. It is connected to the READY input of the 80386 processor.
3	ADS	I	Active low. ADDRESS STROBE input connected to the 80386 ADS pin. A 10KΩ pullup resistor is recommended.
4	W/R	I/O	READ/WRITE STATUS input from the 80386 W/R signal. It indicates a write bus cycle if it is high and a read cycle if it is low. A 10KΩ pull-up resistor is recommended.
5	D/C	I	DATA/CONTROL STATUS input from the 80386 D/C signal. A 10KΩ pull-up resistor is recommended.
6	M/IO	I	MEMORY/IO STATUS input from the 80386 M/IO signal. A 10KΩ pull-up resistor is recommended.
78	HOLD	O	Active high. HOLD REQUEST is an output to the 80386 HOLD input pin. This signal is used to request the CPU to relinquish the bus to another requesting master upon HRQ1, HRQ2 or REFREQ.
79	HLDA	I	Active high. HOLD ACKNOWLEDGE input connected to the 80386 HLDA signal. When the signal is HIGH it indicates that the processor has relinquished the system bus in response to the HOLD request. When active, it forces all commands (IOR, IOW, MEMR, MEMW, INTA) to be tri-stated.
10-7	BE<3:0>	I/O	Active low. BYTE ENABLE signals input from the 80386 BE<3:0> during a CPU cycle. BE3 controls the most significant byte while BE0 controls the least significant byte. BE<3:0> are generated by 82C301 during DMA cycles based on the status signals XA0, XA1 and XBHE.
81	NMI	O	Active HI. NON-MASKABLE INTERRUPT connects to the 80386 NMI pin and is generated by 82C301 to cause an NMI.

82C301 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
Decodes			
48	$\overline{\text{PORTBCS}}$	I	Active low. PORT B CHIP SELECT is the address decode input from the 82A304 as enable for the Port B register at address 061H.
49	$\overline{\text{NMICS}}$	I	Active low. NMI CHIP SELECT is the address decode input from the 82A304 as enable for the NMI enable bit at address 070H.
50	$\overline{\text{IO2XCS}}$	I	Active low. IO2X CHIP SELECT is the address decode input from the 82A304 as chip select for the IO registers at 022H and 023H used to access the 82C301 internal configuration registers.
IO Channel Interface			
53	$\overline{\text{0WS}}$	I	ZERO WAIT STATE (0WS) is an active low input from the AT bus, causing termination of the AT bus cycle. 16-bit Memory/I/O cards residing on the AT expansion bus use this line to speed up accesses. It requires a 330Ω pull-up resistor.
52	IOCHRDY	I	Active high. IO CHANNEL READY input from the AT bus. When low it indicates a 'not ready' condition and forces the insertion of wait states in I/O or memory accesses. When HIGH it will allow the completion of the current memory or I/O access.
51	$\overline{\text{IOCHCK}}$	I	Active low. IO CHANNEL CHECK input from the AT bus which causes an NMI to be generated if enabled. It is used to signal an Error condition from a device residing on the AT bus. A 10KΩ pull-up resistor is recommended.
70	$\overline{\text{LPAR}}$	I	Active low. PARITY ERROR is an input from local memory system which causes an NMI to be generated if enabled.
69	$\overline{\text{PFAIL}}$	I	Active low. POWER FAIL WARNING signal is an input from the power supply.
54	ALE	O	Active high. ADDRESS LATCH ENABLE is an output to the AT bus. This signal controls the address latches used to hold the address during a bus cycle. The signal should be buffered to drive the AT bus.
DMA Interface			
19	HLDA1	O	Active high. HOLD ACKNOWLEDGE 1 is active when a bus cycle is granted in response to HRQ1.
68	HLDA2	O	Active high. HOLD ACKNOWLEDGE 2 is active when a bus cycle is granted in response to HRQ2.

82C301 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
DMA Interface (Continued)			
18	HRQ1	I	Active high. HOLD REQUEST 1 is active when a DMA/ Master is requesting a bus cycle. For an AT compatible architecture it should be connected to the HOLD REQUEST signal from DMA1 and DMA2.
67	HRQ2	I	Active high. HOLD REQUEST 2 is active when a DMA/ Master is requesting a bus cycle. This should be grounded if not used.
14	$\overline{\text{AEN1}}$	I	ADDRESS ENABLE 1 is an active low input from one of the two DMA controllers enabling the address latches for 8 bit DMA transfers.
15	$\overline{\text{AEN2}}$	I	ADDRESS ENABLE 2 is an active low input from one of the two DMA controllers enabling the address latches for 16 bit DMA transfers.
Control Strobes			
46	$\overline{\text{MCS16}}$	I	Active low. $\overline{\text{MCS16}}$ is active during 16 bit memory accesses on IO channel. If $\overline{\text{MEMCS32}}$ and $\overline{\text{MEMCS16}}$ are both high it implies a 8 bit memory transfer. A pull-up resistor of 330Ω is recommended.
72	$\overline{\text{MCS32}}$	I	Active low. $\overline{\text{MCS32}}$ is active during 32 bit memory accesses on IO channel.
47	$\overline{\text{IOCS16}}$	I	Active low. $\overline{\text{IOCS16}}$ is active during 16 bit IO accesses on IO channel. If $\overline{\text{IOCS32}}$ and $\overline{\text{IOCS16}}$ are both high, it implies a 8 bit I/O transfer. A pull-up resistor of 330Ω is recommended.
71	$\overline{\text{IOCS32}}$	I	Active low. $\overline{\text{IOCS32}}$ is active during 32 bit IO accesses on IO channel.
75	$\overline{\text{SMCMD}}$	O	Active low. SYSTEM MEMORY COMMAND indicates the current access cycle is a memory cycle.
Refresh			
16	REFREQ	I	Active high. REFresh REQuest initiates a DRAM refresh sequence. It is generated by the 8254 compatible timer controller #1 of the 82C206 IPC in a PC/AT implementation.
65	$\overline{\text{REF}}$	I/O	Active low. REFresh is an open drain signal. It initiates a refresh cycle for the DRAMs. As an input it can be used to force a refresh cycle from an I/O device. An external pull up of 620Ω is required.

82C301 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
X Bus Interface			
20	$\overline{\text{XMEMR}}$	I/O	X BUS MEMORY READ is an active low control strobe directing memory to place valid data on the data bus. It is an output if the CPU is controlling the bus. It is an input if a DMA controller is in control of the bus.
23	$\overline{\text{XMEMW}}$	I/O	X BUS MEMORY WRITE is an active low control strobe directing memory to accept data from the data bus. It is an output if the CPU is controlling the bus and is an input if a DMA controller is in control of the bus.
24	$\overline{\text{XIOR}}$	I/O	X BUS I/O READ is an active low strobe directing an I/O device to place data on the data bus. It is an output if the CPU is controlling the bus or an input if a DMA controller is in control of the bus.
25	$\overline{\text{XIOW}}$	I/O	X BUS I/O WRITE is an active low strobe directing an I/O device to accept data from the data bus. It is an output if the CPU is controlling the bus or an input if a DMA controller is in control of the bus.
55	$\overline{\text{XBHE}}$	I/O	X BYTE HIGH ENABLE is an active low signal indicating the high byte has valid data on the bus. It is an output if the CPU is controlling the bus or an input if a DMA controller is in control of the bus.
35-34	XD<7:6>	I/O	EXPANSION DATA BUS bits <7:6>
32-27	XD<5:0>	I/O	EXPANSION DATA BUS bits <5:0>
57	SDIR	O	SYSTEM BUS DIRECTION controls the direction of data transfer between the IO channel and the local bus. When low it enables data transfer from the IO channel to local bus.
58	$\overline{\text{ACEN}}$	O	Active low. ACTION CODE ENABLE validates the action code signals AC<3:0>.
59-62	AC<3:0>	O	ACTION CODE is a four bit encoded command for bus size control and byte assembly operations performed by the 82A305s.
Memory Control			
77	$\overline{\text{AF32}}$	I	$\overline{\text{AF32}}$ is an active low input indicating that the current cycle is a local 32-bit cycle not requiring data size conversion. A high indicates an AT bus cycle. A 10KΩ pull-up resistor is recommended.
76	$\overline{\text{BUSY}}$	I	Active low. BUSY from memory controller.
83	$\overline{\text{MALE}}$	O	Active low. Address Latch Enable for accesses to on board memory/IO. It also indicates start of a new CPU cycle.

82C301 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
Memory Control (continued)			
11	TMRGATE	O	Active high. TIMER GATE signal enables the timer on 8254 Timer to generate the tone signal for the speaker.
12	TMROUT2	I	Active high. TIMER OUT 2 is the output from the timer 8254. It can be read from port B.
13	SPKDATA	O	Active high. SPEAKER DATA is used to gate the 8254 tone signal to the speaker.
17	$\overline{\text{INTA}}$	O	Active low. Interrupt acknowledge is an output to the interrupt controller. It is also used to direct data from the XD to the SD bus during an interrupt acknowledge cycle.
45	$\overline{\text{ATEN}}$	O	Active low. AT ENABLE indicates the current CPU access is an AT bus cycle.
73	XA00	I/O	X Address bit 0. It is sourced from the 82C301 when 80386 or DMA (16 bit) is a bus master.
74	XA01	I/O	X Address bit 1. It is sourced from the 82C301 when 80386 is a bus master.
26,36	NC		No connection
21,42 63,84	VDD VDD		Power
1 22,33 43,64	VSS VSS VSS		Ground

82C301 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C301 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C301 DC Characterisitcs

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=8mA (Note 1)	V_{OL}		0.45	V
Output High Voltage I_{OH}=-200 μA	V_{OH}	2.4		V
Input Current $0 < V_{IN} < V_{CC}$	I_{IL}		±10	μA
Output Short Circuit Current V_O=0V	I_{OS}	TBD	TBD	mA
Input Clamp Voltage	V_{IC}		TBD	V
Power Supply Current @ 25 MHz Clock	I_{CC}		100	mA
Output HI-Z Leak Current $0.45 < V_{OUT} < V_{CC}$	I_{OZ1}		±10	μA
CLK2 Output Low Voltage @ I_{OL} = 5 mA	V_{OLC}		0.45	V
CLK2 Output High Voltage @ I_{OH} = -1 mA	V_{OHC}	4.0		V

NOTE:
1. $\overline{REF}$ has I_{OL} = 16mA.
   CLK2, $\overline{MALE}$ have I_{OL} = 8mA.
   All other outputs and I/O pins have I_{OL} = 4mA. In all cases all I_{OL} = I_{OH} for the pin.

82C301 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C301-16 Min	Typ	Max	82C301-20 Min	Typ	Max	Unit	Notes
t101	CLK2 period	31			25			ns	
t102	CLK2 low time	10			9			ns	at 2V
t103	CLK2 high time	10			9			ns	at 2V
t104	CLK2 rise time			5			4	ns	
t105	CLK2 fall time			5			4	ns	
t106	SCLK delay from CLK2	1		6	1		6	ns	
t107	RESET3, RESET4 active delay	3		11	3		11	ns	
t108	RESET3, RESET4 inactive delay	4		15	4		12	ns	
t109	$\overline{\text{SMCMD}}$ delay from $\overline{\text{MALE}}$ active	2	7	10	2		7	ns	
t110	$\overline{\text{AF32}}$ setup time to CLK2	15			11			ns	
t111	$\overline{\text{AF32}}$ hold time to CLK2	0			0			ns	
t112	HOLD delay from CLK2			25			25	ns	
t113	$\overline{\text{READY}}$ input set-up time from CLK2	13			10			ns	
t114	$\overline{\text{READY}}$ input hold time from CLK2	5			5			ns	
t115	$\overline{\text{ATEN}}$ active delay from CLK2			20			20	ns	
t116	$\overline{\text{ATEN}}$ inactive delay from CLK2			20			20	ns	
t117	$\overline{\text{MALE}}$ active delay from CLK2			15			15	ns	
t118	$\overline{\text{MALE}}$ inactive delay from CLK2			15			10	ns	
t119	$\overline{\text{READY}}$ output active delay from CLK2			20			20	ns	
t120	$\overline{\text{READY}}$ output inactive delay from CLK2	4		20	4		15	ns	
t121	ATSCLK period	100			100			ns	
t122	ATSCLK low time	45			45			ns	at 2V
t123	ATSCLK high time	45			45			ns	at 0.8V
t124	ATSCLK rise time			8			8	ns	

Test Load = 65pF unless otherwise specified.

82C301 AC Characteristics (Continued)

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C301-16 Min	Typ	Max	82C301-20 Min	Typ	Max	Unit	Notes
t125	ATSCLK fall time			8			8	ns	
t126	ALE delay from ATSCLK (or)			10			10	ns	
t127	$\overline{XIOR}$, $\overline{XMEMR}$, $\overline{INTA}$ active delay from ATSCLK (or)			15			15	ns	
t128	$\overline{XIOR}$, $\overline{XMEMR}$, $\overline{INTA}$ inactive delay from ATSCLK	3		15	3		15	ns	
t129	IOCHRDY set-up time to ATSCLK	17			17			ns	
t130	IOCHRDY hold time to ATSCLK	0			0			ns	
t131	$\overline{MCS16}$, $\overline{IOCS16}$ set-up time to ATS CLK	25			25			ns	
t132	$\overline{MCS16}$, $\overline{IOCS16}$ hold time from ATSCLK		25			25		ns	
t133	$\overline{MCS32}$, $\overline{IOCS32}$ set-up time to ATSCLK	25			25			ns	
t134	$\overline{MCS32}$, $\overline{IOCS32}$ hold time from ATSCLK		25			25		ns	
t135	XA0, XA1, $\overline{XBHE}$ active delay from ATSCLK			20			20	ns	
t136	XA0, XA1, $\overline{XBHE}$ inactive delay from ATSCLK			15			15	ns	
t137	$\overline{ACEN}$ active delay (read) from ATSCLK	12			12			ns	
t138	$\overline{ACEN}$ inactive delay (read) from ATSCLK	0	10		0	10		ns	
t139	AC<3:0> active delay from ATSCLK	3		15	3		15	ns	
t140	AC<3:0> inactive delay from ATSCLK	3		10	3		10	ns	
t145	$\overline{XMEMR}$, $\overline{XMEMW}$ active delay from ATSCLK (with zero command delay)	3		12	3		12	ns	
t146	$\overline{ACEN}$ active delay (write) from ATSCLK	10			10			ns	
t147	$\overline{ACEN}$ inactive delay (write) from ATSCLK	0			0			ns	
t148	$\overline{0WS}$ set-up time to ATSCLK	25			25			ns	

Test Load = 65pF unless otherwise specified.

82C301 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C301-16 Min	Typ	Max	82C301-20 Min	Typ	Max	Unit	Notes
t149	$\overline{0WS}$ hold time from ATSCLK	0			0			ns	
t151	$\overline{NMICS}$ setup time to $\overline{XIOW}$ active	20			20			ns	
t152	$\overline{NMICS}$ hold time from $\overline{XIOW}$ inactive	20			20			ns	
t153	Data (XD7) set-up time to $\overline{XIOW}$ inactive	30			30			ns	
t154	Data (XD7) hold time from $\overline{XIOW}$ inactive	20			20			ns	
t155	NMI delay from $\overline{XIOW}$ inactive		25			25		ns	
t156	$\overline{PORTBCS}$ set-up to $\overline{XIOR}$, $\overline{XIOW}$ active	20			20			ns	
t157	$\overline{PORTBCS}$ hold time from $\overline{XIOR}$, $\overline{XIOW}$ inactive	20			20			ns	
t158	Data (XD<7:0>) valid delay from $\overline{XIOR}$ active	15			15			ns	
t159	Data (XD<7:0>) hold time from $\overline{XIOR}$ inactive	15			15			ns	
t160	$\overline{IO2XCS}$ set-up time to $\overline{XIOR}$, $\overline{XIOW}$ active		10			10		ns	
t161	$\overline{IO2XCS}$ hold time from $\overline{XIOR}$, $\overline{XIOW}$ inactive		15			15		ns	
t162	$\overline{LPAR}$, $\overline{IOCHK}$, $\overline{PFAIL}$ pulse width		15			15		ns	
t165	REFREQ pulse width	15			15			ns	
t166	$\overline{REF}$ set-up time to ATSCLK		10			10		ns	
t167	$\overline{XMEMR}$ active delay (refresh cycle) from ATSCLK		15			15		ns	
t168	$\overline{XMEMR}$ inactive delay (refresh cycle) from ATSCLK		15			15		ns	
t169	IOCHRDY set-up time (refresh cycle) from ATSCLK	25			25			ns	
t170	IOCHRDY hold time (refresh cycle) from ATSCLK	0			0			ns	
t171	$\overline{BE<3:0>}$ active delay from XA0, XA1, $\overline{XBHE}$ valid		15			15		ns	
t172	$\overline{BE<3:0>}$ inactive delay		15			15		ns	

Test Load = 65pF unless otherwise specified.

82C301 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C301-16 Min	82C301-16 Typ	82C301-16 Max	82C301-20 Min	82C301-20 Typ	82C301-20 Max	Unit	Notes
t173	$\overline{\text{SMCMD}}$ active delay from $\overline{\text{XMEMR}}$, $\overline{\text{XMEMW}}$ active		20			20		ns	
t174	$\overline{\text{SMCMD}}$ inactive delay from $\overline{\text{XMEMR}}$, $\overline{\text{XMEMW}}$ inactive		20			20		ns	
t175	$\overline{\text{ACEN}}$ active delay from HLDA1 active		20			20		ns	
t176	$\overline{\text{ACEN}}$ inactive delay from HLDA1 inactive		20			20		ns	
t177	AC<0:3> active delay from XA0, XA1, $\overline{\text{XBHE}}$ not valid	25			25			ns	
t178	AC<0:3> inactive delay from XA0, XA1, $\overline{\text{XBHE}}$ valid	25			25			ns	
t179	AC<0:3> active delay from $\overline{\text{XMEMR}}$ active	25			25			ns	
t180	AC<0:3> inactive delay from $\overline{\text{XMEMR}}$ inactive	25			25			ns	
t181	RESET1, RESET2 input set-up time	28			28			ns	at 2V
t182	RESET1, RESET2 input hold time	10			10			ns	at 2V
t183	RESET1, RESET2 minimum pulse width	250			250			ns	
t191	$\overline{\text{MALE}}$ delay from $\overline{\text{ADSM}}$	22			18			ns	
t192	$\overline{\text{MALE}}$ delay from $\overline{\text{READY}}$	24			20			ns	

Test Load = 65pF unless specified.

82C301 AC Characteristics (Continued)

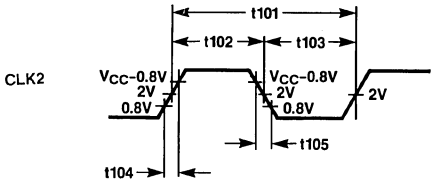
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

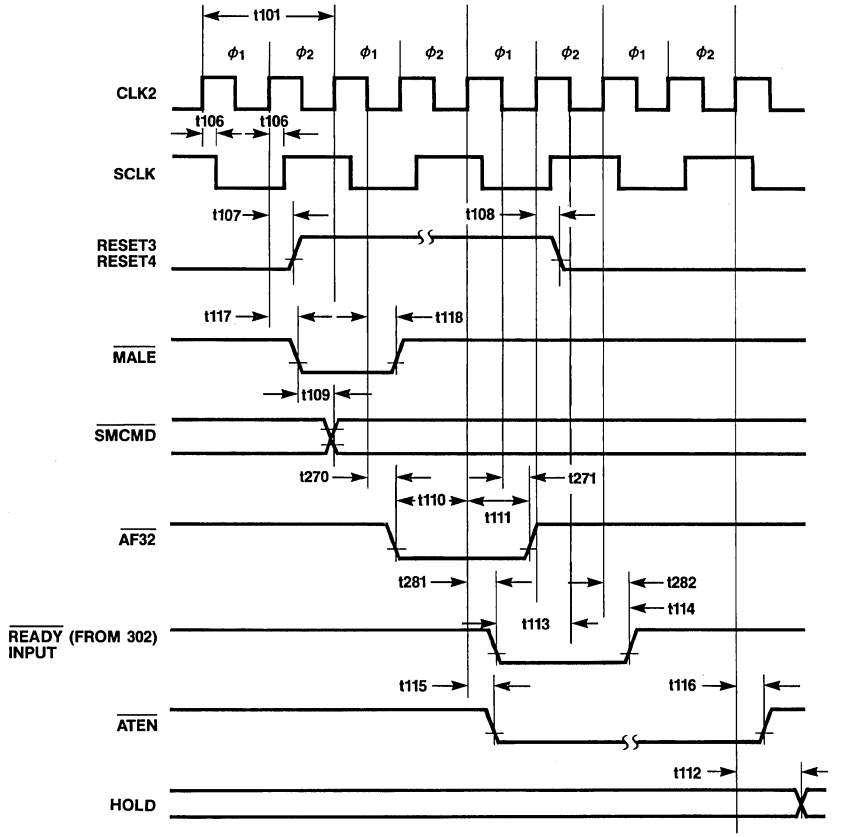
Sym	Description	82C301-25 Min	Typ	Max	Unit	Notes
t101	CLK2 period	20		125	ns	
t102	CLK2 low time	7			ns	
t103	CLK2 high time	7			ns	
t104	CLK2 rise time			7	ns	
t105	CLK2 fall time			7	ns	
t108	RESET3, RESET4 inactive delay	4		10	ns	
t109	$\overline{\text{SMCMD}}$ delay from $\overline{\text{MALE}}$ active	2		7	ns	
t110	$\overline{\text{AF32}}$ setup time to CLK2	8			ns	
t118	$\overline{\text{MALE}}$ inactive delay from CLK2			10	ns	
t191	$\overline{\text{MALE}}$ delay from $\overline{\text{ADS}}$			13	ns	
t192	$\overline{\text{MALE}}$ delay from $\overline{\text{READY}}$			17	ns	

Test Load = 65pF unless specified.

Note: All other parameters not specified at 25 MHz are the same as the 82C301-20 MHz specifications.

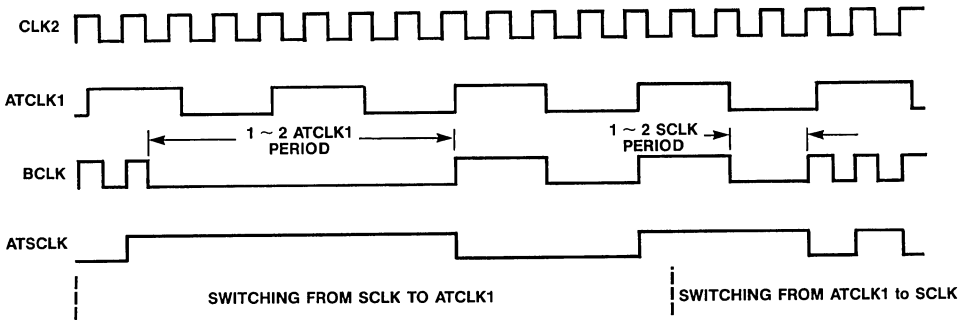
82C301 TIMING DIAGRAMS

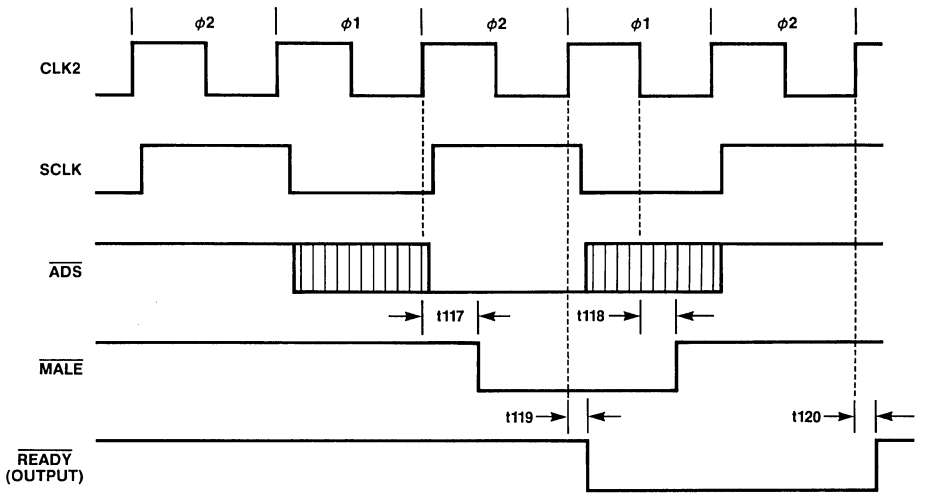


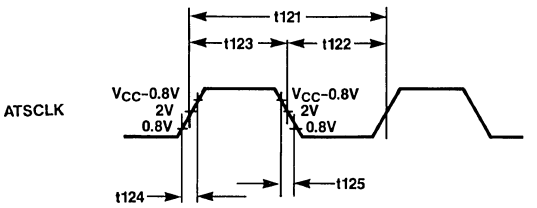


82C301 TIMING DIAGRAMS

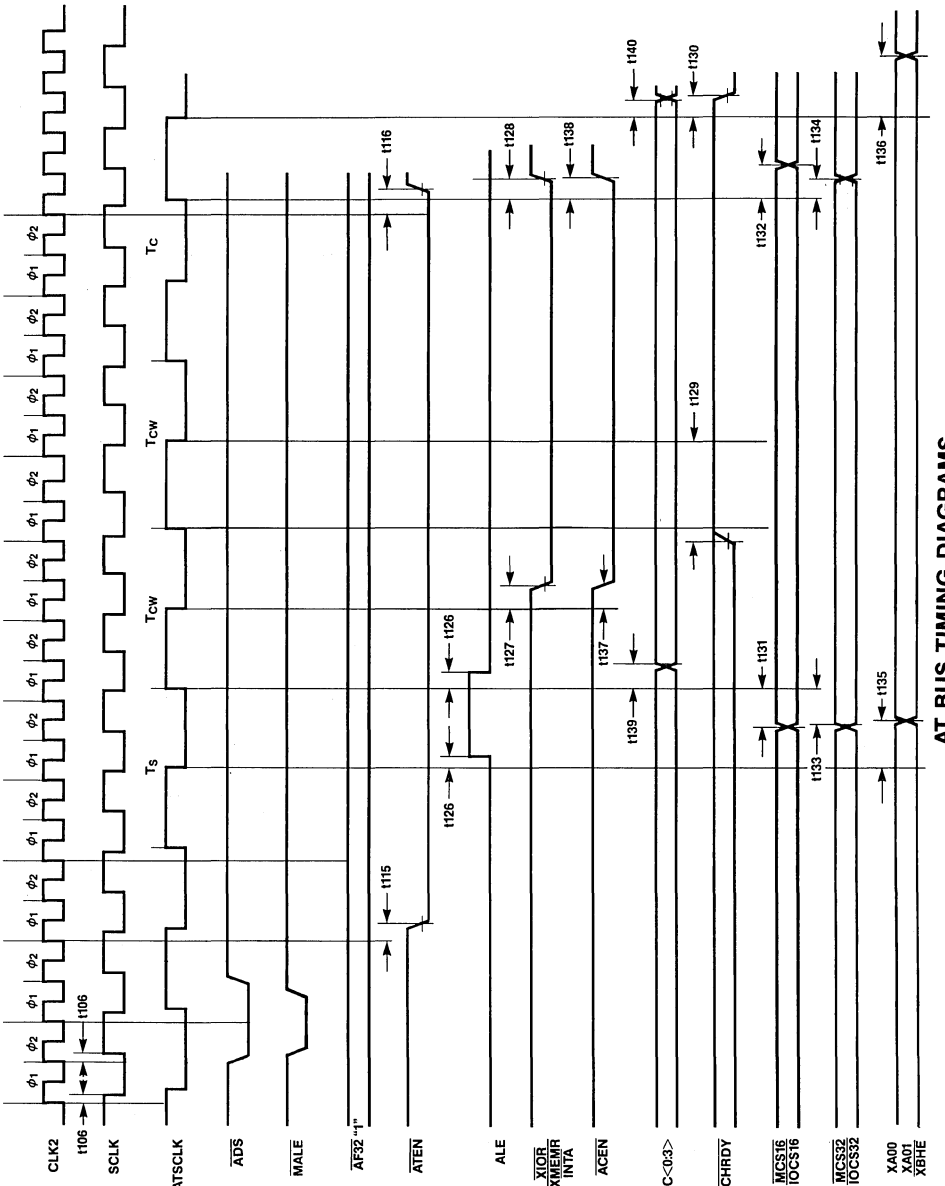
Clock Switching



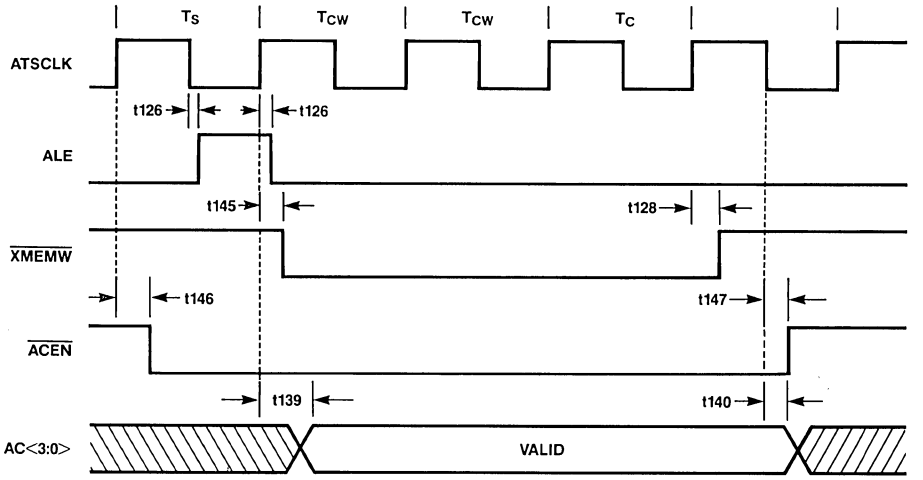




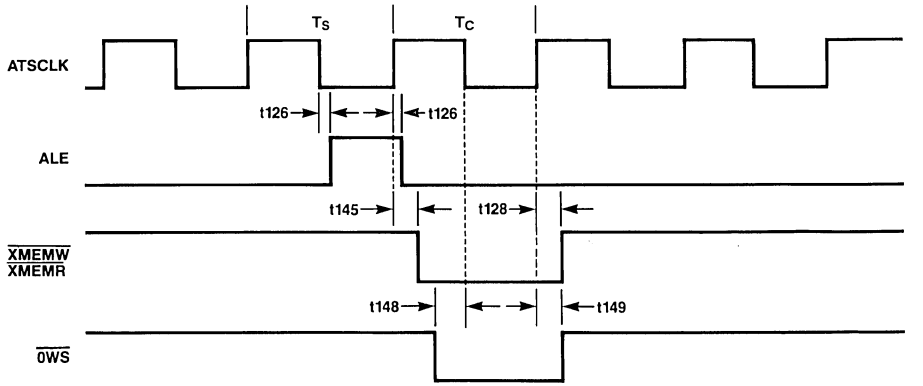
82C301 TIMING DIAGRAMS



82C301 TIMING DIAGRAMS

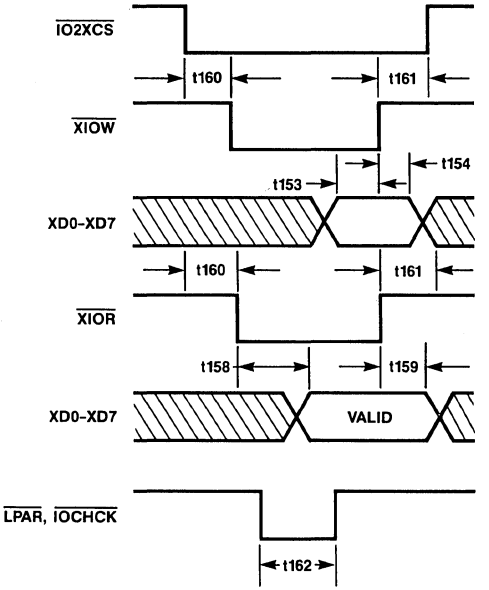


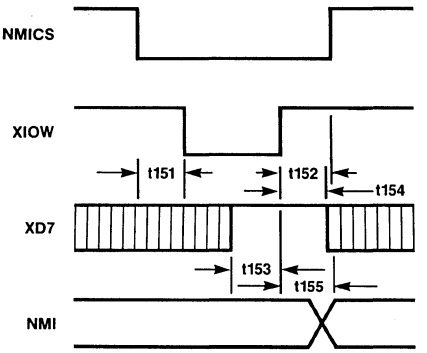
AT Bus

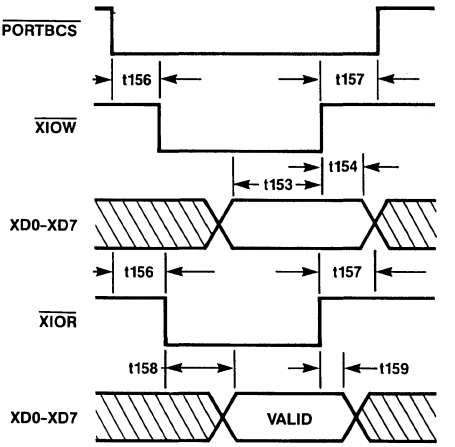


0WS AT Bus

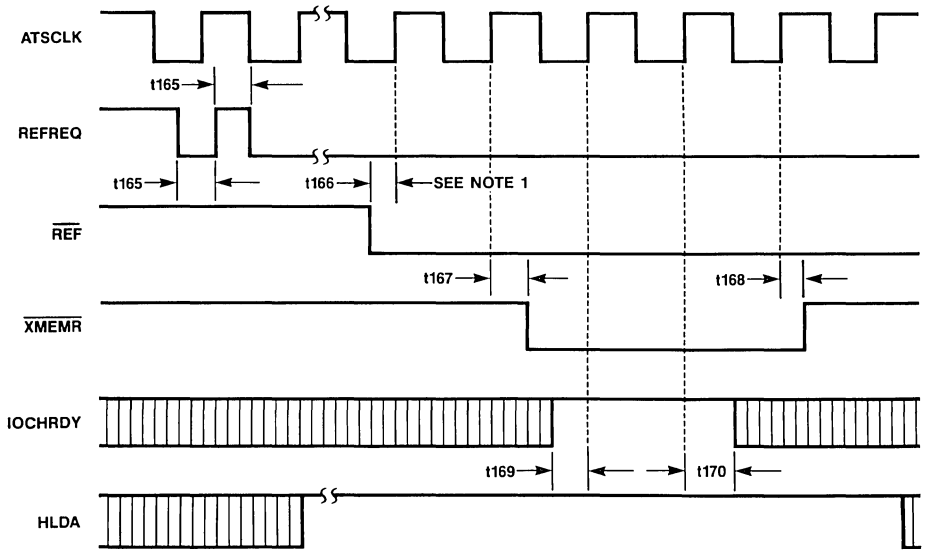
82C301 TIMING DIAGRAMS (I/O READ/WRITE)





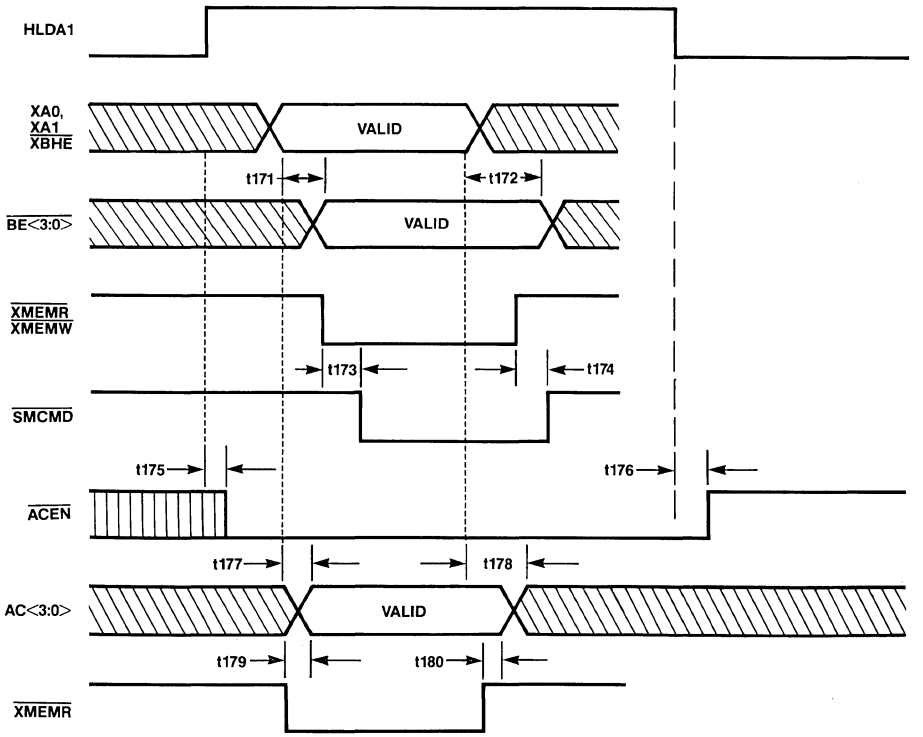


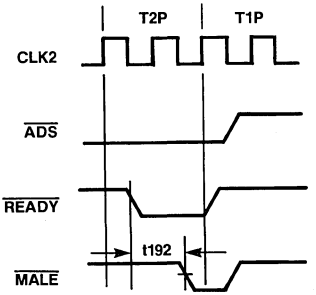
82C301 TIMING DIAGRAMS (REFRESH CYCLE)

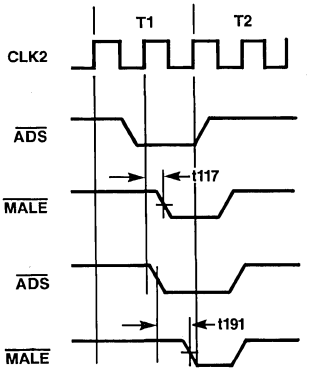


NOTE
REF is an asynchronous signal and the setup time is specified only to guarantee starting a refresh cycle on that clock cycle instead of next one.

82C301 TIMING DIAGRAMS







82C302 Page/Interleave Memory Controller

- Page mode access with interleaved memory banks achieves higher performance than conventional DRAM arrays.
- Zero wait state access at 16, 20 and 25 MHz.
- Minimum configuration of 1 bank of 36 bits, 1MB using 256K x 1 or 4MB using 1M × 1 DRAMs.
- Maximum configuration of 4 banks of 36 bits, 4MB using 256K × 1 or 16MB using 1M × 1 DRAMs.
- Memory configurations of 1, 2 and 4 banks.
- Shadow RAM feature for efficient BIOS execution
- Staggered refresh to reduce power supply noise.

Overview

The 82C302 performs the memory control functions in a 80386-based systems that utilize page mode access DRAMs. The memory configurations can be one bank (non-interleaved) or multiple banks (2 or 4) interleaved on 2KB-page basis.

Array Configuration

The 82C302 organizes memory as banks of 36 bits consisting of 32 bits of data and 4 bits of parity. A common design may use either 36 by-1 DRAMs or 8 by-4 and 4 by-1 DRAMs. The minimum configuration can be a single bank operating in non-interleaved mode or can be one to two pairs of banks operating in two-way page interleaved mode at higher performance.

The memory controller is designed such that the memory can be up-graded from one to two banks by making it a two-way interleaved organization. Because of the interleaved page operation, the third and fourth banks must be added as a pair. Furthermore, the DRAM types must be identical in each bank of a pair due to the interleaved configuration. However, each pair of banks can use different DRAM types. With one or two banks of smaller DRAM types and later upgraded with additional pairs of banks of larger DRAMs.

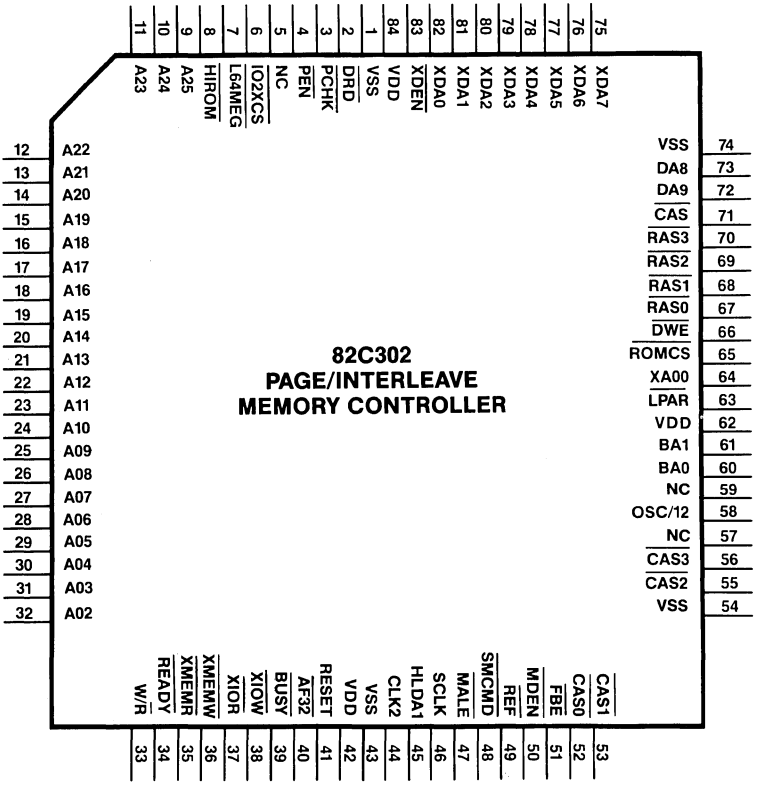
Page Interleaved Operation

The 82C302 uses a page interleaved design that is different from most interleaved memory designs. Normal two-way interleaving uses two banks of DRAMs with even (double word) addresses stored in one bank and odd addresses in the other. If accesses are sequential (or at least to alternating even and odd addresses) the RAS precharge time of one set can be overlapped with the access time of the second set. Typically the hit rate (fraction of times that the required bank is available) is 50%. This is especially true since operand accesses (which tend to be more random) can be interspersed with (most likely sequential) instruction fetches.

Page mode operation available with most DRAMs operates because the access to the row address of the internal DRAM array makes available a large number of bits (512 bits in a 256K × 1) that are subsequently selected using the column address. Once a row access has been made higher speed random access can be made to any bit (1 of 512) within the row. The page mode access and cycle times are typically half that of the normal access and cycle times respectively. If 36 256K × 1 DRAMs are used to implement a bank, a page would have 512 × 4 bytes = 2KB. Thus memory could be interleaved on a 2KB page rather than 4 byte basis. Any access to the currently active RAS page would occur in the page access rather than the normal access time and any subsequent access could be to anywhere in the same 2KB without incurring any penalty due to RAS precharge.

When memory is configured to take advantage of this DRAM organization, significantly better performance can be achieved over normal interleaving. There are two reasons for this:

— The page mode access is faster than the normal access time. This permits more relaxed timing in order to achieve the same 0 wait-state "hit" access.


82C302
PAGE/INTERLEAVE
MEMORY CONTROLLER
1 VSS
2 DRD
3 PCHK
4 PEN
5 NC
6 IO2XCS
7 L64MEG
8 HIROM
9 A25
10 A24
11 A23
12 A22
13 A21
14 A20
15 A19
16 A18
17 A17
18 A16
19 A15
20 A14
21 A13
22 A12
23 A11
24 A10
25 A09
26 A08
27 A07
28 A06
29 A05
30 A04
31 A03
32 A02
33 W/R
34 READY
35 XMEMR
36 XMEMW
37 XIOR
38 XIOW
39 BUSY
40 AF32
41 RESET
42 VDD
43 VSS
44 CLK2
45 HLDA1
46 SCLK
47 MALE
48 SMCMD
49 REF
50 MDEN
51 FBE
52 CAS0
53 CAS1
54 VSS
55 CAS2
56 CAS3
57 NC
58 OSC/12
59 NC
60 BA0
61 BA1
62 VDD
63 LPAR
64 XA00
65 ROMCS
66 DWE
67 RAS0
68 RAS1
69 RAS2
70 RAS3
71 CAS
72 DA9
73 DA8
74 VSS
75 XDA7
76 XDA6
77 XDA5
78 XDA4
79 XDA3
80 XDA2
81 XDA1
82 XDA0
83 XDEN
84 VDD

— The frequency of the next access being fast (same or alternate page vs. alternate address in interleaved mode) is significantly higher. This is because of the principle of locality of reference, instructions and data tend to be clustered together.

However, the complexity is somewhat higher in the page mode controller, making VLSI an ideal implementation vehicle.

Functional Description

The 82C302 performs four major functions as shown in figure 2-1:

- DRAM memory access arbitration
- DRAM memory access cycle control
- DRAM refresh
- Memory mapping

Memory Access State Machines and Arbitration

The 82C302 controls the DRAM memory access from three sources: CPU, DMA, and refresh requests. These accesses are arbitrated based on the inputs HLDA1 and REF and are handled by three state machines controlling each type of accesses. The CPU state machine controls the memory operation for CPU accesses, the DMA state machine for DMA accesses, and the refresh state machine controls the DRAM refresh operation.

The refresh state machine is in control whenever REF is active. When HLDA1 is active the DMA state machine is in control. In all other cases, the CPU state machine is in control for valid DRAM memory accesses as defined by the memory map in the configuration registers. The arbitration is not preemptive in that the current active state machine always runs to completion before relinquishing the control. Therefore, it is possible for the HLDA1 with active IOR or XMEMR to prevent refresh cycles to take place.

CPU Access State Machine

The CPU initiated accesses are decoded according to the memory map defined in the configuration registers. These are the only accesses that use the page mode operation of the DRAMs. The 82C302 maintains four page registers storing the page addresses of the most recently accessed DRAM pages of the two-way page-interleaved banks. These four registers are called active page registers. Accesses to the active pages are called "hits" and are faster because the DRAM is operated in the page mode with the RAS staying asserted.

The 82C302 supports memory configurations with either one, two, or four banks. Since one active register is provided for each bank, the number of active pages varies with the amount of memory installed. In a non-interleaved minimum memory configuration only one active page register is in use. For each active page register in use, the corresponding RAS stays asserted after the previous access. If an access does not hit any active pages, a "miss" cycle, normal DRAM access cycle is entered by first de-asserting the RAS associated with the bank accessed. Refer to the timing diagram for the timing sequence for each of these cases.

RAS and CAS Generation

The 82C302 is based on 2K byte page-interleaved organization. To maintain this organization, the following table shows the address lines used for the different organizations:

For non-interleaved operation (one bank only):

	Row	Column
256K DRAM's	A<19:11>	A<10:2>
1M DRAM's	A<21:12>	A<11:2>

For interleaved memory (two or four banks):

	Row	Column
256K DRAM's	A<20:12>	A<10:2>
1M DRAM's	A<21:12>	A<22>, A<10:2>

Table 2-1. Row and Column Address Definition

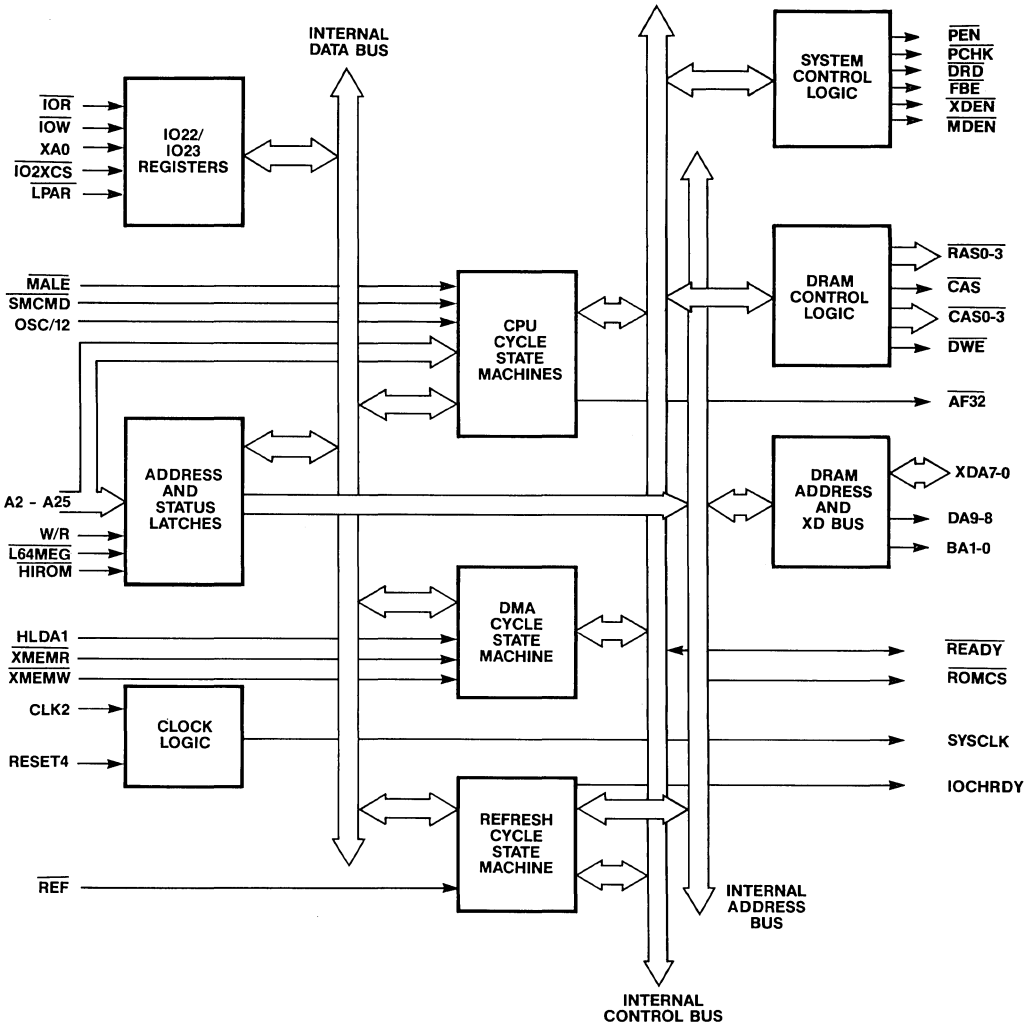


Figure 2-1. 82C302 Functional Block Diagram

In interleaved memory cases bit A<11> determines which one of the even page banks or odd page banks is accessed in the two-way interleaved organization. For 4 bank memory configurations, populated with 256K DRAMs, A<21> is used to select either RAS0 and RAS1 (A21 = 0) or RAS2 and RAS3 (A21 = 1). A<11> determines if the even bank (A11 = 0), Bank 0 or Bank 2) or the odd bank (A11 = 1, Bank1, Bank3) is accessed in a two way interleaved organization.

For 4 bank memory configurations, populated with 1 Megabit DRAMs, A<23> is used to select either RAS0 and RAS1 (A23 = 0) or RAS2 and RAS3 (A23 = 1). A<11> determines if the even or the odd bank is currently being accessed.

When 256K and 1 MBit DRAMs are used, it is required that 1 MBit DRAMs occupy the first two banks and the 256K DRAMs occupy the second two banks. This constraint is there to ensure that there will not be a hole in the address space without actual DRAMs. Figure 2.2 shows the memory addressing scheme for the allowable memory configurations.

RAS Timeout

When using DRAM page mode, the maximum RAS pulse width must be observed. For most DRAMs this is 10 microseconds (although some have 30 or 100 microsecond limits). Timers are maintained for each bank to assure data integrity using the OSC/12 (1.19MHz = 840nS) clock available on the system board. RAS is de-asserted for each bank when its counter times out at about 10 microseconds intervals. The RAS time out feature can be disabled by disconnecting the OSC/12 input.

CPU Access Cycles Sequences

There are many basic CPU memory access patterns: memory read-hit access, memory write-hit access, memory read-miss access, and memory write-miss access, and CPU IO access to 82C301 configuration registers. These basic access sequences and timing for the critical signals are shown in the timing charts. In addition to these basic patterns, the configuration register REG13H<6> may be programmed to have one wait state inserted for supporting slow DRAM's. Note that the default setting after the system reset is for one wait state insertion.

DMA Access State Machine

DMA accesses are initiated by asserting HLDA1. The XMEMR an IOR determines if it is a read or a write memory access. The bytes accessed are controlled externally with the BE<3:0> signals generated by the 82C301 Bus Controller. The DMA state machine makes one memory access per DMA bus cycle and does not attempt to pack or unpack data transfers to make full 32-bit transfers. Refer to the timing charts for a DMA access cycle sequence and timing.

EPROM and DRAM Control Logic

The EPROM and DRAM control logic in the 82C302 is responsible for the generation of RAS, CAS and DWE signals for DRAM accesses and the generation of ROMCS for EPROM accesses. This module also generates READY to the CPU upon completion of the local 32-bit DRAM access. The 82C301 generates the READY for the ROM access. CPU, DMA and refresh addresses use DA<9:8>, XDA<0:7> and BA<1:0> (Note that in the current version of the 82C302, the signals BA<1:0> default to zero). The system control logic provides MDEN to control the buffer chips. MDEN enables the data buffers on the 82A305 for the MD bus for non-refresh DRAM cycles.

System Control Logic

This module of the 82C302 generates the MDEN, MDRD, CAS (DLE), XDEN and AF32 for system control. XDEN is issued for I/O accesses to the internal configuration registers on the 82C302. It is used to enable the XD<7:0> onto the XDA<7:0> address lines from an external buffer, for accessing the internal registers. MDEN and MDRD are generated for enabling and controlling the data buffers between the MD data bus and the CPU data bus. AF32 is issued by the 82C302 CPU state machine. It is activated for local 32 bit memory cycles and satisfies the setup and hold requirement with respect to CLK2 of the 82C301 bus controller.

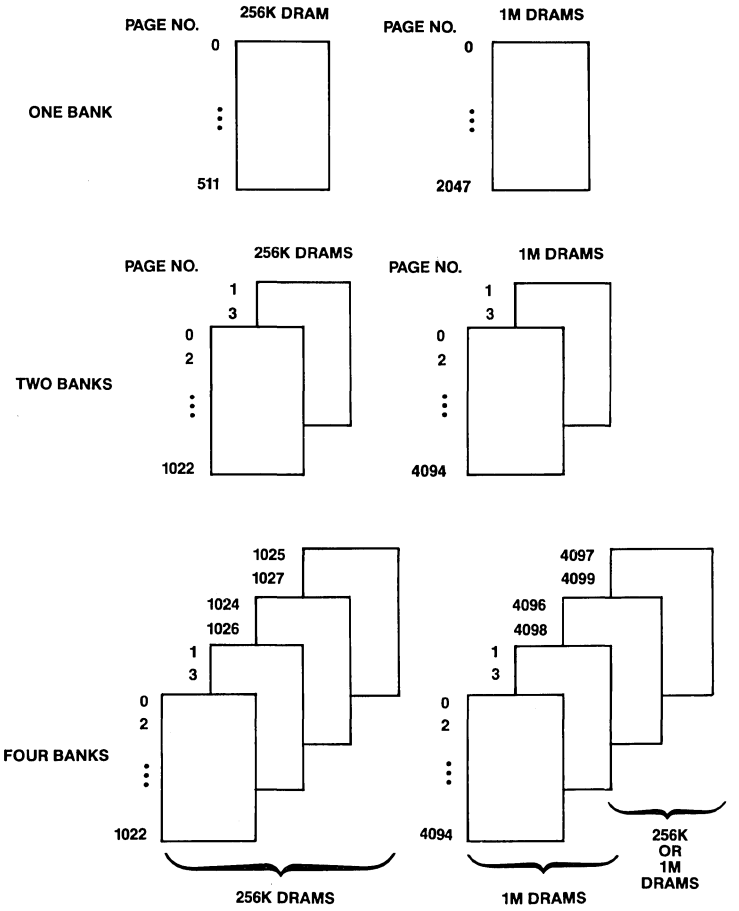


Figure 2-2. Memory Addressing

Refresh Cycles

To reduce power supply noise generation due to the surges caused during RAS transitions, RAS pulses to each bank are staggered by one CLK2 cycle, as shown in Figure 2-3. Because all RAS's could be active for page mode operation, a refresh cycle requires that all RAS's be first de-asserted for the RAS pre-charge period. IOCHRDY is activated low, to extend the cycle. Following the RAS pre-charge period, RAS0 is asserted, followed by RAS1 after a CLK2 cycle delay. RAS3 and RAS4 are also staggered by one CLK2 cycle. IOCHRDY is deasserted in the middle of RAS3 low time, to terminate the refresh cycle.

Memory Mapping Logic

The configuration registers REG08H to REG13H define what is a valid local memory access, and what is a ROM memory access according to the local bus addresses. REG08H and REG09H determines how ROM areas (as defined by an IBM PC AT) between the 768K to 1M address range are accessed.

For valid local memory accesses it asserts the AF32 to indicate that it has control of the local bus and also asserts the READY signal at the end of the access cycle. If an access is a ROM access, it asserts LDAC to provide controls for the ROM's or PROM's; in this case, the READY signal must be provided to the CPU and 82C302 by another source (82C301 will provide this signal in a chip set solution).

Shadow RAM Feature

For efficient BIOS execution, it is preferable to execute BIOS from the fast RAM rather than from the slower EPROM devices. The 82C302 supports the shadow RAM feature, which if invoked, allows the BIOS code to be executed from the system RAM resident at the same physical address as the BIOS EPROM. It is the responsibility of the system software to transfer the code stored in BIOS EPROMs to system RAM before enabling the shadow RAM feature. Shadowing EPROMs into RAM significantly improves performance in BIOS call intensive applications. Performance improve-

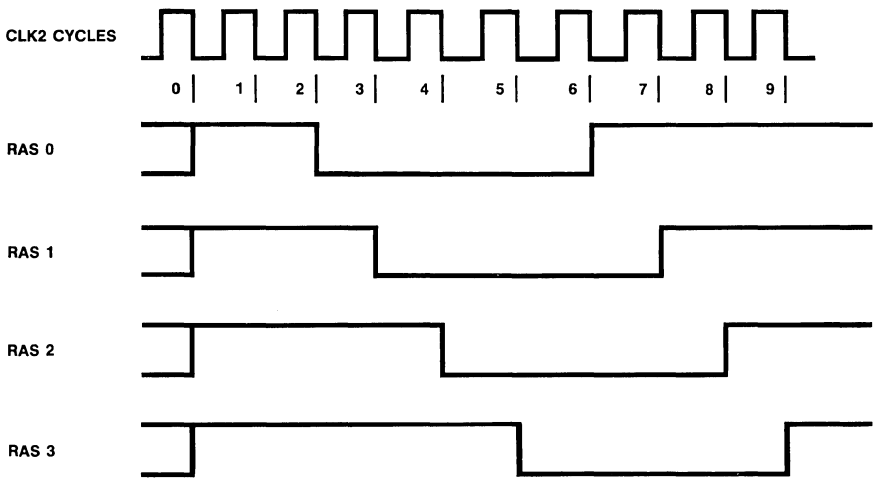


Figure 2-3. Staggered RAS pulses during refresh

ments as high as 300 to 400% have been observed in bench mark tests on shadow RAM. The shadow RAM feature is invoked by enabling the corresponding bits in the ROM enable register and the RAM mapping registers.

Clock, Reset and Other Miscellaneous Logic

The RESET4 input causes all internal registers to be reset to their default values. Configuration registers not specified with a default value are not reinitialized and may not retain its old value. The system control logic generates the RESETand MEMRsignals to be used for enabling parity error checking.

Configuration/Diagnostic Registers

There are 14 bytes of configuration and diagnostic registers in the 82C302. These are accessed through IO ports 22H and 23H normally found in the interrupt controller. Accesses to these configuration and diagnostic registers are done first by writing the index of the desired register into port 22H and then followed by an access (either read or write) to 23H for the data. XDEN is asserted for these accesses to control the buffer connecting the XD and XDA buses.

Memory Configuration Registers

The configuration registers REG08H to REG0FH are used to control how the CPU memory accesses are defined. They define all address as ROM accesses, system memory accesses (or DRAM accesses for short), other local CPU bus accesses, or as IO channel accesses . These provisions are made because the low one megabyte is both occupied by DRAM's, ROM's and also devices on the AT bus. For ROM accesses it generates the LDAC to control the PROM access; for system memory accesses it generates the necessary DRAM controls to the system memory under its control; it generates AF32 for all other local CPU bus accesses; and it does not control the IO channel accesses.

The 82C302 provides three 256KB areas where the ROM's can be located. The low ROM space is located just below the 1MB address, the middle ROM space is located below 16MB address, and the high ROM space is below 4GB address. The low ROM is used for 8086 compatible operation, the middle ROM is for 80286, and the high ROM is for 80386. Upon system reset, the default configuration register setting causes accesses to these three ROM areas to generate LDAC. With the exception of the high ROM area which is always recognized as ROM accesses, the other two ROM areas can be mapped to be either ROM or RAM accesses.

After reset, REG08<4:3> may be programmed to make the entire middle ROM area mapped to DRAM and with write protection if desired. REG08H<2> determines if the 82C301 recognizes the addresses generated beyond 16 MB as local CPU bus cycles. REG08H<1> is used to enable REG0AH to REG0FH which controls the "Low Meg DRAM" (40000H to FFFFFH) address mapping for 256KB to 1MB addresses in 16 KB blocks. This bit defaults upon reset so that only the 0 to 256KB areas are accessible. Accesses to the low megabyte DRAM can be made by enabling the mapping after the necessary configuration registers are correctly programmed. REG08H<0> defaults to single bank memory configuration upon reset and must be programmed to enable page/interleaved operation.

The REG09H control the address mapping and write protection for the low ROM area (from C0000H to FFFFFH) in 64KB blocks. REG0AH to REG0FH define for each 16 KB address range if it is a DRAM block in the system memory or on the IO channel.

INDEX	7	6	5	4	3	2	1	0	
08H	0	VERS		MW	MR	HM	SM	NI	IDENTIFICATION
09H	R3	R2	R1	R0	D3	D2	D1	D0	ROM CONFIGURATION
0AH	368K						256K		MEMORY ENABLE (16KB RESOLUTION)
0BH	496K						384K		
0CH	624K						512K		
0DH	752K						640K		
0EH	880K						768K		
0FH	1008K						896K		MEMORY ENABLE (16KB RESOLUTION)
2A									LOWER 256K (ENABLE/DISABLE)

Figure 2-5 Control and Address Space Map Register Summary

Table 2-2. Memory Configuration Register Definition

Index	Bits	Function
08H		Identification
	7	Controller Type Part type
		0 Interleaved Memory Controller (82C302)
	6:5	Version
		0 Initial
	4	MW - Middle Boot Space Write Protect. This bit is used in conjunction with bit 3 allowing the BIOS code to be copied into RAM and write protected at this location as well as below 1MB. It should only be used if there is RAM present at this address (16MB installed). Executing out of RAM will result in better performance than out of narrower (usually 8 or 16 bits) EPROMs.
		0 Read/Write of 256KB RAM at 16128K 00FC0000H. Default. 1 Read-Only of 256KB RAM at 16128K 00FC0000H
	3	MR - Middle Boot ROM disable
		1 The boot/BIOS ROM located just below 16MB is enabled. This is necessary for 286 compatibility. Default. 0 The boot/BIOS ROM located just below 16MB is disabled.
	2	HM - 16MB IO Channel Memory Limit
		0 $\overline{AF32}$ will not be asserted for addresses $\geq$ 16MB. This should only be used if external logic can recognize addresses above 16MB. Default. 1 $\overline{AF32}$ is asserted for addresses $\geq$ 16MB (01000000H). Since IO channel memory cannot normally be configured above 16MB, accessing above 16MB will cause a READY timeout if that feature is enabled. This is necessary during setup because memory address above 16MB that are not enabled for local memory could wrap into a valid IO channel memory location.
	1	SM - Minimum memory configuration after reset. Used during initialization.
		0 256K only enabled. Default. Ignore memory address configuration registers 0AH to 0FH. 1 Normal configuration controlled by registers 0AH to 0FH.
	0	NI - Single bank/interleave select 0 Disable interleave (single bank). Default. 1 Enable interleave

Table 2-2. Memory Configuration Register Definition (Continued)

Index	Bits	Function
09H		RAM/ROM Configuration in boot area.
	7	RAM at 768K C0000-CFFFFH (EGA)
	6	RAM at 832K D0000-DFFFFH
	5	RAM at 896K E0000-EFFFFH
	4	RAM at 960K F0000-FFFFFH (BIOS)
		Bits 7:4 disable writing to RAM located in the BIOS area in 64KB blocks. BIOS data.
		0 Read/Write. Default. 1 Read-Only
	3	ROM at 768K C0000-CFFFFH (EGA)
	2	ROM at 832K D0000-DFFFFH
	1	ROM at 896K E0000-EFFFFH
	0	ROM at 960K F0000-FFFFFH (BIOS)
		Bits 3:0 enable substitution of the BIOS ROM located below 1MB with RAM at the same location in 64KB blocks. This should be done after the BIOS code is copied from the ROM and the RAM locations have been write protected using bits 7:4. (Default is 0001)
		0 Disabled 1 Enabled
0AH		Address Map 256K 040000-05FFFFH (16K Resolution)
0BH		Address Map 384K 060000-07FFFFH
0CH		Address Map 512K 080000-09FFFFH
0DH		Address Map 640K 0A0000-0BFFFFH
0EH		Address Map 768K 0C0000-0DFFFFH
0FH		Address Map 896K 0E0000-0FFFFFH
		0 Address is on or controlled by the system board 1 Address is on the IO Channel.
		This permits 16K blocks of memory to be disabled allowing ROMs, memory expansion mechanisms (EMS or XMA) or memory mapped IO devices to reside within the lower 1MB address space.
2A<0>		Enable/Disable the lowest 256K RAM on the local memory bus.
		0 Disable. $\overline{AF32}$ = 1 1 Enable (default). $\overline{AF32}$ = 0
		When this bit is set (REG2A<0> = 1), any access to the lower 256K of memory will be a local memory cycle and will result in generation of $\overline{AF32}$.
		When bit is zero (REG2A<0> = 0), any access to the lower 256K of memory will be considered as an AT bus cycle and therefore, $\overline{AF32}$ will not be generated.

DRAM Array Configuration and Timing

The configuration registers REG10H to REG13H provides the DRAM type definition and starting address for each pair of banks, banks 0 and 1, and banks 2 and 3. The REG10H<7:6> and REG12H<7:6> defines if the DRAM's are enabled, uses 256K DRAM's, or uses 1M DRAM's. These bits defaults to 256K DRAM's upon reset. The REG10H<6:0> and REG12H<6:0> defines the address bits <25:20> of the starting address of the pairs of banks. Some of these bits may not be valid because the memory banks must start at some predefined boundaries. For 256K DRAM's, all bits <25:20> are valid if only single bank is enabled -it can be on any 1MB boundary; otherwise only bits <25:21> are valid starting address bits on 2MB boundaries. For 1M DRAM's, only bits <25:23> are valid forcing it on 8 MB boundaries. The REG11H<7> and REG13H<7> define the RAS precharge time required when a page miss occurs so that DRAM's of different speeds can be supported for each pair of banks. The REG11H<6> and REG13H<6> define the wait state to be inserted to meet the DRAM speed. These parameters default to the slower timing upon reset so that the system can be powered up with minimal assumptions on the DRAM speed and the memory configuration. Refer to Table 2-3 for details of the bit definitions.

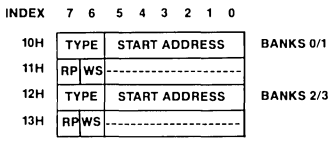


Figure 2.6. DRAM Configuration/Timing Register Summary

Index	Bits	Function
10H		bank 0/1 Type/Start Address
12H		bank 2/3 Type/Start Address
	7:6	DRAM Type
		0 none (bank disabled)
		1 256K words, default value for REG10H and REG12H
		2 1M words
		3 Reserved
	5:0	Starting Address 25:20 The DRAM type determines which address bits are valid in the address recognition process. This field of REG10H defaults to zero after reset.
		25:20 256K DRAM's. 1MB boundary 1MB per bank, single bank only. Valid for the first register only.
		25:21 256K DRAM's. 2MB boundary 1MB per bank, two banks required for interleaved operation.
		25:23 1M DRAM's. 8MB boundary 4MB per bank, two banks required for interleaved operation.

Table 2-3 DRAM Configuration and Timing Register Definition

Index	Bits	Function
11H		banks 0/1 Timing
13H		banks 2/3 Timing
	7	DRAM RAS precharge. Specifies the amount of time for RAS precharge when a page miss occurs. 0 3 CLK2 times (93 nS at 16MHz) 1 5 CLK2 times (155nS at 16MHz). Default.
	6	Access wait states Specifies the number of wait states in SCLK units to allow the use of slower DRAMs. 0 0 wait-state 1 1 wait-state. Default.
	5:0	Reserved

Table 2-3 DRAM Configuration and Timing Register Definition (Continued)

Diagnostic Access Register

REG28H<7> controls the parity check enable and defaults to "disable" after reset. This bit generates the $\overline{\text{PEN}}$ signal for enabling the parity check by 82A306. When parity errors occur REG28H<1:0> and REG29H<7:0> will latch the error address <25:16>.

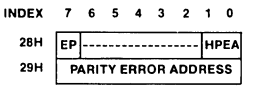


Figure 2.7. Diagnostic Access Register Summary

Index	Bits	Function
28H		Error Source/Address (MSBs)
	7	Parity check disable 0 Enabled 1 Disabled (default)
	6:2	Not used, returns unpredictable value.
	1:0	High Parity Error Address bits <25:24>
29H		Parity Error Address (LSBs)
	7:0	Error address bits <23:16>

Table 2-4. Diagnostic Access Registers Definition

Features of 82C302 Rev. C

The default state of the 82C302 Rev C is similar to 82C302 except for the 3 non-programmable features listed at the bottom of this page.

In addition to the registers which the 82C302 version B has, a new register at location 20H is implemented in version C, and is accessible through I/O ports 22H and 23H. This new register allows the user to enable the additional features that we have incorporated into the 82C302 Rev C.

4 bits are used in this byte and they are defined as follows:

REG20<7>: Deassert $\overline{RAS}$ for non-pipelined cycles.

0 default value, same as version B.

1 All 4 CPU DRAM control state machines will be reset to idle when a pipelined cycle is followed by a non-pipelined cycle. Therefore, all $\overline{RAS}$'s will be deasserted and the minimum $\overline{RAS}$ precharge time could be 75ns at 20 MHz system speed.

REG20<6>: Disable stagger $\overline{RAS}$ refresh mode

0 default value, Staggered refresh.

1 All 4 $\overline{RAS}$'s will be active at the same time.

REG20<5:4>: Fast $\overline{CAS}$ precharge time.

0 default value

1 $\overline{CAS}$ precharge time can be 1 CLK2 cycle. This will eliminate the extra wait state of a read cycle immediately following a write cycle to the same bank. REG20<5> controls CAS<1:0> and REG20<4> controls CAS<3:2> precharge timings.

REG20<3:0>: These bits are not used.

Non-programmable features of 82C302 version C includes:

- 1 wait state non-pipelined write cycle instead of 2 wait states
- Bits 6 and 5 of register 08 will read 01 instead of 00
- The page size of 1MEG DRAM is 4KB instead of 2KB.

The The 82C302 Rev C has 2KB page size for 256K type DRAM's and 4K page size for 1M type DRAM's. Following table shows the address multiplexing for different organizations:

Address Assignment	Row MA9-MA0	Column MA9-MA0
One bank		
256K DRAM's	A<19:11>	A<10:2>
1M DRAM's	A<21:12>	A<11:2>
Interleave		
256K DRAM's	A<20:12>	A<10:2>
1M DRAM's	A<22:13>	A<11:2>

In interleaved memory cases, for 256K DRAM's, address bit A<11> determines which bank is accessed. Address bit A<12> is used in 1M DRAM's to determine which bank is accessed.

The Column addresses shown in the above table are in sequence, however, the row addresses shown are not necessarily in sequence. Following table shows the row address multiplexing:

	Row Address MA9 MA0
One bank, 256K DRAM	19,18,17,16,15,14,13,12,11
One bank, 1M DRAM's	21,19,18,17,16,15,14,13,12,20
Interleave, 256K DRAM	19,18,17,16,15,14,13,12,20
Interleave, 1M DRAM's	21,19,18,17,16,15,14,13,22,20

82C302 Pin Description

Pin No.	Symbol	Pin Type	Description
Clocks and Control			
44	CLK2	I	Processor Clock input from 82C301.
46	SCLK	O	Generated CLK2/2 for reference.
41	RESET	I	RESET4 is the active high reset input from the 82C301. It resets the configuration registers to their default values. When active, RAS<0:3> and CAS <0:3> remain high, and OSC and OSC/12 remain inactive.
49	$\overline{REF}$	I	REFRESH is an active low input for DRAM refresh control from the 82C301. It initiates a refresh cycle for the DRAMs.
47	$\overline{MALE}$	I	Active low. Address Latch Enable.
33	W/$\overline{R}$	I	System WRITE/$\overline{READ}$ status input.
48	$\overline{SMCMD}$	I	Active low. System Memory Command. Indicates that the current command is for memory.
37	$\overline{XIOR}$	I	Active low. I/O READ command is used to qualify $\overline{IO2XCS}$.
38	$\overline{XIOW}$	I	Active low. I/O WRITE command is used to qualify $\overline{IO2XCS}$.
35	$\overline{XMEMR}$	I	Active low. X Bus memory READ command.
36	$\overline{XMEMW}$	I	Active low. X Bus memory WRITE command.
45	HLDA1	I	Active high. HOLD ACKNOWLEDGE 1 is an input from 82C301. It is used to generate RAS and CAS signals for the DMA cycles, in response to a HOLD request.
63	$\overline{LPAR}$	I	Active low. Latched Parity error indication during a DRAM read. The failing address will be latched inside the chip for diagnostic purposes.
8	$\overline{HIROM}$	I	Active low. High ROM address chip select asserted when the highest 16 MBytes of memory is addressed (A<31:24>=FFH). Unlatched. This is used in conjunction with the remaining address bits to generate the $\overline{ROMCS}$ signal.
7	$\overline{L64MEG}$	I	Active low. Low 64M address that is asserted when A<31:26>=00H. This is an active low input, which is normally sourced from the 82A303 high order address buffer. This input is asserted when A<31:26> = 00H. It is not latched internally. This input can optionally be de-activated by external logic to prevent the 82C302 from activating either $\overline{AF32}$ or memory control signals.
65	$\overline{ROMCS}$	O	Active low ROM. Chip select for the BIOS EPROMs that is qualified with W/$\overline{R}$ and $\overline{SMCMD}$.

82C302 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
Clocks and Control (Continued)			
6	$\overline{IO2XCS}$	I	Active low. IO address 22H and 23H chip selects. I/O port 22H is the index register for the configuration register set and and I/O 23H is accessed as the 8 bit configuration register selected by the index written to I/O port 22H.
09-32	A<25:02>	I	Address from the CPU local bus.
64	XA00	I	Address from the X Bus.
34	$\overline{READY}$	I/O	$\overline{READY}$ is the system ready signal to the CPU. It is an active low output, activated when the requested memory data transfer is being completed. It is an input when the current bus cycle is an AT bus cycle ($\overline{AF32}$ = 1) and an output during local 32 bit memory cycle ($\overline{AF32}$ = 0).
39	$\overline{BUSY}$		Active low. BUSY indicates that the memory controller is still servicing a previous request. This should be connected to IOCHRDY through an open collector buffer. This signal should not be confused with the BUSY of 80386.
40	$\overline{AF32}$	O	Active low, open drain. If asserted indicates that the current address is for local 32-bit memory on the system board (DRAM or possibly EPROM). Otherwise the current address is assumed to be on the AT IO channel.
Memory Expansion			
61-60	NC		No connect.
2	$\overline{DRD}$	O	Active low. DRAM Read controls the direction of data transfer between the DRAM and local bus. When low, it enables data transfer from the memory bus <MD BUS> to the local data bus. When high, the data transfer is from the local data bus to the memory data bus.
DRAM Interface			
70-67	$\overline{RAS}$<3:0>	O	Row Address Strobes <3:0> are active low outputs. There is one RAS for each bank. RAS0 selects the lowest bank and RAS3 selects the highest bank. These lines should be buffered and line terminated with 33Ω resistor before driving the DRAM RAS lines.
71	$\overline{CAS}$	O	Active low. Column Address Strobe. Used to latch data in the 82A305 data buffer.

82C302 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
DRAM Interface (Continued)			
56-55 53-52	$\overline{CAS}$<3:2> $\overline{CAS}$<1:0>	O	Active low. Column Address Strobe. A strobe per bank that must be externally gated with byte enables for each byte of DRAM chips. These signals should be buffered and line terminated with 33Ω resistors before driving the DRAM CAS lines.
58	OSC/12	I	1.19MHz Clock input is used for RAS low time out. This input can optionally be strapped high to disable RAS time out.
66	$\overline{DWE}$	O	Active low. DRAM Write Enable.
51	$\overline{FBE}$	O	Force Byte Enable. This is an active low signal. It is activated during local memory read cycles. When active, all the byte enables are forced low, independent of $\overline{MALE}$ or the BE<3:0>, thereby resulting in 32-bit memory read operation. This signal is connected to the FBE input on the 82A306.
72-73	DA<9:8>	O	DRAM address lines DA9 and DA8. These lines should be buffered and line terminated with 75Ω resistors before driving the DRAM array.
75-82	XDA<7:0>	I/O	These are multiplexed bi-directional pins. During accesses to the internal registers, these lines provide the index value and configuration information. During DRAM cycles, DA<7:0> generate the lower address bits for the DRAM array. A 74LS245 is required to isolate DRAM addresses during a memory access. These lines should be buffered and line terminated with 75Ω resistors before driving the DRAM array.
83	$\overline{XDEN}$	O	Active low. XD bus buffer Enable. $\overline{XDEN}$ is asserted during IO access cycles to 022H and 023H internal registers of 82C302. $\overline{XDEN}$ is used to control the chip enable for the buffer between the XD and XDA buses.
3	$\overline{PCHK}$	O	Active low. Parity Check.
4	$\overline{PEN}$	O	Active low. Overall Parity Enable.
50	$\overline{MDEN}$	O	Active low. MEMORY DATA BUFFER ENABLE is by default always low and is connected to $\overline{MDEN}$ of 82A305.
Miscellaneous			
5,57,59			No Connect.
42,84,62	VDD		Power.
1,43 54,74	VSS VSS		Ground.

82C302 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C302 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C302 DC Characterisitcs

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=8mA (Note 1)	V_{OL}		0.45	V
Output High Voltage I_{OH}=-200 μA	V_{OH}	2.4		V
Input Current $0 < V_{IN} < V_{CC}$	I_{IL}		±10	μA
Output Short Circuit Current V_O=0V	I_{OS}	TBD	TBD	mA
Input Clamp Voltage	V_{IC}		TBD	V
Power Supply Current @ 25 MHz Clock	I_{CC}		40	mA
Output HI-Z Leak Current $0.45 < V_{OUT} < V_{CC}$	I_{OZ1}		±10	μA

NOTE:
1. SYSCLK, $\overline{\text{DWE}}$, $\overline{\text{RAS<3:0>}}$, $\overline{\text{CAS}}$, $\overline{\text{CAS<3:0>}}$ have I_{OL} = 8mA. All other outputs and I/O pins have I_{OL} = 4mA. In all cases all I_{OL} = I_{OH} for the pin.

82C302 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C302-16 Min	Typ	Max	82C302-20 Min	Typ	Max	Unit	Notes
t200	CLK2 input cycle time	31			25			ns	
t201	CLK2 fall time	2		5	2		5	ns	
t202	CLK2 rise time	2		5	2		5	ns	
t203	CLK2 low time	10			9			ns	at 2V
t204	CLK2 high time	10			9			ns	at 2V
t205	RESET hold time	6			6			ns	
t206	RESET set-up time	5			5			ns	
t207	SCLK delay time	6	12	22	6	12	22	ns	
DMA Sequence									
t210	$\overline{RAS}i$ de-assertion time from HLDA1	13			13			ns	
t211	$\overline{RAS}i$ active delay from commands active	17		25	17		25	ns	
t212	Address set-up time to commands active	35			35			ns	
t213	Address hold time from commands inactive	0			0			ns	
t214	$\overline{AF32}$ active time from commands active	22	26		22	26		ns	
t215	$\overline{DRD}$ active time from commands active	10		25	10		25	ns	
t216	$\overline{Row}$ address set-up time to $\overline{RAS}$ active	10			10			ns	
t217	$\overline{Row}$ address hold time from $\overline{RAS}$ active	15			13		19	ns	
t218	$\overline{CAS}i$ active delay from $\overline{RAS}$ active for DMA memory read cycle	1.0 CLK2			1.0 CLK2			ns	
t219	$\overline{CAS}i$ active delay from $\overline{RAS}$ active for DMA memory write cycle	1.5 CLK2			1.5 CLK2			ns	
t220	$\overline{DWE}$ active delay from $\overline{RAS}$ active	0.5 CLK2			0.5 CLK2			ns	
t222	$\overline{RAS}i$ de-assertion time from commands inactive			15			15	ns	

Test Load = 65pF unless otherwise specified.

82C302 AC Characteristics (Continued)

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C302-16 Min	82C302-16 Typ	82C302-16 Max	82C302-20 Min	82C302-20 Typ	82C302-20 Max	Unit	Notes
DMA Sequence (Continued)									
t223	Column address hold time from commands active	16			16			ns	
t224	$\overline{CASi}$ de-assertion from commands inactive		22	28		22	28	ns	
t225	$\overline{AF32}$ tri-state delay from commands inactive		21	25		21	25	ns	
t226	$\overline{DWE}$ de-assertion time from commands inactive		11	15		11	15	ns	
t228	$\overline{DRD}$ de-assertion time from commands inactive		12			12		ns	
ROMCS Sequence									
t235	$\overline{ROMCS}$ active delay from CLK2			27			27	ns	
t236	$\overline{ROMCS}$ inactive delay from CLK2			22			22	ns	
t237	$\overline{READY}$ input set-up time to CLK2	8			8			ns	
t238	$\overline{READY}$ input hold time from CLK2	0			0			ns	
REFRESH Sequence									
t240	IOCHRDY going low from $\overline{REF}$ active		14	18		14	18	ns	
t241	IOCHRDY float delay from CLK2		18	25		18	25	ns	
t242	$\overline{RAS0}$ precharge time		3 CLK2			3 CLK2		ns	
t243	$\overline{RASi}$ (0 to 3) pulse width		4 CLK2			4 CLK2		ns	
t244	$\overline{RAS(i+1)}$ active delay from $\overline{RASi}$ active		1 CLK2			1 CLK2		ns	
t245	Refresh address set-up time to $\overline{RASi}$		3 CLK2			3 CLK2		ns	
t246	Refresh address hold time from $\overline{RASi}$		2 CLK2			2 CLK2		ns	
t247	$\overline{RASi}$ inactive delay from CLK2		14	18		14	18	ns	
t248	$\overline{RASi}$ active delay from CLK2		15	18		15	18	ns	

Test Load = 65pF unless otherwise specified.

82C302 AC Characteristics (Continued)

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C302-16 Min	Typ	Max	82C302-20 Min	Typ	Max	Unit	Notes
IO Read/Write Sequence									
t250	$\overline{IO2XCS}$ set-up time to $\overline{XIOR}$ or $\overline{XIOW}$	10			10			ns	
t251	XA0 set-up time to $\overline{XIOR}$ or $\overline{XIOW}$	10			10			ns	
t252	$\overline{IOCS16}$ hold time from $\overline{XIOR}$ or $\overline{XIOW}$	15			15			ns	
t253	XA0 hold time from $\overline{XIOR}$ or $\overline{XIOW}$	15			15			ns	
t254	$\overline{XDEN}$ active delay from $\overline{XIOR}$ or $\overline{XIOW}$	15		19	15		19	ns	
t255	$\overline{XDEN}$ inactive delay from $\overline{XIOR}$ or $\overline{XIOW}$	12			12			ns	
t256	XDA<7:0> input set-up time to $\overline{XIOW}$	10			10			ns	
t257	XDA<0:7> input hold time to $\overline{XIOW}$	8			8			ns	
t258	XDA<7:0> output valid delay from $\overline{XIOR}$			37			37	ns	
t259	XDA<7:0> hold time from $\overline{XIOR}$			15			15	ns	
CPU to Memory Sequence									
t260	$\overline{MALE}$ active setup time to CLK2	5			5			ns	
t261	$\overline{MALE}$ inactive delay from CLK2	10			10			ns	
t262	Address/Status set-up time to CLK2	10			10			ns	
t263	Address/Status hold time from $\overline{MALE}$	10			10			ns	
t264	$\overline{L64MEG}$, $\overline{HIROM}$ set-up time to CLK2	10			10			ns	
t265	$\overline{L64MEG}$, $\overline{HIROM}$ hold time to $\overline{MALE}$	10			10			ns	
t266	$\overline{SMCMD}$ setup time to CLK2↓	10			6			ns	

Test Load = 65pF unless otherwise specified.

82C302 AC Characteristics (Continued)

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C302-16 Min	Typ	Max	82C302-20 Min	Typ	Max	Unit	Notes
CPU Cycle Timing									
t270	$\overline{AF32}$ active delay from CLK2			26			25	ns	C_L=35pF
t271	$\overline{AF32}$ inactive delay from CLK2		17	20		14	18	ns	
t272	$\overline{CASi}$ active delay from CLK2 for read hit cycles			13			11	ns	C_L=35pF
t273	$\overline{CASi}$ inactive delay from CLK2	8		17	8		17	ns	C_L=35pF
t274	$\overline{CAS}$ active delay from CLK2 for read hit cycles	13		18	13		18	ns	
t275	$\overline{CAS}$ inactive delay from CLK2	9		18	9		18	ns	
t276	Column address stable from $\overline{ADS}$			25			25	ns	
t277	$\overline{DRD}$ active delay from CLK2		21	30		21	30	ns	
t278	$\overline{DRD}$ inactive delay from CLK2		17	22		17	22	ns	
t279	$\overline{FBE}$ active delay from CLK2		23	25		23	25	ns	
t280	$\overline{FBE}$ inactive delay from CLK2			20			20	ns	
t281	$\overline{READY}$ active delay from CLK2			18			15	ns	
t282	$\overline{READY}$ inactive delay from CLK2			18			18	ns	
t283	$\overline{RASi}$ active delay from CLK2	10	15	18	10	13	16	ns	C_L=35pF
t284	Row address set-up time to $\overline{RASi}$	10			10			ns	
t285	Row address hold time from CLK2	15			15			ns	
t286	$\overline{CASi}$ active delay from CLK2			18			18	ns	C_L=35pF
t287	$\overline{CAS}$ active delay from CLK2			22			22	ns	
t288	$\overline{RASi}$ inactive delay from CLK2			18			18	ns	
t289	$\overline{RASi}$ precharge time		3 CLK2			3 CLK2		ns	
t290	$\overline{CASi}$ precharge time		1.5 CLK2			1.5 CLK2		ns	
t291	$\overline{DWE}$ active delay from CLK2			18			18	ns	
t292	$\overline{DWE}$ inactive delay from CLK2			19			19	ns	
t293	IOCHRDY going low from $\overline{XMEMR}$ or $\overline{XMEMW}$			32			32	ns	

82C302 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C302-16 Min	82C302-16 Typ	82C302-16 Max	82C302-20 Min	82C302-20 Typ	82C302-20 Max	Unit	Notes
CPU Cycle Timing (Continued)									
t294	IOCHRDY going high from $\overline{CAS}$ (read cycle)			23			21	ns	
t295	IOCHRDY going high from $\overline{CAS}$ (write cycle)			9			9	ns	

Test Load = 65pF unless otherwise specified.

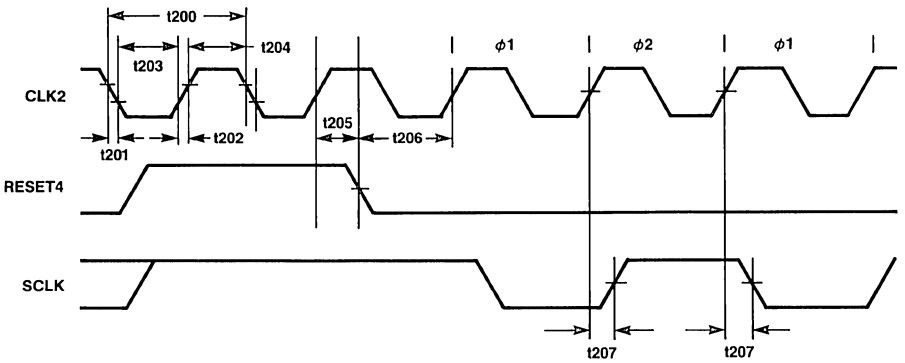
82C302 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C302-25 Min	82C302-25 Typ	82C302-25 Max	Unit	Notes
t200	CLK2 input cycle time	20			ns	
t217	Row address hold time from $\overline{RAS}$ active	10		15	ns	
t260	$\overline{MALE}$ active setup time to CLK2	3			ns	
t266	$\overline{SMCMD}$ setup time to CLK2↓	4			ns	
t270	$\overline{AF32}$ active delay from CLK2			19	ns	
t273	$\overline{CASi}$ inactive delay from CLK2			17	ns	
t283	$\overline{RASi}$ active delay from CLK2			16	ns	
t286	$\overline{CASi}$ active delay from CLK2			12	ns	

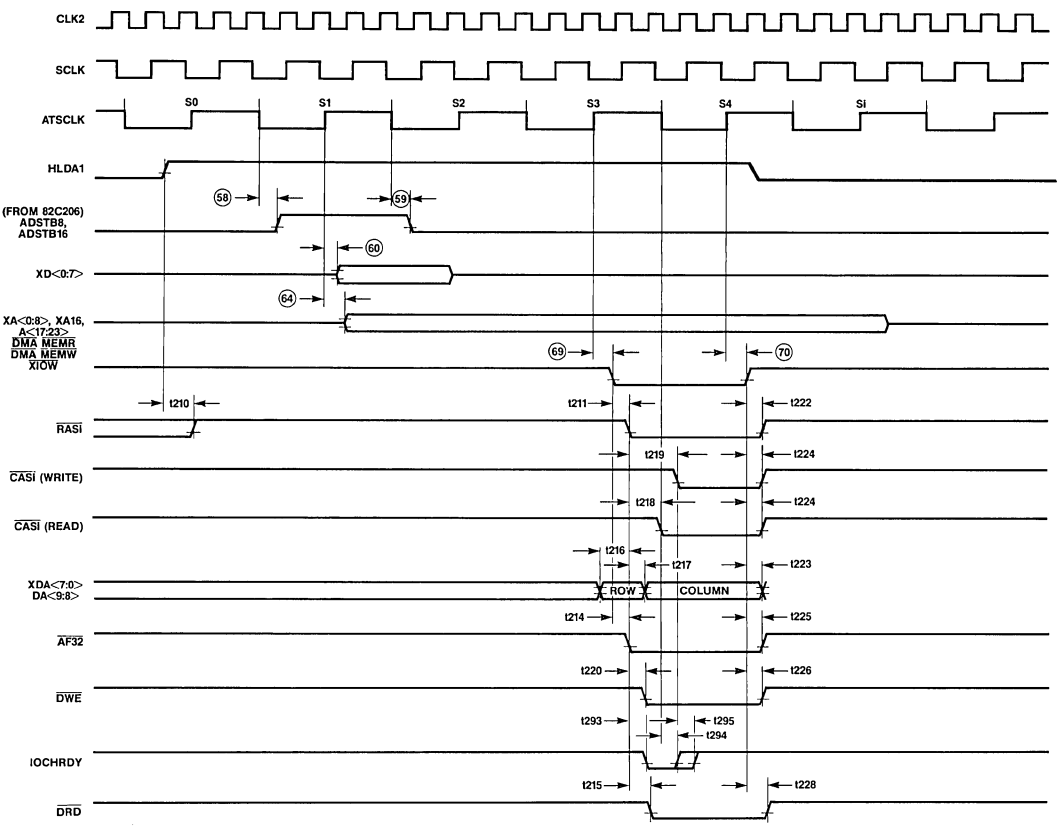
Test Load = 65pF unless otherwise specified.

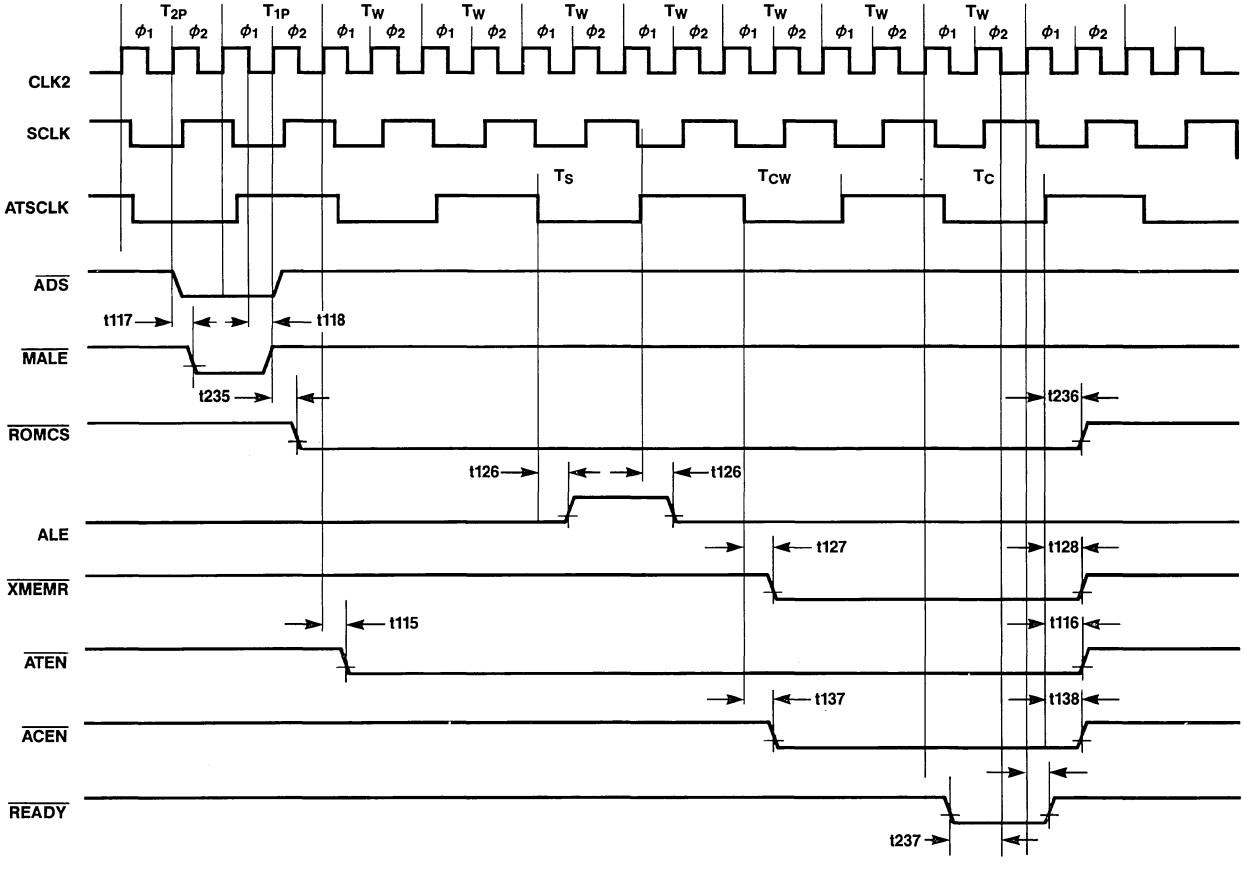
Note: All other parameters not specified at 25MHz are the same as the 82C302-20 specifications.

82C302 TIMING DIAGRAM (RESET SEQUENCE)



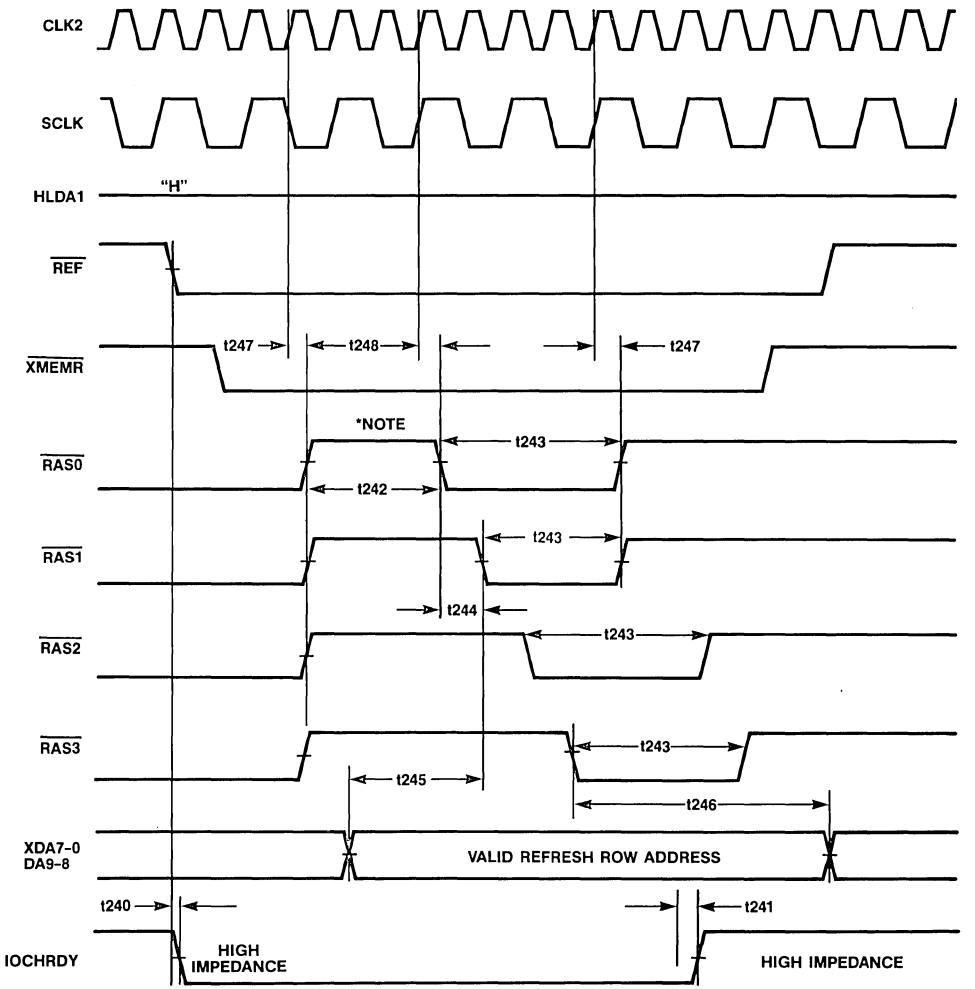
82C302 DMA Cycle





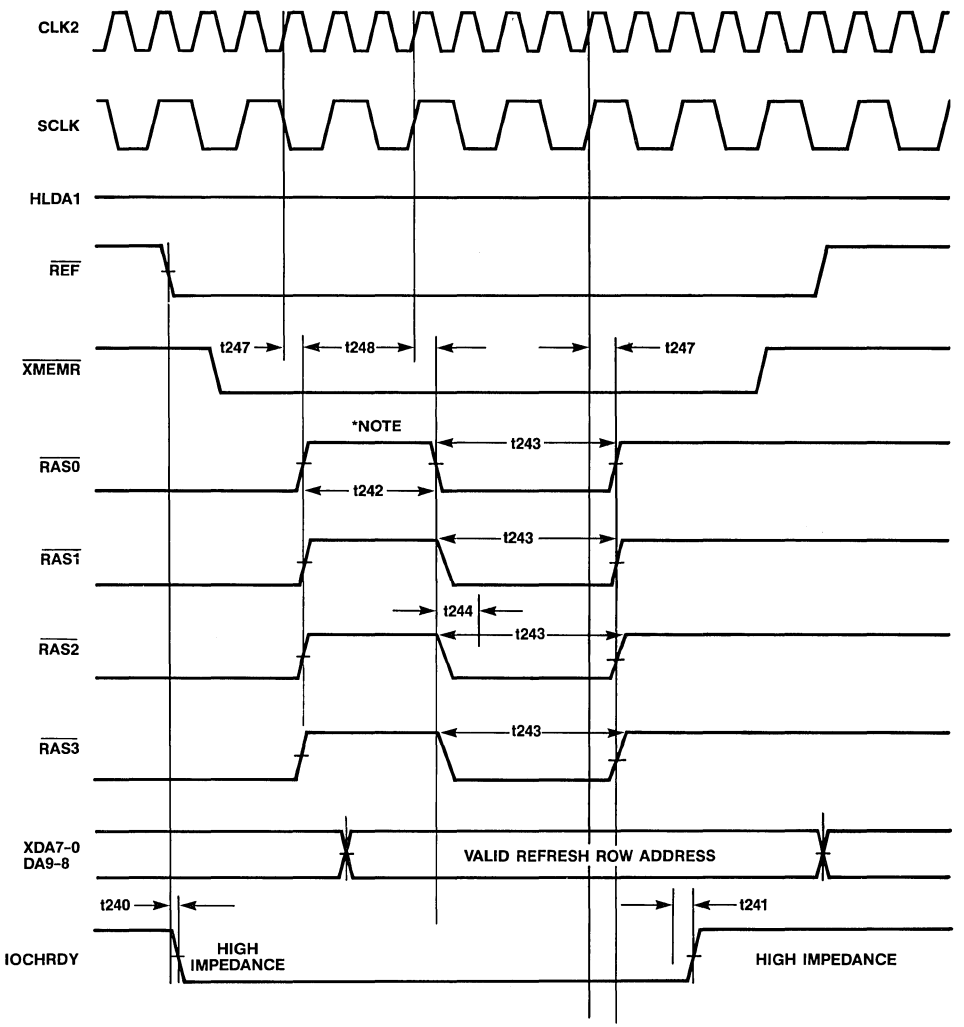
82C302 ROM Read Cycle

82C302 Refresh Cycle Waveform (Staggered)



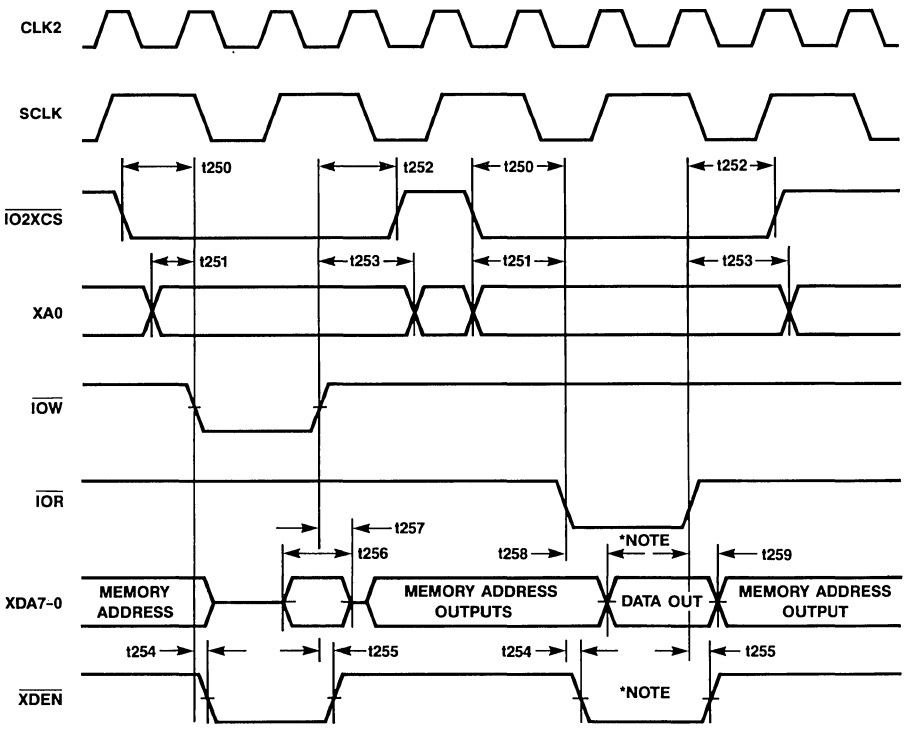
***NOTE:** Add 2 more clock cycles if either Bit 7 of register 11 is 1 or Bit 7 of register 13 is 1.

82C302 Rev. C Non-Staggered Refresh Cycle Waveform



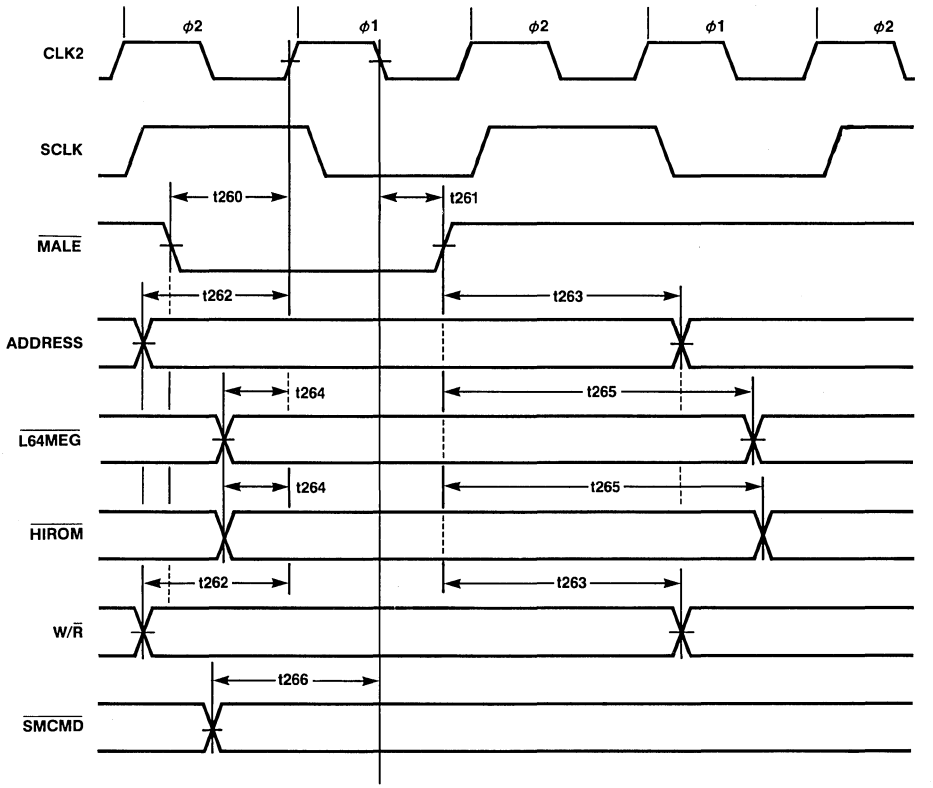
***NOTE:** Add 2 more clock cycles if either Bit 7 of register 11 is 1 or Bit 7 of register 13 is 1.

82C302 TIMING DIAGRAM (IO READ/WRITE)

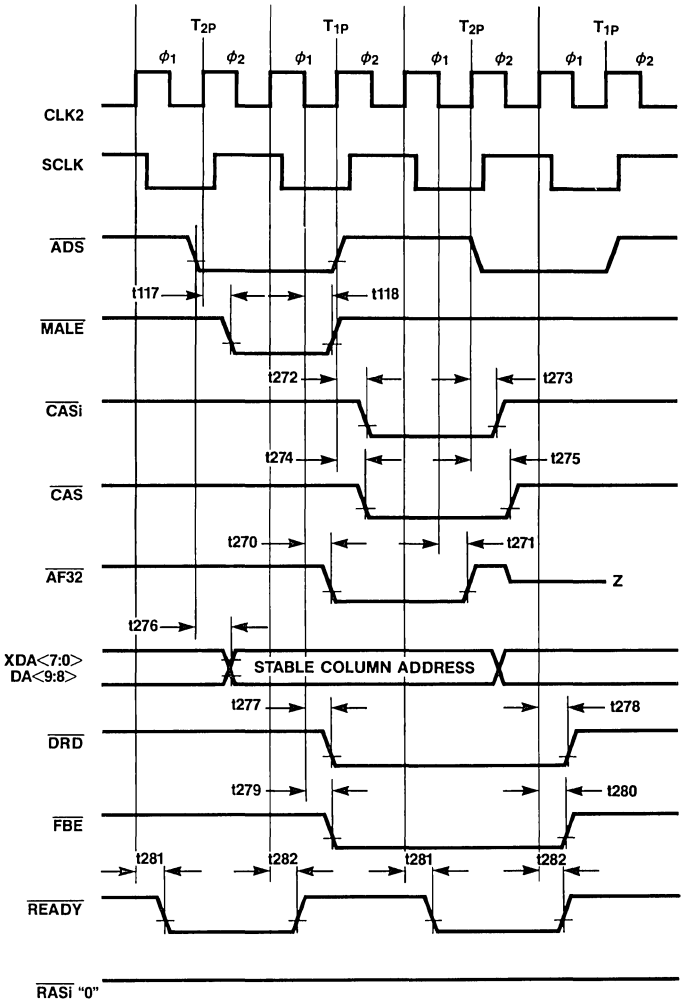


***NOTE:** No data output and XDEN is inactive if the index set up by the previous IO22 Write doesn't point to a valid IO23 register of 82C302.
Valid registers of IO23: 08H-0FH, 10H-13H, 28H-29H.

82C302 TIMING DIAGRAM (INPUT SETUP/HOLD TIME FOR CPU CYCLES)

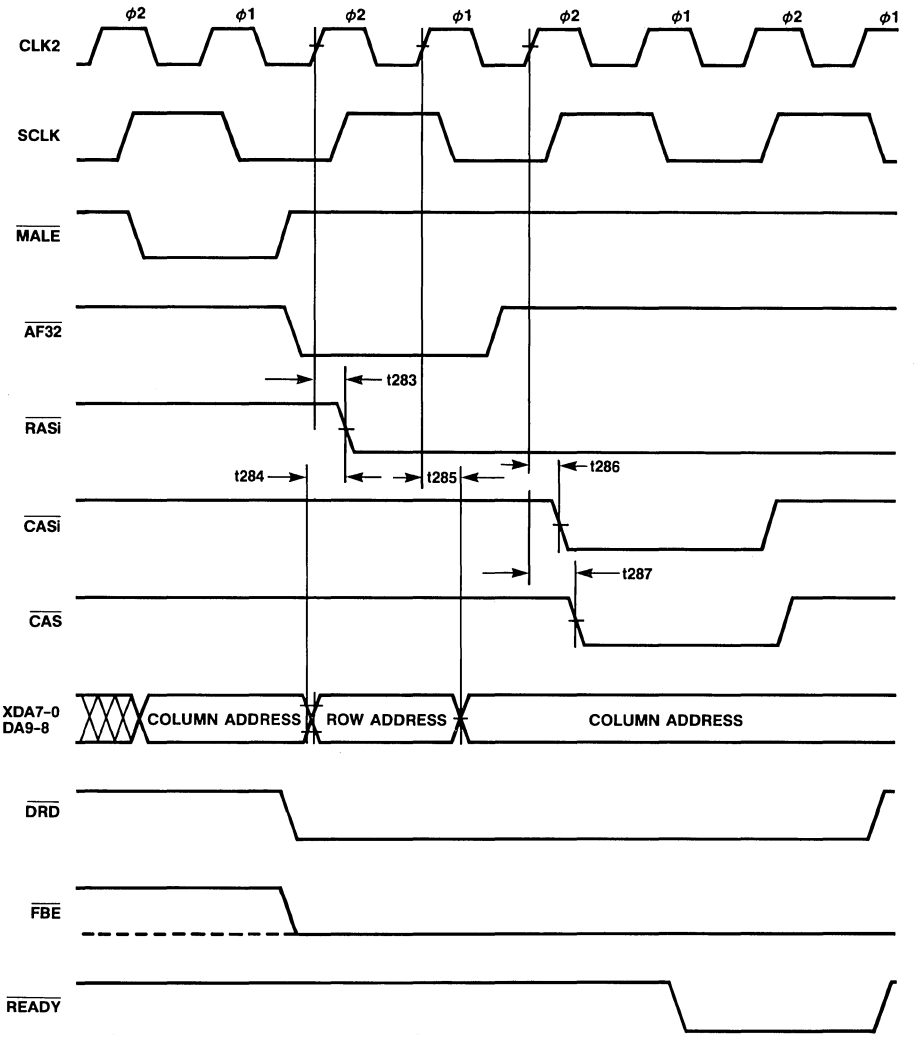


82C302 Timing Diagram (CPU to Local Memory Cycle) Read Hit 0WS

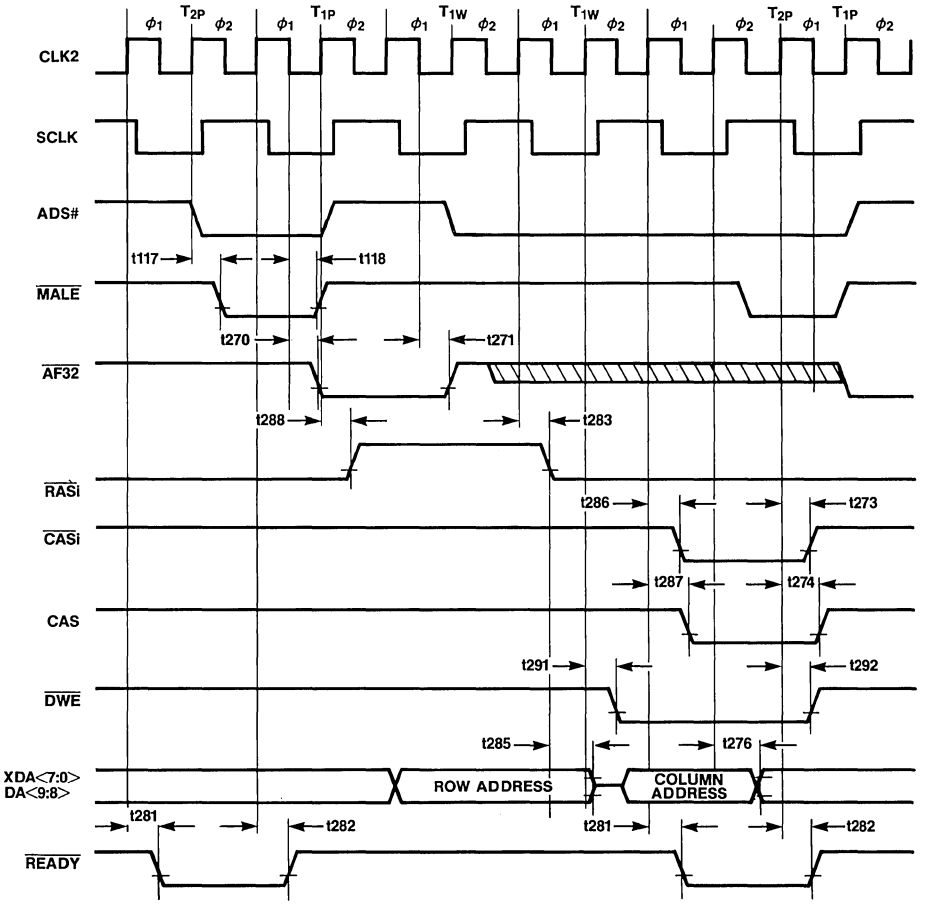


*INTEL 80386 DATA SHEET, A.C. TIMING SPECIFICATIONS.

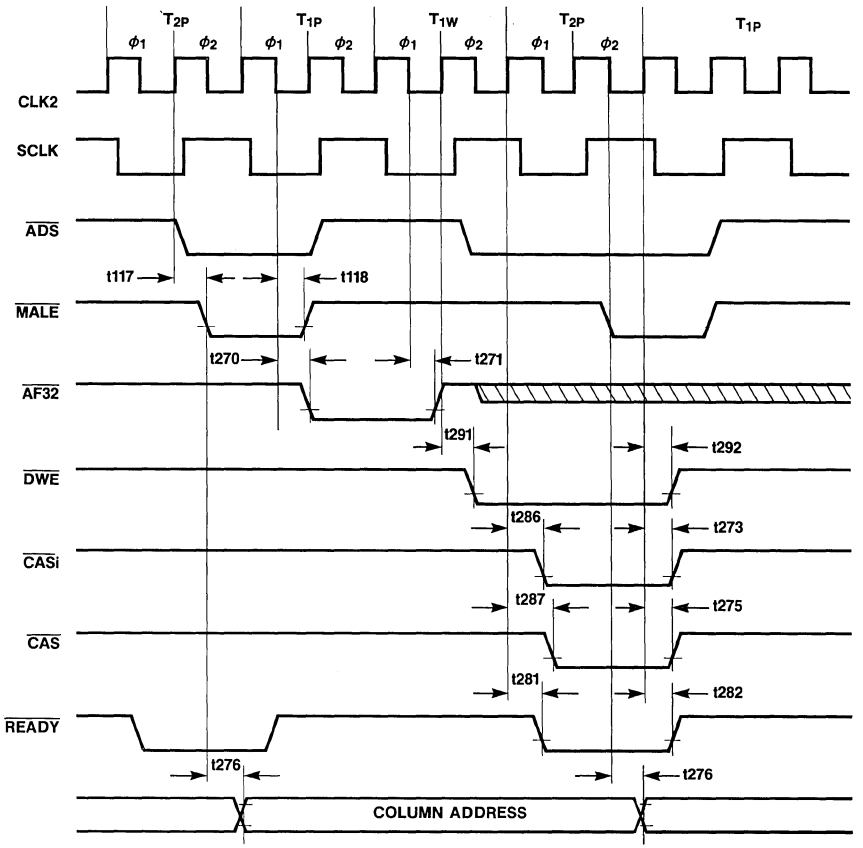
82C302 TIMING DIAGRAM (CPU TO LOCAL MEMORY)
READ CYCLE WITH RAS BEING INACTIVE



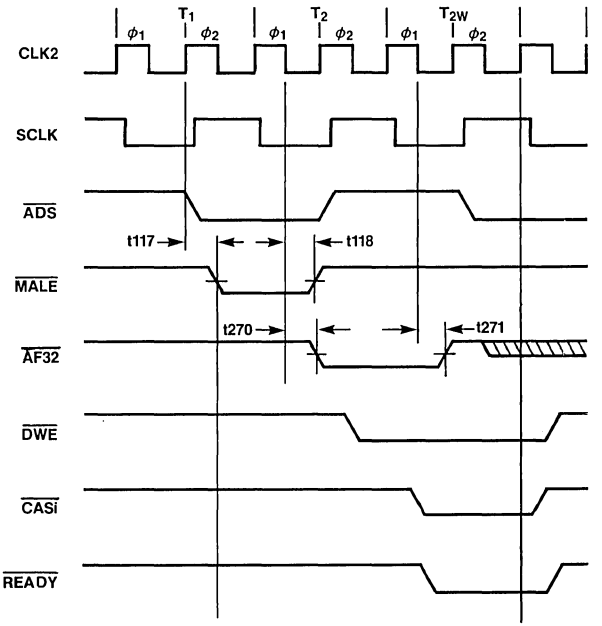
82C302 Write Miss Cycle with RAS Low



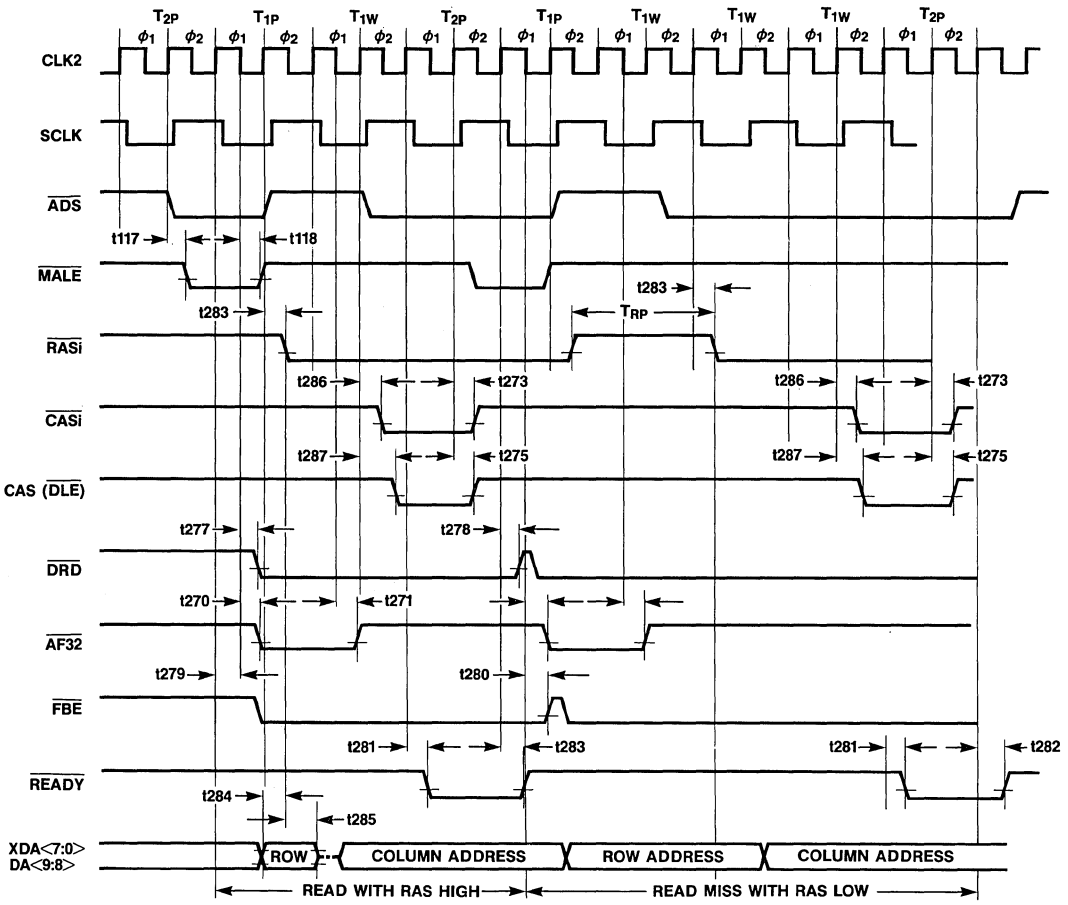
82C302 DRAM Write Hit, Pipelined Cycle



82C302 Rev. C DRAM Write Hit, Non-Pipelined Cycle



Read Cycle with RAS Being High



82A303/82C303
High Address Buffers

- Buffer for bits 31:12 of the Local, X and System address buses.
- X and S address busses can be extended to 27 bits (128MB).
- Direct interface to AT Bus.
- Advanced Schottky TTL technology.

Functional Description

The 82A303 as shown in figure 3-1 provides two functions:

- Generation of address decoding signals required by other chips.
- Interface between the local, X and System address busses.

Address Decode

The address decoding circuit provides outputs LIOCS, LMEGCS, L64MEG, and HIROM.

Signal	Decode Condition
LIOCS	A<15:12> = 00H
LMEGCS	A<31:20> = 00H
L64MEG	A<31:26> = 00H
HIROM	A<31:24> = 3FH

Table 3-1. High Address Decodes Definition

These signals are active if the address accesses satisfy the conditions defined in table 3-1. The signal decodes for LIOCS and LMEGCS are controlled by HLDA1 and latched on the trailing edge of MALE. The L64MEG and HIROM are simply decoded from the address signals.

Address Bus Interfaces

The 82A303 interconnects the local, X and system address buses with bidirectional drivers connecting each bus and the internal buses. These drivers have 24mA current drives for direct connection to the system address bus. The table 3-2 shows how the drivers are configured between the buses for each type of active bus requests. Note that the default configuration is set up so that the CPU address bus drives the memory address bus for local memory CPU access cycles.

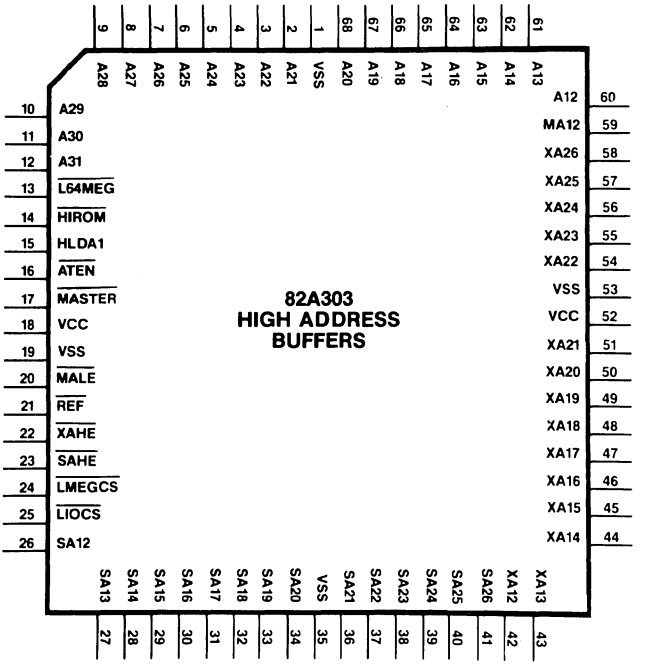
For all CPU sourced accesses, the addresses are latched on the trailing edge of MALE.

27 Bit Address Extensions

The standard AT implementation supports only 24-bit addresses. The CS 8230 allows for address extension on the SA and XA buses to 27 bits (128MB). This is done by grounding the enable pin XBHE for XA bus and SBHE for SA bus. Internal pullups are provided so that if the enable pins are left unconnected bits 24 to 27 of the respective bus are forced low.

HLDA	ATEN	REF	MASTER	Cycle Type	A Bus		S Bus		X Bus	
					Source	Output	Source	Output	Source	Output
0	1	1	1	CPU, non-AT	—	Disable	—	Disable	—	Disable
0	0	1	1	CPU AT bus cycle	—	Disable	A Bus	Enable	A Bus	Enable
0	1	0	1	CPU Refresh	—	Disable	X Bus	Enable	—	Disable
1	1	1	0	Master	S Bus	Enable	—	Disable	S Bus	Enable
1	1	0	0	Master Refresh	—	Disable	—	Enable	—	Disable
1	1	1	1	DMA	X Bus	Enable	X Bus	Enable	—	Disable

Table 3-2. High Address Bus Control


82A303
HIGH ADDRESS
BUFFERS
1 VSS
2 A21
3 A22
4 A23
5 A24
6 A25
7 A26
8 A27
9 A28
10 A29
11 A30
12 A31
13 L64MEG
14 HIROM
15 HLDA1
16 ATEN
17 MASTER
18 VCC
19 VSS
20 MALE
21 REF
22 XAHE
23 SAHE
24 LMEGCS
25 LIOCS
26 SA12
27 SA13
28 SA14
29 SA15
30 SA16
31 SA17
32 SA18
33 SA19
34 SA20
35 VSS
36 SA21
37 SA22
38 SA23
39 SA24
40 SA25
41 SA26
42 XA12
43 XA13
44 XA14
45 XA15
46 XA16
47 XA17
48 XA18
49 XA19
50 XA20
51 XA21
52 VCC
53 VSS
54 XA22
55 XA23
56 XA24
57 XA25
58 XA26
59 MA12
60 A12
61 A13
62 A14
63 A15
64 A16
65 A17
66 A18
67 A19
68 A20

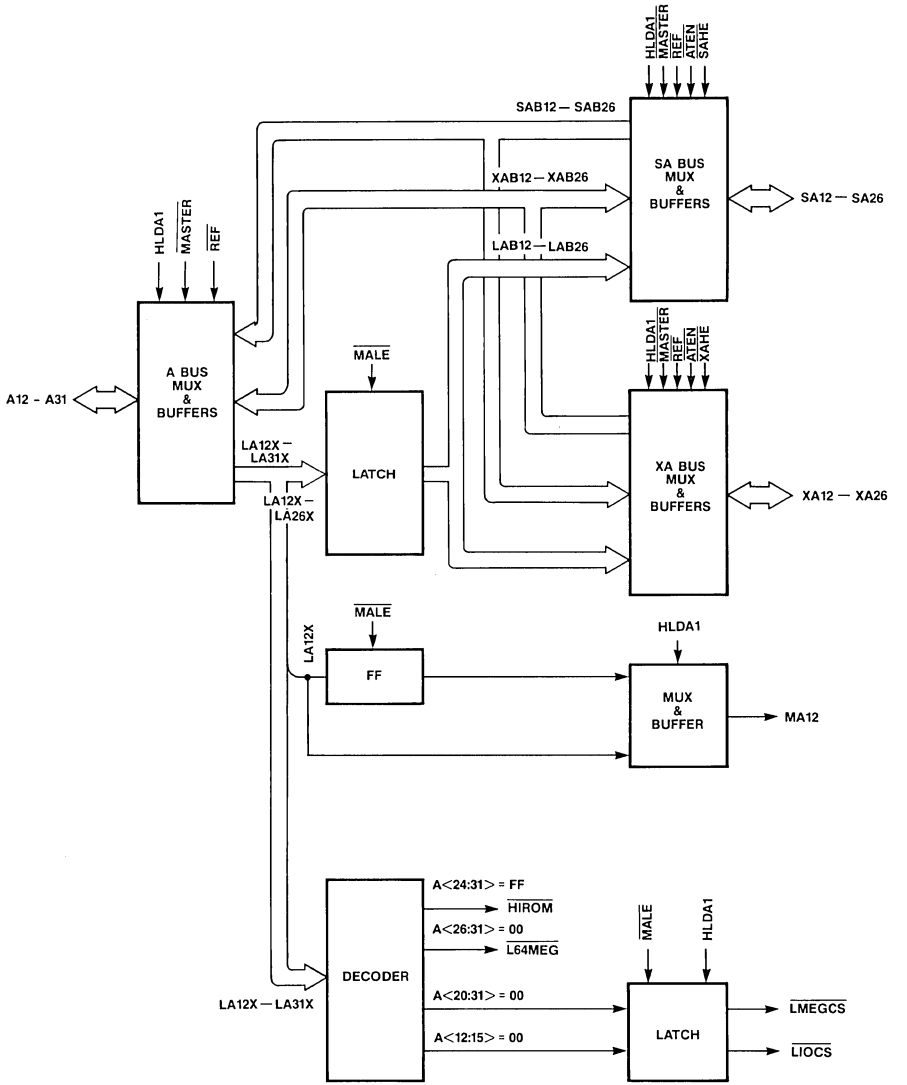
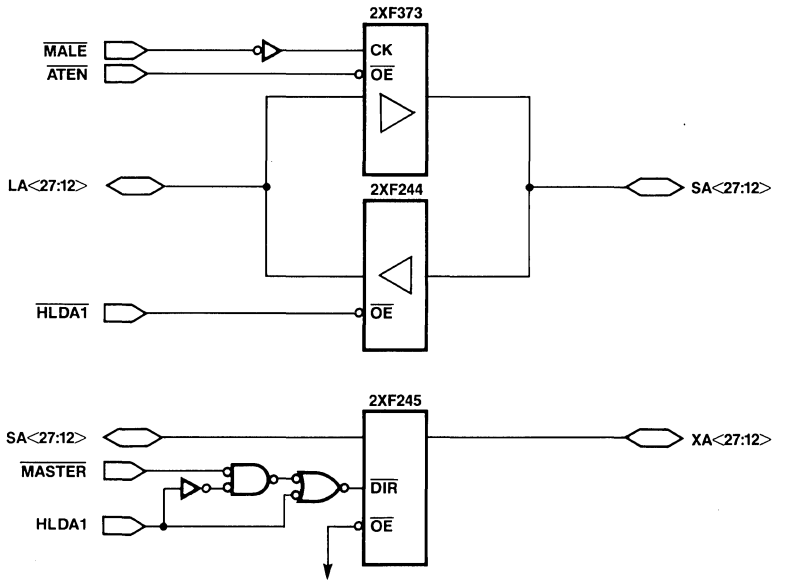
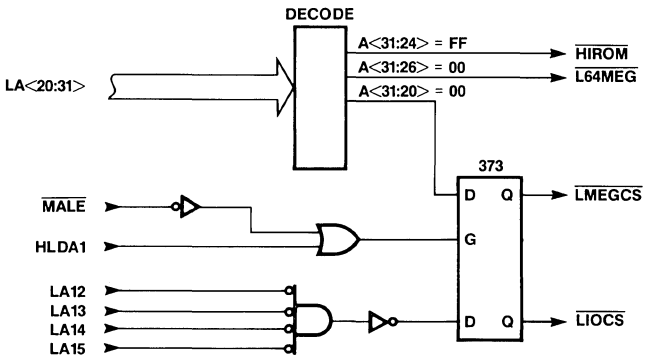


Figure 3-1. 82A303 Functional Block Diagram



82A303 SA to XA TTL Equivalent Address Buffer Architecture



82A303 TTL Equivalent Address Decode Logic

82A303 Pin Description

Pin No.	Symbol	Pin Type	Description
Control			
17	$\overline{\text{MASTER}}$	I	Active low. Bus MASTER is generated by a device that is active on the expansion bus. After $\overline{\text{MASTER}}$ is forced low by an I/O device, the I/O CPU must wait for one system clock period before forcing the address and data lines. $\overline{\text{MASTER}}$ must not be held low for more than 15 microseconds, or else data in the system memory may be lost due to lack of a refresh cycle.
15	HLDA1	I	Hold Acknowledge is an active high from the 82C301 and it is used for address and data direction control during DMA cycles.
20	$\overline{\text{MALE}}$	I	Active low. MEMORY ADDRESS LATCH ENABLE clocks addresses into the address registers on the rising edge.
21	$\overline{\text{REF}}$	I	REFRESH is an active low input. This signal controls the address buffer direction. When REF is active, the contents of the refresh address counter on the 82A304 is gated to the SA address bus.
16	$\overline{\text{ATEN}}$	I	Active low. AT BUS ENABLE is active when the CPU makes an AT bus access.
25	$\overline{\text{LIOCS}}$	O	Active low. LOW IO ADDRESS CHIP SELECT is asserted when A<15:12> = 0H.
24	$\overline{\text{LMEGCS}}$	O	LOW MEG CHIP SELECT is an unlatched active low output asserted when the low Meg memory address space (0 to 1024Kbytes) is accessed or during refresh cycles.
13	$\overline{\text{L64MEG}}$	O	Active low. LOW 64 MB SELECT is active when the access address decodes to the low 64MB address space: A<31:26> = 0H.
14	$\overline{\text{HIROM}}$	O	Active low. HI ROM SELECT is active when A<31:26> = 3FH.
Processor/Bus Interface			
12-2 68-60	A<31:21> A<20:12>	I/O	Local Address Bus.
58-54 51-42	XA<26:22> XA<21:12>	I/O	X Address Bus.
22	$\overline{\text{XAHE}}$	I	Active low XBUS Address High Enable. It enables bits 26:24 from the XA bus. A pullup is provided so that the input can be left open if only 24 bits are sourced externally.

82A303 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
41-36 34-26	SA<26:21> SA<20:12>	I/O I/O	System Address Bus. These outputs have 24mA drive.
23	$\overline{\text{SAHE}}$	I	Active low SBUS Address High Enable. It enables bits 26:24 from the SA bus. A pullup is provided so that the input can be left open if only 24 bits are sourced externally.
59	MA12	O	Memory Address Bus Latched on the trailing edge of $\overline{\text{MALE}}$.
Miscellaneous			
18,52	VCC		Power
1,19 35,53	VSS		Ground

82A303 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82A303 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82A303 DC Characterisitcs

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=10mA (Note 1)	V_{OL1}		0.5	V
Output Low Voltage I_{OL}=24mA (Note 2)	V_{OL2}		0.5	V
Output High Voltage I_{OH}-3.3mA (Note 3)	V_{OH}	2.4		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}		200	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

NOTES
1. All bus outputs other than SA<20:12> and XA<26:21>.
2. All SA<20:12> and XA<26:21> have I_{OL} = 24mA.
3. All outputs and bidirectional pins.

82C303 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	-0.5	6.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C303 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C303 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=3.2mA (Note 1)	V_{OL1}	V_{SS}	0.4	V
Output Low Voltage I_{OL}=12mA (Note 2)	V_{OL2}	V_{SS}	0.4	V
Output High Voltage I_{OH}=-0.2mA	V_{OH1}	4.2	V_{CC}	V
Output High Voltage I_{OH}=-0.4mA	V_{OH2}	4.2	V_{CC}	V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}		100	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

NOTES
1. All bus outputs other than SA<20:12> and XA<26:21>.
2. All SA<20:12> and XA<26:21> have I_{OL} = 12mA.
3. All outputs and bidirectional pins.

82A303 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82A303 82C303 Min	Typ	Max	Unit	Notes
t301	A to MA input set-up time to $\overline{MALE}$↑	5			ns	
t302	A to MA input hold time from $\overline{MALE}$↑	10			ns	
t303	MA output valid delay from $\overline{MALE}$↓	5		27	ns	
t304	A to SA, XA input set-up time to $\overline{MALE}$↑	5			ns	
t305	A to SA,XA input hold time from $\overline{MALE}$↑	5			ns	
t306	SA output valid delay from $\overline{ATEN}$ active	8		28	ns	
t307	SA tri-state delay from $\overline{ATEN}$ inactive	6		25	ns	
t308	XA output valid delay from $\overline{ATEN}$ active	11		35	ns	
t309	XA tri-state delay from $\overline{ATEN}$ inactive	9		35	ns	
t310	$\overline{HIROM}$ decode active from A<32:26> valid	4		15	ns	
t311	$\overline{HIROM}$ decode inactive from A<32:26> invalid	2		16	ns	
t312	$\overline{L64MEG}$ decode active from A<32:26> valid	4		19	ns	
t313	$\overline{L64MEG}$ decode inactive from A<32:26> invalid	2		15	ns	
t314	$\overline{LIOCS}$ decode active from $\overline{MALE}$ active	6		26	ns	
t315	$\overline{LIOCS}$ decode inactive from $\overline{MALE}$ active	4		23	ns	
t316	$\overline{LMEGCS}$ decode active from $\overline{MALE}$ active	6		26	ns	
t317	$\overline{LMEGCS}$ decode inactive from $\overline{MALE}$ active	4		23	ns	
t318	A data valid delay from SA data valid	4		23	ns	
t319	XA data valid delay from SA data valid	7		30	ns	
t320	MA data valid delay from SA data valid	9		40	ns	
t321	$\overline{LIOCS}$ decode active from SA data valid	13		50	ns	
t322	$\overline{LIOCS}$ decode inactive from SA data invalid	10		39	ns	
t323	$\overline{L64MEG}$ decode active from SA data valid	12		47	ns	
t324	$\overline{L64MEG}$ decode inactive from SA data invalid	9		35	ns	
t325	$\overline{LMEGCS}$ decode active from SA data valid	14		53	ns	
t326	$\overline{LMEGCS}$ decode active from SA data invalid	10		40	ns	
t327	A data valid delay from XA data valid	4		27	ns	
t328	SA data valid delay from XA data valid	6		30	ns	

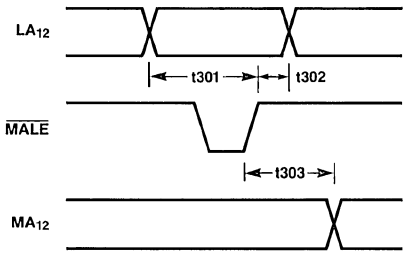
Test Load = 65pF unless otherwise specified.

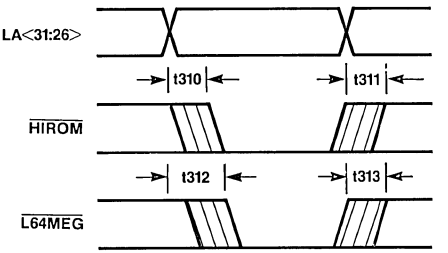
82A303 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

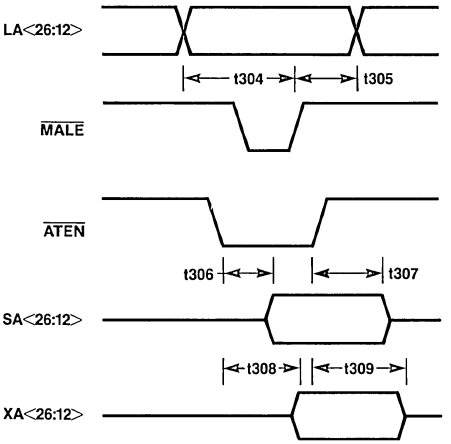
Sym	Description	82A303 82C303 Min	Typ	Max	Unit	Notes
t329	MA data valid delay from XA data valid	9		40	ns	
t330	$\overline{\text{LIOCS}}$ decode active from XA data valid	13		50	ns	
t331	$\overline{\text{LIOCS}}$ decode inactive from XA data valid	9		38	ns	
t332	$\overline{\text{L64MEG}}$ decode active from XA data valid	12		47	ns	
t333	$\overline{\text{L64MEG}}$ decode inactive from XA data valid	9		35	ns	
t334	$\overline{\text{LMEGCS}}$ decode active from XA data valid	14		53	ns	
t335	$\overline{\text{LMEGCS}}$ decode inactive from XA data valid	10		40	ns	
t336	SA valid delay from $\overline{\text{REF}}$ active	18		64	ns	
t337	SA tri-state delay from $\overline{\text{REF}}$ inactive	8		33	ns	

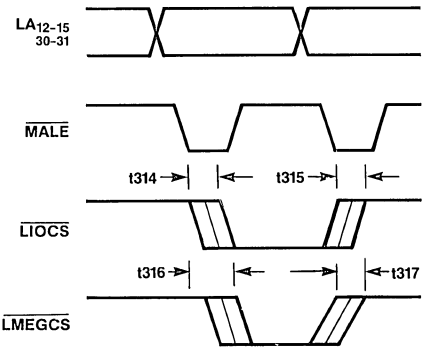
Test Load = 65pF unless otherwise specified.

82A303 TIMING DIAGRAMS

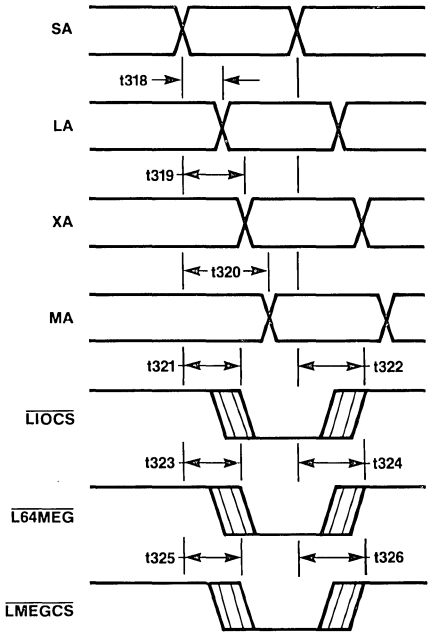


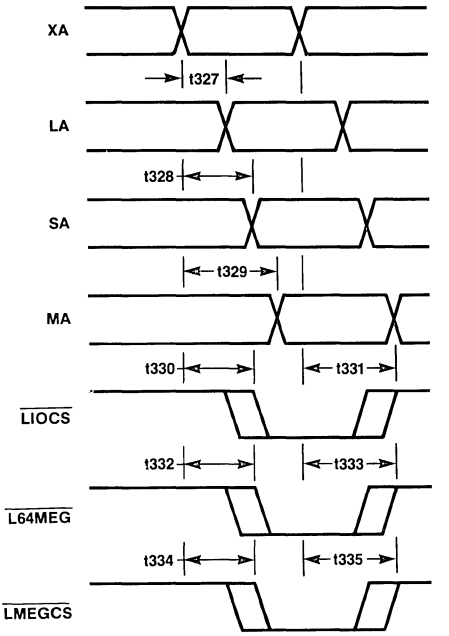


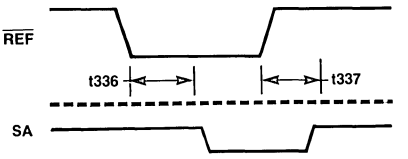




82A303 TIMING DIAGRAMS







82A304/82C304
Low Address Buffers

- Buffer for bits 11:00 of the Local, X and System address buses.
- Peripheral device decode
- Direct interface to AT Bus
- Refresh Address Generation
- Advanced Schottky TTL technology

Functional Description

Address Decode

The signals IO2XCS, 8042CS, PORTBCS, NMICS, 287CS, and AS provides the lower address decodes for the corresponding devices after being qualified by the LIOCS generated by the high address buffer decoder. The resulting decode is as defined by the IBM PC AT IO addresses and is as shown in table 4-1. For applications where these devices are required to be relocated, the EXDEC can be tied LOW to ignore the LIOCS qualification and the MA<11:10> address bits.

Signal	Addresses Decoded
IO2XCS	022H, 023H
8042CS	060H, 064H
PORTBCS	061H
NMICS	070H
287CS	0E0H to 0FFH

Table 4-1. Low Address Decode Definition

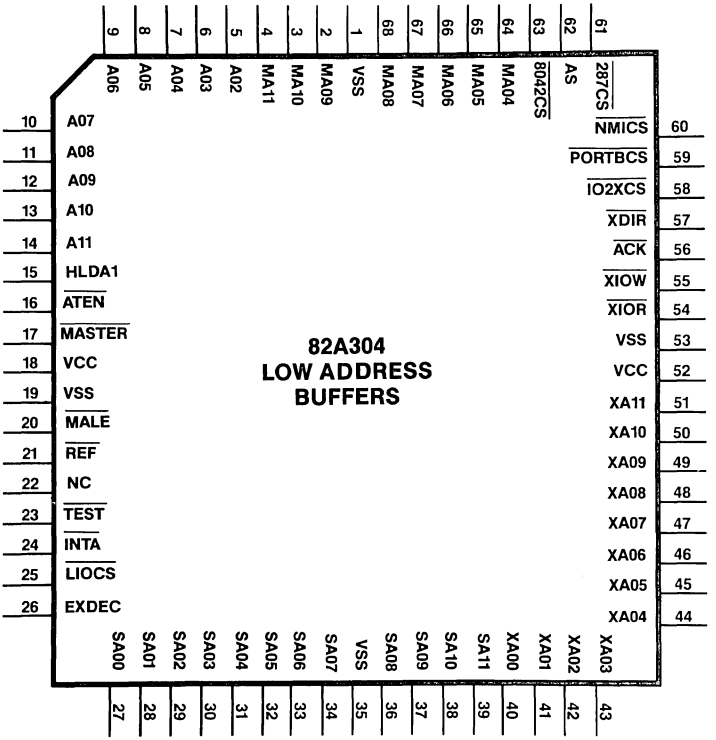
Address Bus Interfaces

The 82A304 interfaces between the bits 00 to 11 of A, SA, XA, and MA address buses. The buffers and multiplexers are controlled by the HLDA1, MASTER, REF, and ATEN to drive the signals from the source to the target buses as defined by table 4-2 for each signal when active. When REF is asserted, the refresh counter is gated to the SA bus as refresh row address and is incremented. When none of the listed signals are active, the default buffer configuration is that the A bus drives the MA bus for memory accesses by CPU.

The SA<11:00> are 24mA address buffers for direct interface to the AT bus.

HLDA1	ATEN	REF	MASTER	Cycle Type	A Bus Source	A Bus Output	S Bus Source	S Bus Output	X Bus Source	X Bus Output
0	1	1	1	CPU, non-AT	—	Disable	—	Disable	—	Disable
0	0	1	1	CPU AT	—	Disable	A Bus	Enable	A Bus	Enable
0	1	0	1	CPU Refresh	—	Disable	REFCTR	Enable	—	Disable
1	1	1	0	Master	S Bus	Enable	—	Disable	S Bus	Enable
1	1	0	0	Master Refresh	X Bus	Enable	X Bus	Enable	—	Disable
1	1	1	1	DMA	X Bus	Enable	X Bus	Enable	—	Disable

Table 4-2. Bus Control Definition


82A304
LOW ADDRESS
BUFFERS
1 VSS
2 MA09
3 MA10
4 MA11
5 A02
6 A03
7 A04
8 A05
9 A06
10 A07
11 A08
12 A09
13 A10
14 A11
15 HLDA1
16 ATEN
17 MASTER
18 VCC
19 VSS
20 MALE
21 REF
22 NC
23 TEST
24 INTA
25 LIOCS
26 EXDEC
27 SA00
28 SA01
29 SA02
30 SA03
31 SA04
32 SA05
33 SA06
34 SA07
35 VSS
36 SA08
37 SA09
38 SA10
39 SA11
40 XA00
41 XA01
42 XA02
43 XA03
44 XA04
45 XA05
46 XA06
47 XA07
48 XA08
49 XA09
50 XA10
51 XA11
52 VCC
53 VSS
54 XIOR
55 XIOW
56 ACK
57 XDIR
58 IO2XCS
59 PORTBCS
60 NMICS
61 287CS
62 AS
63 8042CS
64 MA04
65 MA05
66 MA06
67 MA07
68 MA08

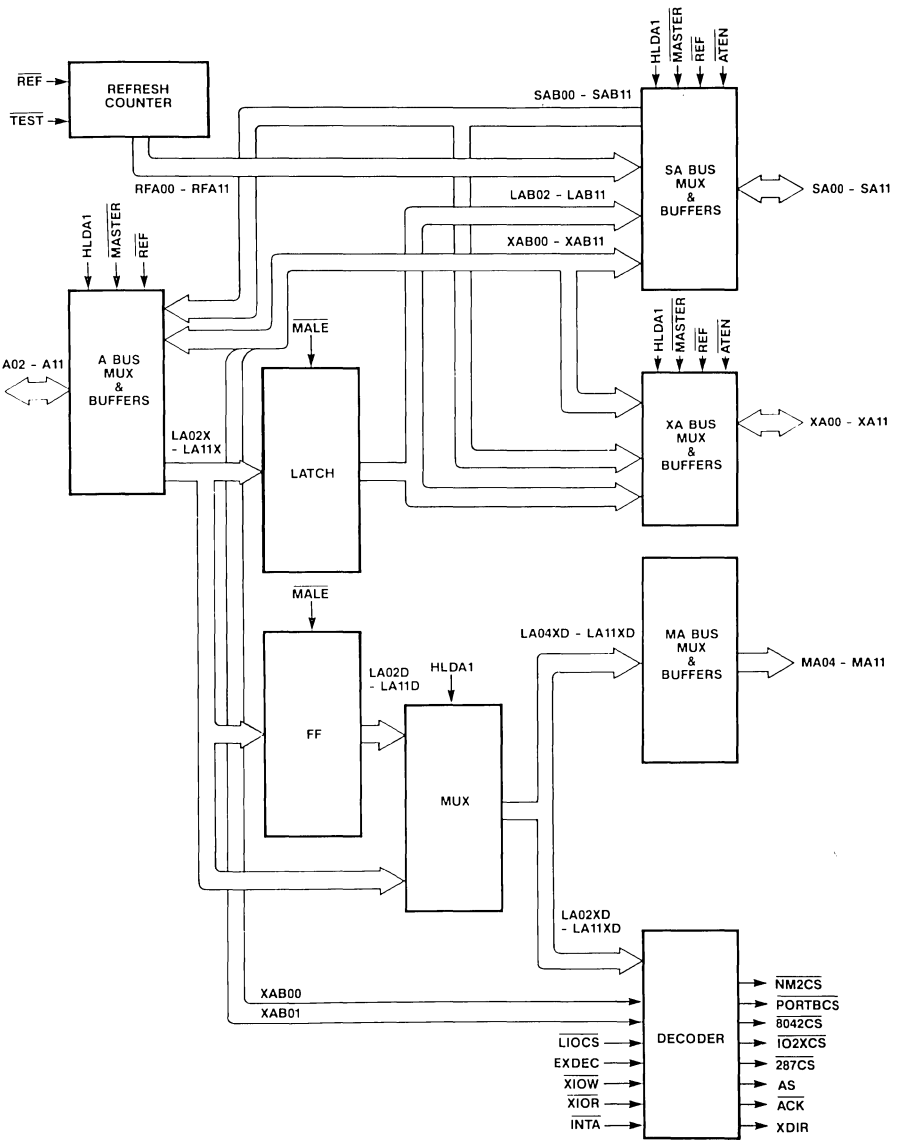
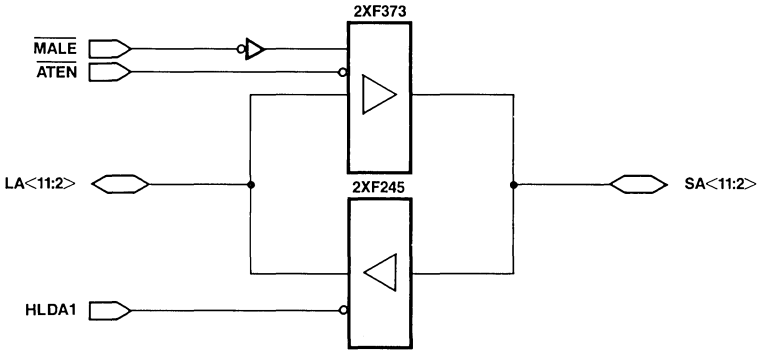
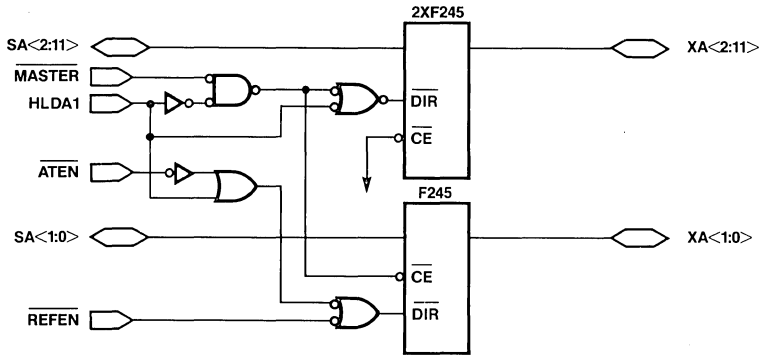


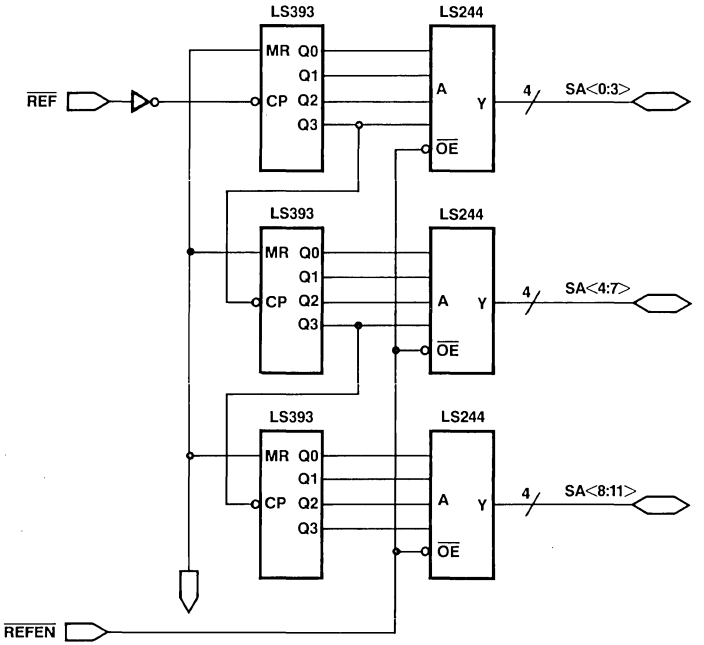
Figure 4-1. 82A304 Functional Block Diagram



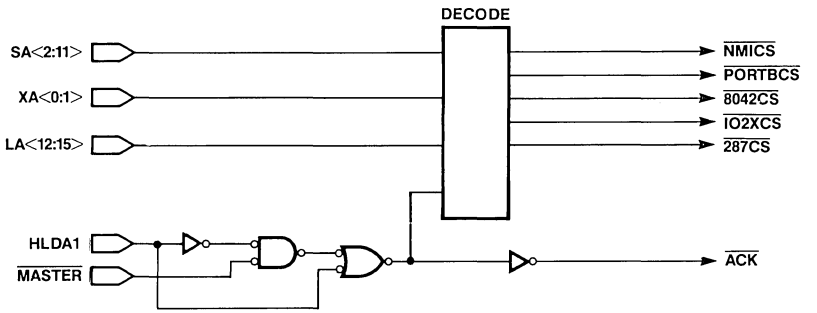
82A304 LA to SA TTL Equivalent Address Buffer Architecture



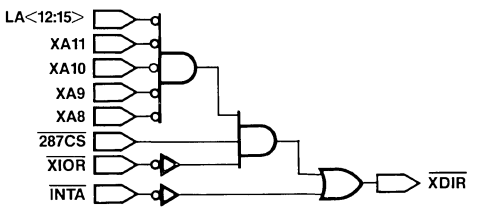
82A304 SA to XA TTL Equivalent Address Buffer Architecture



82A304 AT Bus Refresh Address Generation Circuitry



82A304 TTL Equivalent Chip Select Generation Logic



82A304 TTL Equivalent XDIR Generation Logic

82A304 Pin Description

Pin No.	Symbol	Pin Type	Description
Control			
17	$\overline{\text{MASTER}}$	I	Active low. BUS MASTER is generated by a device active on the expansion bus.
15	HLDA1	I	Hold Acknowledge is an active high input from the 82C301 used for address and data direction control during DMA cycles.
20	$\overline{\text{MALE}}$	I	Active low. MEMORY ADDRESS LATCH ENABLE clocks addresses into the address registers on the rising (trailing) edge.
21	$\overline{\text{REF}}$	I	REFRESH is an active low input. This signal controls the address buffer direction. When REF is active, the contents of the refresh address counter on the 82A304 is gated to the SA address bus.
16	$\overline{\text{ATEN}}$	I	Active low. AT BUS ENABLE is active when the CPU makes an AT bus access.
25	$\overline{\text{LIOCS}}$	I	Active low. LOW IO ADDRESS CHIP SELECT.
54	$\overline{\text{XIOR}}$	I	Active low. X BUS IO Read.
55	$\overline{\text{XIOW}}$	I	Active low. X BUS IO Write
57	$\overline{\text{XDIR}}$	O	X BUS DIRECTION is used to control the drivers between the X bus and S bus. The drivers should be used such that S bus signals are driven toward X bus when $\overline{\text{XDIR}}$ is low and in the other direction when high.
26	EXDEC	I	Active high. EXTENDED IO DECODE. A strapping option that when low ignores A<11:10> and $\overline{\text{LIOCS}}$ (which is decoded based on A<15:12>) for decoding the system board IO ports. An internal pullup is provided.
58	$\overline{\text{IO2XCS}}$	O	Active low. IO 2x SELECT is decode of IO address 022H or 023H.
63	$\overline{\text{8042CS}}$	O	Active low. 8042 SELECT is decode of 8042 address at 060H or 064H.
59	$\overline{\text{PORTBCS}}$	O	Active low. PORTB SELECT is decode of Port B address at 061H
60	$\overline{\text{NMICS}}$	O	Active low. NMI SELECT is decode of NMI address at 070H.
61	$\overline{\text{287CS}}$	O	Active low. 80287 SELECT is decode of 287 address at 0E0-0FFH.
56	$\overline{\text{ACK}}$	O	Active low. ACKNOWLEDGE indicates that AEN1 or AEN2 has been asserted. This signal is used to generate the AEN signal on the AT I/O channel.

82A304 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
62	AS	O	Active high. Address Strobe for the RTC. IO address 7xH is conditioned with $\overline{\text{XIOW}}$.
24	$\overline{\text{INTA}}$	I	Active low. INTERRUPT ACKNOWLEDGE bus cycle indication.
Processor/Bus Interface			
14-5	A<11:02>	I/O	Local address
51-40	XA<11:00>	I/O	X bus address
39-36 34-27	SA<11:08> SA<07:00>	I/O I/O	System address. These outputs have 24mA drive.
4-2 68-64	MA<11:09> MA<08:04>	O O	Memory address
23	$\overline{\text{TEST}}$	I	Active low. TEST when active resets the refresh counter to zero. A pullup is provided.
Miscellaneous			
18,52	VCC		Power
1,19,22 35,53	VSS VSS		Ground

82A304 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82A304 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82A304 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=10mA (Note 1)	V_{OL1}		0.5	V
Output Low Voltage I_{OL}=24mA (Note 2)	V_{OL2}		0.5	V
Output High Voltage I_{OH}-3.3mA (Note 3)	V_{OH}	2.4		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}	140	230	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

NOTES
1. All bus outputs other than SA<20:12>.
2. All SA<20:12> have I_{OL} = 24mA.
3. All outputs and bidirectional pins.

82C304 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	-0.5	6.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C304 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C304 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=3.2mA (Note 1)	V_{OL1}	V_{SS}	0.4	V
Output Low Voltage I_{OL}=12mA (Note 2)	V_{OL2}	V_{SS}	0.4	V
Output High Voltage I_{OH}=-0.2mA (Note 3)	V_{OH1}	4.2	V_{CC}	V
Output High Voltage I_{OH}=-0.4mA	V_{OH2}	4.2	V_{CC}	V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}		100	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

NOTES
1. All bus outputs other than SA<11:00>.
2. All SA<11:00> have I_{OL} = 12mA.
3. All outputs and bidirectional pins.

82A304 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C304 82A304 Min	Typ	Max	Unit	Notes
t401	A to MA input set-up time to $\overline{MALE}$↑	5			ns	
t402	A to MA input hold time from $\overline{MALE}$↑	5			ns	
t403	MA output valid delay from $\overline{MALE}$↑	5		30	ns	
t404	A to SA, XA input set-up time to $\overline{MALE}$↑	5			ns	
t405	A to SA, XA input hold time from $\overline{MALE}$↑	5			ns	
t406	SA output valid delay from $\overline{ATEN}$ active	8		30	ns	
t407	SA tri-state delay from $\overline{ATEN}$ inactive	6		24	ns	
t408	XA output valid delay from $\overline{ATEN}$ active	10		37	ns	
t409	XA tri-state delay from $\overline{ATEN}$ inactive	9		33	ns	
t410	$\overline{NMICS}$ decode active from $\overline{MALE}$↑	11		44	ns	
t411	$\overline{NMICS}$ decode inactive from $\overline{MALE}$↑	10		40	ns	
t412	$\overline{PORTBCS}$ decode active from $\overline{MALE}$↑	11		44	ns	
t413	$\overline{PORTBCS}$ decode inactive from $\overline{MALE}$↑	10		40	ns	
t414	$\overline{8042CS}$ decode active from $\overline{MALE}$↑	11		44	ns	
t415	$\overline{8042CS}$ decode inactive from $\overline{MALE}$↑	10		40	ns	
t416	$\overline{IO2XCS}$ decode active from $\overline{MALE}$↑	11		44	ns	
t417	$\overline{IO2XCS}$ decode inactive from $\overline{MALE}$↑	10		40	ns	
t418	$\overline{287CS}$ decode active from $\overline{MALE}$↑	11		44	ns	
t419	$\overline{287CS}$ decode inactive from $\overline{MALE}$↑	10		40	ns	
t420	A data valid delay from SA data valid	4		26	ns	
t421	XA data valid delay from SA data valid	3		27	ns	
t422	MA data valid delay from SA data valid	9		37	ns	
t423	$\overline{NMICS}$ decode active from SA data valid	14		58	ns	
t424	$\overline{NMICS}$ decode inactive delay from SA data invalid	11		46	ns	
t425	$\overline{PORTBCS}$ decode active from SA data valid	15		59	ns	
t426	$\overline{PORTBCS}$ decode inactive from SA data	11		46	ns	
t427	$\overline{8042CS}$ decode active from SA data valid	15		59	ns	
t428	$\overline{8042CS}$ decode inactive from SA data invalid	11		46	ns	
t429	$\overline{IO2XCS}$ decode active from SA data valid	12		59	ns	

Test Load = 65pF unless otherwise specified.

82A304 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C304 82A304 Min	Typ	Max	Unit	Notes
t430	$\overline{IO2XCS}$ decode inactive from SA data invalid	12		46	ns	
t431	$\overline{287CS}$ decode active from SA data valid	16		59	ns	
t432	$\overline{287CS}$ decode inactive from SA data invalid	13		46	ns	
t433	$\overline{XDIR}$ decode active from SA data valid	15		59	ns	
t434	$\overline{XDIR}$ decode inactive from SA data invalid	15		60	ns	
t435	A data valid delay from XA data valid	4		23	ns	
t436	SA data valid delay from XA data valid	7		30	ns	
t437	MA data valid delay from XA data valid	9		43	ns	
t438	$\overline{NMICS}$ decode active from XA data valid	14		58	ns	
t439	$\overline{NMICS}$ decode inactive from XA data invalid	11		46	ns	
t440	$\overline{PORTBCS}$ decode active from XA data valid	15		59	ns	
t441	$\overline{PORTBCS}$ decode inactive from XA data invalid	11		46	ns	
t442	$\overline{8042CS}$ decode active delay from XA data valid	15		50	ns	
t443	$\overline{8042CS}$ decode inactive delay from XA data invalid	11		46	ns	
t444	$\overline{IO2XCS}$ decode active from XA data valid	12		59	ns	
t445	$\overline{IO2XCS}$ decode inactive from XA data invalid	12		46	ns	
t446	$\overline{287CS}$ decode active from XA data valid	16		59	ns	
t447	$\overline{287CS}$ decode inactive from XA data invalid	13		46	ns	
t448	$\overline{XDIR}$ decode active from XA data valid	15		55	ns	
t449	$\overline{XDIR}$ decode inactive from XA data invalid	15		55	ns	
t450	$\overline{NMICS}$ decode active from $\overline{LIOCS}$ active	7		31	ns	
t451	$\overline{NMICS}$ decode inactive from $\overline{LIOCS}$ inactive	5		24	ns	
t452	$\overline{PORTBCS}$ decode active from $\overline{LIOCS}$ active	7		31	ns	
t453	$\overline{PORTBCS}$ decode inactive from $\overline{LIOCS}$ inactive	5		24	ns	
t454	$\overline{8042CS}$ decode active from $\overline{LIOCS}$ active	7		30	ns	
t455	$\overline{8042CS}$ decode inactive from $\overline{LIOCS}$ inactive	5		24	ns	
t456	$\overline{IO2XCS}$ decode active from $\overline{LIOCS}$ active	7		30	ns	

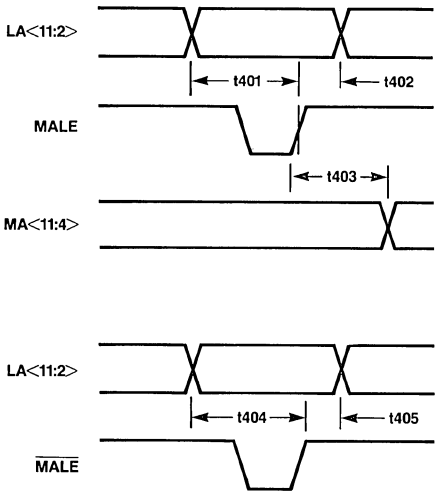
Test Load = 65pF unless otherwise specified.

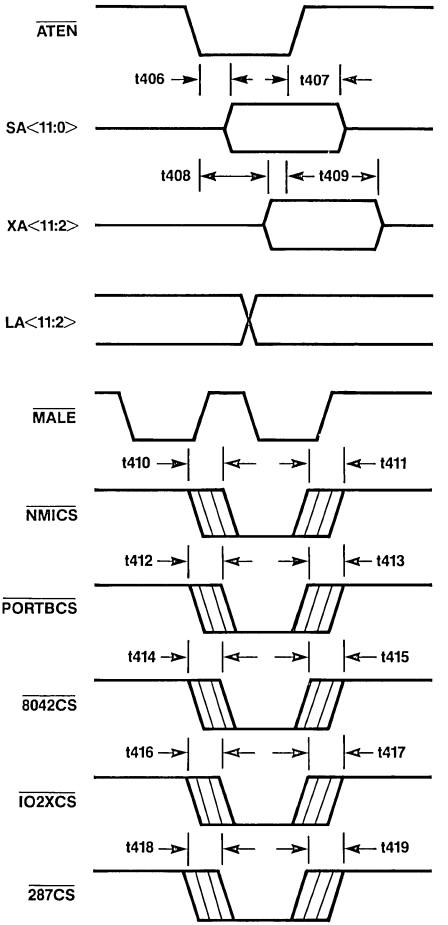
82A304 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	Min	82C304 82A304 Typ	Max	Unit	Notes
t457	$\overline{IO2XCS}$ decode inactive from $\overline{LIOCS}$ inactive	5		24	ns	
t458	$\overline{287CS}$ decode active from $\overline{LIOCS}$ active	7		30	ns	
t459	$\overline{287CS}$ decode inactive from $\overline{LIOCS}$ inactive	5		24	ns	
t460	$\overline{XDIR}$ decode active from $\overline{LIOCS}$ active	8		32	ns	
t461	$\overline{XDIR}$ decode inactive from $\overline{LIOCS}$ inactive	5		26	ns	
t462	$\overline{XDIR}$ decode active from $\overline{INTA}$ active	4		23	ns	
t463	$\overline{XDIR}$ decode inactive from $\overline{INTA}$ inactive	2		17	ns	
t464	$\overline{XDIR}$ decode active from $\overline{XIOR}$ active	6		27	ns	
t465	$\overline{XDIR}$ decode inactive from $\overline{XIOR}$ inactive	4		20	ns	
t466	$\overline{ACK}$ decode active from HLDA1 active	9		37	ns	
t467	$\overline{ACK}$ decode inactive from HLDA1 inactive	7		32	ns	
t468	$\overline{ACK}$ decode active from $\overline{MASTER}$ active	8		33	ns	
t469	$\overline{ACK}$ decode inactive from $\overline{MASTER}$ inactive	6		26	ns	
t470	SA data valid delay from $\overline{REF}$ active	18		64	ns	
t471	SA tri-state delay from $\overline{REF}$	8		33	ns	

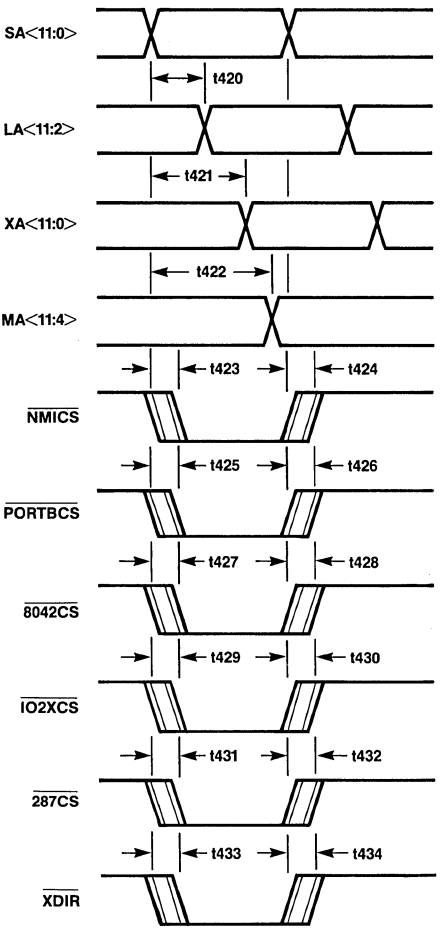
Test Load = 65pF unless otherwise specified.

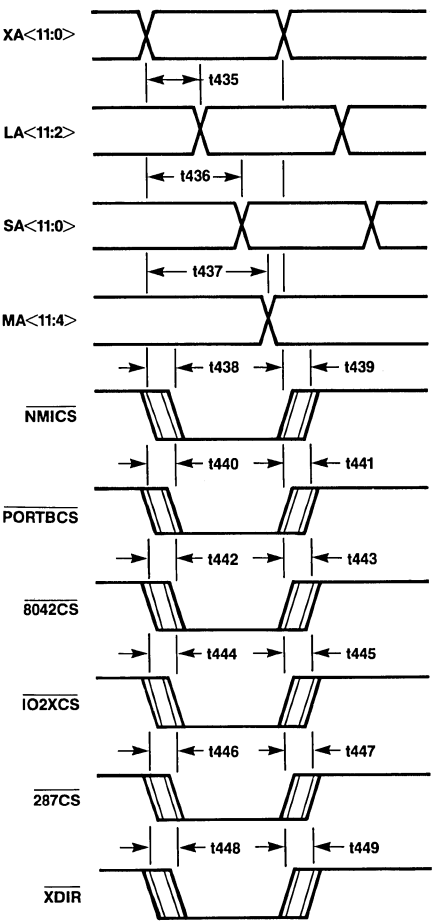
82A304 TIMING DIAGRAMS



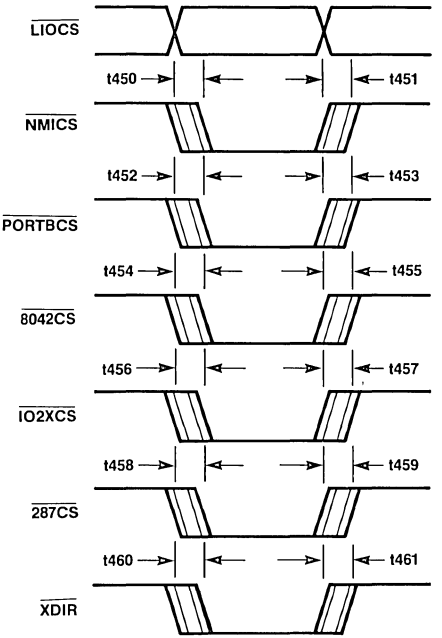


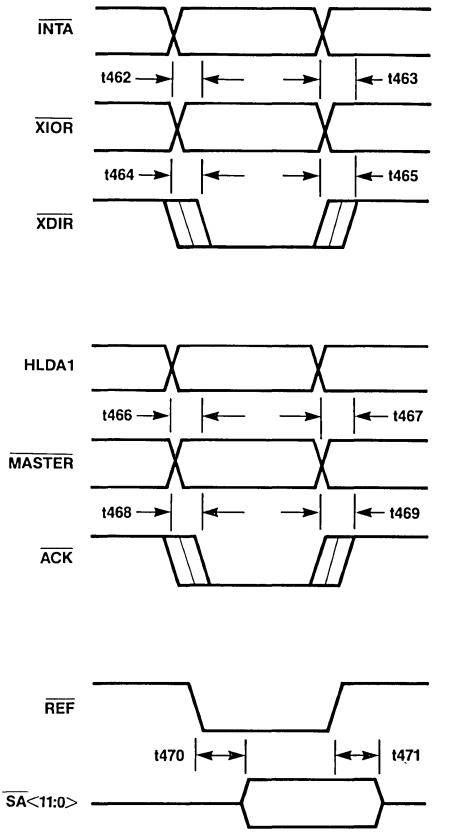
82A304 TIMING DIAGRAMS





82A304 TIMING DIAGRAMS





82A305/82B305/82C305 Data Buffer

- Nibble Slice of Memory and AT Data Bus Interface
- Data Size Conversion
- Advanced Schottky technology

Functional Description

The 82A305 interfaces between the Local, Memory and System (AT IO channel) data busses and provides data alignment and size conversion for AT IO channel operations. It is designed as a nibble slice to reduce pin count and simplify system design. Two parts are used to interface all data buses.

Bus Controls

The 82A305 controls the bus buffers according to the signals HLDA1, $\overline{ATEN}$, $\overline{CS}$, $\overline{LDEN}$, SDIR, $\overline{MRD}$, and AC<3:0>. The first group of signals HLDA1, $\overline{ATEN}$, $\overline{CS}$, and $\overline{LDEN}$ determines which buses are connected, and the second group of signals SDIR, $\overline{MRD}$, and AC<3:0> determines the direction of the buffers drivers. Table 5-1 shows the bus connections for different bus cycles.

All drivers are active for the active buses, and external bus controls are required if selective data bits need to be controlled. For the DRAM interface, the $\overline{LBE}$<3:0> must be used to ensure that only the valid data bytes are written into the DRAM's during a write cycle.

Data Conversion

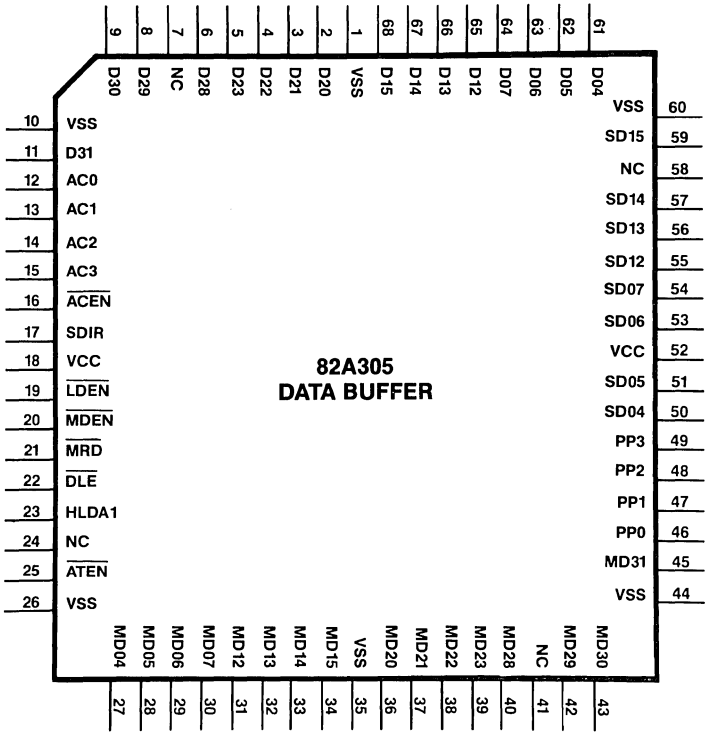
The 82A305 provides the data bus connections so that data conversions are done correctly for CPU accesses to the AT bus. The action codes AC<3:0> are used to control how bus bits are connected between the IO channel SD bus and the CPU local bus D or the system memory MD bus. The action codes are provided by the 82C301 bus controller for CPU to AT bus access cycles and is qualified by the ACEN. The meaning of the action codes are:

AC<3:0>	FROM	TO
0	AB	EF
1	B	EF
2	CD	EF
3	D	EF
4	ABCD	EFGH
5	E	A
6	E	B
7	E	C
8	E	D
9	EF	AB
A	EF	CD
B	—	—
C	EFGH	ABCD
D	—	—
E	—	—
F	—	—

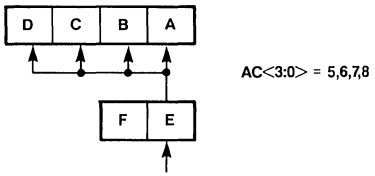
Table 5-2. Action Code Definition

HLDA	ATEN	SDIR	$\overline{MDEN}$	$\overline{MRD}$	$\overline{LDEN}$	Cycle Type	D Bus Source	D Bus Output	S Bus Source	S Bus Output	M Bus Source	M Bus Output
0	1	X	0	0	X	CPU, non-AT Read	M Bus	Enable	—	Disable	—	Disable
0	1	X	0	1	X	CPU non-AT Write	—	Disable	—	Disable	D Bus	Enable
0	0	0	X	X	X	CPU AT Read	S Bus	Enable	—	Disable	—	Disable
0	0	1	X	X	X	CPU AT Write	—	Disable	D Bus	Enable	—	Disable
1	1	1	X	0	X	MASTER/DMA MemRd	—	Disable	M Bus	Enable	—	Disable
1	1	1	X	1	0	MASTER/DMA IocRd	—	Disable	D Bus	Enable	—	Disable
1	1	0	X	1	X	MASTER/DMA IocWR	S Bus	Enable	—	Disable	S Bus	Enable

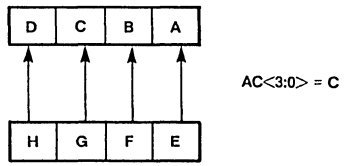
Table 5-1. Bus Control Definitions


82A305
DATA BUFFER
1 VSS
2 D31
3 AC0
4 AC1
5 AC2
6 AC3
7 ACEN
8 SDIR
9 VCC
10 LDEN
11 MDEN
12 MRD
13 DLE
14 HLDA1
15 NC
16 ATEN
17 VSS
18 MD04
19 MD05
20 MD06
21 MD07
22 MD12
23 MD13
24 MD14
25 MD15
26 VSS
27 MD20
28 MD21
29 MD22
30 MD23
31 MD28
32 NC
33 MD29
34 MD30
35 VSS
36 MD31
37 PP0
38 PP1
39 PP2
40 PP3
41 SD04
42 SD05
43 VCC
44 SD06
45 SD07
46 SD12
47 SD13
48 SD14
49 NC
50 SD15
51 VSS
52 D04
53 D05
54 D06
55 D07
56 D12
57 D13
58 D14
59 D15
60 VSS
61 D20
62 D21
63 D22
64 D23
65 D28
66 NC
67 D29
68 D30

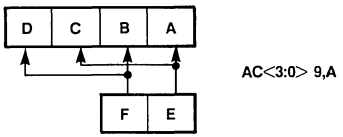
CPU Read from 8-Bit Devices



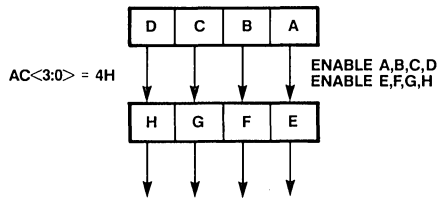
CPU Read from 32-Bit Device



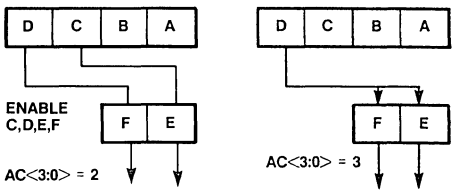
CPU Read from 16-Bit Devices

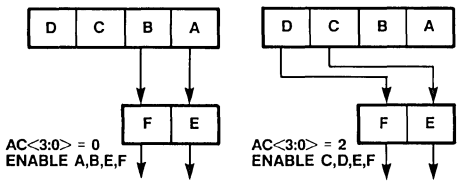


Write to 32-Bit Device

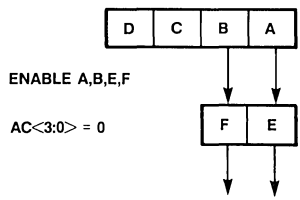


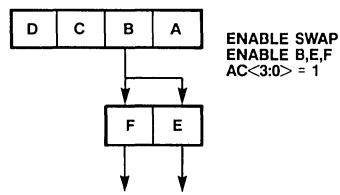
Write to 8-Bit Device





Write to 16-Bit Device





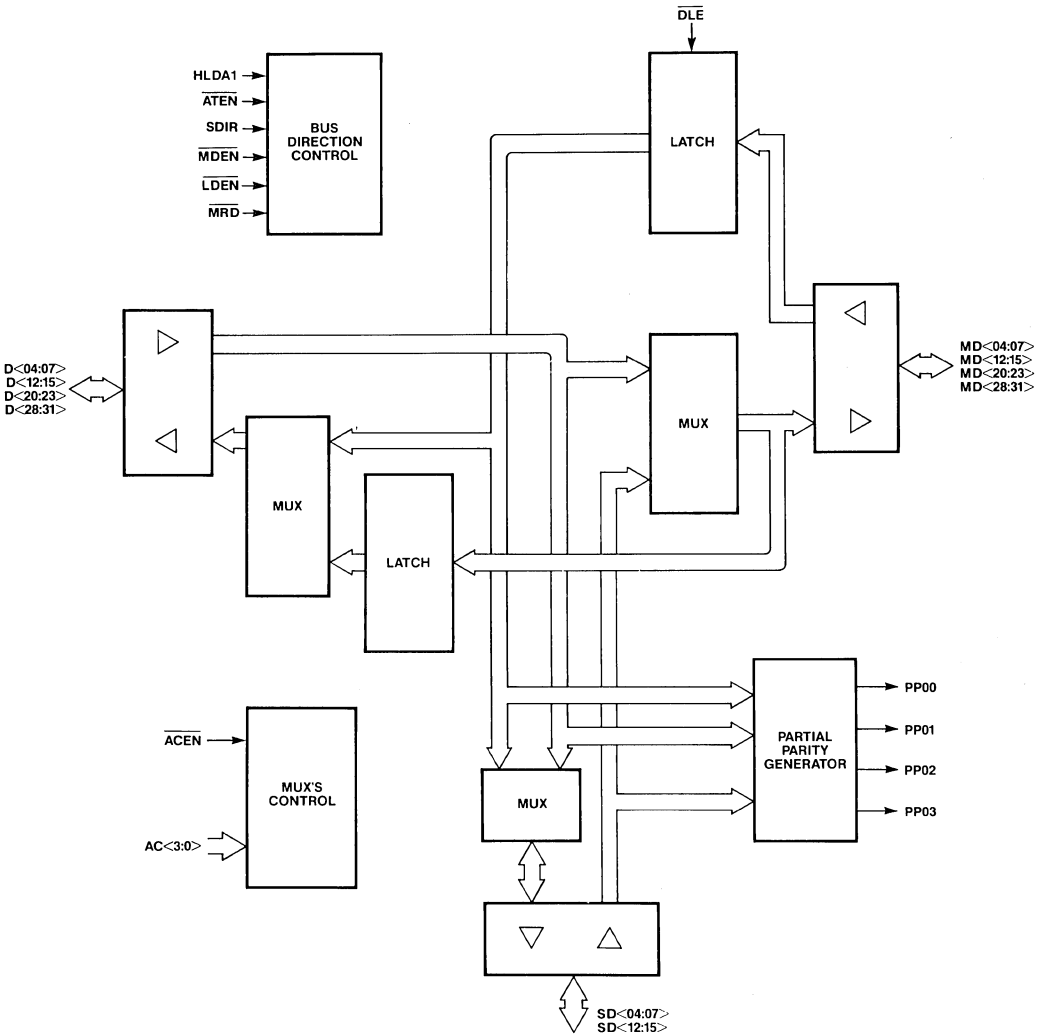
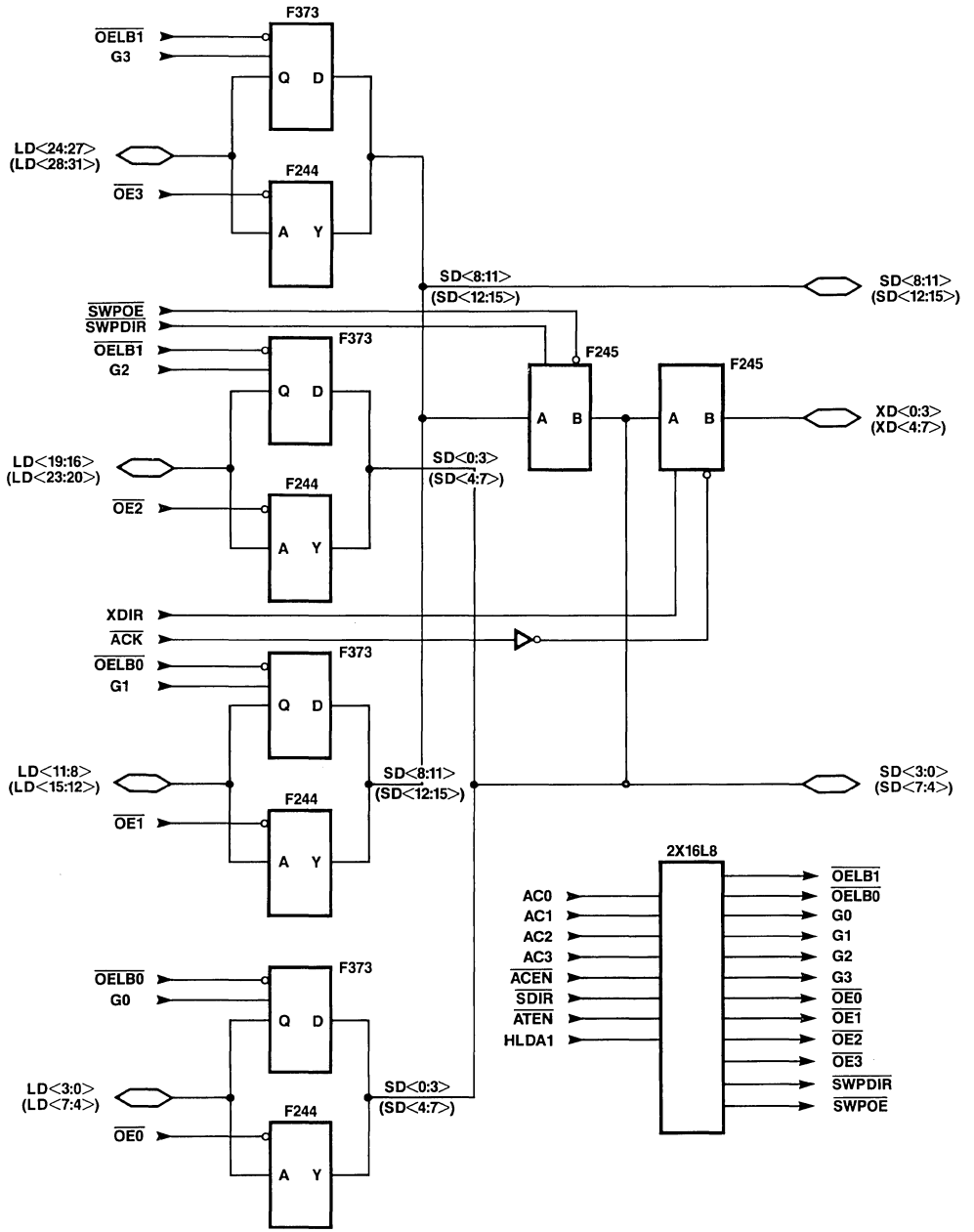
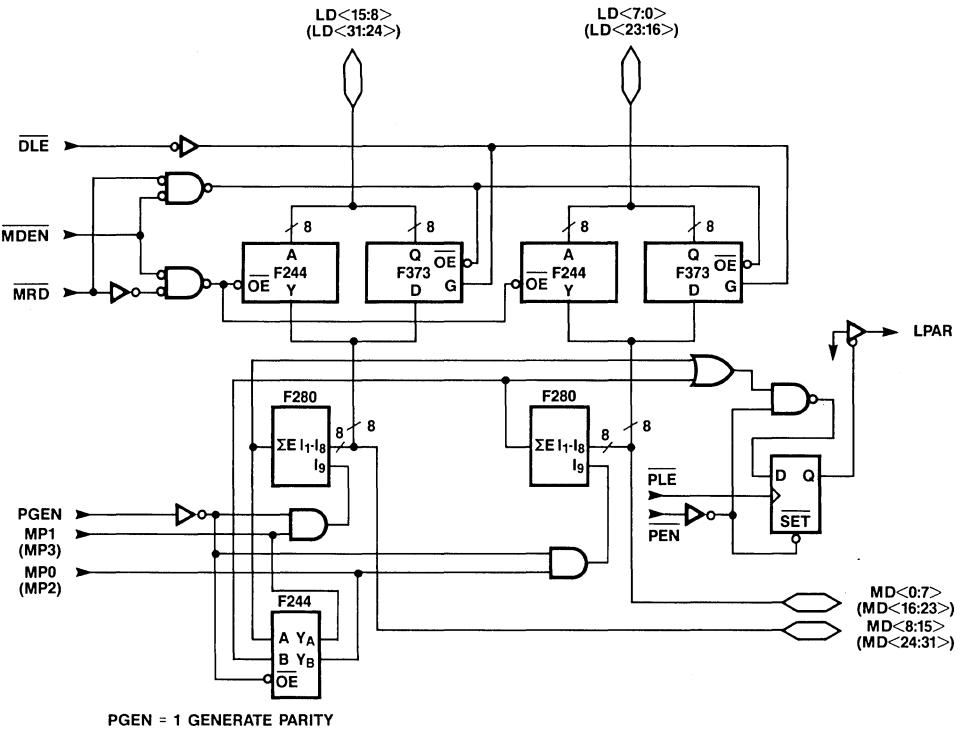


Figure 5-1. 82A305 Functional Block Diagram



82A305 TTL Equivalent Data Buffer Architecture



82A305 TTL Equivalent Data Buffer Architecture

82A305 Pin Description

Pin No.	Symbol	Pin Type	Description
Control			
15-12	AC<3:0>	I	ACTION CODES input from the 82C301 are used for data bus sizing and byte assembly operations.
16	$\overline{\text{ACEN}}$	I	Active low. Action Code Enable when active validates the action codes.
17	SDIR	I	System bus DIRection. A low enables data transfers from the System to Local bus and in the other direction when high.
25	$\overline{\text{ATEN}}$	I	Active low. AT Bus Enable.
23	HLDA1	I	Active high. HoLD Acknowledge.
20	$\overline{\text{MDEN}}$	I	Active low. MEMORY DATA BUFFER ENABLE. When low enables the memory data buffers for transfer between the processor and memory subsystem. When high disables these bus buffers. Should be connected to $\overline{\text{MDEN}}$ on the 82C302.
19	$\overline{\text{LDEN}}$	I	Active low. Selects LD as a source for the SD bus during MASTER or DMA reads. When HI selects MD. Asserting $\overline{\text{MRD}}$ overrides $\overline{\text{LDEN}}$ and gates MD to the SD bus. A pullup is provided.
21	$\overline{\text{MRD}}$	I	Active low. Memory Bus DIRection. When low enables data movement for a processor read from the memory to local bus. $\overline{\text{MRD}}$ when Hi enables drivers from local to memory bus.
22	$\overline{\text{DLE}}$	I	DATA LATCH ENABLE is an active low signal used to latch the data in the 82A305 data buffers. This is normally connected to the CAS output (pin 71) of the 82C302.
11, 9	D<31:30>	I/O	
8, 6	D<29:28>	I/O	
5-2	D<23:20>	I/O	Local Data Bus
68-65	D<15:12>	I/O	
64-61	D<07:04>	I/O	
45,43	MD<31:30>	I/O	
42,40	MD<29:28>	I/O	
39-36	MD<23:20>	I/O	Memory Data Bus
34-31	MD<15:12>	I/O	
30-27	MD<07:04>	I/O	
49-46	PP<03:00>	O	Memory Partial Parity

82A305 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
59,57	SD<15:14>	I/O	IO Channel Data Bus
56,55	SD<13:12>	I/O	
54-53	SD<07:06>	I/O	
51-50	SD<05:04>	I/O	
7,24	NC		Reserved.
41,58	NC		
Power Supplies			
18,52	VCC		Power
1,10	VSS		Ground
26,35	VSS		
44,60	VSS		

82A305 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82A305 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82A305 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=10mA	V_{OL}		0.5	V
Output High Voltage I_{OH}= .3.3mA	V_{OH}	2.4		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	A305 B305	140	230 100	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

82C305 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	-0.5	6.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C305 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C305 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=3.2mA	V_{OL1}	V_{SS}	0.4	V
Output Low Voltage I_{OL}=12mA	V_{OL2}	V_{SS}	0.4	V
Output High Voltage I_{OH}=-0.2mA (Note 2)	V_{OH1}	4.2		V
Output High Voltage I_{OH}=-0.4mA	V_{OH2}	4.2		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}		60	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

NOTES
1. All bus outputs and PP<3:0> have I_{OL} = 3.2mA.
2. All outputs and bidirectional pins.

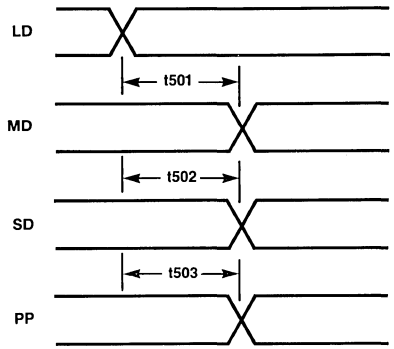
82A305 AC Characteristics

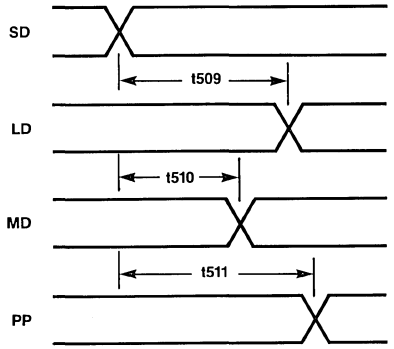
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

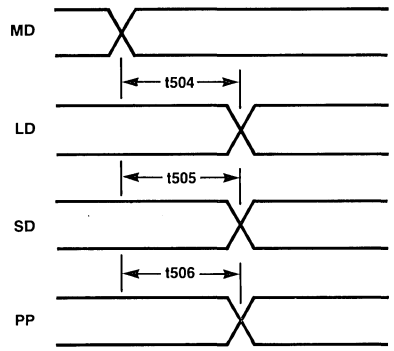
Sym	Description	82A305-16 82C305-16 Min	Typ	Max	82B305-20 Min	Typ	Max	Unit	Notes
t501	MD data valid from LD data valid	4		15	4		13	ns	C_L=35pF
t502	SD data valid delay from LD data valid	4		27	4		23	ns	
t503	PP data valid delay from LD data valid	5		29	5		25	ns	
t504	LD data valid delay from MD data valid	4	17	15	4	13	13	ns	C_L=35pF
t505	SD data valid delay from MD data valid	4		28	4		25	ns	
t506	PP data valid delay from MD data valid	5		30	5		25	ns	
t507	MD data set-up time to $\overline{DLE}$	4			1			ns	
t508	MD data hold time from $\overline{DLE}$	5			5			ns	
t509	LD data valid delay from SD data valid	8		38	8		36	ns	
t510	MD data valid delay from SD data valid	4		27	4		25	ns	
t511	PP data valid delay from SD data valid	5		33	5		30	ns	
t512	SD data set-up time to $\overline{ACEN}$	10			10			ns	
t513	SD data hold time from $\overline{ACEN}$	0		5	0		5	ns	
t514	MD data valid delay from $\overline{MDEN}$	7		29	7		25	ns	
t515	MD tri-state delay from $\overline{MDEN}$	7		15	7		15	ns	
t516	LD data valid delay from $\overline{MDEN}$	7		30	7		30	ns	
t517	LD tri-state delay from $\overline{MDEN}$	5		23	5		23	ns	

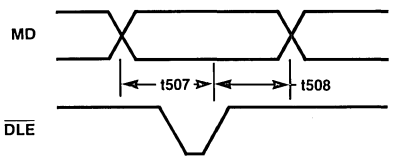
Test Load = 65pF unless otherwise specified.

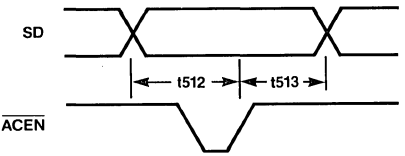
82A305 TIMING DIAGRAMS

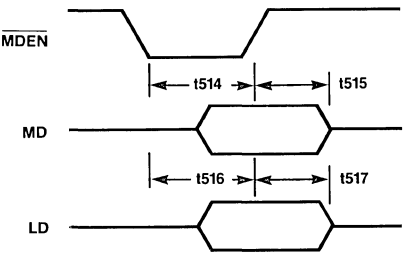












82A306/82C306 Control Buffer

- 14.318MHz oscillator and divide by 12 counter
- Byte enable latch
- Parity Checking
- Direct interface to AT Bus
- Advanced Schottky TTL technology

Functional Description

14MHz Oscillator and Divider

The color reference oscillator is provided eliminating the 8224 normally used in AT compatible systems. A divide by 12 counter is also included to generate the OSC/12 (1.19MHz) signal used on the system board.

$\overline{\text{AF32}}$ Generation

The $\overline{\text{AF32}}$ is used in the CS 8230 system to indicate that the current bus cycle is a CPU local bus cycle.

Byte Enable Latch

The register that holds the byte enables valid during a memory cycle is located on the 82A306. A LBOP input is provided to indicate the edge that is used to latch the $\overline{\text{BE}}$<3:0>. If LBOP = 0, then $\overline{\text{MALE}}$↑ is used to latch the $\overline{\text{BE}}$<3:0>. If LBOP = 1, then SCLK↓ is used to latch the $\overline{\text{BE}}$<3:0>. An additional input $\overline{\text{FBE}}$ is provided to force all byte enables active during certain memory operations. A pullup resistor is provided on the $\overline{\text{FBE}}$ input for implementations not requiring this feature.

Parity Checking and Generation

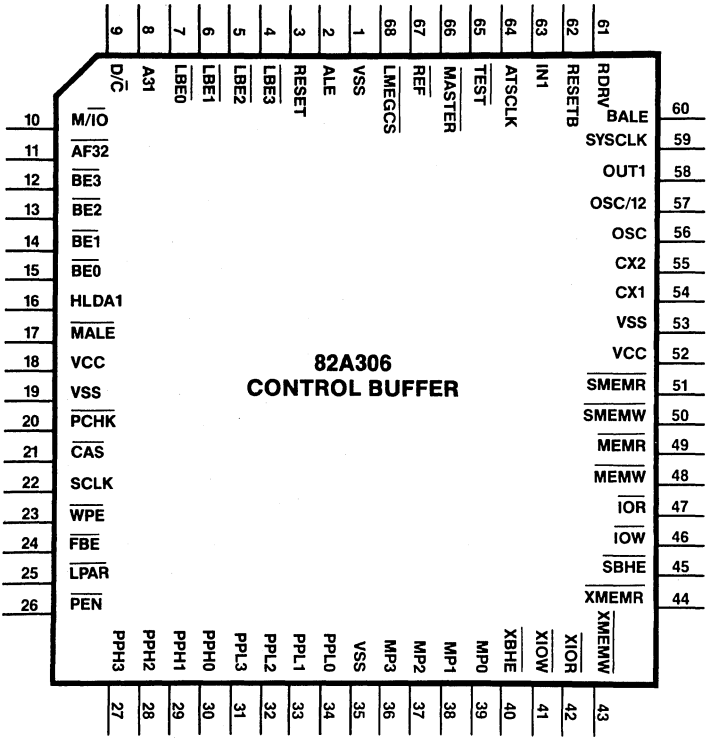
The 82A306 provides the necessary exclusive OR'ing to generate full (byte) write and read parity from the partial parity bits PPH<3:0> and PPL<3:0> generated on the two (nibble wide) data buffers 82A305.

For a memory read access, read parity PPH<3:0> and PPL<3:0> are checked against the parity bits MP<3:0> read from memory. These parity bits are latched by $\overline{\text{CAS}}$ and $\overline{\text{PCHK}}$ so that they are kept valid during parity checking. The results of the byte-wise comparison are further gated by byte enables to ignore errors for bytes which are not valid. The OR'ed byte-wise parity error is then latched as the output $\overline{\text{LPAR}}$ if $\overline{\text{PEN}}$ input is asserted.

During a memory write access, write parity for each byte is generated from PPH<3:0> and PPL<3:0> and can be gated onto the memory parity bus MP<3:0> if enabled by $\overline{\text{WPE}}$ controlling the tri-state drivers. If an external parity generation circuit is used, an internal pullup resistor is provided for $\overline{\text{WPE}}$ to disable the write parity output buffers if left unconnected.

Bus Drivers

24mA drivers are provided for some of the control signals on the IO channel. These include SYSCLK, OSC, OSC/12, RDRV, $\overline{\text{SBHE}}$, BALE, $\overline{\text{IOR}}$, $\overline{\text{IOW}}$, $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{SMEMR}}$, and $\overline{\text{SMEMW}}$.


82A306
CONTROL BUFFER
1 VSS
2 ALE
3 RESET
4 LBE3
5 LBE2
6 LBE1
7 LBE0
8 A31
9 D/C
10 M/IO
11 AF32
12 BE3
13 BE2
14 BE1
15 BE0
16 HLDA1
17 MALE
18 VCC
19 VSS
20 PCHK
21 CAS
22 SCLK
23 WPE
24 FBE
25 LPAR
26 PEN
27 PPH3
28 PPH2
29 PPH1
30 PPH0
31 PPL3
32 PPL2
33 PPL1
34 PPL0
35 VSS
36 MP3
37 MP2
38 MP1
39 MP0
40 XBHE
41 XIOW
42 XIOR
43 XMEMW
44 XMEMR
45 SBHE
46 IOW
47 IOR
48 MEMW
49 MEMR
50 SMEMW
51 SMEMR
52 VCC
53 VSS
54 CX1
55 CX2
56 OSC
57 OSC/12
58 OUT1
59 SYSCLK
60 BALE
61 RDRV
62 RESETB
63 IN1
64 ATSCLK
65 TEST
66 MASTER
67 REF
68 LMEGCS

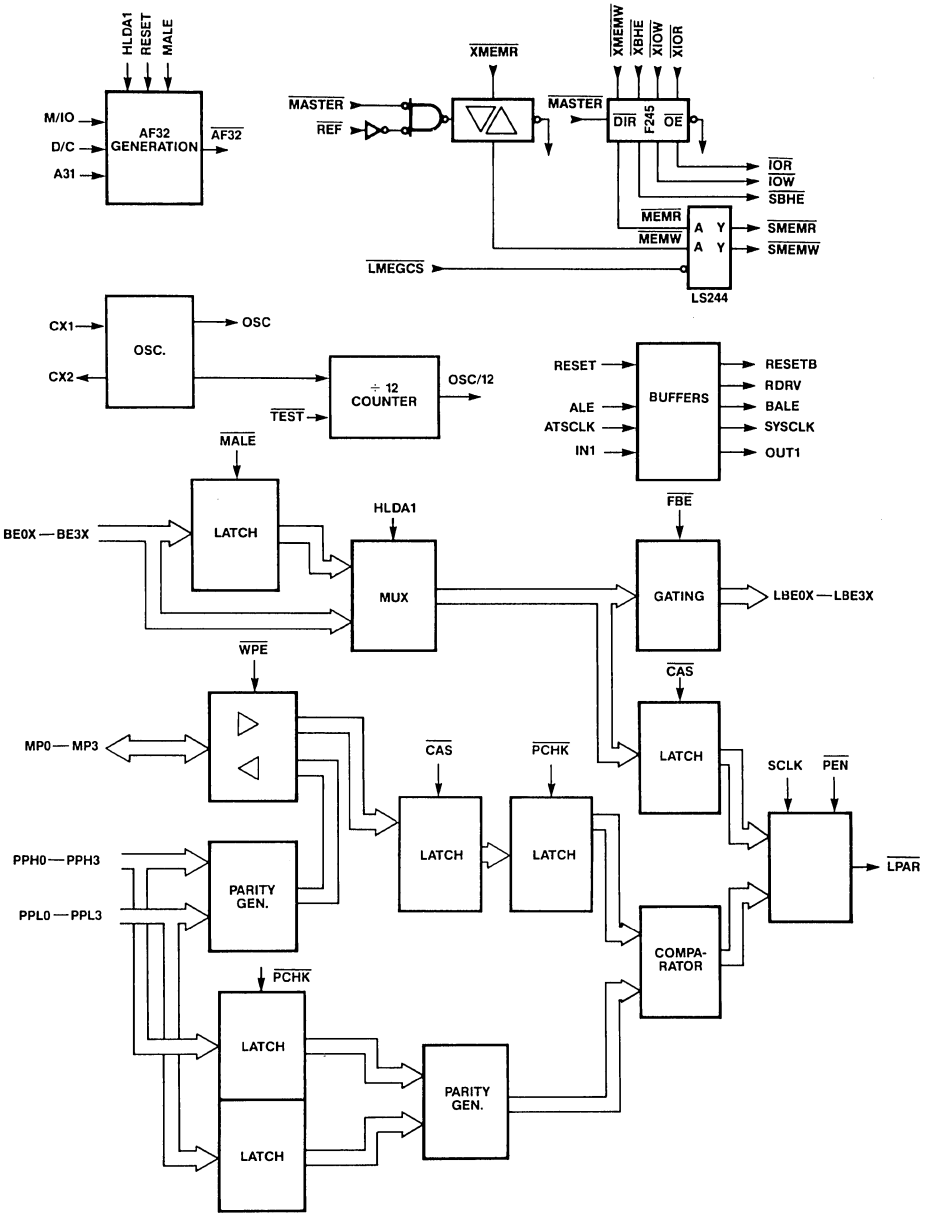


Figure 6-1. 82A306 Functional Block Diagram

82A306 Pin Description

Pin No.	Symbol	Pin Type	Description
64	ATSCLK	I	AT IO channel SYSCLK input.
59	SYSCLK	O	Buffered 24mA SYSCLK to AT IO channel. Nominally one half of the bus state machine clock frequency.
Control			
54	CX1	I	14.318MHz oscillator input from crystal.
55	CX2	O	14.318MHz oscillator output to crystal.
56	OSC	O	System 14.318MHz output. This output has 24mA drive capability.
57	OSC/12	O	14.318MHz/12 = 1.19MHz output. This output has 24mA drive capability.
17	$\overline{\text{MALE}}$	I	Active low. Address Latch Enable for on board access.
12-15	$\overline{\text{BE<3:0>}}$	I	Active low. BYTE ENABLES.
4-7	$\overline{\text{LBE<3:0>}}$	O	Active low. LATCHED BYTE ENABLE on the trailing edge of $\overline{\text{MALE}}$.
24	$\overline{\text{FBE}}$	I	Active low. FORCE BYTE ENABLE Forces all byte enables LBE active independent of $\overline{\text{MALE}}$ and the $\overline{\text{BE<3:0>}}$ inputs.
67	$\overline{\text{REF}}$	I	Active low. REFRESH.
8	A<31>	I	Local Address Bus bit 31.
10	M/$\overline{\text{IO}}$	I	80386 Status used to generate $\overline{\text{AF32}}$ for the 80387 and other 32 bit IO devices.
9	D/$\overline{\text{C}}$	I	80386 Status used to generate $\overline{\text{AF32}}$ for the 80387 and other 32 bit IO devices.
68	$\overline{\text{LMEGCS}}$	I	LOW MEG CHIP SELECT is an unlatched active low output asserted when the low Meg memory address space (0 to 1024Kbytes) is accessed or during refresh cycles.
11	$\overline{\text{AF32}}$	T	Active low. Tri-state output $\overline{\text{AF32}}$ when active indicates a 32 bit local bus memory or an I/O access cycle on the system board. It is generated from M/$\overline{\text{IO}}$, D/$\overline{\text{C}}$, <31>, and HLDA1.

82A306 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
66	$\overline{\text{MASTER}}$	I	Active low. Bus MASTER input from the AT IO channel.
3	RESET	I	Active high. RESET input. Should be connected to RESET4 of 82C301.
62	RESETB	O	Active high. Buffered RESET to X bus.
61	RDRV	O	Active high. RESET to AT bus. 24mA drive capability.
2	ALE	I	Active high. ALE for AT bus.
40	$\overline{\text{XBHE}}$	I/O	Active low. X Bus BHE.
44	$\overline{\text{XMEMR}}$	I/O	Active low. X Bus Memory Read.
43	$\overline{\text{XMEMW}}$	I/O	Active low. X Bus Memory Write.
42	$\overline{\text{XIOR}}$	I/O	Active low. X Bus IO Read.
41	$\overline{\text{XIOW}}$	I/O	Active low. X Bus IO Write.
60	BALE	O	Active high. Buffered ALE to AT bus. 24mA drive capability.
45	$\overline{\text{SBHE}}$	I/O	Active low. System bus BHE. 24mA drive capability.
51	$\overline{\text{SMEMR}}$	O	Active low. System bus MEMory Read. 24mA drive capability.
50	$\overline{\text{SMEMW}}$	O	Active low. System bus MEMory Write. 24mA drive capability.
49	$\overline{\text{MEMR}}$	I/O	Active low. Memory Read. 24mA drive capability.
48	$\overline{\text{MEMW}}$	I/O	Active low. Memory Write. 24mA drive capability.
47	$\overline{\text{IOR}}$	I/O	Active low. IO Read. 24mA drive capability.
46	$\overline{\text{IOW}}$	I/O	Active low. IO Write. 24mA drive capability.
16	HLDA1	I	Active high. HOLD ACKNOWLEDGE from 82C301.
22	SCLK	I	CLK2/2 clock input. Should be connected to SCLK output of 82C302 or 82C307.
27-30	PPH<3:0>	I	PARTIAL PARITY HIGH computed by 82A305 for the high nibble data bits.
31-34	PPL<3:0>	I	PARTIAL PARITY lowW computed by 82A305 for the low nibble data bits.
36-39	MP<3:0>	I/O	Data Parity bits for the DRAMs.
21	$\overline{\text{CAS}}$	I	Active low. Read Parity latch enable.
20	$\overline{\text{PCHK}}$	I	Active low. PARITY CHECK STROBE for generating LPAR from the partial parity and data parity bits.
26	$\overline{\text{PEN}}$	I	Active low. Overall PARITY CHECK ENABLE.

82A306 Pin Description (Continued)

Pin No.	Symbol	Pin Type	Description
23	$\overline{\text{WPE}}$	I	Active low. WRITE PARITY ENABLE. Enables the sourcing of write parity onto the MP bus. A pullup is provided.
25	$\overline{\text{LPAR}}$	O	Active low. LATCHED PARITY ERROR signal.
65	$\overline{\text{TEST}}$	I	Active low. Enables testing of the OSC/12 counter. A pullup is provided.
63	LBOP	I	Latch Byte enable option. A pull up is provided.
58	NC		
Power Supply			
18,52	VCC		Power
1,19 35,53	VSS VSS		Ground

82A306 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82A306 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82A306 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=10mA (Note 1)	V_{OL1}		0.5	V
Output Low Voltage I_{OL}=24mA (Note 2)	V_{OL2}		0.5	V
Output High Voltage I_{OH}-3.3mA (Note 3)	V_{OH}	2.4		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}	140	230	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

NOTES
1. $\overline{MP<3:0>}$, $\overline{XIOW}$, $\overline{XIOR}$, $\overline{XBHE}$, $\overline{XMEMW}$, $\overline{XMEMR}$, $\overline{RESTEB}$, $\overline{LBE<3:0>}$ all have I_{OL} = 10mA.
2. $\overline{SBHE}$, $\overline{IOW}$, $\overline{IOR}$, $\overline{MEMW}$, $\overline{MEMR}$, $\overline{SMEMW}$, $\overline{SMEMR}$, OSC, OSC/12, OUT1, SYSCLK, BALE, RDRV all have I_{OL} = 24mA.
3. All outputs and bidirectional pins.

82C306 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	-0.5	6.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C306 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C306 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=3.2mA (Note 1)	V_{OL1}	V_{SS}	0.4	V
Output Low Voltage I_{OL}=12mA (Note 2)	V_{OL2}	V_{SS}	0.4	V
Output High Voltage I_{OH}=-0.2mA (Note 3)	V_{OH1}	4.2		V
Output High Voltage I_{OH}=-0.4mA	V_{OH2}	4.2		V
Input Low Current V_I = 0.5V, V_{CC} = 5.25V	I_{IL}		-200	μA
Input High Current V_I = 2.4V, V_{CC} = 5.25V	I_{IH}		20	μA
Input High Current V_I = 5.5V, V_{CC} = 5.25V	I_I		200	μA
Output Short Circuit Current V_O=0V	I_{OS}	-15	-100	mA
Input Clamp Voltage I_I = -18mA, V_{CC} = 4.75V	V_{IC}		-1.5	V
Power Supply Current	I_{CC}		60	mA
Output HI-Z Leak Current 3-State Output Pins	I_{OZ1}	-100	100	μA
Output HI-Z Leak Current Bidirectional Pins	I_{OZ2}	-300	120	μA

NOTES

1. MP<3:0>, $\overline{\text{XIOW}}$, $\overline{\text{XIOR}}$, $\overline{\text{XBHE}}$, $\overline{\text{XMEMW}}$, $\overline{\text{XMEMR}}$, RESETB, $\overline{\text{LBE}}$<3:0> all have I_{OL} = 3.2mA.
2. SBHE, $\overline{\text{IOW}}$, $\overline{\text{IOR}}$, $\overline{\text{MEMW}}$, $\overline{\text{MEMR}}$, $\overline{\text{SMEMW}}$, $\overline{\text{SMEMR}}$, OSC, OSC/12, OUT1, SYSCLK, BALE, RDRV all have I_{OL} = 24mA.
3. All outputs and bidirectional pins.

82A306 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C306 82A306 Min	Typ	Max	Unit	Notes
t601	OSC delay from CX1↑	4		22	ns	
t602	OSC delay from CX1↓	5		26	ns	
t603	OSC/12 delay from CX1↑	9		35	ns	
t604	OSC/12 delay from CX1↓	9		37	ns	
t605	$\overline{BE}$<3:0> set-up time to $\overline{MALE}$↑	5			ns	
t606	$\overline{BE}$<3:0> hold time to $\overline{MALE}$↑	5			ns	
t607	$\overline{LBE}$<3:0> valid delay from $\overline{MALE}$↑ or SCLK↓	7		22	ns	
t608	$\overline{LBE}$<3:0> valid delay from $\overline{BE}$<3:0> valid	3		25	ns	
t609	$\overline{LBE}$<3:0> LO delay from $\overline{FBE}$↓	5		25	ns	
t610	$\overline{LBE}$<3:0> de-asserted from $\overline{FBE}$↑	3		19	ns	
t611	PPH<3:0>, PPL<3:0> set-up time to $\overline{PCHK}$↑	5			ns	
t612	PPH<3:0>, PPL<3:0> hold time to $\overline{PCHK}$↑	5			ns	
t613	MP<3:0> valid delay from corresponding PPH<3:0> and PPL<3:0>	2		21	ns	
t614	MP<3:0> set-up time from $\overline{CAS}$↑	5			ns	
t615	MP<3:0> hold time from $\overline{CAS}$↑	5			ns	
t616	$\overline{LPAR}$ delay from SCLK↑	4		23	ns	
t617	$\overline{LPAE}$ delay from SCLK↑	6		24	ns	
t618	$\overline{LPAR}$ delay from $\overline{PEN}$↑	1		13	ns	
t619	$\overline{LPAR}$ delay from $\overline{PEN}$↓	3		19	ns	
t620	$\overline{MEMW}$ (or $\overline{MEMR}$) delay from $\overline{XMEMW}$ (or $\overline{XMEMR}$)↓	3		19	ns	
t621	$\overline{MEMW}$ (or $\overline{MEMR}$) delay from $\overline{XMEMW}$ (or $\overline{XMEMR}$)	1		14	ns	
t622	$\overline{XMEMW}$ (or $\overline{XMEMR}$) delay from $\overline{MEMW}$ (or $\overline{MEMR}$)↓	4		21	ns	
t623	$\overline{XMEMW}$ (or $\overline{XMEMR}$) delay from $\overline{MEMW}$ (or $\overline{MEMR}$)	1		14	ns	
t624	$\overline{SMEMW}$ (or $\overline{SMEMR}$) delay from $\overline{XMEMW}$ (or $\overline{XMEMR}$)↓	5		23	ns	
t625	$\overline{SMEMW}$ (or $\overline{SMEMR}$) LO to HI-Z transition delay from LMEGCS↓	4		23	ns	
t626	$\overline{SMEMW}$ (or $\overline{SMEMR}$) LO to HI-Z transition delay from low to high transition of LMEGCS	6		28	ns	

Test Load = 65pF unless otherwise specified.

82A306 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C306 82A306 Min	Typ	Max	Unit	Notes
t627	$\overline{SMEMW}$ (or $\overline{SMEMR}$) LO to HI-Z transition delay from $\overline{REF}$↓	6		28	ns	
t628	$\overline{SMEMW}$ (or $\overline{SMEMR}$) HI-Z to LO transition delay from $\overline{REF}$↑	8		32	ns	
t629	$\overline{SMEMW}$ (or $\overline{SMEMR}$) delay from $\overline{XMEMW}$ (or $\overline{XMEMR}$)↑	3		19	ns	
t630	$\overline{SMEMW}$ (or $\overline{SMEMR}$) HI to HI-Z transition delay from $\overline{LMEGCS}$↓	4		23	ns	
t631	$\overline{SMEMW}$ (or $\overline{SMEMR}$) HI-Z to HI transition delay from $\overline{LMEGCS}$↑	6		28	ns	
t632	$\overline{SMEMW}$ (or $\overline{SMEMR}$) HI to HI-Z transition delay from $\overline{REF}$↓	6		28	ns	
t633	$\overline{SMEMW}$ (or $\overline{SMEMR}$) HI-Z to HI transition delay from $\overline{REF}$↑	8		32	ns	
t634	$\overline{SMEMW}$ (or $\overline{SMEMR}$) delay from $\overline{MEMW}$ (or $\overline{MEMR}$)↓	5		23	ns	
t635	$\overline{SMEMW}$ (or $\overline{SMEMR}$) delay from $\overline{MEMW}$ (or $\overline{MEMR}$)↑	3		19	ns	
t636	$\overline{IOW}$ (or $\overline{IOR}$) delay from $\overline{XIOW}$ (or $\overline{XIOR}$)↓	3		18	ns	
t637	$\overline{IOW}$ (or $\overline{IOR}$) delay from $\overline{XIOW}$ (or $\overline{XIOR}$)↑	1		14	ns	
t638	$\overline{XIOW}$ (or $\overline{XIOR}$) delay from $\overline{IOW}$ (or $\overline{IOR}$)↓	4		21	ns	
t639	$\overline{XIOW}$ (or $\overline{XIOR}$) delay from $\overline{IOW}$ (or $\overline{IOR}$)↑	1		14	ns	
t640	$\overline{SBHE}$ delay from $\overline{XBHE}$↓	3		18	ns	
t641	$\overline{SBHE}$ delay from $\overline{XBHE}$↑	1		14	ns	
t642	$\overline{XBHE}$ delay from $\overline{SBHE}$↓	4		21	ns	
t643	$\overline{XBHE}$ delay from $\overline{SBHE}$↑	1		14	ns	
t644	RESETB delay from RESET↓	3		20	ns	
t645	RESETB delay from RESET↑	1		14	ns	
t646	RDRV delay from RESET↓	3		18	ns	
t647	RDRV delay from RESET↑	1		14	ns	
t648	$\overline{BALE}$ delay from ALE↑ SYSCLK delay from ATSCLK↓ OUT1 delay from IN1↓	2		17	ns	

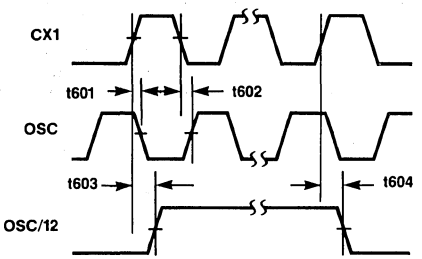
Test Load = 65pF unless otherwise specified.

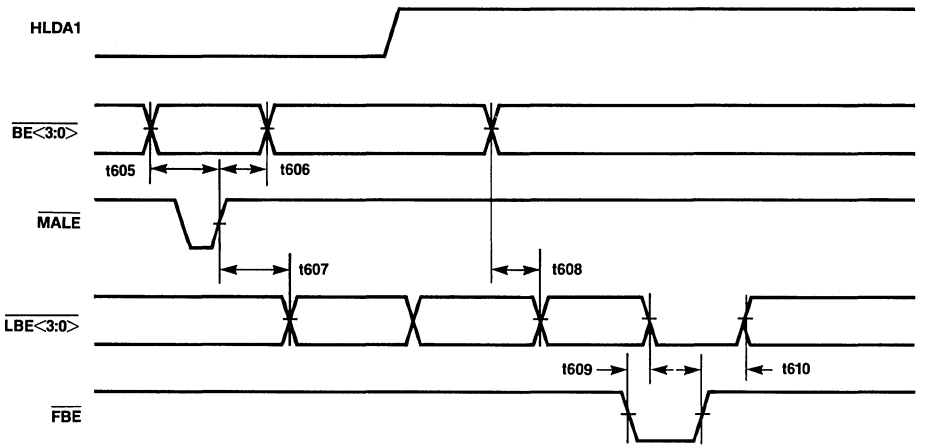
82A306 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

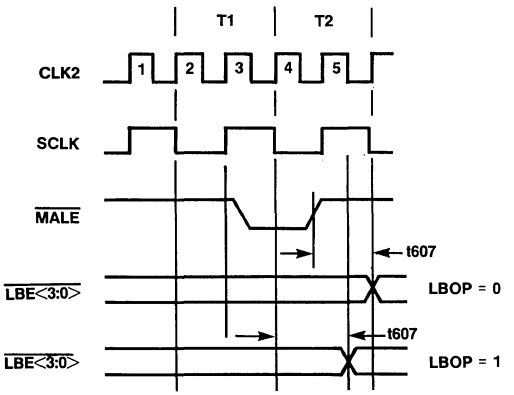
Sym	Description	82C306 82A306 Min	Typ	Max	Unit	Notes
t649	$\overline{BALE}$ delay from ALE↑ SYSCLK delay from ATSCLK↑ OUT1 delay from IN1↑	1		13	ns	
t650	M/$\overline{IO}$, D/$\overline{C}$, A31 set-up time to $\overline{MALE}$↑	5			ns	
t651	M/$\overline{IO}$, D/$\overline{C}$, A31 hold time to $\overline{MALE}$↑	5			ns	
t652	$\overline{AF32}$ HI-Z to LO transition delay from $\overline{MALE}$↑	7		32	ns	
t653	$\overline{AF32}$ LO to HI-Z transition delay from $\overline{MALE}$↑	6		29	ns	
t654	$\overline{AF32}$ LO to HI-Z transition delay from RESET	6		28	ns	
t655	$\overline{AF32}$ HI-Z transition delay from HLDA1	6		29	ns	

Test Load = 65pF unless otherwise specified.

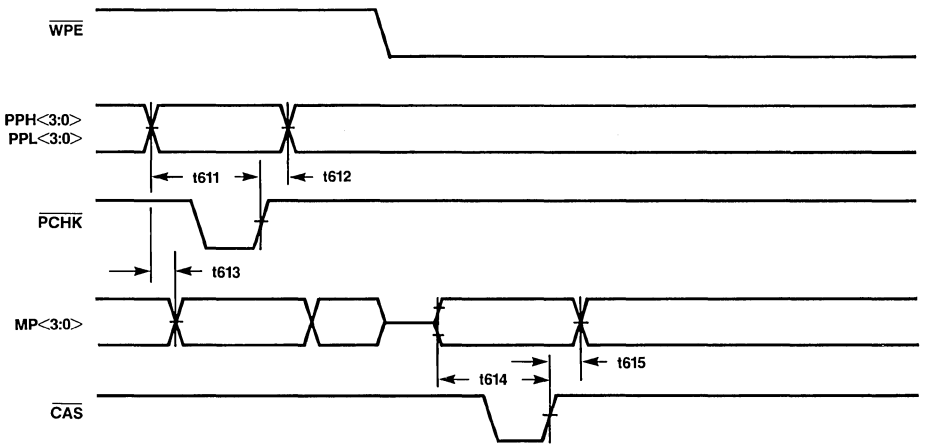
82A306 TIMING DIAGRAMS

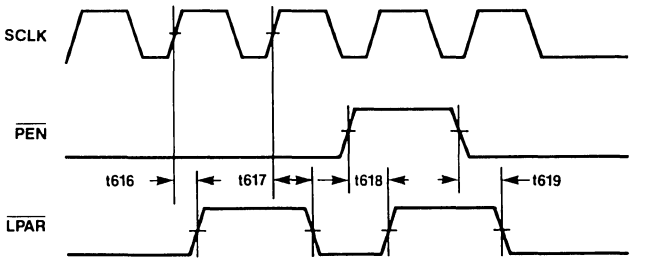




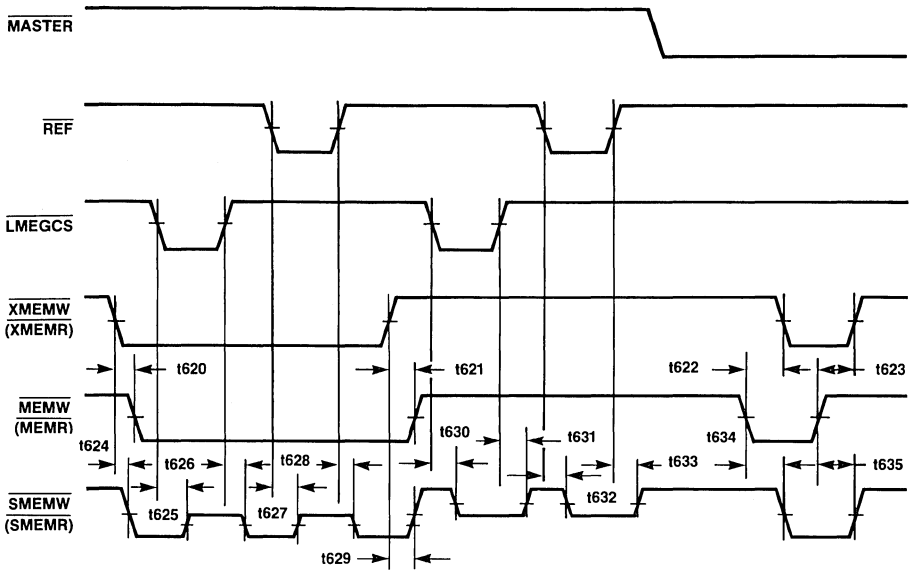


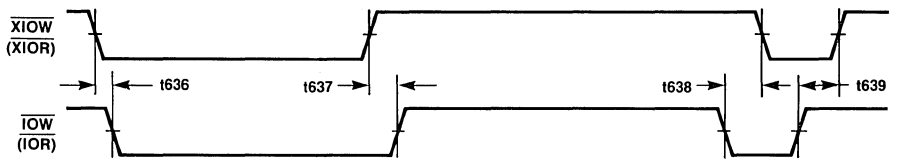
82A306 TIMING DIAGRAMS

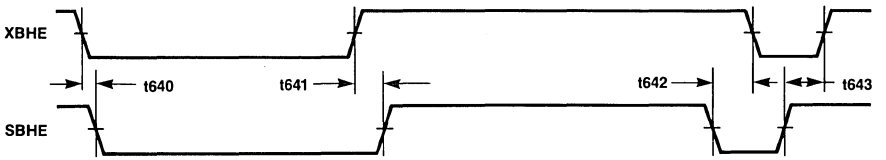




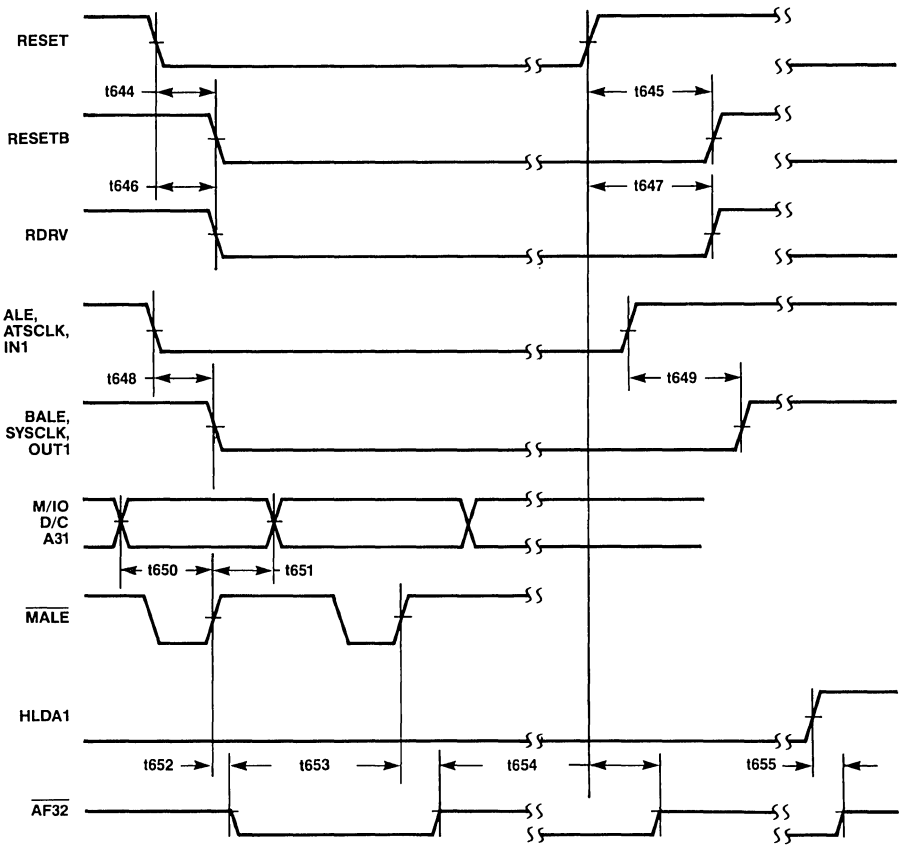
82A306 TIMING DIAGRAMS







82A306 TIMING DIAGRAMS



82C307 Cache/DRAM Controller Overview

The Functional Overview outlines the Cache architecture and provides an insight into the operation of the 82C307/80386 interface. The 82C307 performs as an integrated cache/memory controller in a 80386 based system. By maintaining the most frequently accessed code and data in high speed memory, it allows the 80386 processor to operate at its maximum rated frequency with near zero waitstates.

The 82C307 Cache Controller is designed to be a cost effective solution for achieving the full performance of the 80386 based system. This is accomplished by maintaining the most frequently accessed code and data in high speed memory (cache memory) such that most memory requests can be satisfied from this memory. If the data resides in the cache memory (hit), the data is returned to the 80386 without waitstates. If the data is not present in the cache memory (miss), then it is retrieved from the slower main memory with waitstates.

Since the cache controller and the main memory controller are both integrated into a single device, cache memory access is performed in parallel with the main memory access. In case of a hit, main memory access cycle will be terminated and the data is provided by the cache memory. In case of a miss, the main memory cycle will be completed. Performing cache access and main memory access in parallel will reduce the miss penalty.

During write operation, the data is held in a temporary buffer and the CPU is released so that it can start a new cycle before the write cycle to main memory is completed. However, if another write cycle or a read miss cycle is performed, then additional wait states are inserted until the previous cycle is completed.

The effectiveness of the cache is determined predominantly by the size and organization of the cache, the hit and miss access times, and the dynamic behavior of the program. An efficient cache organization will result in a high hit rate. Majority of the accesses are to cache and are completed without waitstates. Very few accesses are to the main memory. Consequently, the average access time will approach that of the fast cache memory.

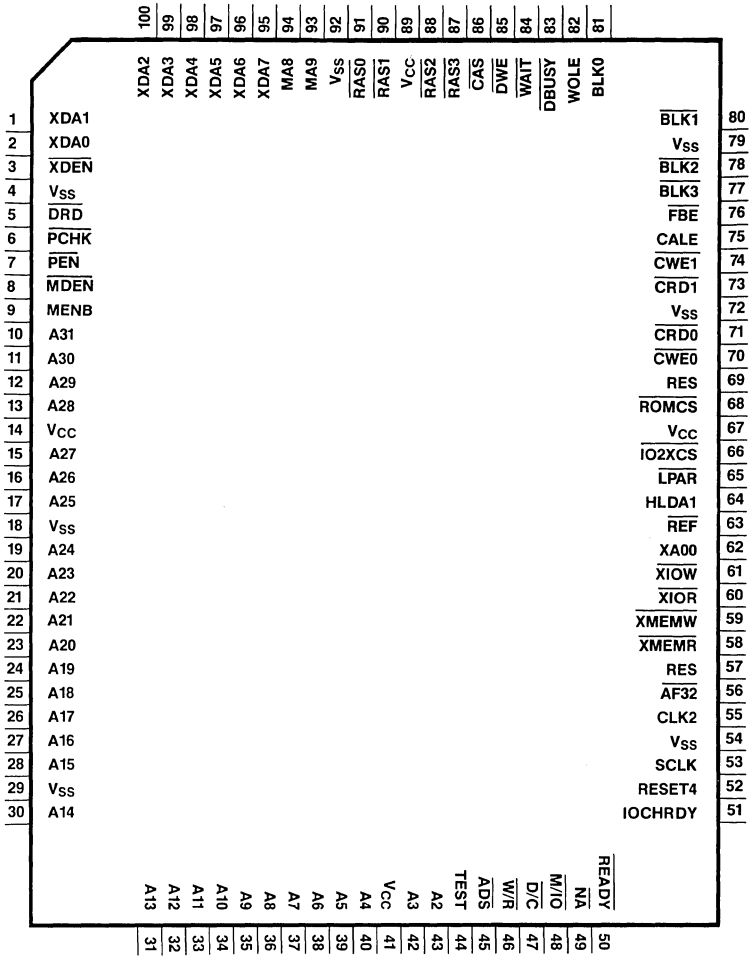
The 82C307 integrates the cache directory and the control logic required to support an external 16/32 KByte Cache and up to 4 blocks of 4 banks of DRAMs. The cache directory supports two way set-associative cache organization and maps 64 Mbytes of memory space. The minimum amount of local memory is 1 Mbyte if 256K memory devices are used (If 1 MBit DRAMs are employed, the minimum amount of local memory is 4 MBytes). A memory enable map is provided for memory residing within the 1 MByte memory address space. This mechanism can be used to prevent contention between the 1 MByte local memory and memory residing at pre-defined addresses on the AT expansion bus. For system memory above 1 MByte, it can be installed in increments of 1 MByte.

All DRAM access and refresh control signals are presented by the 82C307 with programmable configuration for 256Kx1, 256Kx4, 1 MBx1, 1 MBx4 devices. Different blocks can have different type/speed of memory devices. Parity generation and checking is implemented in conjunction with the 82A305 data buffers. Optional EDC support is included to work with generically available 32-Bit EDC circuits like the 74ALS632.

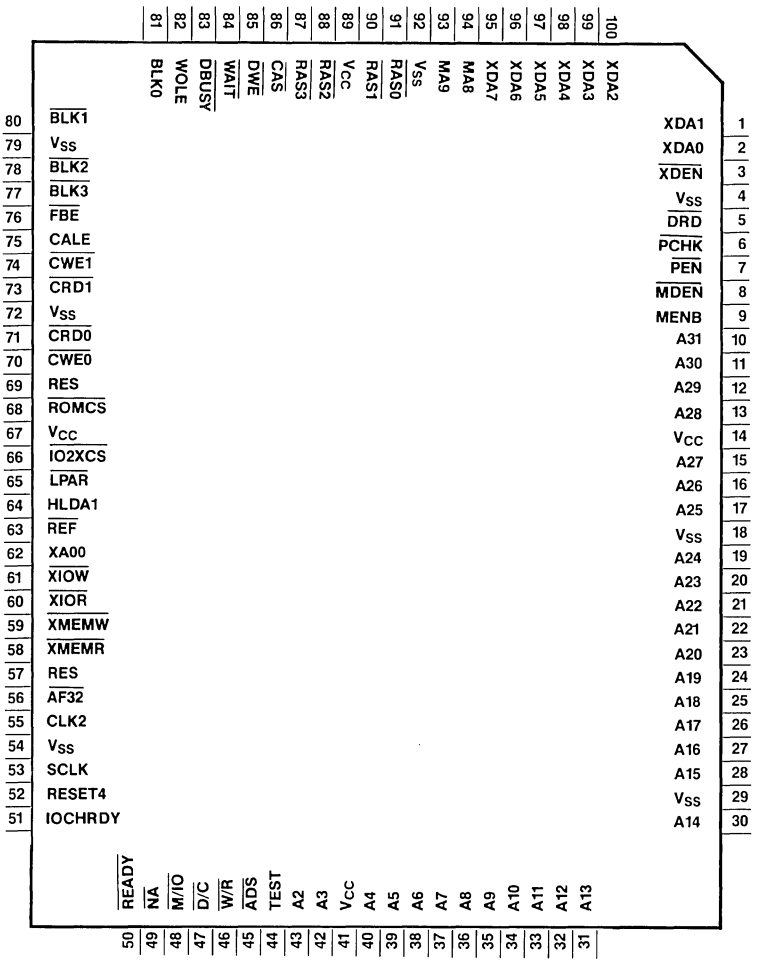
The on-chip tag RAM directory can be accessed through the 8-bit peripheral data bus. The entire tag directory RAM can be written or read from through I/O instructions for initialization or diagnostic purposes.

Cache Concepts

Cache memory optimizes processor performance and enhances bus-bandwidth within cost, size and power limitations. A Cache reduces the average access time if it is organized such that it holds the most often requested code and data. The effectiveness of the Cache is determined by the size, the physical organization, cache replacement algorithm and the behavior of the program. When a cache satisfies the processor access



82C307 Pin-Out Top View
100-Pin Rect. PFP



82C307 Pin-Out Bottom View
100-Pin Rect. PFP

requirements, the overhead resulting from accessing the slower main memory is eliminated. The cache can operate at the speed of static memories while maintaining the economic advantages of a slower main memory storage.

Program Locality

Almost all programs exhibit some "locality of references". Programs usually access memory in the neighborhood of locations already accessed recently. Program locality makes cache systems possible. There are two aspects of locality:

- temporal
- spatial

According to temporal locality, information that will be used in the future will already be in use. This type of program behavior is exhibited by program loops, in which the code and data are reused.

According to spatial locality, programs generally consist of fairly small numbers of individually contiguous segments of memory. A cache memory buffers these contiguous segments, thereby increasing the probability that the requested code and data can be found in the cache.

Cache Size

The cache size is one of the most important parameter in terms of both cost and performance trade-offs. Cache miss rate reduces asymptotically with the size of the cache. The increase in performance with an ever increasing cache size reaches a saturation point. Increasing the cache size beyond this point only increases the cost of the memory sub-system with minimal improvement in performance.

Cache Organization

The basic characteristic of a cache is the fast access time. Therefore very little or no time must be wasted when searching for words in the cache. For maximum efficiency, the cache is sub-divided into many smaller blocks of storage called lines that range in size from a single machine word (4 bytes in a 80386) to multiple words (32 to 64 bytes).

Each line has an address associated with it, that must be stored and compared against the address of the memory request. These are kept as entries (one per line) in a directory that establishes the correspondence between the data in the cache and the particular fragment of main memory that are represented.

If the size of the lines are as small as possible, then the cache directory becomes large since there is a cache directory entry for each line in the cache. Doubling the size of a cache line while holding the cache size fixed reduces the size of the directory by factor of two because two items (sub-lines) in the same line share the same directory entry.

Figure 2.1 shows a typical implementation of a line of cache memory. This line is 8-sub-line wide where each sub-line is a double word (single addressable item of 80386). Address lines A2 thru A4 will determine the desired sub-line within the line.

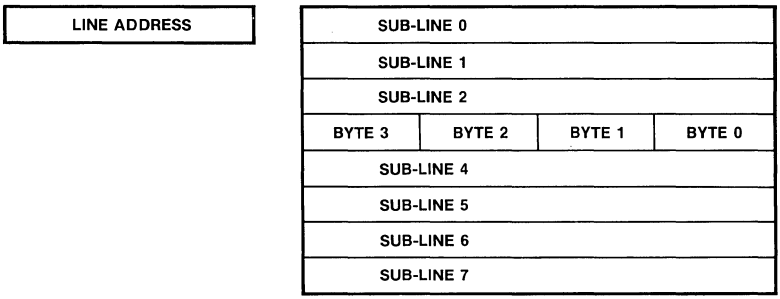


Figure 2.1.

By fragmenting the cache into smaller sections of memory that can be separately loaded, the chance of a different section of memory being requested is lowered and the time required to replace a wrong segment of memory is minimized.

The transformation of data from main memory to cache is referred to as the mapping process. Three mapping schemes are normally used:

- fully associative
- set associative
- direct mapped

Fully Associative

Programs constitute of various subroutines, stack areas and data variables located at different address locations. An efficient cache should be capable of holding several non-contiguous blocks of memory. A fully associative cache includes a tag comparator with each entry. A 16 block cache could hold 16 most often accessed blocks. As there is no relationship between the various blocks, it is necessary to maintain the entire address of the block. When the processor presents the address for the next instruction, the cache has to compare the addresses with the 16 addresses maintained in the cache. This would require 16 comparisons, to determine if a match is found.

Few caches use this organization due to the complex circuitry required and also the decrease in the miss rate achieved is very small. Additionally, the number of comparisons required to determine if it is a hit or miss is unacceptably slow and expensive.

Direct Mapped Cache

In a direct mapped cache every block has only one possible location in cache. The lower order addresses presented by the processor is used as an index to select one of the entries in the tag directory. The most significant processor address bits are compared with the contents of the tag directory to determine if it is a hit or a miss access. Unlike the fully associative cache organization, only one address comparison is required to determine if the requested data is in the cache.

Direct mapping while being the simplest to realize has certain drawbacks. No two addresses with the same index can reside in the cache memory at the same time. If the code jumps back and forth between two address locations that have the same index, the cache controller must access the main memory frequently, as only one of the addressed location can exist in the cache.

Set Associative Cache

The set associative cache compromises between the direct mapped and the fully associative cache. In a set associative cache, the index selects several entries. In a two way set associative cache, two entries can have the same index or the same lower order address bits.

The set associative cache is more complex than the direct mapped cache. In the two way set associative cache, there are two locations for each index field. Two comparisons are required to determine if the requested data is in the cache. Additionally, the tag field is wider and requires larger SRAMs to store the tag information.

Now that two locations exist for each index field, the controller must decide which block to update. When a cache miss occurs and all the locations have been used up, the controller has to decide which location to over-write. The most common replacement algorithms used are: Random Replacement, First-in-first-out (FIFO), and the Least Recently Used (LRU). With the random replacement policy, the cache controller choses one tag data item for replacement at random. The FIFO procedure replaces the item that has been in the set the longest. The LRU algorithm selects for replacement the item that has been least recently used by the CPU. The LRU algorithm is the most efficient and can be implemented by adding a few extra bits in each word of the cache.

Cache Illustration

Consider a 32KB cache memory, with 8 Double-Word wide lines.

Figure 2.2 shows the implementation of this cache in a fully associative manner. Each tag entry is 21 bits wide and each validity field is 8 bits. To construct this cache, 32KB of cache memory, 1KX21 bits wide (21K bits) for cache directory, 1KX8 bits wide (8K bits) for validity field, and 1024 21-bit comparators are required. When the processor presents the address for the next instruction, address lines A5 thru A25 are compared with all 1024 entries of the cache directory to determine a match. A2 thru A4 will select a sub-line within the line.

Figure 2.3 shows the implementation of the same cache in a direct mapped manner. Each tag entry is 11 bits wide and each validity field is 8 bits. To construct this cache, 32KB of cache memory, 1KX11 bits wide (11K bits) for cache directory, 1KX8 bits wide (8K bits) for validity field, and one 11-bit comparator is required. When the processor presents the address for the next instruction, address lines A5 thru A14 are used as an index to select one entry from the cache directory. The value contained in the tag directory is compared with A15 thru A25. If there is a match, then the data is fetched from the cache memory. If a miss is detected, then the data is obtained from the main memory.

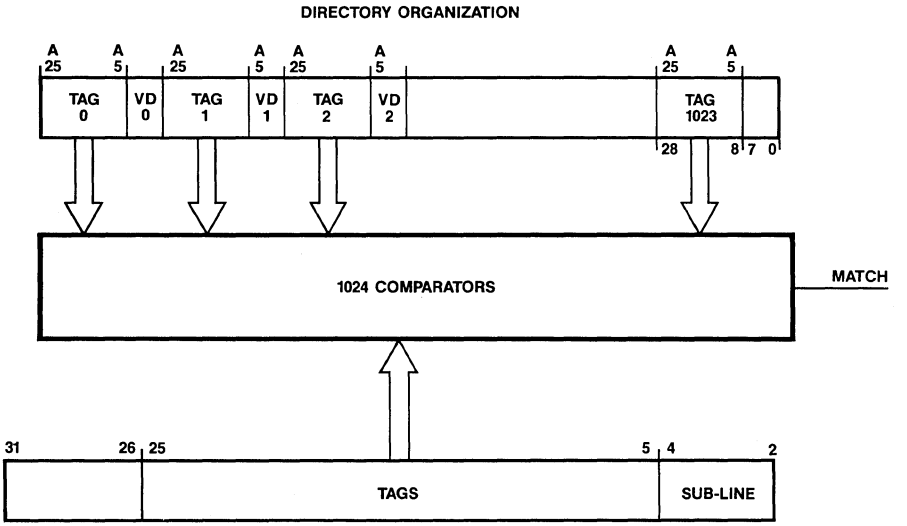


Figure 2.2. Fully Associative Cache Organization

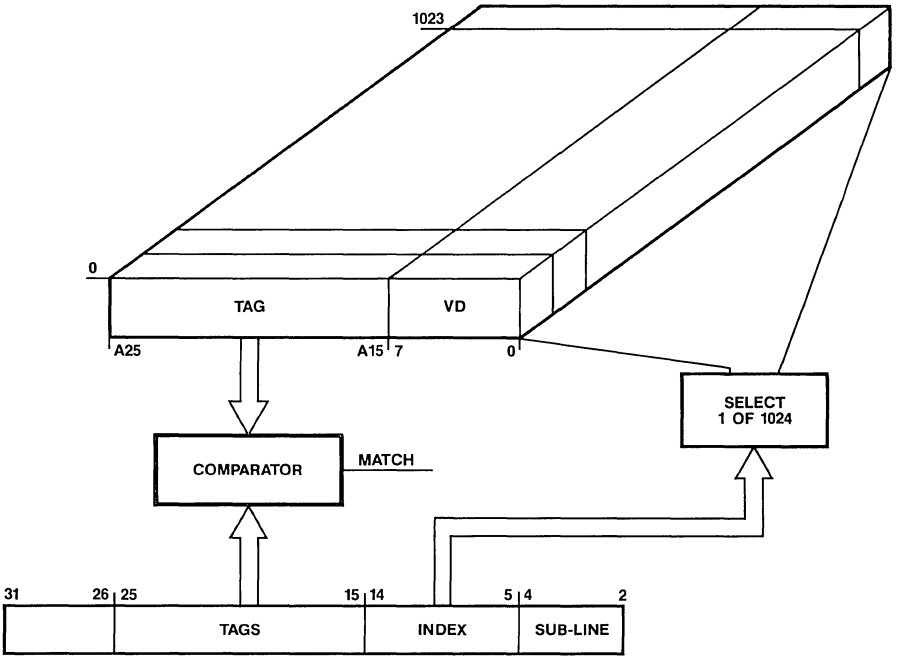


Figure 2.3. Direct Mapped Cache Organization

Figure 2.4 shows the implementation of the same cache in a two-way set associative manner. Each tag entry is 12 bits wide and each validity field is 8 bits. To construct this cache, 32KB of cache memory, 2X512X12 bits wide (12K bits) for cache directory, 2X512X8 bits wide (8K bits) for validity field, and two 12-bits comparators are required. When the processor presents the address for the next instruction, address lines A5 thru A13 are used as an index to select one line form the cache directory which points to two entries. The values contained in the tag directory are compared with A14 thru A25 to determine a match.

Figure 2.5 shows the hardware required to implement the cache in three different manners. Amount of hardware required to implement the two-way set associative cache is very close to the direct mapped cache, however, there is a significant difference between the two-way set and fully associative cache. The additional hardware required to implement the fully associative cache does not compensate for the percentile gain in its hit rate.

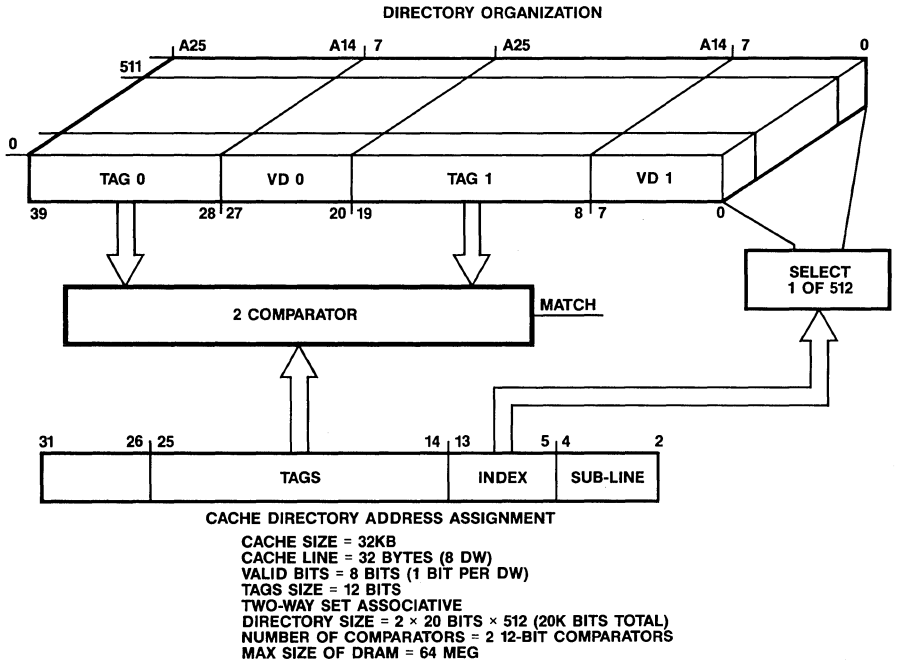


Figure 2.4. Two-Way Set Associative Cache Organization

	NUMBER OF COMPARATORS	TOTAL TAG DIRECTORY MEMORY (IN BITS)
FULLY ASSOCIATIVE	1024 21-BIT	29K
TWO-WAY SET	2 12-BIT	20K
DIRECT MAPPED	1 11-BIT	19K

Figure 2.5.

82C307 Cache Organization

The 82C307 supports 16K/32K two way set associative cache organizations. The 82C307, depending upon the size of the cache, uses a configuration of two sets of 256 lines or 512 lines. This allows two addresses with the same index to be resident in the cache concurrently. For a given cache size, the two way set associative organization will yield a significantly better cache hit rate as compared to direct mapped cache. The increase in hit rate for a four way set associative is not substantial to justify the additional complexity.

Two way set associative Cache architecture

Each entry in the 82C307 tag directory corresponds to 32 bytes and is further sub-divided into eight sub-lines of four bytes each. This reduces the number of tag directory entries and correspondingly the tag directory size. For 16 K two way set associative organization, the number of tag directory entries are 256 while for 32K organization it is 512 entries.

Figure 3.1. illustrates the relationship between the cache and the main memory. In a two way set associative organization, there are two banks of cache SRAMs and tag directory. For the 16K organization, each SRAM bank is 2K double words and the tag directory comprise of 256 entries. For the 32K organization, each SRAM bank is 4K double words, and the tag directory consist of 512 entries. Each entry in the tag directory represents 32 bytes of data.

Physical Address Field Assignment

The 80386 supports 32 address bits (30 address bits and four byte enables). While the 82C307 monitors all the 30 bits, it supports a maximum of 64 Mbytes of physical memory (A0 thru A25).

The physical address assignments for the 16KB cache memory are as follows:

Bits	Address Field
A31:A26	Highest order address bits. These bits have to be zero, as the system memory has to be located below 64 Mbytes.
A25:A13	Address Tag These are the most significant 13 bits of address stored in the tag directory. This address is compared against the tag selected by the line index to determine if the correct line is available in the cache. The size of the address tag field varies with the size of the cache data RAM.
A12:A05	Line Index Selects the correct line within the cache directory. The line index varies with the size of the cache RAM. For 16 KB, there are 8 address bits corresponding to 256 entries in the directory RAM.
A04:A02	Sub-line Index Selects the sub-line within a line. There are 8 sub-lines in a line and each subline can be individually validated/invalidated.
A01:A00	Byte Address Selects the desired byte with in a double word. The byte address is decoded into four byte enables from the 80386. The 82C307 does not monitor these 4 bytes enable lines.

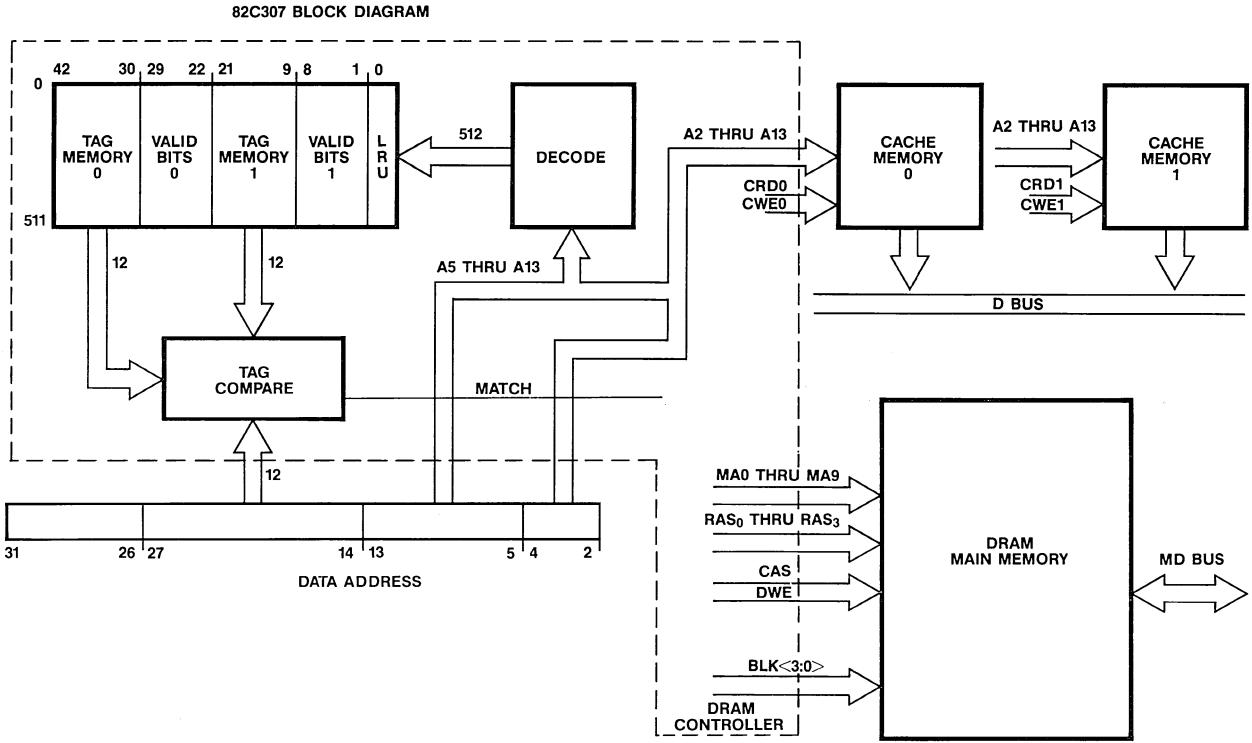


Figure 3.1. Block Diagram of Cache and Main Memory

The physical address assignments for the 32KB cache memory are as follows:

Bits	Address Field
A31:A26	Highest order address bits. These bits have to be zero, as the system memory has to be located below 64 Mbytes.
A25:A14	Address Tag These are the most significant 12 bits of address stored in the tag directory. This address is compared against the tag selected by the line index to determine if the correct line is available in the cache. The size of the address tag field varies with the size of the cache data RAM.
A13:A05	Line Index Selects the correct line within the cache directory. The line index varies with the size of the cache RAM. For 32 KB, there are 9 address bits corresponding to 512 entries in the directory RAM.
A04:A02	Sub-line Index Selects the sub-line within a line. There are 8 sub-lines in a line and each subline can be individually validated/in-validated.
A01:A00	Byte Address Selects the desired byte within a double word. The byte address is decoded into four byte enables from the 80386. The 82C307 does not monitor these 4 bytes enable lines.

Figures 3.2 and 3.3 illustrates the cache directory assignment for 16KB and 32KB.

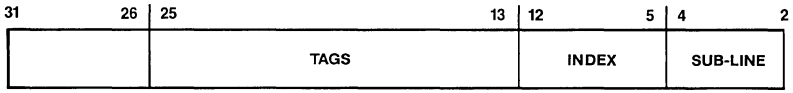


Figure 3.2. Cache Address Assignment for 16KB Data SRAM

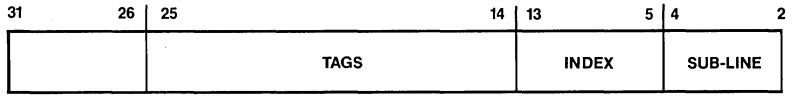


Figure 3.3. Cache Address Assignment for 32KB Data SRAM

Directory Organization

There are 43 bits per entry in the cache directory. The various fields within the entry are defined as follows:

Cache Directory Organization

Bits	Entry Field
42:30	Tag0 Bits A25:A13 of the address line selected by the line index in set 0.
29:22	VD0 Valid bits for set 0, sub-block 7:0
21:9	Tag1 Bits A25:A13 of the address line selected by the line index in set 1
8:1	VD1 Valid bits for set 1, sub-block 7:0
0	LRU Indicates which set was most recently used The valid bits are used to determine if the data in SRAM's are valid (either have been copied from the DRAM or have been initialized). In the event of a read miss, the LRU bit determines which one of the two banks receive the data. The LRU points to the block that was least recently used, thereby ensuring that the least likely to be used data is being overwritten.

Figure 3.4 and 3.5 illustrates the cache directory organization for 16KB and 32KB cache memory respectively.

NOTE: Address bit A13 in the tag field is not used for comparison purpose in the 32KB cache memory, it is part of the line index.

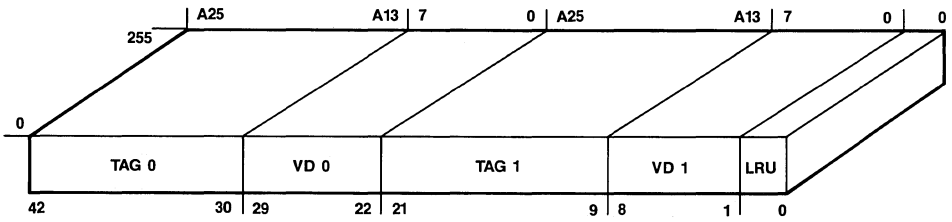


Figure 3.4. Cache Directory Orgnization for 16KB Cache Memory

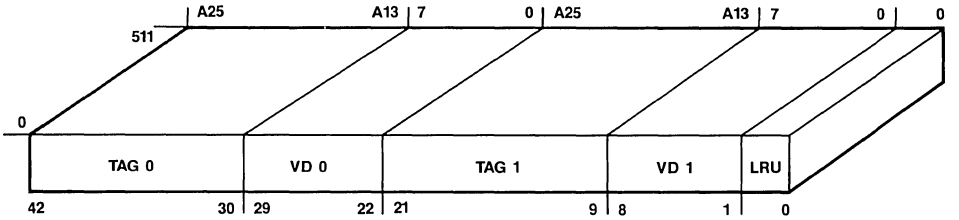


Figure 3.5. Cache Directory Organization for 32KB Cache Memory

Cache Organization

16KB Cache

The cache data array is configured as two sets of 2048 double words each. It can be implemented using 8 generically available 2K by 8 fast SRAMs. The SRAMs selected must have fast output enable of chipselect access times. Separate byte write control is provided to allow partial byte writes into a double word.

The two read select lines should be connected to all the four chips in a set. The two write enables provided must be gated with latched byte enables to enable partial writes.

Figure 3.6 and 3.7 illustrate the logical and physical cache organization for 16KB cache memory.

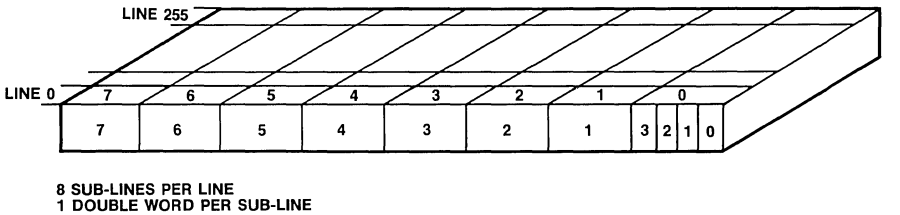


Figure 3.6. Cache Logical Organization for 16KB Cache Memory

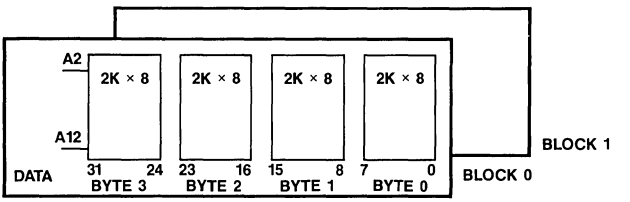


Figure 3.7. Cache Physical Configuration for 16KB Cache Using 2K × 8 SRAMs

32KB Cache

The cache data array for this size cache is configured as two sets of 4096 double words. A simple design could use 16 off the shelf 4K by 4 fast SRAMs, with 8 chips for each set. Certain versions of SRAMs do not have a separate output enables control input. The 82C307 supports a programmable feature that allow the generation of chip select instead of output enable signal. Special byte oriented functions should be provided to allow partial writes into a double word.

When operating in the pipelined mode, the addresses from the CPU change before the completion of the cycle. To ensure proper operation, the 82C307 generates CALE (Cache Address Latch Enable), signal to latch SRAM addresses.

Figure 3.8 and 3.9 illustrate the logical and physical cache organization for 32KB cache memory.

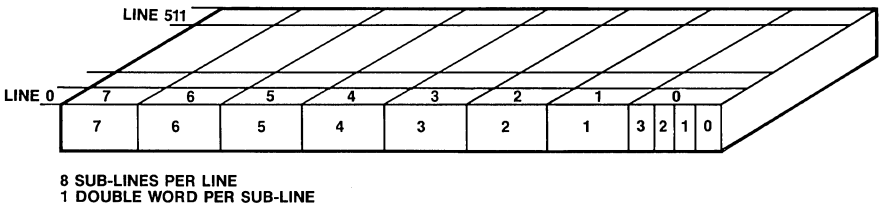


Figure 3.8. Cache Logical Organization for 32KB Cache Memory

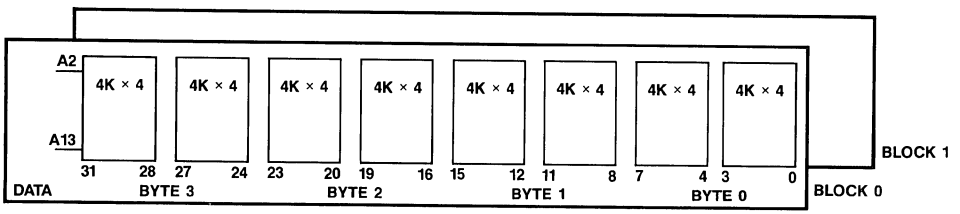


Figure 3.9. Cache Physical Configuration for 32KB Cache Using 4K × 4 SRAMs

Cache Updating

Cache maintains a copy of the most often used code of the main memory. The data in the cache should be identical to the main memory. When the cache memory is modified, the data in the main memory has to be updated as well. To meet this end, there are two basic approaches: write through and write back.

In a write through system, the controller copies the data into memory as well as the cache. This ensures that the main memory and the cache contain the same data. The drawback with this type of implementation is that each write cycle is treated as a write miss cycle, and the CPU has to wait for the slow memory to be updated.

Using a buffered write through algorithm, alleviates the problem. During the write operation, data is written into a temporary buffer. The CPU is released to begin a new cycle before the write cycle to the main memory is completed. If a write access is followed by a read hit cycle, the cache access is performed while the main memory is being updated. However, if a write cycle is followed by another write cycle or a read miss cycle, the processor has to wait for the completion of the previous cycle. The buffered write through is by far the most popular implementation.

In a write back system, the memory updates are not performed immediately. This method of implementation adds another bit called the altered bit. This bit is set if the cache is being written to with new data. This bit indicates that the cache data and the main memory data are different and that the cache contains the most up to date information. When the cache is fully occupied and a new data has to be brought into the cache, the altered bit is checked to see if the cache and the main memory contain the same data. If this bit is set, then the main memory is updated with the old data present in the cache, before overwriting its contents.

This policy is more efficient as the number of accesses to main memory is minimized (main memory is not always updated). But the circuit complexity required to implement this policy defeats the minimal performance improvement.

Cache Coherency

The buffered write through and the write back schemes ensure under normal operations, that the data present in the cache mirrors the data in the main memory. But in a system environment, other bus masters and slave DMA devices access main memory and modify the contents. The cache controllers that have built in mechanism to update the corresponding cache contents are said to maintain coherency. Many schemes are used to maintain cache coherency, the easiest being to invalidate/flush the cache during DMA operation. This though convenient, degrades the performance, as all subsequent memory accesses will be misses until the cache is filled with new data. The most popular method of maintaining cache coherency is by ensuring all accesses to the main memory through the cache controller.

Cache Operation

Processor Interface

This section will illustrate the 80386/82C301/82C307 hardware interface and discusses the interactions of these devices. Figure 4.1 shows a diagram of a 80386/82C301/82C307 based system.

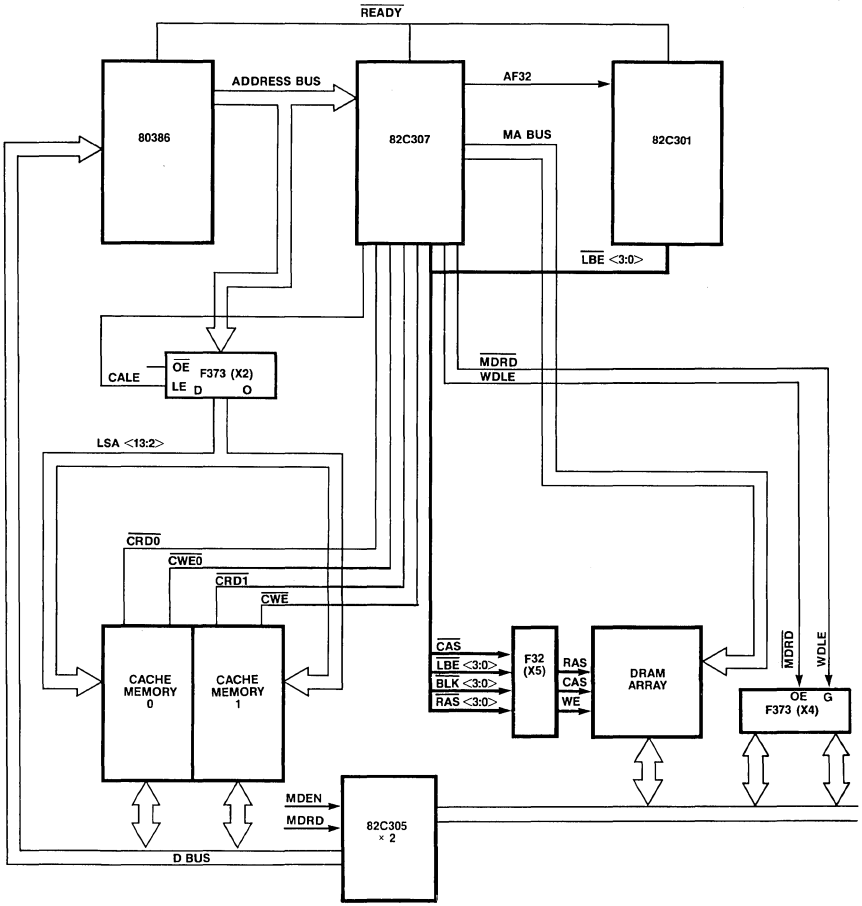


Figure 4.1. 80386/82C301/82C307 System Implementation

Read Hit Operation

When a physical address is presented to the 82C307, it uses the line index field (A5 thru A13 in 32KB cache memory) to select a line from the cache directory. A line of a cache directory points to two tag entries, one from each set. The tags stored in these locations are simultaneously compared against the processor address A14 thru A25. If a tag hit is detected and the corresponding valid bit for the selected sub-line is valid, then a hit is indicated and the the corresponding data in the cache is forwarded to the processor.

However, if the current address matches the tag of both sets and both sets are valid, a cache error occurs. An error flag is set and no memory accesses are performed. This will force a READY time out and generate an interrupt to the 82C301. The interrupt service routine should check the error flag bit of REG28 <06>.

When a hit occurs, the 32C307 drives the $\overline{\text{READY}}$ signal low to terminate the read cycle. Figures 4.2 A thru C show the timing diagrams for the read hit cycle in pipeline and non-pipeline mode.

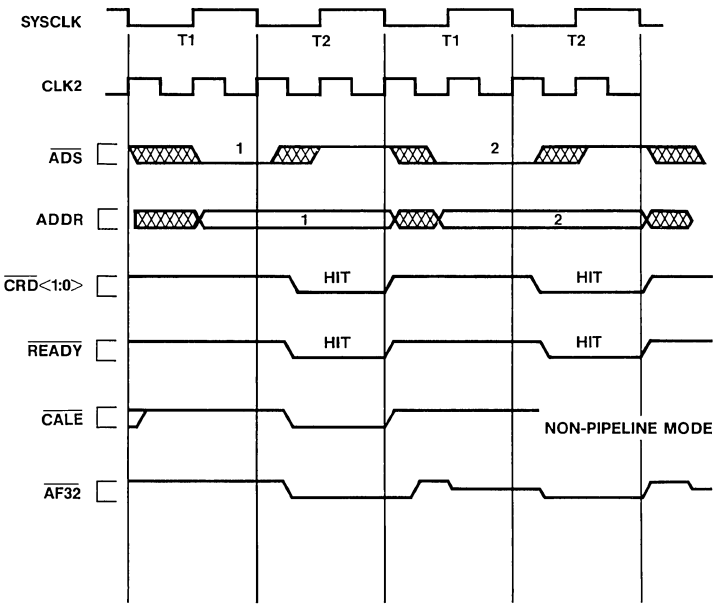


Figure 4.2A. Read Hit Cycle, 0 WS SRAM, Non-Pipeline Mode

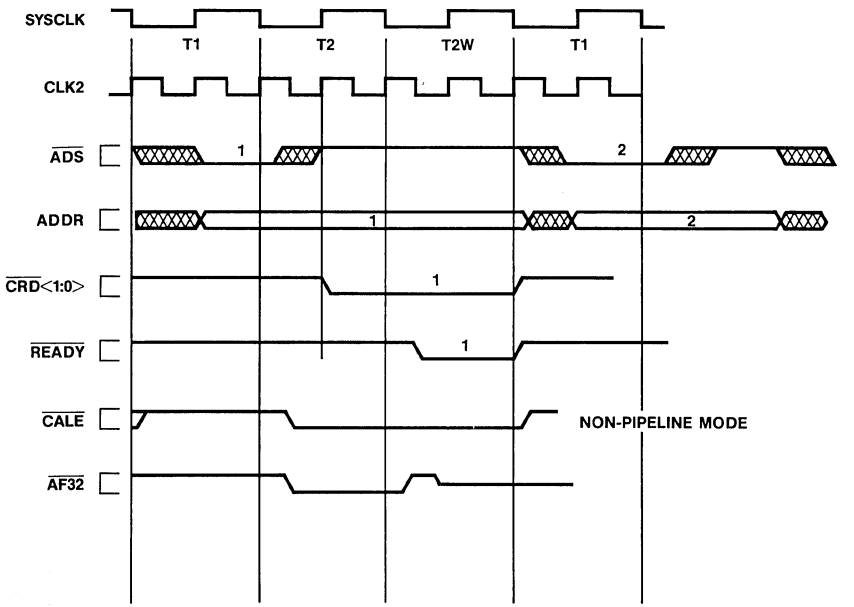


Figure 4.2B. Read Hit Cycle, 1 WS SRAM, Non-Pipeline Mode

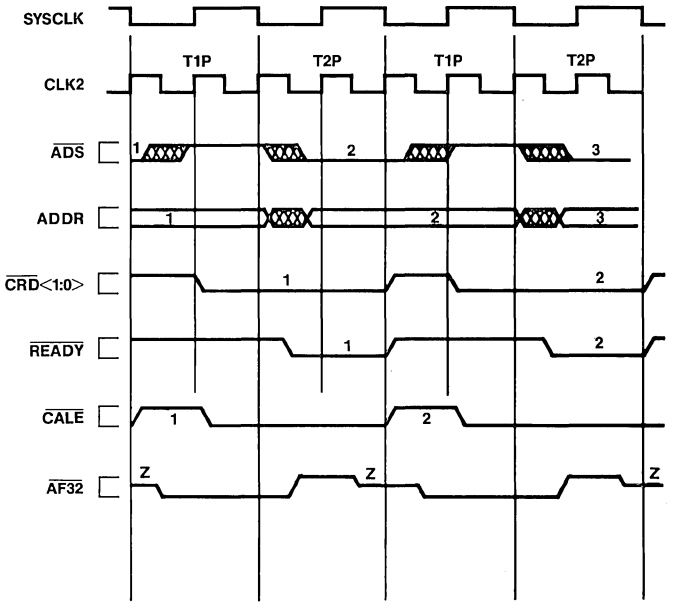


Figure 4.2C. Read Hit Cycle, 0 WS/1 WS SRAM, Pipeline Mode

Read Miss Operation

When a cache read miss occurs, the main DRAM memory will provide the data for CPU and it will also present the same data to cache memory. A replacement algorithm which has the least amount of potential performance penalty is used. The least-recently-used (LRU) bit is an indication of which set should be replaced—the set which is not recently used, therefore less likely to be used in the near future is the set that should be replaced.

Figures 4.3 A thru E show the timing diagrams for the cache read miss cycle

Write Hit Operation

If a CPU initiated write cycle starts, a DRAM cycle will also start immediately independent of cache hit or miss result. If a cache hit happens in a write cycle, a SRAM and DRAM write cycle will be initiated simultaneously. Since SRAM cycle is much faster than DRAM cycle, different number of wait states are required. Instead of having the CPU wait for the completion of the DRAM cycle, a temporary register between CPU and the main memory will temporarily hold the data for DRAM so that the processor can continue.

If a cache miss occurs in a write cycle, no cache write operation will be done, only data in the main memory will be updated. Figures 4.5 A thru E show the timing diagrams for the cache write miss cycle.

If any of the cycles, immediately following the first write cycle requires another DRAM access while the main memory is still busy with the first write cycle, then additional wait states will be asserted until the DRAM has completed the previous operation. Figures 4.4G and 4.4H show the timing diagrams for write cycle followed by another write cycle and a write cycle followed by a read miss cycle respectively.

Direct DRAM Access

The CPU can bypass the cache to access the data in the DRAM directly. This feature is necessary during initial boot up to check the integrity of the DRAM subsystem. In this mode, no SRAM cycle will be done. Every memory cycle will be a single RAS followed by CAS access with an user's option of 2 to 4 wait states.

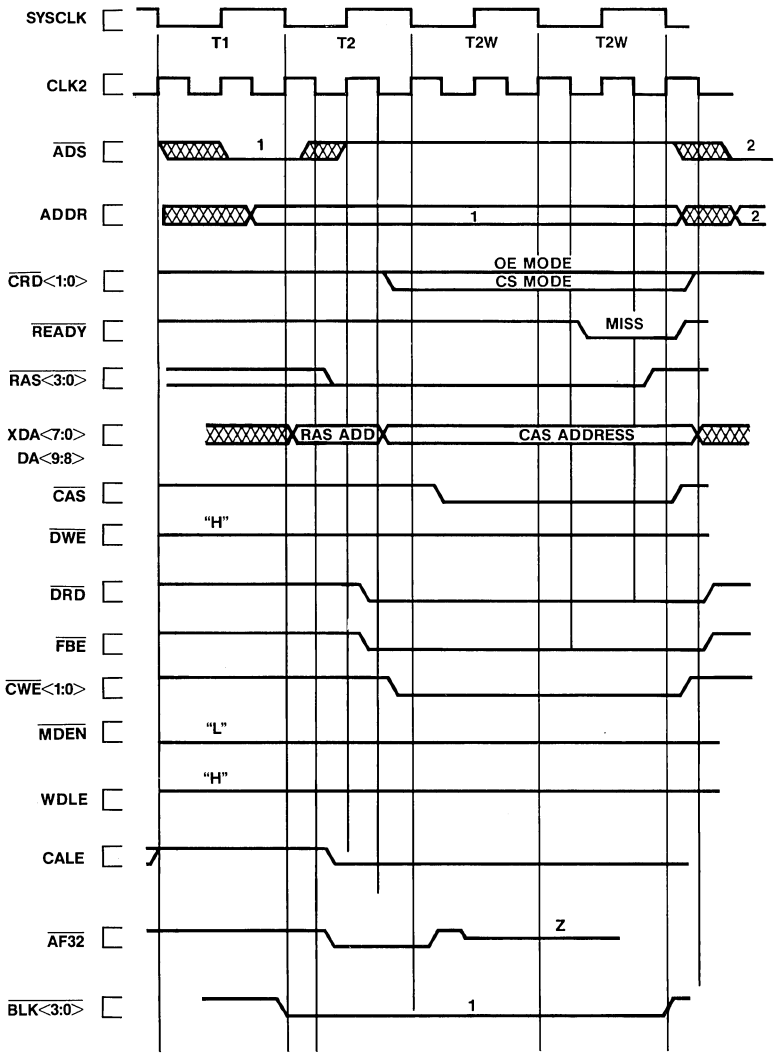


Figure 4.3A. Read Miss Cycle, 2 WS DRAM, 0 WS SRAM, Non-Pipeline Mode

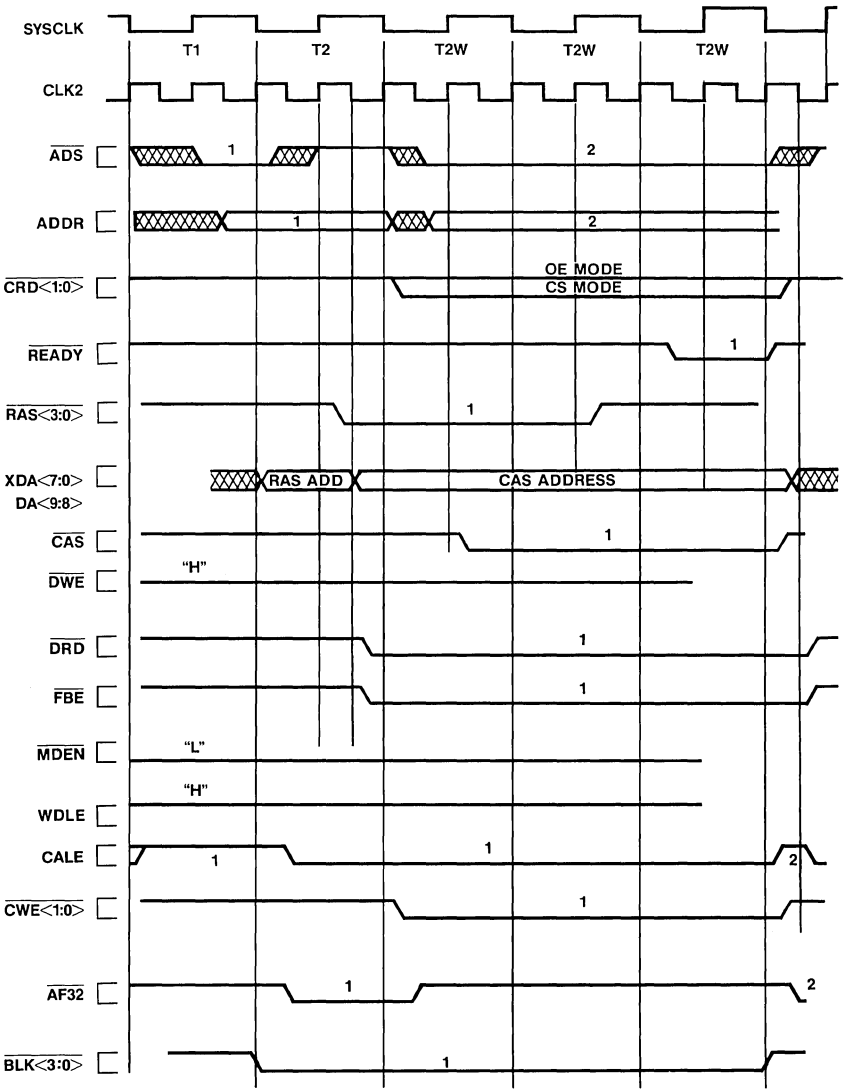


Figure 4.3B. Read Miss Cycle, 2 WS DRAM, 1 WS SRAM, Non-Pipeline Mode

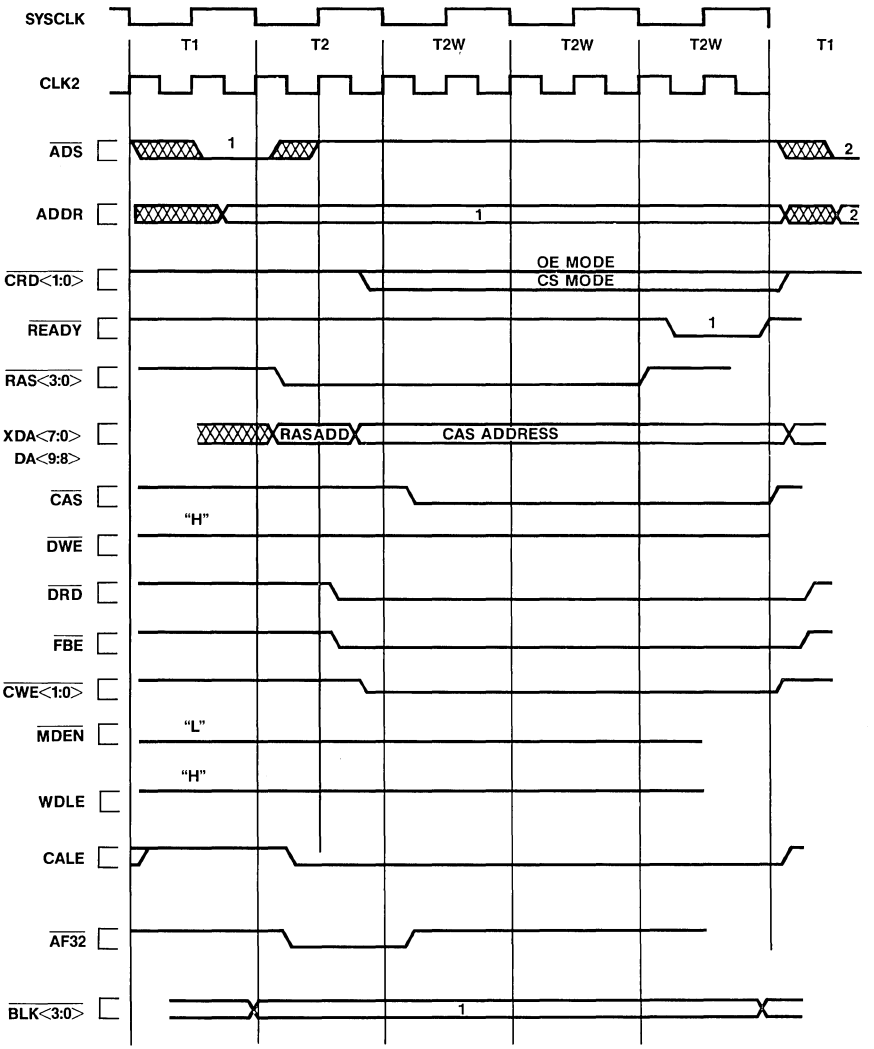


Figure 4.3C. Read Miss Cycle, 3 WS DRAM, 0 WS SRAM, Non-Pipeline Mode

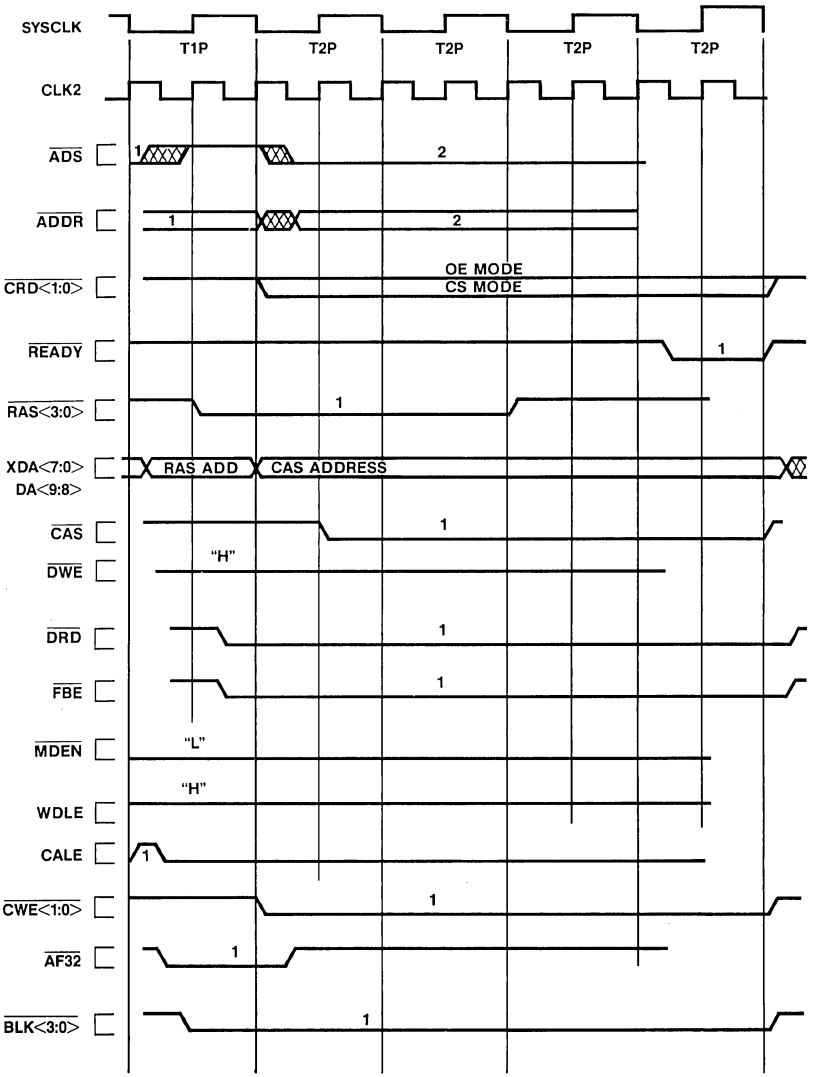


Figure 4.3D. Read Miss Cycle, 3 WS DRAM, 0/1 WS SRAM, Pipeline Mode

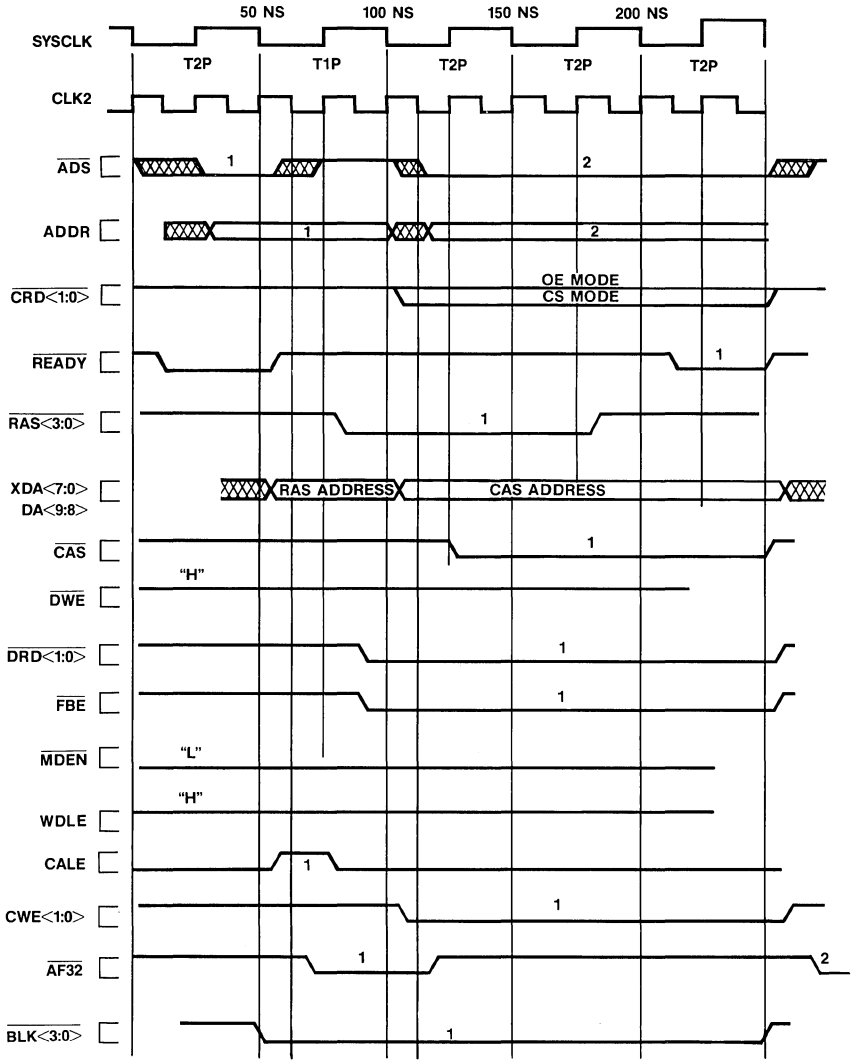


Figure 4.3E. Read Miss Cycle, 2 WS DRAM, 0/1 WS SRAM, Pipeline Mode

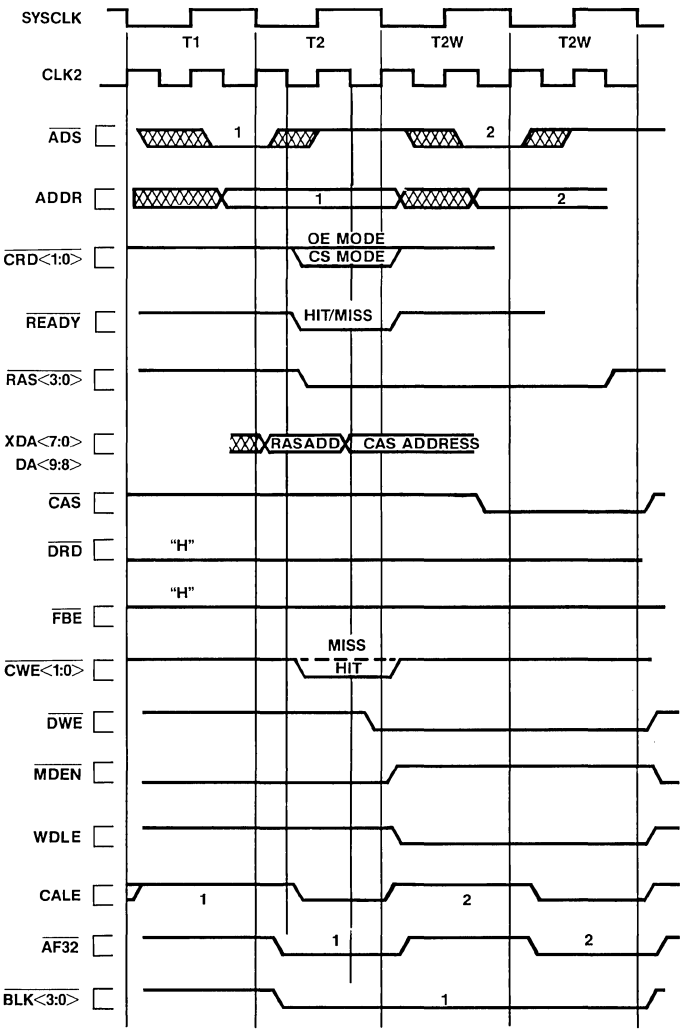


Figure 4.4A. Write Hit/Miss Cycle, 2 WS DRAM, 0 WS SRAM, Non-Pipeline Mode

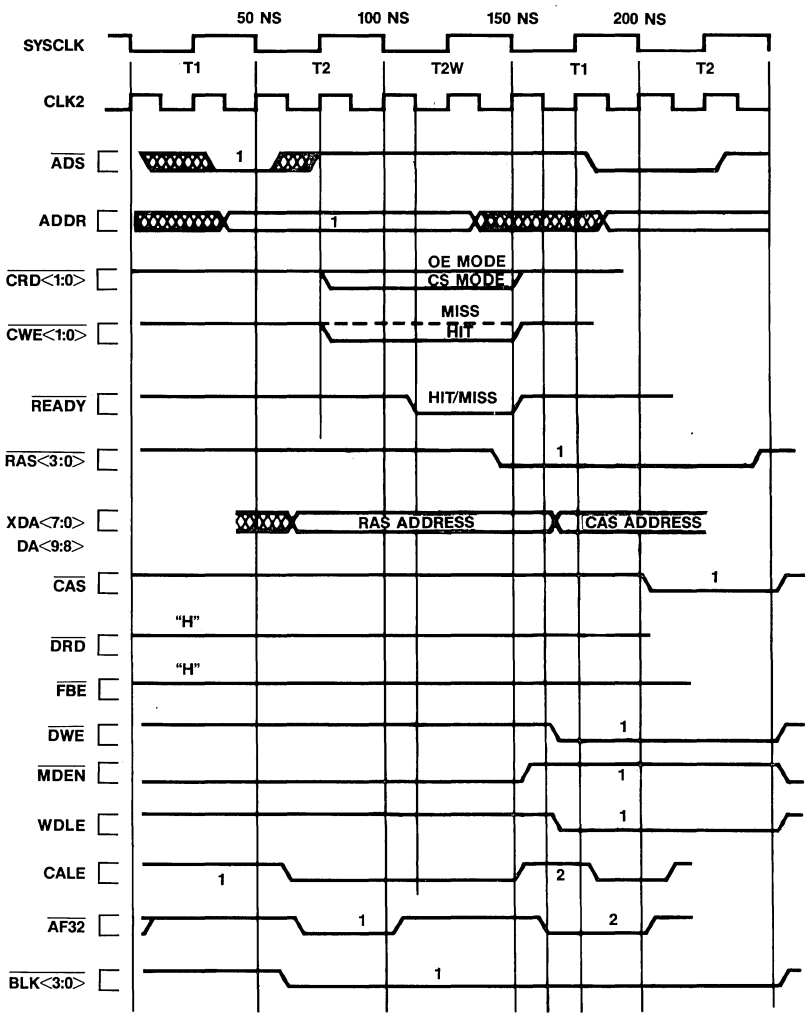


Figure 4.4B. Write Hit/Miss Cycle, 2 WS DRAM, 1 WS SRAM, Non-Pipeline Mode

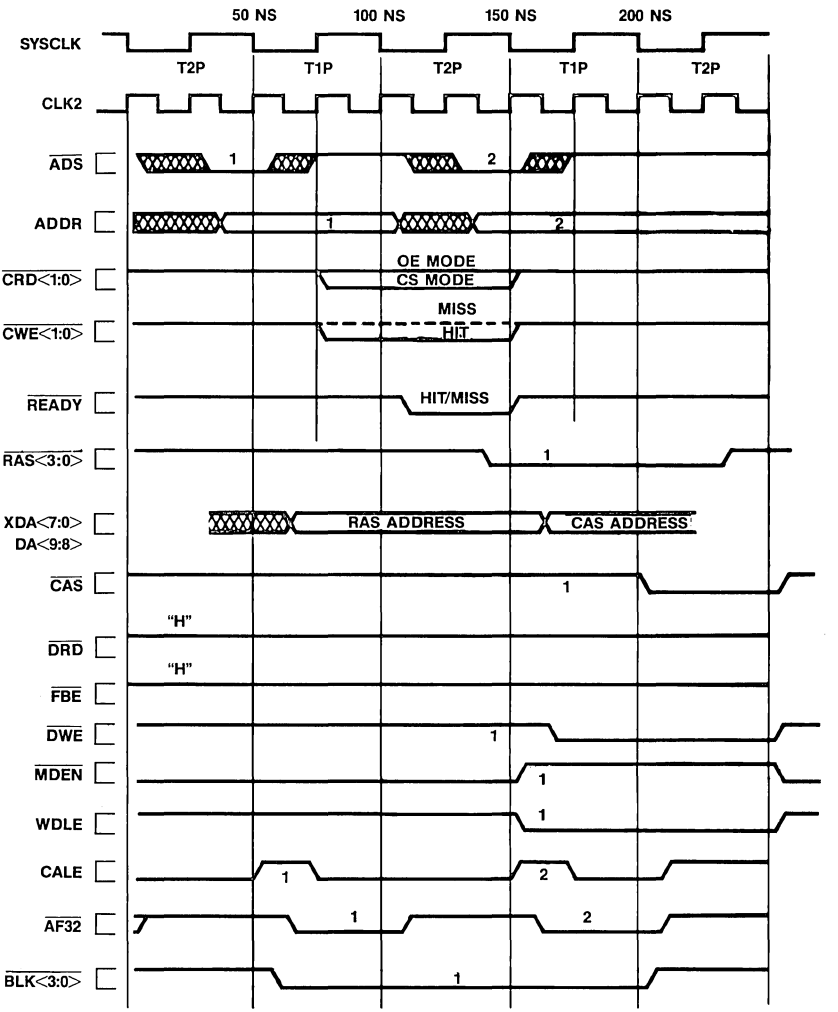


Figure 4.4C. Write Hit/Miss Cycle, 2 WS DRAM, 0/1 WS SRAM, Pipeline Mode

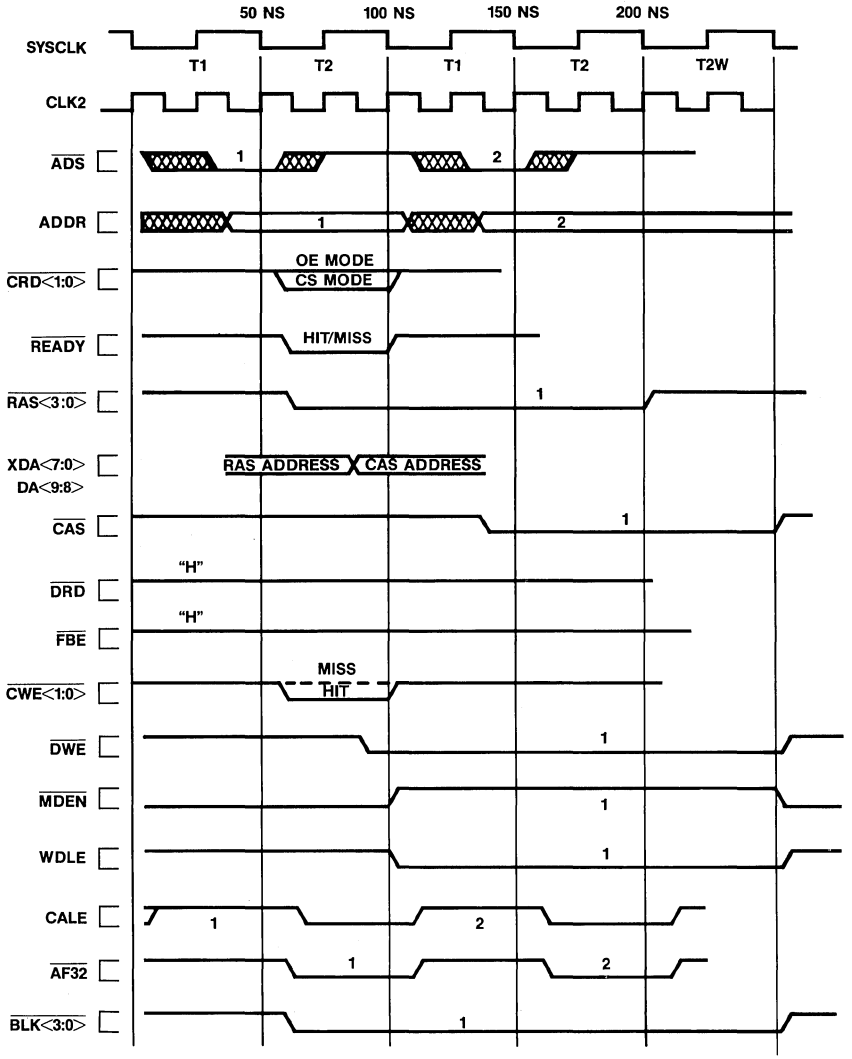


Figure 4.4D. Write Hit/Miss Cycle, 3 WS DRAM, 0 WS SRAM, Non-Pipeline Mode

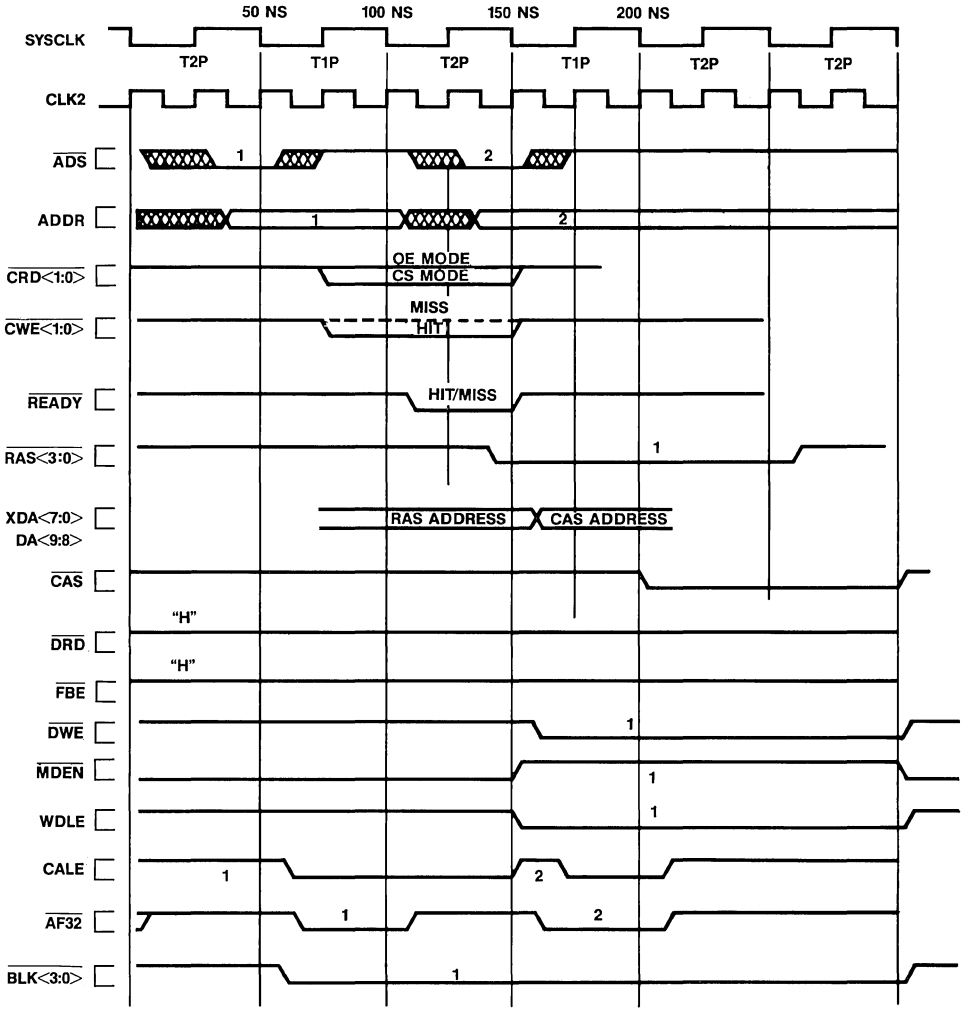


Figure 4.4E. Write Hit/Miss Cycle, 3 WS DRAM, 0/1 WS SRAM, Pipeline Mode

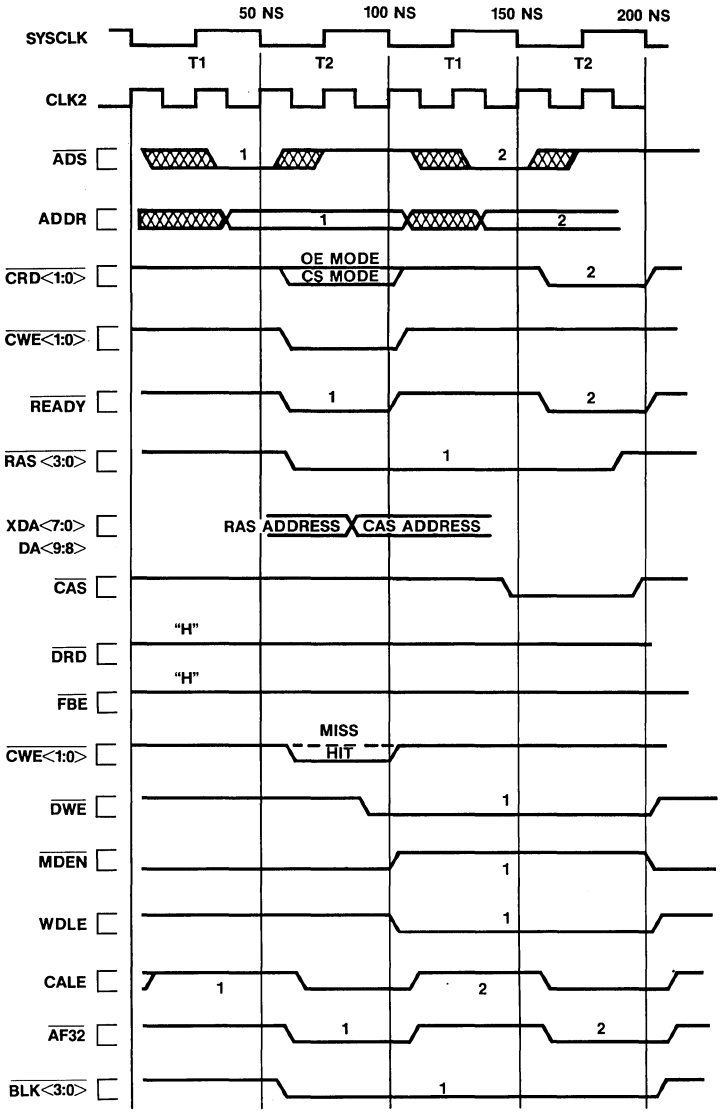


Figure 4.4F. Write Hit Followed by a Read Hit,
0 WS SRAM, 2 WS DRAM
Non-Pipeline Mode

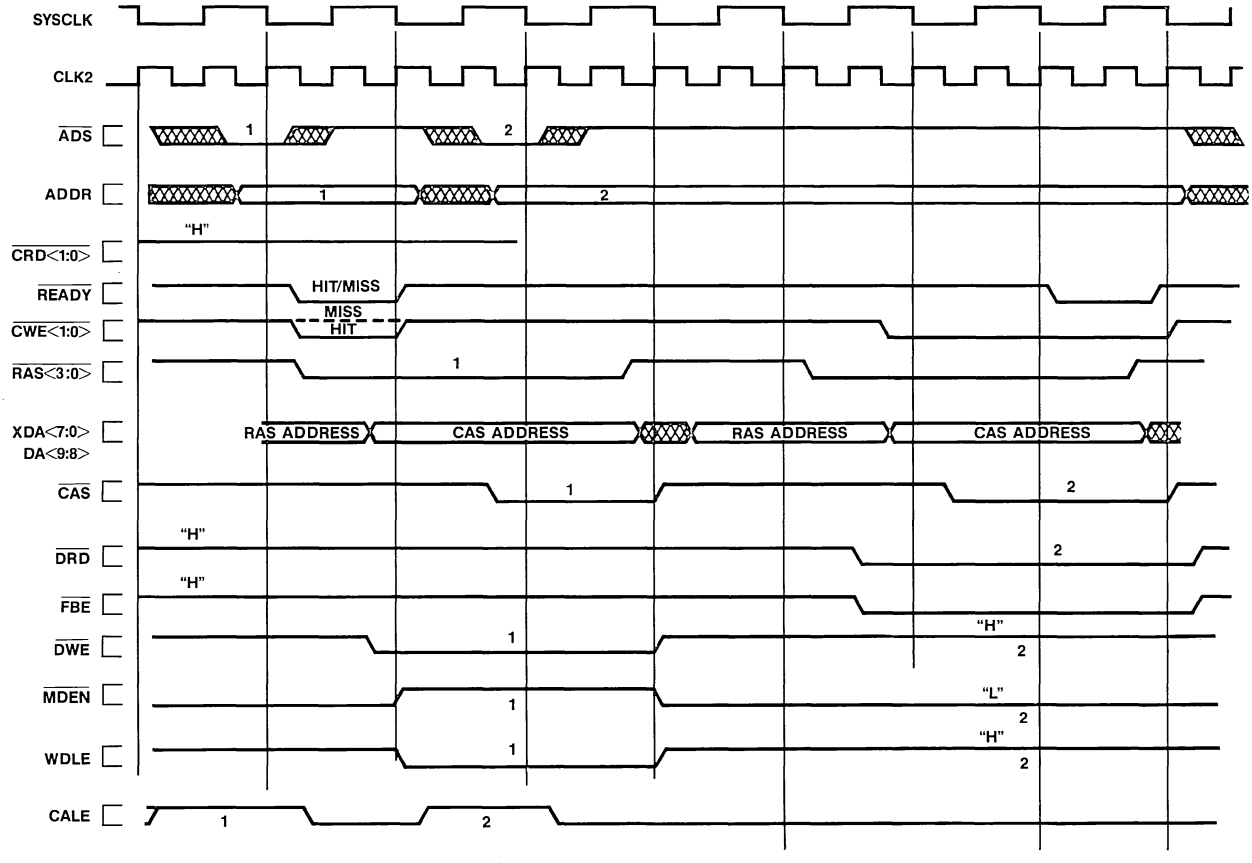


Figure 4.4G. Write Followed by a Read Miss Cycle, 0 WS SRAM, 2 WS DRAM, Non-Pipeline

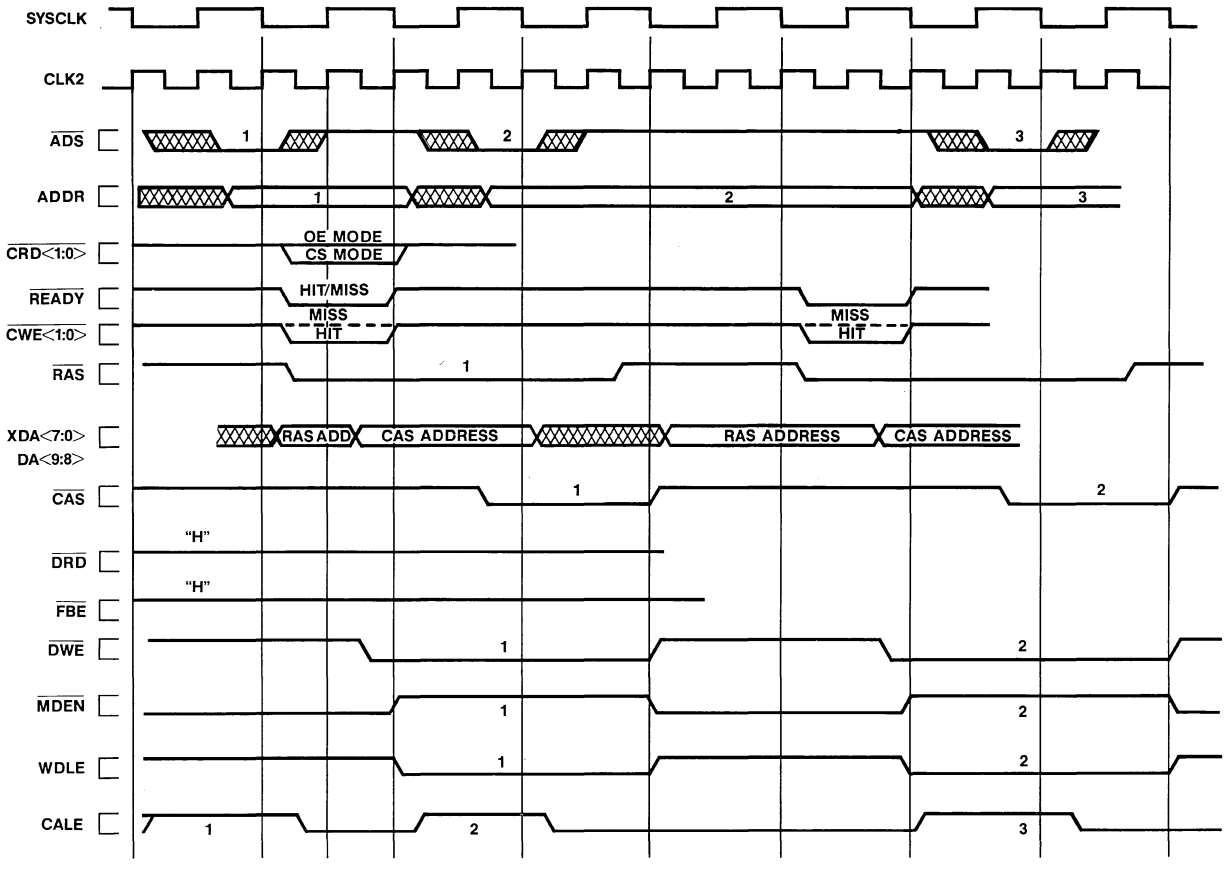


Figure 4.4H. Write Followed by Another Write Cycle, 0 WS SRAM, 2 WS DRAM, Non-Pipeline

DMA Operation

For local memory read cycles initiated by DMA or other masters on the bus, regardless of cache hit or miss, no SRAM will be accessed. All memory read cycles will be directed to main memory and the data buffer (82C305) will receive data from the MD bus and drive the LD and SD buses.

For a local memory write cycle, the buffer's direction is from SD bus toward MD and LD buses. Therefore a cache miss will cause the data to be written into the DRAM only and a cache hit will write the data into the DRAM and SRAM to maintain the coherency.

Figures 4.6 and 4.7 show the timing diagrams for the DMA read and DMA write cycles.

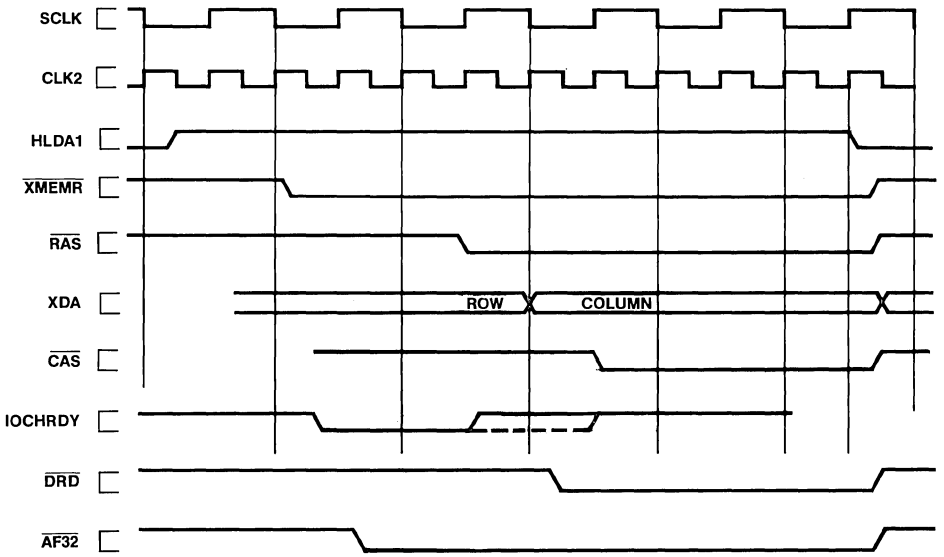


Figure 4.6. DMA Read Cycle

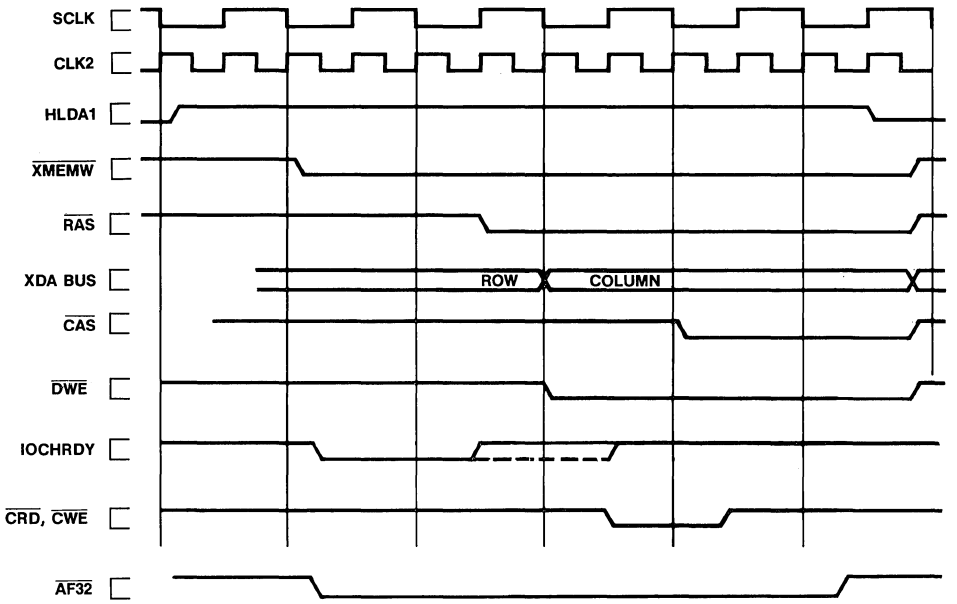


Figure 4.7. DMA Write Hit Cycle

Figure 4.8 shows the timing diagrams for the Refresh Cycle.

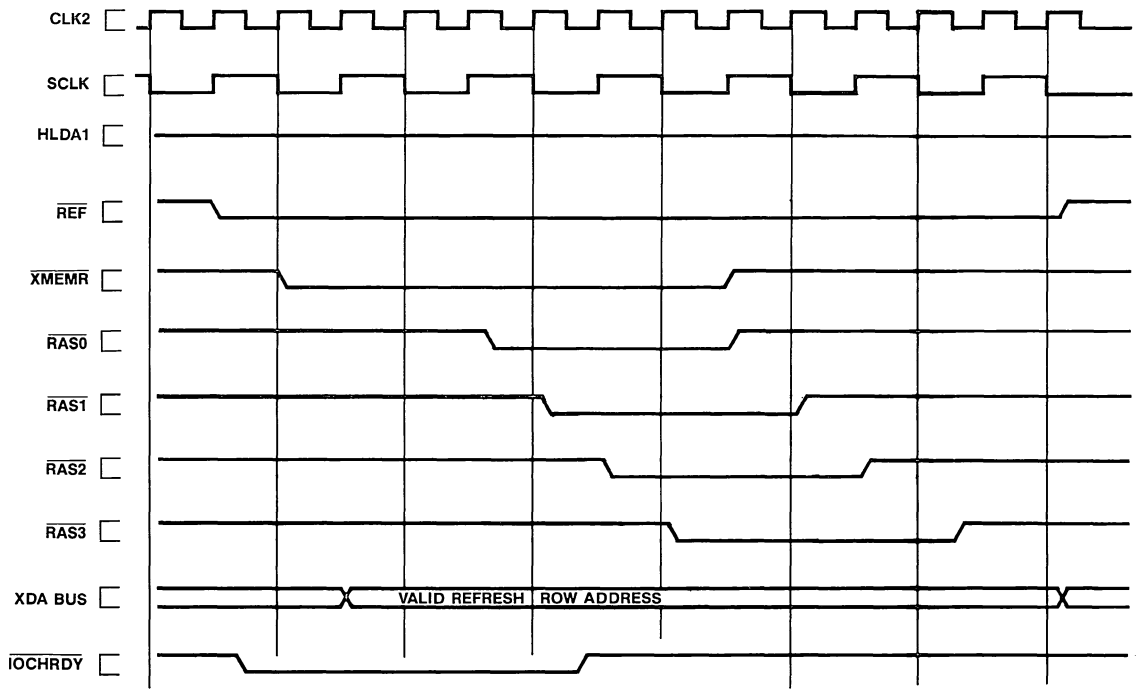


Figure 4.8. Refresh Cycle

Figure 4-9 shows the timing for ROM Read Cycle.

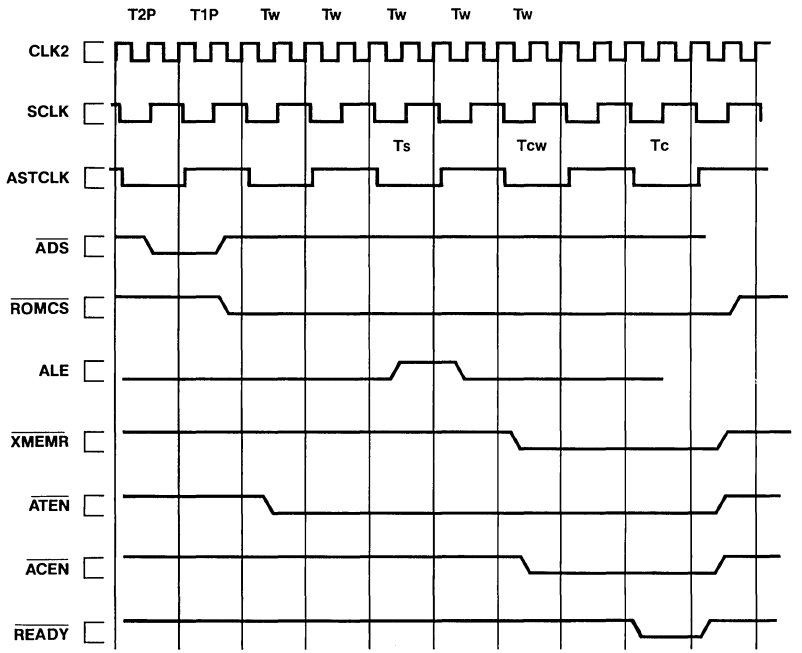


Figure 4.9. ROM Read Cycle

Functions Supported by BIOS Extension

Line Invalidation

Any line in the cache directory can be selectively validated/invalidated through the configuration registers. The registers involved are REG21-23.

Directory/Cache Purge

The directory purge can be done in the same way as line invalidation by I/O cycles through REG21-23. The I/O read cycles will read the current values in the directory RAM and the IO write cycles will load the desired values into the directory. The advantage of this mode of purging is that a program can non-destructively examine the contents of cache directory RAM.

To purge the cache data RAM, the cache has to be disabled REG20<7> and the SRAM direct access bit REG20<4> should be turned on. Then the cache data RAM will appear as part of the main memory in a 32KB block specified by REG24<4:0> in the first 1MB.

Another way to flush the directory RAM is by using REG20<2>. If this bit is set to 0, then all following memory access will act differently. The valid field of both sets of the particular line selected by the index field will be reset to invalid (all 8 sub-lines/8 valid bits). To flush the entire TAG RAM, one pass through the entire line index field is required. The LRU field in this case is ignored.

Cache Enable/Disable Sequence

After power-on reset, the cache is disabled. Valid data can be loaded into DRAM without effecting the cache. All valid bits in cache directory should be disabled by executing I/O cycles. Then the cache can be enabled. As soon as the cache is enabled, the hit rate will be zero since all valid bits are set to be invalid and the cache data RAM is empty. As the program is executed, the cache data RAM will be filled up gradually and the hit rate will increase until and equilibrium point is reached.

To disable the cache, REG20<7> can be turned off again to become direct DRAM access mode only. Since the consistence between cache memory and main memory is always maintained, the program can continue execution from main memory without intrusion.

82C307 Internal Registers

The 82C307 has 24 bytes of internal registers used for system configurations and diagnostics. These registers are accessed through I/O ports 22H and 23H normally found in the interrupt controller. An indexing scheme is used to reduce the number of I/O addresses required to access all registers needed to configure and control cache controller. Port 22H is used as an index value for the required data accessed through port 23H. Each access to an internal register is done by first writing its index into the port 22H. This index then controls the multiplexers gating the appropriate register data accessible on port 23H. Every access to port 23H must be preceded by writing the index value to port 22H even if the same data port is being accessed again.

Memory Configuration Registers

There are 9 bytes of memory configuration registers which are used to control and map the address space as shown in figure 5.2. The definitions for these registers are given in table 5.1.

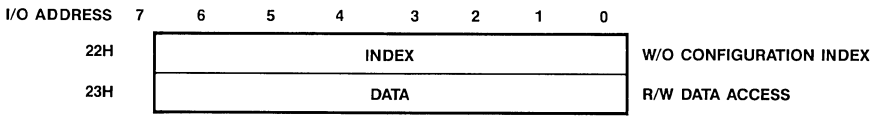


Figure 5.1. Configuration Register Access Ports

INDEX	7	6	5	4	3	2	1	0	
08H	1	VERS		MW	MR	HM	SM	NA	IDENTIFICATION
09H	R3	R2	R1	R0	D3	D2	D1	D0	ROM CONFIGURATION
2AH								0	MEMORY ENABLE (1 BLK OF 256KB)
0AH	368K							256K	MEMORY ENABLE (16KB PER BIT)
0BH	496K							384K	
0CH	624K							512K	
0DH	752K							640K	MEMORY ENABLE (16KB PER BIT)
0EH	880K							768K	
0FH	1008K							896K	

Figure 5.2. Control and Address Space-Map Register Summary

Index	Definition
08H	Identification
Bits	Field definition
7	Controller Type Value: 1 — Semantics: Cache controller (82C307)
6:5	Version Value: 0 — Semantics: Initial
4	Middle Boot Space Write Protect. This bit is used in conjunction with the bit 3 to allow BIOS code to be copied into RAM and write protected at this location as well as the below 1MB. It should be used if there is RAM present at this address (16 MB installed). Executing out of RAM will result in better performance than out of narrower (8 or 16 bit) EPROMS. The middle boot space starts at 16128K (00FC0000H) which is 256KB below the 16MB boundary. Value: 0 — Semantics: Enable R/W. Default Value: 1 — Semantics: Disable Write, Read Only.
3	MR-Middle Boot ROM Disable Value: 0 — Semantics: The boot/BIOS ROM located just below 16 MB is disabled. This bit should be set when physical memory greater than 16 MB is installed to allow a contiguous RAM address space and if no boot/BIOS ROM is located at this address range. Value: 1 — Semantics: Just below 16 MB is enabled (with $\overline{\text{ROMCS}}$ output) being active. This is necessary for 286 compatibility. Default.
2	HM-16MB I/O Channel Memory Limit. Controls the assertion of $\overline{\text{AF32}}$ for addresses greater than 16 MB. Since I/O channel memory cannot normally be configured above 16 MB, accessing above 16MB will cause a ready time out if that feature is enabled. This is necessary during setup because memory address above 16 MB that are not enabled for local memory could wrap into a valid I/O channel memory location. The maximum amount of memory for 82C307 based memory system is 64MB. This bit should be used in conjunction with the physical memory. If physical memory is installed above 16 MB and is enabled, this feature will be ignored until the upper limit of physical memory is reached (between 16MB and 64MB).

Index	Definition (continued)	
08H	Identification	
Bits	Field definition	
	Value	Semantics
	0	$\overline{AF32}$ will not be asserted. Should only be used if external logic can recognize addresses above 16 MB. Default.
	1	$\overline{AF32}$ will be asserted. Unless real physical memory is installed for that address range. no memory cycle will start and no $\overline{READY}$ signal will be given to the CPU.
1		SM-Small memory configuration after reset. Used during initialization.
	Value	Semantics
	0	Only 256K enabled. Default. Ignore memory address configuration registers 0AH thru 0FH. When this bit is 0, only lower 256KB of memory is available. Together with bit 0 of register 2AH, all memory on local memory subsystem can be disabled for system debugging/development purposes.
	1	Normal configuration controlled by registers 0AH thru 0FH.
0	NA-Next Address Mode This address controls the $\overline{NA}$ output. It is used to request the 80386 into pipelined/non-pipelined mode.	
	Value	Semantics
	0	Request to 80386 into pipelined mode.
	1	Request to 80386 into non-pipelined mode. Default.

Index	Definition

09H RAM/ROM Configuration in low memory boot area.

Bits	Field Definition
7	64KB of RAM at 768K C0000-CFFFFH (EGA)
6	64KB of RAM at 832K D0000-DFFFFH
5	64KB of RAM at 896K E0000-EFFFFH
4	64KB of RAM at 960K F0000-FFFFFH (BIOS)

Bits 7:4 disable writing to RAM located in the BIOS area in 64KB blocks.

Value	Semantics
0	Read/Write. Default.
1	Read/Only.

3	64KB of ROM at 768K C0000-CFFFFH (EGA)
2	64KB of ROM at 832K D0000-DFFFFH
1	64KB of ROM at 896K E0000-EFFFFH
0	64KB of ROM at 960K F0000-FFFFFH (BIOS)

Bit 3:0 enable substitution of the BIOS RAM located below 1MB with RAM at the same location in 64KB blocks. This should be done after the BIOS code is copied from the ROM and the RAM locations have been write protected using bits 7:4.

Value	Semantics
0	Disabled
1	Enabled

The default values are 0001 for these 4 bits. (Only BIOS ROM at 960K is enabled.)

Sequence of turning on the shadow RAM for BIOS ROM:

1. Enable the ROM space in register 09H. Make the RAM read/write-able. (The default states).
2. Turn on the corresponding memory enable bit in register 0FH.
3. Read the contents of ROM into a temporary register inside the CPU.
4. Write data from temporary register into memory. (Since a memory write cycle will not generate $\overline{\text{ROMCS}}$, the data will be stored in DRAM.)
5. Go back to step 2/3 until all data are transferred from ROM into DRAM. Then program register 09H to disable the ROM and make the DRAM read only.

Index	Definition (continued)

Sequence of turning on the shadow RAM for EGA ROM:

1. Enable the ROM space in register 09H. Make the RAM read/write-able. (The default states.)
2. Disable the DRAM from address 768K to 832K. (register 0EH bits 7-4).
3. Read the contents of ROM into a temporary register inside the CPU.
4. Turn on the corresponding memory enable bit register 0EH.
5. Write data from temporary register into memory. (Since the memory enable bits in register 0EH are turned on, the memory write cycles will go to the local memory system instead of the EGA memory.)
6. Go back to step 2 until all data are transferred from ROM into DRAM. Then program register 09H to disable the ROM and to make the DRAM read only.

2AH — Memory Enable Map 0K 000000-03FFFH (256K Resolution)

Bits	Field Definition
0	Enable the lowest 256K block.

Value	Semantics
0	Lowest 256K memory is disabled on local memory bus ($\overline{AF32}$ is 1).
1	Lowest 256K is enabled on local memory bus ($\overline{AF32}$ is 0). Default.

0AH — Memory Enable Map 256K 040000-05FFFFH (16K Resolution)
0BH — Memory Enable Map 384K 060000-07FFFFH
0CH — Memory Enable Map 512K..080000-09FFFFH
0DH — Memory Enable Map 640K..0A0000-0BFFFFH
0EH — Memory Enable Map 768K 0C0000-0DFFFFH
0FH — Memory Enable Map 896K 0E0000-0FFFFFH (16K Resolution)

Bits	Field Definition
7:0	Enable 16K block. Bit 0 enables the lowest, bit 7 the highest 16K block. For Example, register 0FH, bit 7 will control the 16KB block from 1008K to 1024K. This permits 16K blocks (between 256K and 1M) of memory to be disabled allowing ROMs, memory expansion schemes (EMS, EEMS or XMA) or memory mapped IO devices to reside within the lower 1MB address space.

Index	Definition (continued)

Bits Field Definition

Value	Semantics
0	Address is on or controlled by the system board.
1	Address is on the IO channel.

For those 48 bits, there will be no default values at reset. Before moving the Small Memory limitation (bit 1 of register 08H), these bits should be set properly according to a particular system configuration by POST/BIOS.

INDEX	7	6	5	4	3	2	1	0
10H	TYPE		START ADDRESS					
11H	TIMING							
12H	TYPE		START ADDRESS					
13H	TIMING							
14H	TYPE		START ADDRESS					
15H	TIMING							
16H	TYPE		START ADDRESS					
17H	TIMING							

Figure 5.3. DRAM Configuration/Timing Register Summary

DRAM Array Configuration and Timing

Index	Definition
10H	Block 0 Type/Start Address/Banks Exist
12H	Block 1 Type/Start Address/Banks Exist
14H	Block 2 Type/Start Address/Banks Exist
16H	Block 3 Type/Start Address/Banks Exist

Except register 10H (with a default starting address at 00000000H), the starting address of these registers are not initialized after power-up. The device type of register 10H will be defaulted to 256K DRAM, and registers 12H, 14H, 16H will be disabled. The POST/BIOS should use DRAM configuration data stored in the CMOS RAM in the RTC to set the correct values.

Bits Field definition

7:6 DRAM Type

Value	Semantics
0	none or bank disabled
1	256K x 1 or 256K x 4
2	1M x 1 or 1M x 4
3	Reserved

Index		Definition (continued)
	5:2	Starting address 25:22 the DRAM type determines which address bits are valid in the address recognition process.

Type	Address bits compared
none	none
256K	25:22 (4MB per block)
1M	25:24 (16MB per block)

	1:0	Number of banks populated in the block

Value	Semantics
0	1 bank exists (bank 0)
1	2 banks exist (banks 0 & 1)
2	3 banks exist (banks 0, 1, 2)
3	4 banks exist (banks 0, 1, 2, 3)

11H	Block 0 Timing
13H	Block 1 Timing
15H	Block 2 Timing
17H	Block 3 Timing

Bits	Field Definition
7:6	DRAM wait state The total number of DRAM access time will be 2 plus the number of wait states (in SCLK cycles).

Value	Semantics
0	2 Wait states
1	3 Wait states
2	4 Wait states. Default.
3	Not Used

5	Reserved.
4:3	$\overline{\text{RAS}}$ precharge time

Value	Semantics
0	2 CLK2 cycles. (min)
1	3 CLK2 cycles. (min)
2	4 CLK2 cycles. (min)
3	5 CLK2 cycles. Default. (min)

2:1	$\overline{\text{RAS}}$ pulse width during refresh (Register 11 only)

Value	Semantics
0	4 CLK2
1	4 CLK2
2	5 CLK2
3	6 CLK2 (default)

0	Reserved.

Note: bits 2:0 are reserved in Register 13, 15, and 17.

INDEX	7	6	5	4	3	2	1	0	
20H	CE	EC	EF	SR	CR	FH	1W	——	CACHE CONTROL
21H	DA	T8	S2	S1	S0	V1	V0	LU	TAG RAM CONTROL
22H	DIRECTORY ADDRESS POINTER								
23H	——								(RESERVED BY CHIPS)
24H	——	OE	CM	SAD4 THRU SAD0					SRAM DIRECT ADDRESS
25H	EP	CE	——				PADDR		
26H	PARITY ERROR ADDRESS								

Figure 5.4. Diagnostic Access Register Summary

Diagnostic Access

Index	Definition
20H	Cache Control

Bits — Field Definition

7 — Cache Enable

Value	Semantics
0	Disable Cache access. Default
1	Enable Cache access

6 — EDC Mode Enable

Value	Semantics
0	Disable EDC mode. Default
1	Enable EDC mode.

5 — Enable Freeze cache directory.

Value	Semantics
0	Normal cache operation. Default.
1	Freeze cache directory. A cache read miss will not cause a tag RAM update and change of data in cache data RAM. Instead a normal DRAM read operation will be performed. A cache write hit will update the cache data RAM.

Index	Definition (continued)

20H Cache Control

Bits	Field Definition

4 Enable Direct SRAM access

Value	Semantics
0	Normal cache operation. Default
1	Access SRAM directly. For 16 KB cache, Set 0 at 00000-01FFFH, Set 1 at 02000-03FFFH, Plus the offset value specified by register REG24<4:0>. Only the first 16KB block of the 32KB space is used. Any access to the second 16KB block will result in DRAM cycles. For 32KB cache, Set 0 at 00000-03FFH Set 1 at 04000-07FFH, Plus the offset value specified by register REG24<4:0>.

3 Classical Refresh

Value	Semantics
0	Enable the classic refresh mode. A DRAM refresh cycle will be performed as soon as there is no other request to DRAM pending. In this mode, the $\overline{REF}$ input should be connected to the Refresh-Request output from the timer circuit.
1	AT-type refresh scheme is used in the system (with CPU being in HOLD state). Default.

2 Flush cache directory.

Value	Semantics
0	Enable cache directory flush. When this bit is enabled, any access to cache directory RAM will cause the particular valid field (of both sets) pointed to by the index address field to become invalid.
1	Normal cache operation. Default.

1 One Wait state for cache memory non-pipelined accesses

Value	Semantics
0	One wait state SRAM access for non-pipelined cycles. Default (To force the 80386 cpu into the pipeline mode).
1	Zero wait states for non-pipelined cycles. For pipelined cycles, it is always zero wait states.

0 IOCHRDY delay

Value	Semantics
0	No delay
1	CLK2 delay. Default.

Index	Definition

21H Directory RAM control

Bits	Field Definition

7 Enable Directory Access.

Value	Semantics
0	Disable. Default.
1	Enable Cache directory to be accessed through 8 bit peripheral data bus.

6 T8—Highest pointer bit to directory RAM.

Value	Semantics
0	The 1st 256 entries of directory RAM.
1	The 2nd 256 entries of directory RAM.

5 S2—Bit 2 of pointer to tag field.
4 S1—Bit 1 of pointer to tag field.
3 S0—Bit 0 of pointer to tag field.

Value	Semantics
000	Disable access to tag field. Default.
100	Enable access to the high byte of tag field, set 0.
101	Enable access to the low byte of tag field, set 0.
110	Enable access to the high byte of tag field, set 1.
111	Enable access to the low byte of tag field, set 1. The 13-bit tag field is divided into two bytes. The high byte consists of A25—A21 (5 bits only), and the low byte consists of A20—A13.

2 V1—Enable access to Valid field of set 1.

Value	Semantics
0	Disable access to Valid field of set 1. Default.
1	Enable access to Valid field of set 1. The highest data bit (XD7) corresponds to the line of A<04:02> = 111.

1 V0—Enable access to Valid field of set 0.

Value	Semantics
0	Disable access to Valid field of set 0. Default.
1	Enable access to Valid field of set 0.

0 LU—Enable access to LRU field.

Value	Semantics
0	Disable access to LRU field. Default.
1	Enable access to LRU field. To access the LRU field, use XD0 bit. XD7 through XD1 will be unspecified.

Index	Definition
22H	Low Bits of Directory Address pointer. Together with REG21 <6>, they form a 9-bit address for 512 entries.
Bits	Field Definition
7:0	Low order address bits for on-chip directory RAM.
23H	Reserved. Used as a reference location to directory RAM itself. In order to access the cache directory, following IO23 cycle sequences should be used (each IO23 cycle will be proceeded by an IO22 write cycle to load the correct index): 1. Program register 21H bit 7 to 1. Also setup proper selection for other bits in register 21H. 2. Load register 22H with the intended line number. 3. Then the following IO write to register 23H will load the value into the directory RAM, or the IO read from register 23H will read the contents of the directory RAM.
24H	SRAM configuration and direct access address.
Bits	Field Definition
7	Not used.
6	SRAM Output Enable control. Value: 0 — Semantics: Both $\overline{CRD0}$ and $\overline{CRD1}$ will function as Output Enables for SRAM's. Default. Value: 1 — Semantics: Both $\overline{CRD0}$ and $\overline{CRD1}$ will function as Chip Selects for SRAM's. This is necessary for SRAM's without dedicated Output Enable pin.
5	Cache Memory configuration bit. Value: 0 — Semantics: To support 16KB cache data RAM. Default. Value: 1 — Semantics: To support 32KB cache data RAM.
4:0	The highest 5 address bits for SRAM direct access. This 5 address bits specify a 32KB block in the first 1MB memory space for direct SRAM access. If bit 4 of CREG20 is 1, then all the memory cycles to these 32KB block will access SRAM instead of DRAM. $\overline{RAS}$ and $\overline{CAS}$ will not be issued. The same number of wait states in non-pipelined mode as specified by CREG20 <1> will be used.
25H	Reserved.
26H	Reserved.
27H	Reserved.

Index	Definition

28H Error Source/Address (MSBs)

Bits	Field Definition
7	Parity check enable

Value	Semantics
0	Enabled.
1	Disabled. Default.

Bits	Field Definition
6	Cache Operation Error, both sets matched current tag address

Value	Semantics
0	No error.
1	Cache error No default value will be determined for this bit. The POST should clear this bit before enabling the cache.

Bits	Field Definition
5:2	Not used, returns unpredictable value.
1:0	Error address bits A25:24

29H Error Address (LSBs)

Bits	Field Definition
7:0	Error address bits A23:16

CREG30H-CREG38H: Non-Cacheable Memory Control Registers

These registers allow system designer to set aside up to 4 blocks of variable size of main memory as non-cacheable, which can be used in systems that have memory-mapped I/O or have multiple masters access dual-ported memory via different busses.

Index	Definition

Bits	Field definition
30H	Non-Cacheable memory of block 0, address bits 23-16.
7:0	Address bits 23-16 of non-cacheable memory block 0.
31H	Non-Cacheable memory of block 0, address bits 15-12/Size.
7:4	Address bits 15-12 of non-cacheable memory of block 0.
3:0	Size of the non-cacheable memory of block 0.

Value	Semantics
0000	Disabled. Default.
0001	4KB memory is non-cacheable.

Index		Definition (Continued)

	0010	8KB memory is non-cacheable.
	0011	16KB memory is non-cacheable.
	0100	32KB memory is non-cacheable.
	0101	64KB memory is non-cacheable.
	0110	128KB memory is non-cacheable.
	0111	256KB memory is non-cacheable.
	1000	512KB memory is non-cacheable.
	1001	1024KB memory is non-cacheable.
	1010	2M memory is non-cacheable.
	1011	4M memory is non-cacheable.
	11XX	Reserved.

For example, in a system with 2MB of memory, if memory at 1024K-1028K (00100000-00100FFFH) need to be specified as non-cacheable, CREG30 and CREG31 need to be loaded with 10H and 01H respectively.

32H — Non-Cacheable memory of block 1, address bits 23-16.

Bits	Field definition
7:0	Address bits 23-16 of non-cacheable memory of block 1.

33H — Non-Cacheable memory of block 1, address bits 15-12/Size.

Bits	Field definition
7:4	Address bits 15-12 of non-cacheable memory of block 1.
3:0	Size of the non-cacheable memory of block 1.

Value	Semantics
0000	Disabled. Default.
0001	4KB memory is non-cacheable.
0010	8KB memory is non-cacheable.
0011	16KB memory is non-cacheable.
0100	32KB memory is non-cacheable.
0101	64KB memory is non-cacheable.
0110	128KB memory is non-cacheable.
0111	256KB memory is non-cacheable.
1000	512KB memory is non-cacheable.
1001	1024KB memory is non-cacheable.
1010	2M memory is non-cacheable.
1011	4M memory is non-cacheable.
11XX	Reserved.

34H — Non-Cacheable memory block 2 address bits 23-16.

Bits	Field definition
7:0	Address bits 23-16 of non-cacheable memory block 2.

35H — Non-Cacheable memory of block 2, address bits 15-12/Size.

Bits	Field definition
7:4	Address bits 15-12 of the non-cacheable memory of block 2.
3:0	Size of the non-cacheable memory of block 2.

Value	Semantics
0000	Disabled. Default.

Index		Definition (Continued)	
		0001	4KB memory is non-cacheable.
		0010	8KB memory is non-cacheable.
		0011	16KB memory is non-cacheable.
		0100	32KB memory is non-cacheable.
		0101	64KB memory is non-cacheable.
		0110	128KB memory is non-cacheable.
		0111	256KB memory is non-cacheable.
		1000	512KB memory is non-cacheable.
		1001	1024KB memory is non-cacheable.
		1010	2M memory is non-cacheable.
		1011	4M memory is non-cacheable.
		11XX	Reserved.
36H		Non-Cacheable memory of block 3, address bits 23-16.	
	7:0	Address bit 23-16 of non-cacheable memory block 3.	
	Bits	Field definition	
37H		Non-Cacheable memory of block 3, address bits 15-12/Size.	
	7:4	Address bits 15-12 of the non-cacheable memory of block 3.	
	3:0	Size of the non-cacheable memory of block 3.	
		Value	Semantics
		0000	Disabled. Default.
		0001	4KB memory is non-cacheable.
		0010	8KB memory is non-cacheable.
		0011	16KB memory is non-cacheable.
		0100	32KB memory is non-cacheable.
		0101	64KB memory is non-cacheable.
		0110	128KB memory is non-cacheable.
		0111	256KB memory is non-cacheable.
		1000	512KB memory is non-cacheable.
		1001	1024KB memory is non-cacheable.
		1010	2M memory is non-cacheable.
		1011	4M memory is non-cacheable.
		11XX	Reserved.
38H		Non-Cacheable address bits 25 and 24.	
	7:6	Non-Cacheable address bits 25 and 24 of block 3.	
	5:4	Non-Cacheable address bits 25 and 24 of block 2.	
	3:2	Non-Cacheable address bits 25 and 24 of block 1.	
	1:0	Non-Cacheable address bit 25 and 24 of block 0.	

Configuration Process

1. Determine DRAM type for each bank and block.
2. Look for mixed types.
3. Determine DRAM speed for each bank and block. Set speed for slowest devices in each block.
4. Determine optimum configuration. The largest DRAM types should go at the lowest address.
5. Set starting address, timing and types.
6. Report memory size to low memory.

EDC SUPPORT

DESCRIPTION

Error-Detection-Correction can be performed on the DRAMs in an 82C307 based cache memory system by adding a small amount of additional logic. An external off-the-shelf EDC chip such as the 74ALS632 and an external section of control logic implemented by the system designer referred to as the EDC control logic or EDCC are used in conjunction with 82C307 to complete the memory subsystem.

Features

82C307 can be configured into EDS control mode which enables special EDC support logic and functions:

— Simple handshake interface allows external logic to control off-the-shelf EDC chips.
— External wait input provided to insert delays during error checking or check bit generation.

External logic must be implemented by the system designer to:

— Control the sequencing of read-modify-writes for partial writes to the DRAMs and the EDC chip. This includes modification of the operation of $\overline{CAS}$ and $\overline{WE}$ to the DRAM array as well as control of the data buffers and EDC latches with respect to byte enables.
— Generate addition wait delays to be inserted in the $\overline{CAS}$ pulse during reads and the $\overline{RAS}$ to $\overline{CAS}$ delay period during writes.
— Additional wait states can be inserted by holding the signal IOCHRDY low until proper setup/hold time is satisfied for DRAM array during DMA cycles.

Additional logic/changes required:

- Memory data buffers must have byte control of output enables.
- EDC sequence state machine for cache read miss cycles and write cycles.
- EDC sequence state machine for CPU to DRAM direct accesses. This could be a subset of the cache system.
- EDC control and state machine for DMA accesses.

EDC Controller (EDCC) Logic

Additional optional features can be implemented as required by the system designer. These could include:

1. Capability to enable error interrupts on single errors for memory diagnostic purposes.
2. Ability to verify functionality of the EDC chip by placing it in diagnostic mode.
3. Ability to correct the single bit error in DRAM subsystem after a read cycle error has been detected.
4. Capability to do the scrubbing.
5. Others.

Cache Controller/ EDC/EDCC Interface

74ALS632 EDC Interface

The following 74ALS632 signals must be controlled/monitored by EDCC.

#Pins	Name	Dir	Description
1	MERR	O	Double bit error.
1	ERR	O	Single or double bit error
4	OEB<3:1>	I	Output enable of EDC data buffer
1	OECB	I	Output enable of EDC check bit buffer
2	S<1:0>	I	Function select to EDC
1	LEDB0	I	Latch enable of EDC data buffer

The four encoded select states S<1:0> for the 74ALS632 are:

Value	Semantics
00	Generate check bits
01	Diagnostic Mode
10	Read and check data
11	Latch input

Besides controlling 74ALS632, the EDCC also has to control/modify some of the signals to change the timing and/or direction of data buffers. Following is the proposed pin list for EDCC:

#Pins	Name	Dir	Description
4	LBE<3:0>	I	Latched byte enables.
4	DBE<3:0>	O	Memory data buffer controls by byte.
4	XCNTL	O	Signals to modify some of DRAM's and buffer control signals. These signals include CAS, WE for DRAM's and DRD, MBEN for data buffers.
10	STATUS	I	Status signals from 82C307 and system to indicate what kind of memory access is active. The cycles are DMA read/write, CPU to DRAM direct access, or Cache memory move-in. The signals include, SYSCLK (or CLK2), AF32, PEN, CAS, DWE, WDLE, MDEN, HLDA1, XMEMR, XMEMW. There may be other signals needed for diagnostics and other functions desired by a particular system design.

82C307 Interface

The following pin is added to the 82C307 to allow external generation of addition delays at specified points in a DRAM cycle. It can also be used for requirements other than EDC.

#Pins	Name	Dir	Description
1	WAIT	I	Causes additional CLK2 period delays to be inserted while WAIT is asserted. WAIT is synchronously sampled at during the CAS pulse to allow extension of RAS, CAS and DWE (if asserted). The required setup and hold times must be met to guarantee proper operation.

The following pins on the 82C307 are normally used to control parity generation and checking and are redefined in EDC mode to interface with the 74ALS632 and EDCC.

#Pins	Name	Dir	Description
1	LPAR	I	Active LO. Causes the address of the last memory access to be latched after an error has been detected. It should be connected to ERR of the 74ALS632 which is asserted when single and double bit errors are detected. Normally used to latch the address a memory access after a parity error has been detected.
1	PEN	O	Active LO. A one SCLK long pulse indicating the start of a cache controller initiated DRAM access (either a cache read miss case or direct DRAM access).

Memory control signals generated by the CS8231 components that must be connected to the EDC or EDC Controller include:

#Pins	Name	Dir	Description
4	LBE<3:0>	I	Indicates which bytes are to be written during a CPU or DMA initiated DRAM access. Sourced by the 82A306.
1	CAS	I	Must be intercepted to modify the timing of write operations. Sourced by the 83C312.
1	DWE	I	Must be intercepted to modify the timing of write operations. Sourced by the 82C307.
1	DRD	I	Indicates the direction of transfer between the 82B305's and DRAM's. This signal must be intercepted to allow buffers between 82B305's and DRAM to change direction for Read-Modify-Write operations during memory write cycles. Sourced by the 82C307.
1	DEN	I	Enables data buffers located between the 82B305's and DRAM's. Sourced by the 82C307.
1	WDLE	I	Write-Data-Latch-Enable. This signal should be used to latch LBE<3:1> to generate DBE<3:1> so that the full 32-bit data can be merged between 74F373 and 74ALS632. Sourced by the 82C307.

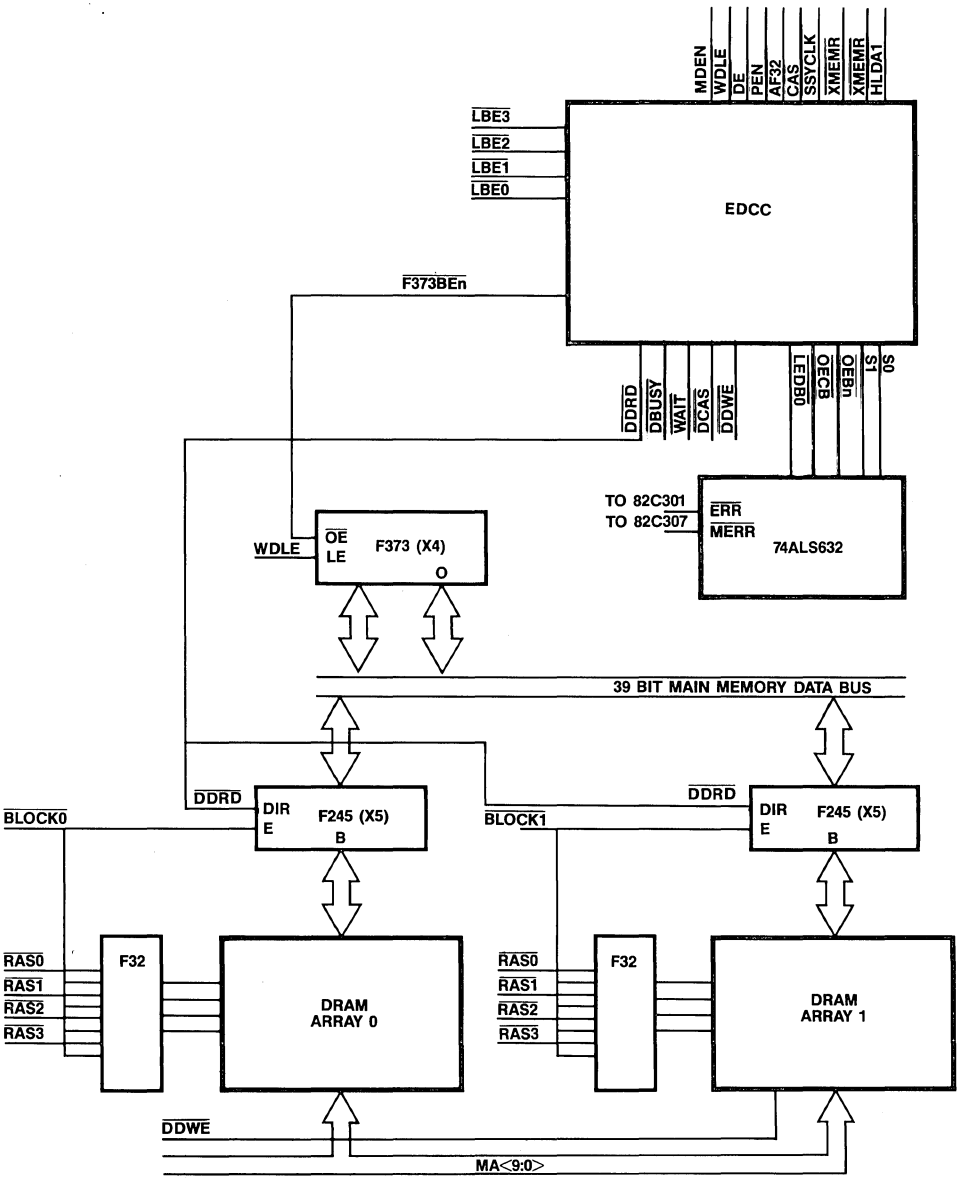


Figure A.1. EDC Implementation with the 82C307

Memory Operations with EDC

Each different type of DRAM cycle must be individually examined with regards to EDC.

Cache Move-in

A cache move-in is composed if a data transfer of one double word in a cache read miss situation. After the data has been latched inside the 74ALS632, the DRAM output buffer will be turned off and the MD bus will be driven by the 74ALS632. Additional wait states are needed to allow enough time for the error checking and correction in the EDC chip.

If single bit error is detected during this move-in cycle, the error will be corrected and good data will be transferred to the local data bus. The error address can be latched inside the 82C307 for later examination. If double bit error occurs, 82C301 should generate a NMI to the processor to stop any further processing. The error address can be also latched inside 82C307. However since there is only one level of latches in 82C307, it will store the first error occurrence.

Writing Main Memory

During writing to the DRAM's, read-modify-write operation is necessary if a partial write (not all 4 bytes to be written) is initiated by the processor.

DMA Write

The DMA or alternate bus master transfers present special problems to an EDC implementation since they can write directly to DRAM. If 8, 16, or 24 bit writes occur, a partial write operation must be performed, with a read-modify-write cycle. Since DRAM's with common input and output pins (SIMMs or x1 parts with an externally connected input and output data line) cannot do a late write operation necessary for a single $\overline{CAS}$ read-modify-write, two $\overline{CAS}$ pulses must be formed from the single $\overline{CAS}$ pulse that the 82C307 will generate. This can easily be done by gating $\overline{CAS}$ at the drivers. This reduces the insertion of several additional levels of logic in a critical timing path.

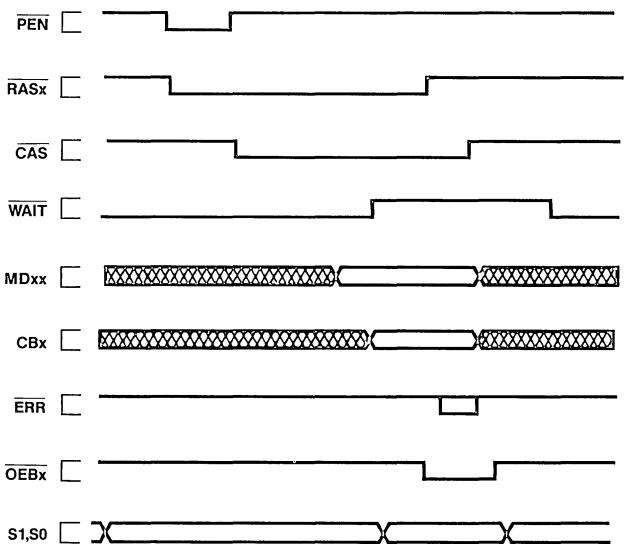


Figure A.2. Sequence of Read Data from DRAM to CPU/Cache

During the first generated $\overline{CAS}$ a read is performed on all 32 bits by asserting $\overline{FBE}$ (force byte enables) to the A306. The 305's output buffers can be disabled by deasserting $\overline{MDEN}$ to allow the DRAM to output read data. After the appropriate $\overline{CAS}$ access time, the data is latched in the input latches by changing S1,S0 to from 2H (read and flag) to 3H (latch input, read and correction). Corrected data is then merged with the new bytes as controlled by the inverse of $\overline{LBE}$<3:0> and changing S1,S0 to 0H (modify/write). The new data and check bits are then written into the DRAM with another $\overline{CAS}$ cycle with $\overline{WE}$ asserted.

Because of the additional $\overline{CAS}$ cycle required the $\overline{XMEMW}$ strobe must be extended by making IOCHRDY inactive.

DMA Read

A normal read and correct cycle can be performed since DRAM will always be accessed regardless of cache hit or miss. Some additional logic would be required to perform the correction only if an error was detected.

$\overline{CAS}$ is asserted after $\overline{RAS}$ causing read data to be sourced by the DRAM. S1,S0 should be set to 2H causing the data word to be input to the 74ALS632 and checked. After the appropriate 74ALS632 data setup time, S1,S0 should be changed from 2H to 3H latching the data and correcting any errors. $\overline{CAS}$ to the DRAM array should be gated off at the CAS drivers disabling the DRAM output buffers. The corrected data can then be enabled onto the MD lines by asserting $\overline{OBEx}$.

DMA read operations should be extended to allow enough time for error checking and correction. This can be done by holding IOCHRDY inactive.

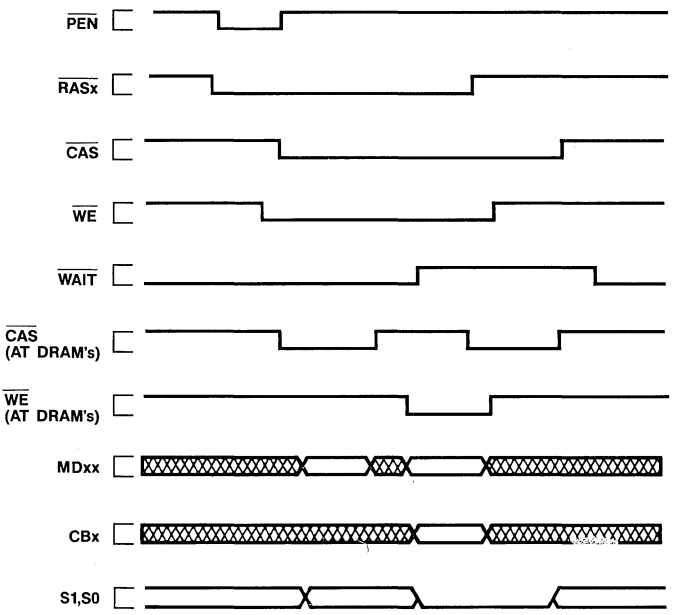


Figure A.3. DRAM Write with Read-Modify-Write Sequence

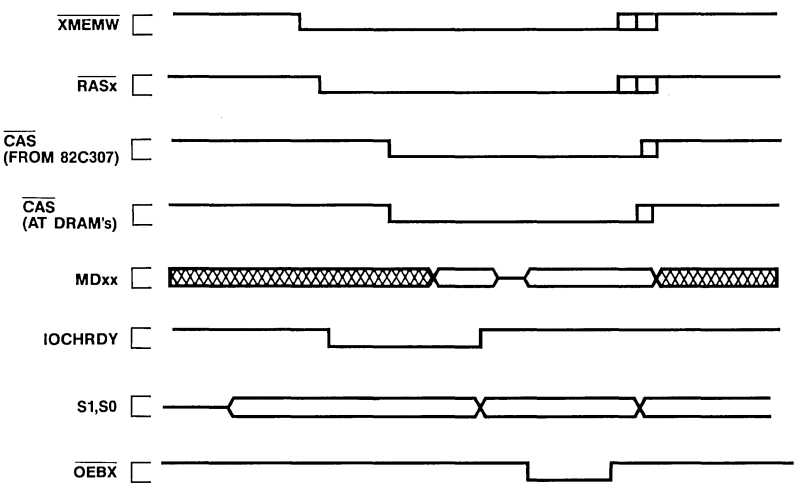


Figure A.4. DMA Read Sequence

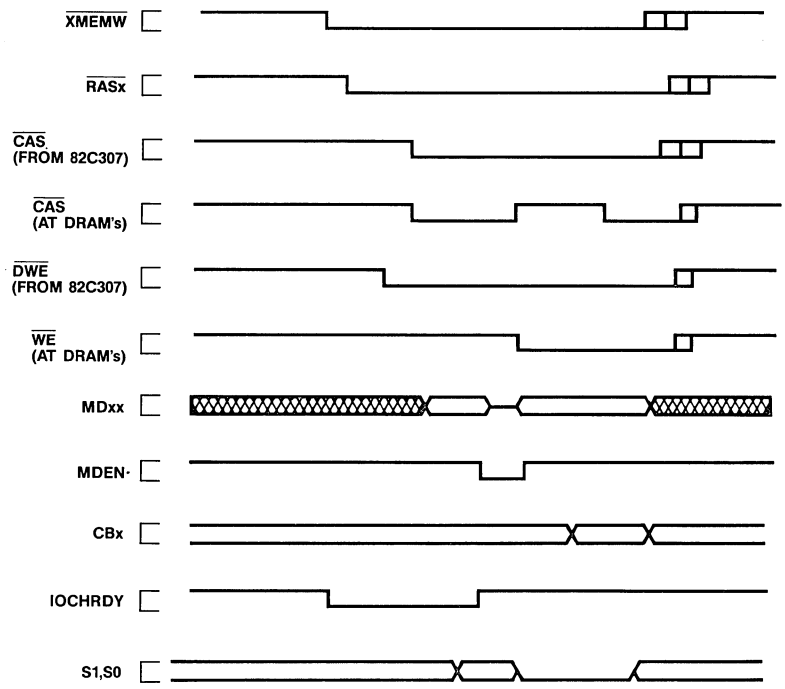


Figure A.5. DMA Write Sequence

Other Considerations

There are additional design considerations that must be taken into account in implementing a workable and testable EDC design. These relate primarily to initialization of the array and some mechanism for removing single bit errors.

Direct CPU Access to DRAM

The 82C307 supports direct CPU access to DRAM (cache disabled) for diagnostic and test purposes. In this mode, EDCC could operates as the same as regular cache read miss or write operation since only one RAS cycle and CAS cycle are needed.

However, write cycles require different consideration if additional performance is to be achieved for partial writes and full 32-bit writes. EDCC should perform read-modify-write cycles for partial writes and it can perform straight check bit generation for 32-bit writes without reading the contents of DRAM first.

Diagnostic Mode of 74ALS632

The EDC chip 74ALS632 can be put into a diagnostic mode by making the status inputs S1,S0 = 01. To support this diagnostic function, the EDCC design can provide this feature. Also to access to the check bits, the 7-bit check bus can be connected to the XD bus in a PC-AT environment through a 74LS245 transceiver.

Memory Data Initialization

A mechanism must be provided to allow for rapid initialization of the memory data and check bits during the POST. This must be performed to prevent any read-modify-writes from detecting false errors when the check bits have not been initialized.

Check Bit Initialization

It would be highly desirable to allow for initialization of the check bits only assuming that the actual data in the array is correct. This would occur if EDC had been disabled for a period during which writes occur. A mode must be provided where CPU read accesses cause read-modify-writes to be performed setting the check bits correctly.

Single Bit Scrubbing

In normal operation, a memory with EDC will correct single bit errors transparently to the system. If these are soft or transient errors a subsequent access will return the correct data without need for correction. However, if the wrong bit value is stored in a DRAM cell (a hard error), correction must be performed on reads. In addition to the obvious performance degradation, there now exists the possibility of a double bit error occurring that cannot be corrected and will cause the system to fail.

For these reasons, most EDC memory systems implement a background function called scrubbing that periodically reads all memory locations and writes them back. If any single bit errors are detected, they will be corrected and written back. The best time to perform the scrubbing function would be during refresh at an approximate rate of 64K words/second (one word every 15 microseconds).

The system designer can use the input DBUSY of 82C307 for background scrubbing function. If this signal is active, no DRAM cycle will be initiated by 82C307.

Performance impact

The addition of EDC to a memory system almost always introduces a performance penalty. The magnitude of the penalty depends largely on method in which EDC is implemented, the frequency of errors and in a cache system, the frequency of DRAM accesses (assuming EDC is only performed on the RAM). For the 82C307 cache based memory system the following conclusions can be made about performance.

Memory Read Cycle

During a cache hit cycle, no DRAM cycle will be necessary. Therefore, no ERROR check is needed. If a cache miss happens, a DRAM read cycle will start. Additional wait states will be inserted to allow error-checking/correction. This delay is unavoidable even if no error is present in the memory system. Since correction will only occur during cache miss the correction penalty will be further reduced by the miss ratio.

If scrubbing is implemented, hard errors (uncorrected data remaining in RAM cells) would be eventually eliminated and should not affect performance. Single hard failures (device failures such as bad cells or stuck-at outputs in DRAMs or bus driver failures) would be corrected as they occurred and would impact performance.

Memory Write Cycle

Regardless of cache hit or miss, write operation always starts DRAM cycle. For the first write cycle, data will be latched into a buffer and the CPU can be released immediately without wait state. As the result, unless another write cycle or a read miss cycle occurs, no additional performance penalty will be induced.

82C307 Clock and Control Signals

PFP	Symbol	Type	Description
55	CLK2	I	CLK2 provides the fundamental timing for the 82C307 state machine. It is derived from the 82C301 CLK2 output. The 82C307 internally divides the CLK2 by two to generate SCLK. The normal frequency ranges from 25 to 50 MHz.
53	SCLK	O	SCLK is derived by dividing the CLK2 by two and is used internally to establish the phase indication. It is low during phase 1 and high during phase 2. The SCLK is internally synchronized on the falling edge of reset4. It is in sync with the SYSCCLK output of the 82C301.
52	RESET4	I	Reset4 is an active high input that initializes the internal state machine to the idle state. Following reset, the cache tag directory contains no valid information. It is the responsibility of the system initialization software to invalidate the entire cache contents before enabling memory caching. The falling edge of reset is used to synchronize the phase of the internal clock.
63	$\overline{REF}$	I	Active Low. DRAM refresh control signal.

CPU Status Interface

PFP	Symbol	Type	Description
45	$\overline{ADS}$	I	Address Strobe is an active low input which connects directly to the $\overline{ADS}$ output of the 80386. When activated, it signals the start of a new cycle and validates the address and the status information being presented on the processor status and address lines.
46	W/$\overline{R}$	I	Write/$\overline{Read}$ is an input which connects directly to the W/$\overline{R}$ output of the 80386. When high, it indicates that the current cycle is a write cycle. When low, it indicates a read cycle.
47	D/$\overline{C}$	I	Data/Code is an input that connects directly to the 80386 D/$\overline{C}$ output. When high, it indicates a data cycle, and when low it indicates a control cycle.
48	M/$\overline{IO}$	I	Memory/$\overline{IO}$ is an input from the 80386, which when high it indicates a memory cycle and when low it indicates a I/O cycle.

Address

PFP	Symbol	Type	Description
10-13 15-17 19-28 30-40 42-43	A<31:28> A<27:25> A<24:15> A<14:04> A<03:02>	I	Address input lines A<31:2> from the CPU local bus. The 82C307 connects directly to the 80386 address outputs. While it monitors all 30 bits, it uses only 26 bits for for tag directory comparison to determine if the requested data resides in the cache.
62	XA00	I	Address input from the X bus. This signal in conjunction with IO2XC is used to differentiate between accesses to port 22 and port 23.
9	MENB	I	Memory enable is an active low input, which when active validated the addresses on the local bus. This input can be used to disable the 82C307 from responding to pre-defined address locations via external decode. When high, the 82C307 does not generate the AF32 output or activate the cache control signals.

CPU/BUS Controller Interface

PFP	Symbol	Type	Description
50	READY	I/O	This is a bi-directional signal. It is an active low output during cache and memory accesses to terminate the current cycle. It is an input when the current cycle is an AT bus cycle (AF32 inactive).
56	AF32	O	This is an open drain active low output. If asserted, it indicates that the current access is to the local memory. It is high for all other cycles.
51	IOCHRDY	O	This is an active low open drain output. This is normally high. When low, it indicates that the current memory access or refresh cycle has not been completed and introduces wait-states to allow the current cycle to complete. A 1 KOhm pull up resistor is recommended.
49	NA	O	This is an active low output to the 80386. This signal controls the pipelining of the 80386. This is an open collector output and allows other circuits in the system to drive this line.

Cache Control Signals

PFP	Symbol	Type	Description
74,70	$\overline{\text{CWE}}$<1:0>	O	$\overline{\text{CWE0}}$ and $\overline{\text{CWE1}}$ are active low cache write enable signals and connect to the write enable inputs of the SRAMs. They either enable set 0 or set 1 to receive the write data from the 80386 data bus during read miss or a write hit cycle. The latched byte enables and $\overline{\text{FBE}}$ select the requested bytes within the double word.
73,71	$\overline{\text{CRD}}$<1:0>	O	$\overline{\text{CRD0}}$ and $\overline{\text{CRD1}}$ are active low cache read signals and connect to either the $\overline{\text{OE}}$ or the $\overline{\text{CS}}$ inputs of the SRAMs. During a read hit cycle, either $\overline{\text{CRD0}}$ or $\overline{\text{CRD1}}$ is enabled to drive the requested data on to the data bus. Only one bank is selected at any given time. When 82C307 is programmed in the Chip Select mode, $\overline{\text{CRD0}}$ and $\overline{\text{CRD1}}$ will become active during any cache memory accesses (read or write). In the output enable mode, $\overline{\text{CRD0}}$ or $\overline{\text{CRD1}}$ are active only during the read cycles.
75	CALE	O	Cache address latch enable. This signal is used to latch the SRAM addresses. This latch is not required when operating in the non-pipelined mode of operation. A 74F373 type transparent latch should be used to latch the SRAM addresses. When CALE is high, the latch is transparent and allows the 80386 addresses to flow through to the SRAMs. On the high to low transition of CALE, the addresses are latched. When CALE is low, the SRAM addresses are the latched version.

Expansion Channel Memory and I/O Interface

PFP	Symbol	Type	Description
60	$\overline{\text{XIOR}}$	I	This is an active low input connected to the $\overline{\text{XIOR}}$ output of the 82C301 bus controller. This input is used to qualify IO2XCS. $\overline{\text{XIOR}}$ is used in conjunction with the IO2XCS to direct the 82C307 to place the contents of the selected configuration registers on the data bus.
61	$\overline{\text{XIOW}}$	I	This is an active low input connected to the $\overline{\text{XIOW}}$ output of the 82C301. It is used to qualify IO2XCS. $\overline{\text{XIOW}}$ is used in conjunction with IO2XCS directs the selected configuration register on the 82C307 to accept the data being presented on the data bus.

Expansion Channel Memory and I/O Interface (Continued)

PFP	Symbol	Type	Description
58	$\overline{\text{XMEMR}}$	I	This is an active low input connected to the $\overline{\text{XMEMR}}$ output of the 82C301 bus controller. When active, it indicates that a DMA or an external bus master requires to read data from the memory.
59	$\overline{\text{XMEMW}}$	I	This is an active low input and is connected to the $\overline{\text{XMEMW}}$ output of the 82C301 bus controller. When active, an external bus master or a DMA device is requesting to write data to the memory.
64	HLDA1	I	Active high hold acknowledge input from the 82C301. When high, it indicates that the CPU has relinquished control of the system bus in response to a HOLD Request. When HLDA1 is active the cache directory contents are frozen. A cache hit or miss will not affect the cache directory. On write hit cycles, cache data will be updated to reflect the new data. This is to ensure that no I/O transfers corrupt the contents of the cache.

DRAM Interface

PFP	Symbol	Type	Description
87,88 90,91	$\overline{\text{RAS}}$<3:2> $\overline{\text{RAS}}$<1:0>	O	Row Address Strobes 3 to 0 are active low outputs. These outputs are used by DRAMs to latch the row address present on the MA<9:0> address lines. $\overline{\text{RAS3}}$ selects the highest bank. $\overline{\text{RAS0}}$ selects the lowest bank. These signals should be buffered and line terminated with 33 Ohms series resistor.
86	$\overline{\text{CAS}}$	O	Column Address Strobe is an active low output. This has to be externally gated with latched byte enables to generate individual $\overline{\text{CAS}}$ for each of the individual bytes. These decoded $\overline{\text{CAS}}$ signals are used by DRAMs to latch the column address information present on the MA<9:0> lines. These decoded signals should be line terminated with 33 Ohms series resistors.
85	$\overline{\text{DWE}}$	O	DRAM Write Enable is an active low write enable for the DRAMs. This line should be buffered and line terminated with 33 Ohms series resistors.

DRAM Interface (Continued)

PFP	Symbol	Type	Description
76	$\overline{FBE}$	O	Force Byte Enable is an active low signal. When active, forces all the byte enables to be active, during a read miss cycle, to ensure that all four bytes of data is fetched from main memory.
95-100 01-02	XDA<7:2> XDA<1:0>	I/O	Multiplexed DRAM address lines MA<7:0>. Also used as bi-directional lines to read/write to the internal registers of the 82C307. An external 74LS245 data transceiver is required to isolate this path during normal memory operation. These lines should be buffered and line terminated with 33 Ohms series resistors before driving the DRAM array.
93,94	MA<9:8>	O	Remaining DRAM address bits to provide a total of 10 address lines to support 256K and 1 Mbit DRAMs. These lines should be buffered and line terminated with 33 Ohms series resistor before driving the DRAM array.
3	$\overline{XDEN}$	O	X DATA BUFFER Enable is an active low output asserted during I/O accesses to locations 22H and 23H. These locations contain the index and configuration information for the 82C307 configuration registers. It is used to enable the buffers between the XD and the MA busses for accessing the internal registers on the 82C307.
82	WDLE	O	Write Data Latch Enable is an active high output used to latch the write data from the CPU into a temporary register for delayed write operation to the DRAM array.

Memory Expansion

PFP	Symbol	Type	Description
77,78 80,81	$\overline{BLK}$<3:2> $\overline{BLK}$<1:0>	O O	Block 3 to Block 0 are active low signals used to select up to 4 blocks of DRAMs. These signals should be gated with $\overline{RAS}$<3:0> to generate $\overline{RAS}$ signals for the individual banks. During refresh, all the blocks are enabled simultaneously.
8	$\overline{MDEN}$	O	Memory Data Enable is an active low signal, which when active enables the drivers between the memory data bus and the local data bus. This signal is connected to the $\overline{MDEN}$ input of the 82B305 data buffers to enable transfers between memory and the processor.
5	$\overline{DRD}$	O	Data Read controls the data transfer direction between the MD to the LD bus. When low, it allows data transfer from the memory data bus to the processor data bus. When high, it transfers data from the processor data bus to the memory data bus.

Decodes

PFP	Symbol	Type	Description
68	$\overline{\text{ROMCS}}$	O	ROM CHIP SELECT is an active low chip select output to the BIOS EPROMs. This output will be active when the top 256K of the 4 Gigabyte or 1 MB address space is accessed. ROM space at the top of 16 MB can be selectively programmed to be enabled or disabled.
66	$\overline{\text{IO2XCS}}$	I	This is an active low output and is activated during accesses to the I/O port addresses 22 and 23H.

Parity/EDC Support

PFP	Symbol	Type	Description
65	$\overline{\text{LPAR}}$	I	Parity error is an active low input indicating a parity error during DRAM read operation. If a system implements parity generation and detection scheme, this input should be connected to the $\overline{\text{LPAR}}$ output of the 82C306. The failing address is latched within the 82C307 for diagnostic purposes. If the system implements the error detection and correction scheme, then this input should be connected to the $\overline{\text{ERR}}$ output of the generically available 32-bit EDCU chips like the 74ALS632. When $\overline{\text{LPAR}}$ is asserted active, it indicates to the 74ALS632 that either a single or a double bit error has occurred.
6	$\overline{\text{PCHK}}$	O	Parity Check is an active low output which controls whether parity is generated or checked. When low, the parity check function is enabled, whereby the data is checked for parity errors. When high, parity generation logic is enabled, and parity bits are generated.
7	$\overline{\text{PEN}}$	O	Parity enable is an active low output that controls the overall parity enable circuitry. This bit is controlled by the configuration register. When in EDC mode, $\overline{\text{PEN}}$ indicates the beginning of the DRAM cycle by generating a pulse which is one CLK2 cycle long.
84	$\overline{\text{WAIT}}$	I	$\overline{\text{WAIT}}$ is an active low input, which when active causes additional CLK2 periods to be inserted while wait is sampled active. This permits stretching of the DRAM timing pulses when operating in the EDC mode. This input can also be used by other logic to extend the DRAM cycle. $\overline{\text{WAIT}}$ is sampled by the CLK2 pulse to allow extension of $\overline{\text{RAS}}$, $\overline{\text{RAS}}$ and $\overline{\text{DWE}}$ (if asserted). The required setup and hold times must be met to guarantee proper operation.
83	$\overline{\text{DBUSY}}$	I	DRAM BUSY is an active low input that indicates that the DRAM sub-system is busy and it cannot accept any new memory requests. However, this input does not affect cache accesses.

Test Pin

PFP	Symbol	Type	Description
44	TEST		A 10K Ohms pull up resistor is required.

Power and Ground

PFP	Symbol	Type	Description
4,18		Vss	
29,54		Vss	
72,79		Vss	
92		Vss	
14,41		Vcc	
67,89		Vcc	

Reserved Pin

PFP	Symbol	Type	Description
69,57			

82C307 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}		7.0	V
Input Voltage	V_I	-.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C307 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C307 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}			
TTL level (All pins except RESET4)			.8	V
SHMT level (RESET4 pin)			1.0	V
Input High Voltage	V_{1H}			
TTL level (All pins except RESET4 and CLK2)		2.0		V
CLK2 level		3.7		V
SHMT level (RESET4 pin)		4.0		V
Output Low Voltage	V_{OL}		.45	V
Output High Voltage All pins except IOCHRDY and NA pins IOCHRDY and NA pins have open drain driver	V_{OH}	2.4		V
Input LOW current @ $V_O = V_{SS}$ CLK2, RESET4, MDEN, XDA<7:0>, and MA<1:0>	I_{IL}	-10		μA
All input and I/O Pins except CLK2, RESET4, MDEN, XDA<7:0>, and MA<1:0>		-90	-10	μA
Input HIGH current @ $V_o = V_{dd}$ CLK2, RESET4, XDA<7:0>, MDEN, and MA<1:0>	I_{IH}		10	μA
All input and I/O pins except CLK2, RESET4, XDA<7:0>, MDEN, and MA<1:0>			40	μA
3-State output OFF current LOW	I_{OZL}		-10	μ2A
3-State output OFF current HIGH	I_{OZH}		10	μA
Output leakage current	I_{OH}		TBD	
Output short circuit current	I_{OS}		TBD	
Power supply current	I_{CC}		200	mA
Input capacitance	C_{IN}		TBD	
Output or I/O capacitance	C_{OUT}		TBD	

NOTES

1. MDEN, XDEN, DRD, PCHK, SCLK, ROMCS, and PEN pins have 4 mA TTL driver.
2. IOCHRDY and NA pins have 4 mA open drain driver.
3. READY, AF32, BLK<3:0>, RAS<3:0>, CAS, WDLE, CWE<1:0>, FBE, CALE, and DWE have 8 mA driver.
4. CRD<1:0> have 12 mA driver.
5. All timing parameters except t711A are specified under Capacitive load of 65 pF. Timing parameter t711A is specified under capacitive load of 35pF.

82C307 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C307-20 Min	Typ	Max	82C307-25 Min	Typ	Max	Unit	Notes
Memory Cycle									
t701	Operating frequency	8		20	8		25	MHz	
t702	CLK2 period	25			20			ns	
t703	CLK2 high time at 2V	8			8			ns	
t704	CLK2 high time at 3.7V	5			5			ns	
t705	CLK2 low time at 2V	7			7			ns	
t706	CLK2 low time at .8V	5			5			ns	
t707	CLK2 fall time (3.7V to .8V)			4			4	ns	
t708	CLK2 rise time (.8V to 3.7V)			4			4	ns	
t709	RESET4 hold time	3			3			ns	
t710	RESET4 setup time	7			7			ns	
t711A	$\overline{CRD}$<1:0> delay from CLK2 low for 0WS non-pipeline read hit cycles	4		12	4		11	ns	
t711B	$\overline{CRD}$<1:0> active delay from CLK2 low for all other cycles	8		24	8		22	ns	
t712	$\overline{CRD}$<1:0> active delay from CLK2 high	6		20	6		16	ns	
t713	$\overline{CRD}$<1:0> inactive delay from CLK2 high	6		20	7		20	ns	
t714	$\overline{READY}$ active delay from CLK2 low	6		20	6		20	ns	
t715	$\overline{READY}$ inactive delay from CLK2 high	6		20	6		18	ns	
t716	$\overline{CALE}$ high to low delay from CLK2 low	6		22	6		18	ns	
t717	$\overline{CALE}$ high to low delay from CLK2 high	10		22	10		18	ns	
t718	$\overline{CALE}$ low to high delay from CLK2 high	10		25	10		25	ns	
t719	$\overline{AF32}$ active delay from CLK2 low	6		20	6		16	ns	
t720	$\overline{AF32}$ inactive delay from CLK2 low	6		20	6		18	ns	
t721	$\overline{RAS}$ active delay from CLK2 low	10		21	10		21	ns	
t722	$\overline{RAS}$ active delay from CLK2 high	10		25	10		25	ns	

Test Load = 65pF unless otherwise specified.

82C307 AC Characteristics (Continued)

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C307-20 Min	Typ	Max	82C307-25 Min	Typ	Max	Unit	Notes
Memory Cycle (Continued)									
t723	$\overline{RAS}$ inactive delay from CLK2 high	10		25	10		25	ns	
t724	$\overline{RAS}$ inactive delay from CLK2 low	10		25	10		25	ns	
t725	Row address set up time from CPU address active			20			16	ns	
t726	Row address hold time from CLK2 low			28			25	ns	
t727	Column address valid to $\overline{CAS}$ active	6			4			ns	
t728	Column address hold time from CLK2 high	10		25	10		25	ns	
t729	$\overline{CAS}$ active delay from CLK2 low	9		21	9		21	ns	
t730	$\overline{CAS}$ active delay from CLK2 high	9		21	9		21	ns	
t731	$\overline{CAS}$ inactive delay from CLK2 high	6		17	6		17	ns	
t732	$\overline{DRD}$ active delay from CLK2 high	10		30	10		25	ns	
t733	$\overline{DRD}$ active delay from CLK2 low	10		30	10		25	ns	
t734	$\overline{DRD}$ inactive delay from CLK2 low	10		25	10		25	ns	
t735	$\overline{FBE}$ active delay from CLK2 low	10		20	10		20	ns	
t736	$\overline{FBE}$ active delay from CLK2 high	10		20	10		20	ns	
t737	$\overline{FBE}$ inactive delay from CLK2 low	8		18	8		18	ns	
t738	$\overline{CWE}$ active delay from CLK2 low	10		22	10		20	ns	
t739	$\overline{CWE}$ active delay from CLK2 high	10		22	10		20	ns	
t740	$\overline{CWE}$ inactive delay from CLK2 high	7		18	7		16	ns	
t741	$\overline{BLK}$ active delay from address valid			20			20	ns	

Test Load = 65pF unless otherwise specified.

82C307 AC Characteristics (Continued)

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C307-20 Min	Typ	Max	82C307-25 Min	Typ	Max	Unit	Notes
Memory Cycle (Continued)									
t742	$\overline{BLK}$ inactive delay from CLK2 high			20			20	ns	
t743	$\overline{DWE}$ active delay from CLK2 low	10		25	10		23	ns	
t744	$\overline{DWE}$ active delay from CLK2 high	5		20	5		18	ns	
t745	$\overline{MDEN}$ low to high delay from CLK2 high	10		20	10		20	ns	
t746	$\overline{MDEN}$ high to low delay from CLK2 high	10		25	10		25	ns	
t747	WDLE high to low delay from CLK2 high	10		20	10		20	ns	
t748	WDLE low to high delay from CLK2 high	6		15	6		15	ns	
t744	$\overline{DWE}$ active delay from CLK2 high	5		20	5		18	ns	
t745	$\overline{MDEN}$ low to high delay from CLK2 high	10		20	10		20	ns	
t746	$\overline{MDEN}$ high to low delay from CLK2 high	10		25	10		25	ns	
t747	WDLE high to low delay from CLK2 high	10		20	10		20	ns	
t748	WDLE low to high delay from CLK2 high	6		15	6		15	ns	
CPU DMA Cycle									
t749	Command setup time to CLK2 high	10			10			ns	
t750	$\overline{RAS}$ active delay from CLK2 high			20			20	ns	
t751	$\overline{RAS}$ inactive delay from commands inactive			25			25	ns	
t752	Row address setup time from address valid			20			20	ns	
t753	Row address hold time from CLK2 high	10		20	10		20	ns	
t754	Column address setup to $\overline{CAS}$ active		1 CLK2			1 CLK2		ns	

Test Load = 65pF unless otherwise specified.

82C307 AC Characteristics (Continued)

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C307-20 Min	82C307-20 Typ	82C307-20 Max	82C307-25 Min	82C307-25 Typ	82C307-25 Max	Unit	Notes
CPU DMA Cycle (Continued)									
t755	Column address hold time from commands active			25			25	ns	
t756	$\overline{CAS}$ active delay from $\overline{RAS}$ active for DMA memory read cycle		2 CLK2			2 CLK2		ns	
t757	$\overline{CAS}$ active delay from $\overline{RAS}$ active for DMA memory write cycle		3 CLK2			3 CLK2		ns	
t758	$\overline{CAS}$ active delay from CLK2 high	8		20	8		18	ns	
t759	$\overline{CAS}$ inactive delay from commands inactive	8		18	8		18	ns	
t760	IOCHRDY high to low delay from command active			15			15	ns	
t761	IOCHRDY low to high delay from CLK2 high			20			20	ns	
t762	$\overline{DRD}$ active delay from CLK2 high			20			20	ns	
t763	$\overline{DRD}$ inactive delay from commands inactive			25			25	ns	
t764	$\overline{AF32}$ active delay from command active			15			15	ns	
t765	$\overline{AF32}$ inactive delay from command inactive			13			13	ns	
t766	$\overline{DWE}$ active delay from $\overline{AF32}$ active			17			17	ns	
t767	$\overline{DWE}$ inactive delay from commands inactive			17			17	ns	
t768	$\overline{CRD}$ and $\overline{CWE}$ active delay from CLK2 high			20			20	ns	
t769	$\overline{CRD}$ and $\overline{CWE}$ inactive delay from CLK2 high	8		20	10		20	ns	
ROM Cycle									
t770	$\overline{ROMCS}$ active delay from CLK2 high			27			27	ns	
t771	$\overline{ROMCS}$ inactive delay from CLK2 high			22			22	ns	
t772	$\overline{READY}$ input setup time to CLK2 low	5			5			ns	
t773	$\overline{READY}$ input hold time to CLK2 high	3			3			ns	

Test Load = 65pF unless otherwise specified.

82C307 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

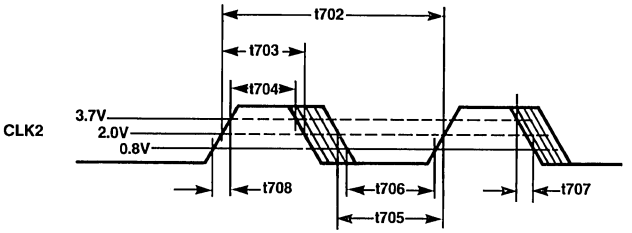
Sym	Description	82C307-20 Min	82C307-20 Typ	82C307-20 Max	82C307-25 Min	82C307-25 Typ	82C307-25 Max	Unit	Notes
REFRESH Cycle									
t774	$\overline{RASi}$ active delay from CLK2 high			20			17	ns	
t775	$\overline{RASi}$ inactive delay from CLK2 high	10			7			ns	
t776	$\overline{RASi}$ pulse width		4 CLK2			4 CLK2		ns	
t777	$\overline{RAS(i+1)}$ active delay from $\overline{RASi}$ active		1 CLK2			1 CLK2		ns	
t778	REFRESH address set-up time to $\overline{RAS0}$		2 CLK2			2 CLK2		ns	
t779	REFRESH address hold time from $\overline{RAS3}$		2 CLK2			2 CLK2		ns	
t780	IOCHRDY going low from CLK2 high			20			20	ns	
t781	IOCHRDY float delay from CLK2			20			20	ns	
I/O Cycle									
t782	IO2XCS setup time to $\overline{XIOR}$ or $\overline{XIOW}$	10			10			ns	
t783	IO2XCS hold time to $\overline{XIOR}$ or $\overline{XIOW}$	10			10			ns	
t784	XA0 setup time to $\overline{XIOR}$ or $\overline{XIOW}$	10			10			ns	
t785	XA0 hold time to $\overline{XIOR}$or $\overline{XIOW}$	10			10			ns	
t786	$\overline{XDEN}$ active delay from $\overline{XIOR}$ or $\overline{XIOW}$	15		19	15		19	ns	
t787	$\overline{XDEN}$ inactive delay from $\overline{XIOR}$ or $\overline{XIOW}$	12			12			ns	
t788	XDA input setup time to $\overline{XIOW}$	10			10			ns	
t789	XDA input hold time to $\overline{XIOW}$	8			8			ns	
t790	XDA output valid delay to $\overline{XIOR}$			30			30	ns	
t791	XDA output hold time to $\overline{XIOR}$			15			15	ns	

Test Load = 65pF unless otherwise specified.

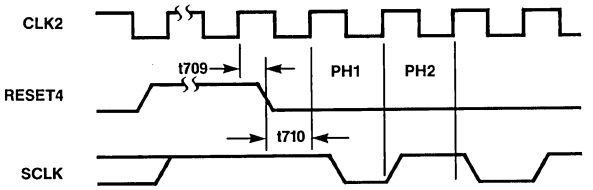
82C307 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	82C307-20 Min	Typ	Max	82C307-25 Min	Typ	Max	Unit	Notes
Misc Timing									
t792	$\overline{\text{PCHK}}$ active delay from $\overline{\text{CAS}}$ active during DRAM read cycles			10			10	ns	
t793	$\overline{\text{PCHK}}$ inactive delay from $\overline{\text{CAS}}$ inactive during DRAM read cycles			10			10	ns	
t794	$\overline{\text{LPAR}}$ input setup time to $\overline{\text{CAS}}$	10			10			ns	
t795	$\overline{\text{MEMB}}$ setup time to CLK2 low for CPU cycles	13			13			ns	
t796	$\overline{\text{MEMB}}$ setup time to command active for DMA cycles	15			15			ns	

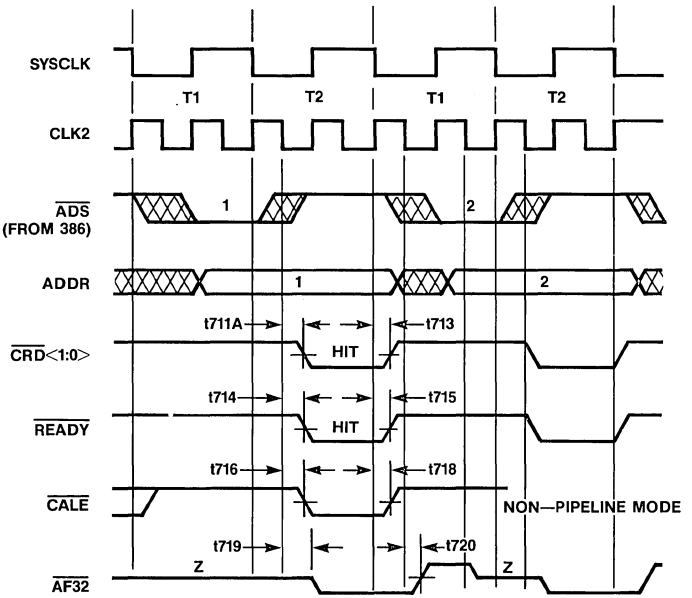
Test Load = 65pF unless otherwise specified.



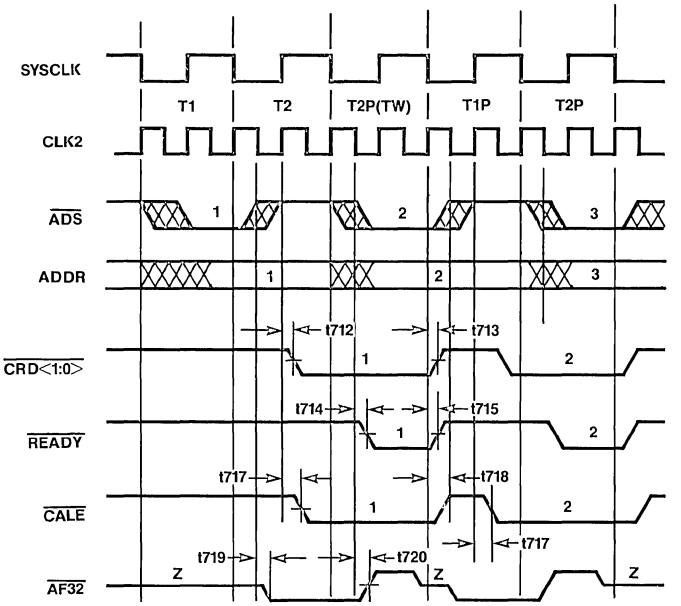
A.C. Timing Waveforms



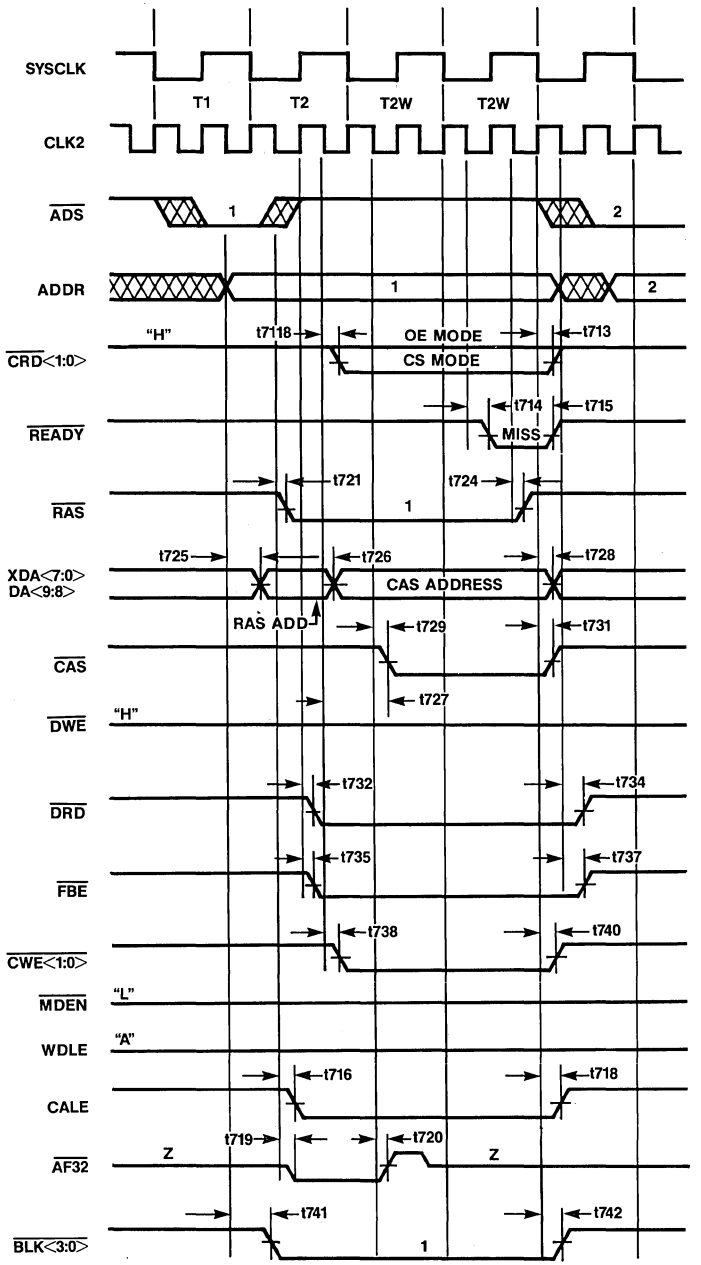
Timing Diagram (RESET Sequence)



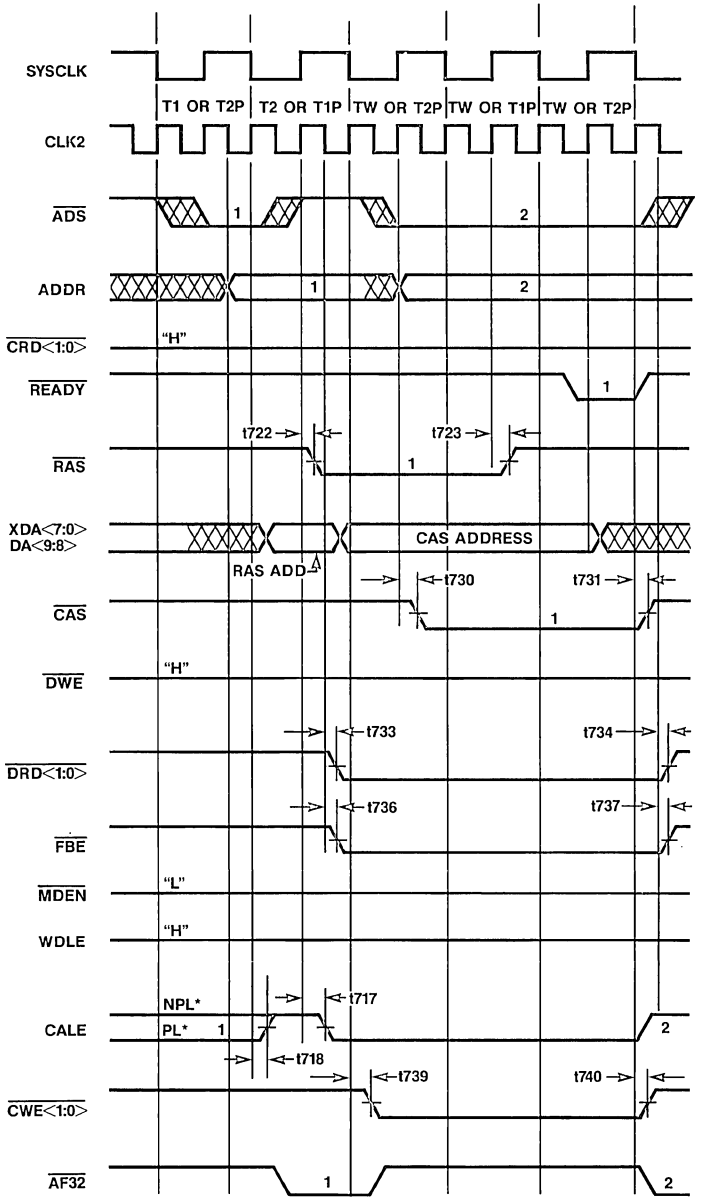
Read Hit Cycle, 0 WS SRAM, Non-Pipeline Mode



Read Hit Cycle, 1WS Non-Pipelined, Followed by a Pipeline Cycle

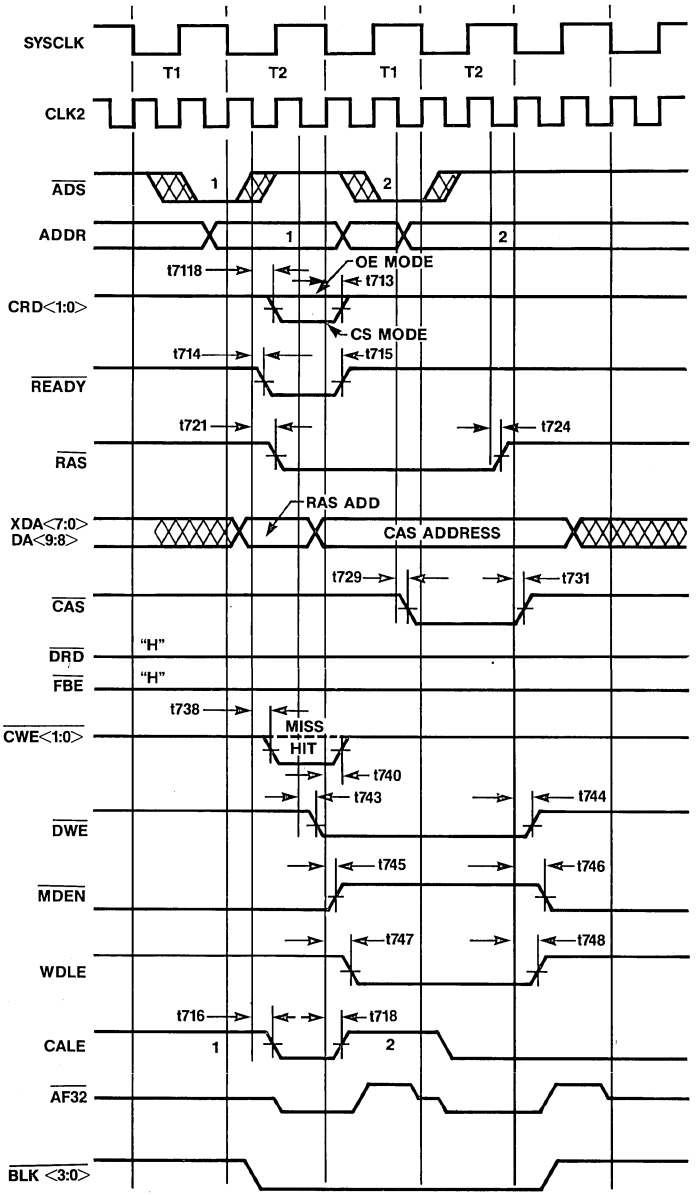


Read Miss Cycle, 2 WS DRAM, 0 WS SRAM, Non-Pipeline Mode



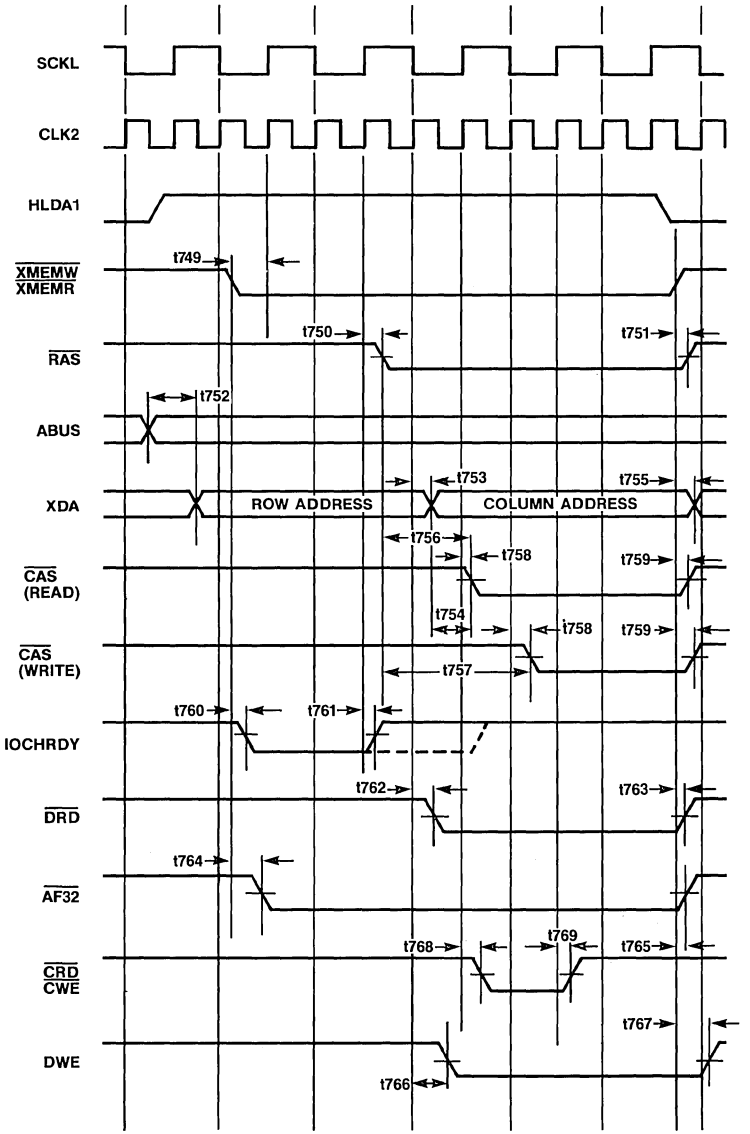
* NPL = Non-Pipeline PL = Pipeline

Read Miss Cycle, 2 WS DRAM, 1 WS SRAM, Non-Pipeline
0 WS SRAM, Pipeline



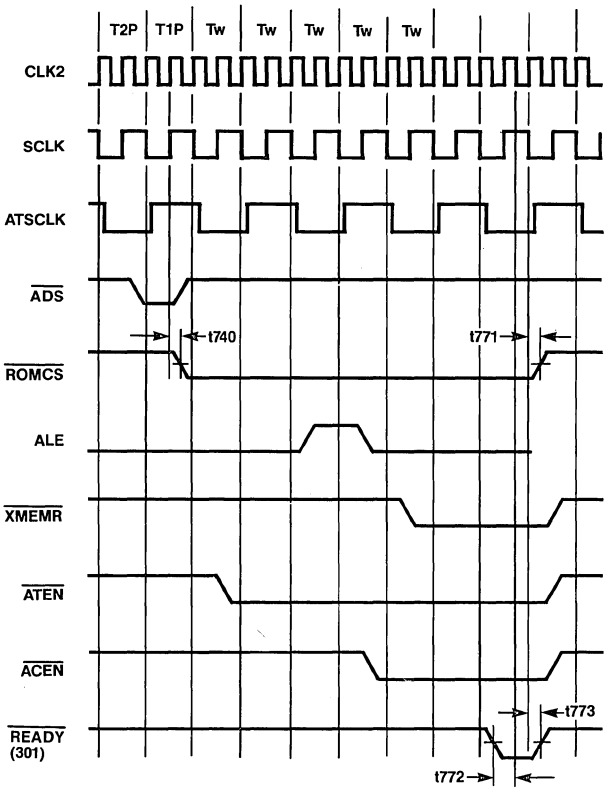
NOTE: $\overline{\text{CRD}}$ and $\overline{\text{CWE}}$ signals are not generated during the Write Miss Cycles. $\overline{\text{CRD}}$ is only generated for the chip select type of SRAMs during the Write Hit Cycles.

Write Hit/Miss Cycle, 2 WS DRAM, 0 WS SRAM, Non-Pipeline Mode

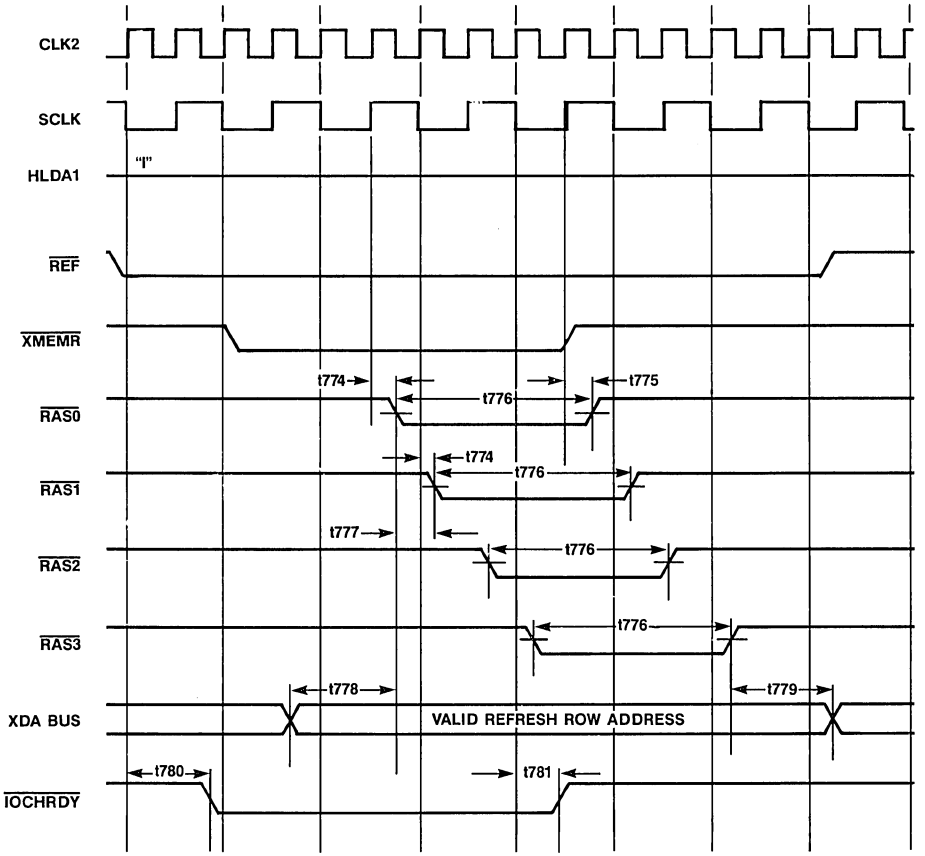


NOTE: $\overline{\text{CRD}}$ and $\overline{\text{CWE}}$ are generated during DMA Write Hit Cycles.
$\overline{\text{CRD}}$ is generated for chip select type SRAMs.
$\overline{\text{AF32}}$ is generated during DMA Cycle for 82C301 to generate the proper Action Code.

DMA Cycle

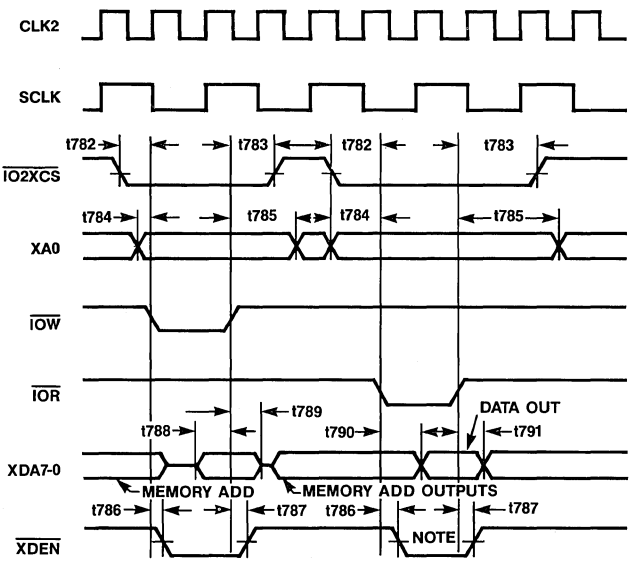


ROM Read Cycle



NOTE: t776 is the $\overline{RAS}$ pulse width during refresh and it is programmable through register 11 bits 1 and 2. IOCHRDY will not be generated during a classical refresh.

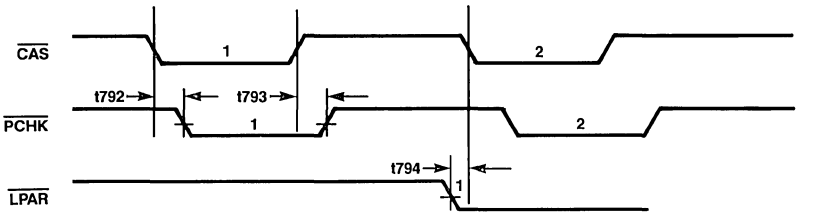
Refresh Cycle



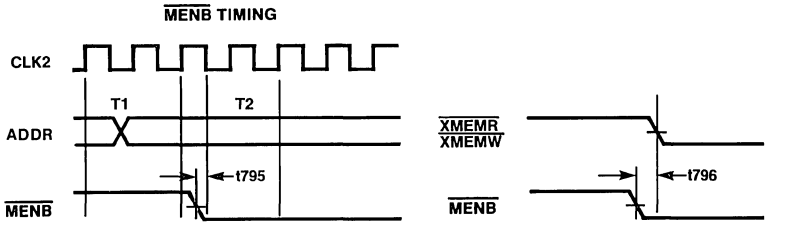
NOTE: No data output and XDEN is inactive if the index set up by the previous IO22 Write doesn't point to a valid IO23 register of 82C302.

I/O Read/Write Cycle

Parity Timing



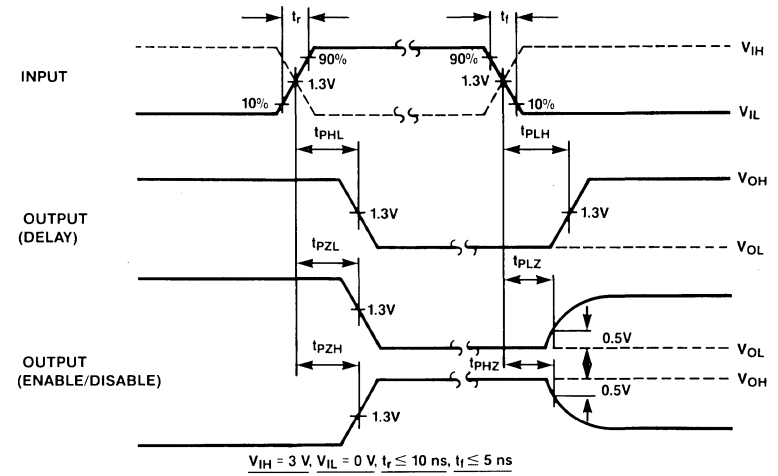
NOTE: $\overline{\text{LPAR}}$ in 82C307 is used to latch the address which caused the parity error, and it has to occur prior to the CAS for the next cycle.



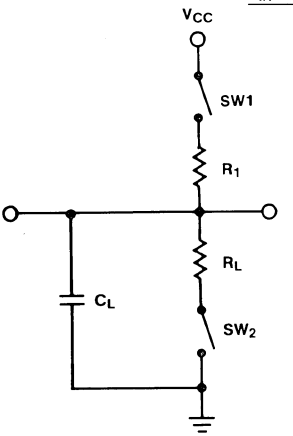
CPU Cycle **DMA Cycle**

Load Circuit Measurement Conditions

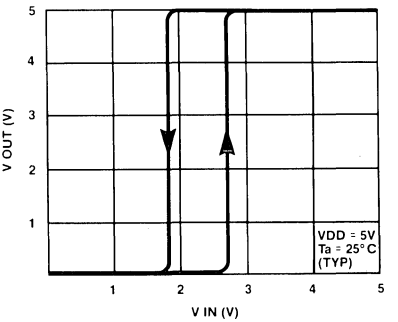
Parameter	Output Type	Symbol	C_L(pF)	R_1 (Ω)	R_L (Ω)	SW_1	SW_2
Propagation Delay Time	Totem pole 3-state Bidirectional	t_{PLH} t_{PHL}	50	—	1.0K	OFF	ON
Propagation Delay Time	Open drain or Open Collector	t_{PLH} t_{PHL}	50	0.5K	—	ON	OFF
Disable Time	3-state Bidirectional	t_{PLZ} t_{PHZ}	5	0.5K	1.0K	ON OFF	ON
Enable Time	3-state Bidirectional	t_{PZL} t_{PZH}	50	0.5K	1.0K	ON OFF	ON ON



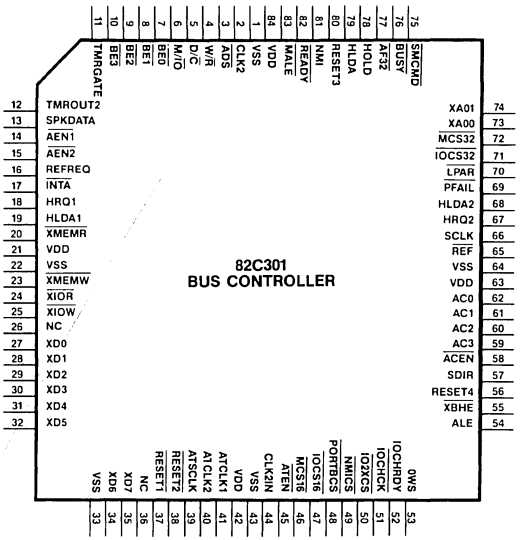
V_{IH} = 3 V, V_{IL} = 0 V, $t_r \leq$ 10 ns, $t_f \leq$ 5 ns

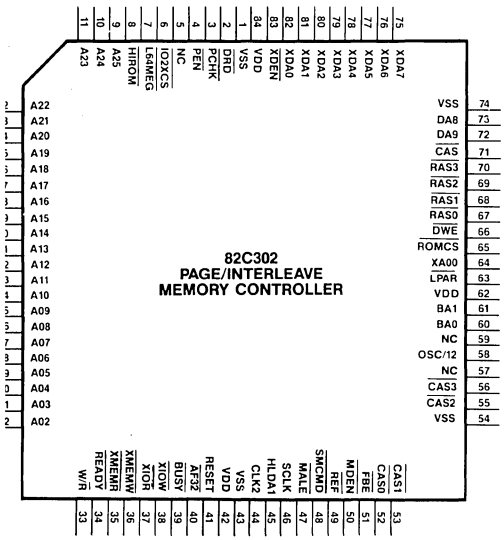


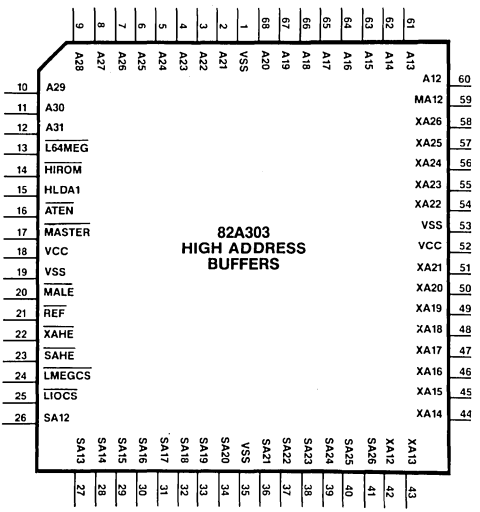
Reset 1 DC Characteristics

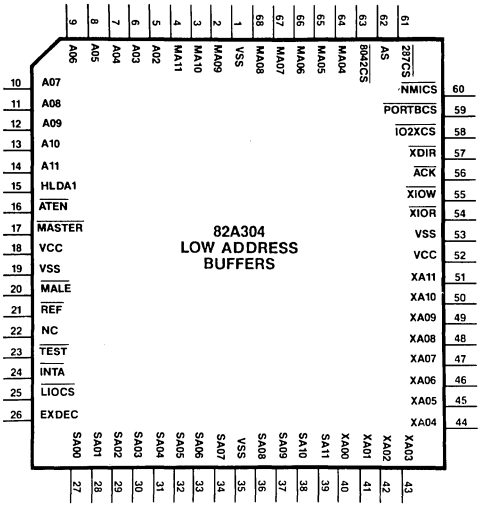


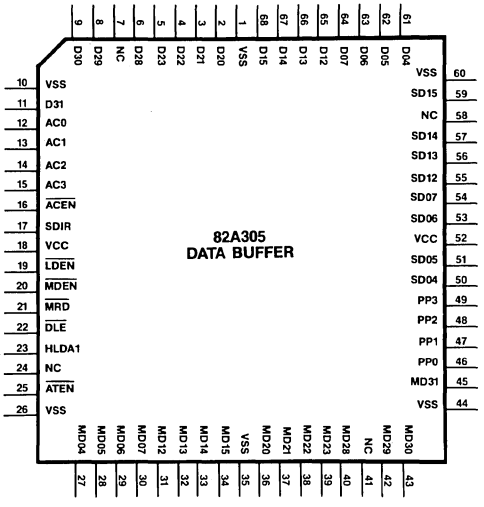
Load Circuit and AC Characteristics Measurement Waveform

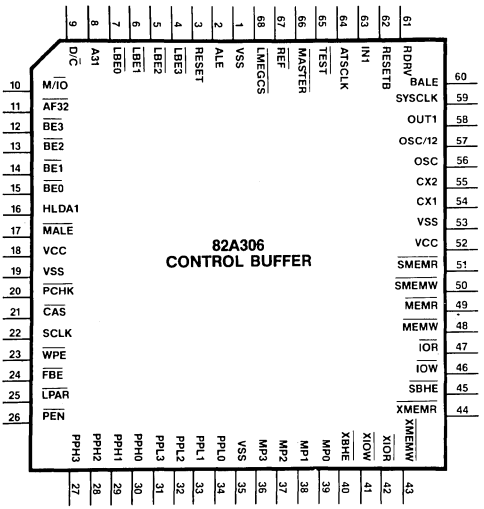

82C301
BUS CONTROLLER
TMRGATE 11
BE3 10
BE2 9
BE1 8
BE0 7
M/IO 6
D/C 5
W/R 4
ADS 3
CLK2 2
VSS 1
VDD 84
ALE 83
READY 82
NMI 81
RESET3 80
HLDA 79
HOLD 78
AF32 77
BUSY 76
SMCMD 75
TMROUT2 12
SPKDATA 13
AEN1 14
AEN2 15
REFREQ 16
INTA 17
HRQ1 18
HLDA1 19
XMEMR 20
VDD 21
VSS 22
XMEMW 23
XIOR 24
XIOW 25
NC 26
XD0 27
XD1 28
XD2 29
XD3 30
XD4 31
XD5 32
VSS 33
XD6 34
XD7 35
NC 36
RESET1 37
RESET2 38
ATSCLK 39
A1CLK2 40
A1CLK1 41
VDD 42
VSS 43
CLK2IN 44
ATEN 45
MCS16 46
IOCS16 47
PORTBCS 48
NMICS 49
IO2XCS 50
IOCHCK 51
IOCHRDY 52
0WS 53
XA01 74
XA00 73
MCS32 72
IOCS32 71
LPAR 70
PFAIL 69
HLDA2 68
HRQ2 67
SCLK 66
REF 65
VSS 64
VDD 63
AC0 62
AC1 61
AC2 60
AC3 59
ACEN 58
SDIR 57
RESET4 56
XBHE 55
ALE 54

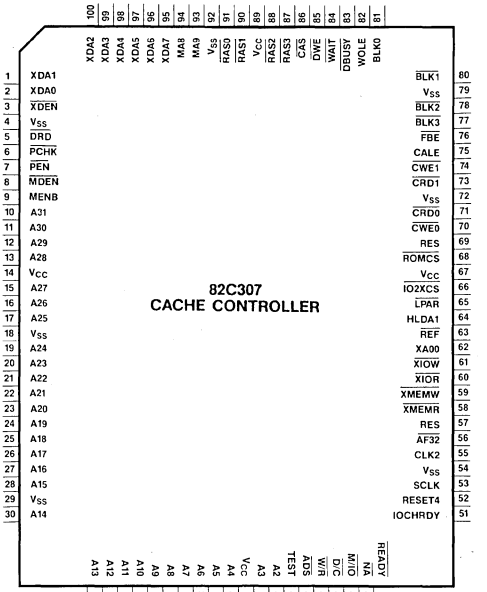

82C302
PAGE/INTERLEAVE
MEMORY CONTROLLER
A23 11
A24 10
A25 9
HIROM 8
L64MEG 7
IO2XCS 6
NC 5
PEN 4
DRD 3
PCHK 2
VDD 1
VSS 84
XDEN 83
XDA0 82
XDA1 81
XDA2 80
XDA3 79
XDA4 78
XDA5 77
XDA6 76
XDA7 75
A02 12
A03 13
A04 14
A05 15
A06 16
A07 17
A08 18
A09 19
A10 20
A11 21
A12 22
A13 23
A14 24
A15 25
A16 26
A17 27
A18 28
A19 29
A20 30
A21 31
A22 32
VSS 74
DA8 73
DA9 72
CAS 71
RAS3 70
RAS2 69
RAS1 68
RAS0 67
DWE 66
ROMCS 65
XA00 64
LPAR 63
VDD 62
BA1 61
BA0 60
NC 59
OSC/12 58
NC 57
CAS3 56
CAS2 55
VSS 54
W/R 33
READY 34
XMEMR 35
XMEMW 36
XIOR 37
XIOW 38
BUSY 39
AF32 40
RESET 41
VDD 42
VSS 43
CLK2 44
HLDA1 45
SCLK 46
MALE 47
SMCMD 48
MDEN 49
REF 50
FBE 51
CAS0 52
CAS1 53


82A303
HIGH ADDRESS
BUFFERS
A28 9
A27 8
A26 7
A25 6
A24 5
A23 4
A22 3
A21 2
VSS 1
A20 68
A19 67
A18 66
A17 65
A16 64
A15 63
A14 62
A13 61
A29 10
A30 11
A31 12
L64MEG 13
HIROM 14
HLDA1 15
ATEN 16
MASTER 17
VCC 18
VSS 19
MALE 20
REF 21
XAHE 22
SAHE 23
LMEGCS 24
LIOCS 25
SA12 26
SA13 27
SA14 28
SA15 29
SA16 30
SA17 31
SA18 32
SA19 33
SA20 34
VSS 35
SA21 36
SA22 37
SA23 38
SA24 39
SA25 40
XA12 41
XA13 42
A12 60
MA12 59
XA26 58
XA25 57
XA24 56
XA23 55
XA22 54
VSS 53
VCC 52
XA21 51
XA20 50
XA19 49
XA18 48
XA17 47
XA16 46
XA15 45
XA14 44

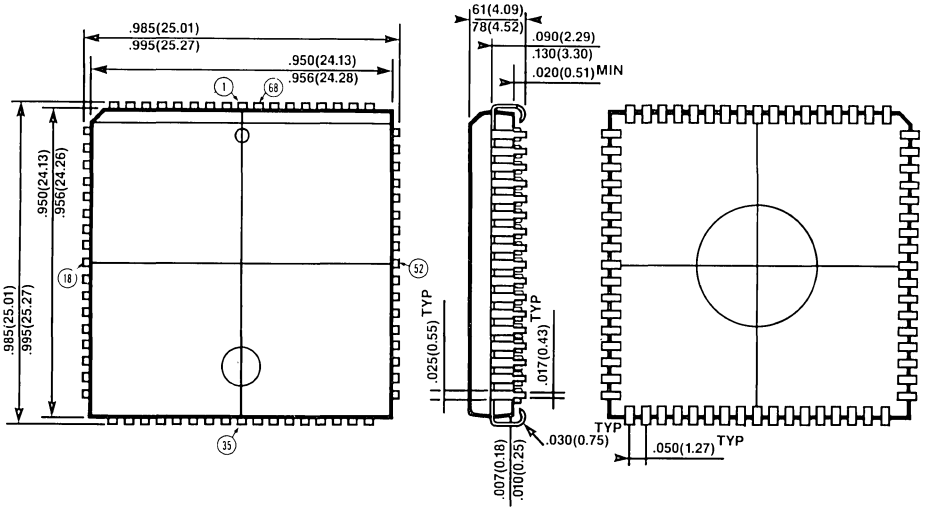

82A304
LOW ADDRESS
BUFFERS
A06
A07
A08
A09
A10
A11
HLDA1
ATEN
MASTER
VCC
VSS
MALE
REF
NC
TEST
INTA
LIOCS
EXDEC
A05
A04
A03
A02
287CS
NMICS
PORTBCS
IO2XCS
XDIR
ACK
XIOW
XIOR
VSS
VCC
XA11
XA10
XA09
XA08
XA07
XA06
XA05
XA04
AS
8042CS
SA00
SA01
SA02
SA03
SA04
SA05
SA06
SA07
SA08
SA09
SA10
SA11
XA00
XA01
XA02
XA03


82A305
DATA BUFFER
D30
D29
D28
D23
D22
D21
D20
VSS
D15
D14
D13
D12
D07
D06
D05
D04
VSS
SD15
NC
SD14
SD13
SD12
SD07
SD06
VCC
SD05
SD04
PP3
PP2
PP1
PP0
MD31
VSS
VSS
D31
AC0
AC1
AC2
AC3
ACEN
SDIR
VCC
LDEN
MDEN
MRD
DLE
HLDA1
NC
ATEN
VSS
MD04
MD05
MD06
MD07
MD12
MD13
MD14
MD15
VSS
MD20
MD21
MD22
MD23
MD28
NC
MD29
MD30


82A306
CONTROL BUFFER
D/C
M/IO
AF32
BE3
BE2
BE1
BE0
HLDA1
MALE
VCC
VSS
PCHK
CAS
SCLK
WPE
FBE
LPAR
PEN
A31
LBE0
LBE1
LBE2
LBE3
RESET
ALE
VSS
LMEGCS
REF
MASTER
TEST
ATCLK
IN1
RESETB
RDRV
BALE
SYSCLK
OUT1
OSC/12
OSC
CX2
CX1
VSS
VCC
SMEMR
SMEMW
MEMR
MEMW
IOR
IOW
SBHE
XMEMR
XMEMW
XIOR
XIOW
XBHE
MP0
MP1
MP2
MP3
VSS
VSS
PPL0
PPL1
PPL2
PPL3
PPH0
PPH1
PPH2
PPH3

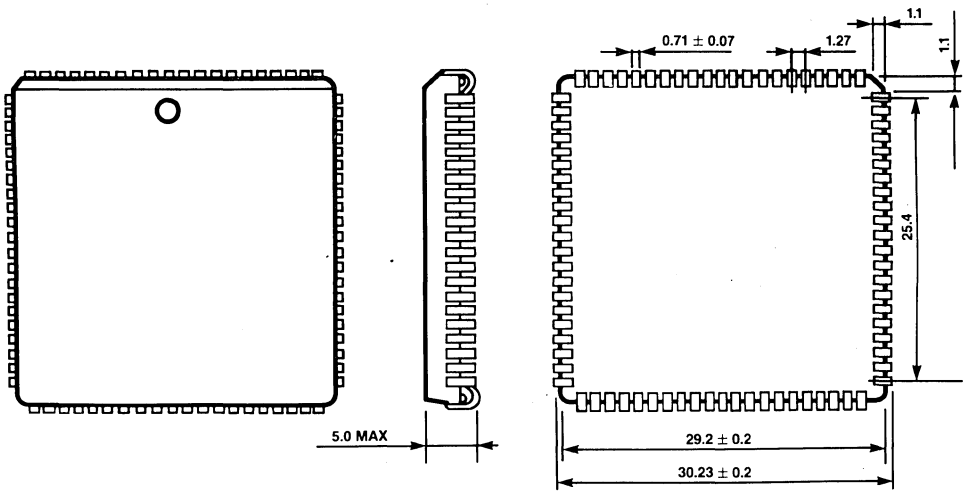

82C307
CACHE CONTROLLER
XDA1
XDA0
XDEN
VSS
DRD
PCHK
PEN
MDEN
MENB
A31
A30
A29
A28
VCC
A27
A26
A25
VSS
A24
A23
A22
A21
A20
A19
A18
A17
A16
A15
VSS
A14
XDA2
XDA3
XDA4
XDA5
XDA6
XDA7
MA8
MA9
VSS
RASD
RAS1
VCC
RAS0
RESD
RESS
CAS
DWE
WAIT
USYD
USYC
VOLT
BLK0
BLK1
VSS
BLK2
BLK3
FBE
CALE
CWE1
CRD1
VSS
CRD0
CWE0
RES
ROMCS
VCC
IO2XCS
LPAR
HLDA1
REF
XA00
XIOW
XIOR
XMEMW
XMEMR
RES
AF32
CLK2
VSS
SCLK
RESET4
IOCHRDY
READY
NA
M/IO
D/C
W/R
ADS
TEST
A2
A3
VCC
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13

68-LEAD PLASTIC CHIP CARRIER



DIMENSIONS IN INCHES (MILLIMETERS) S = 3.6/1

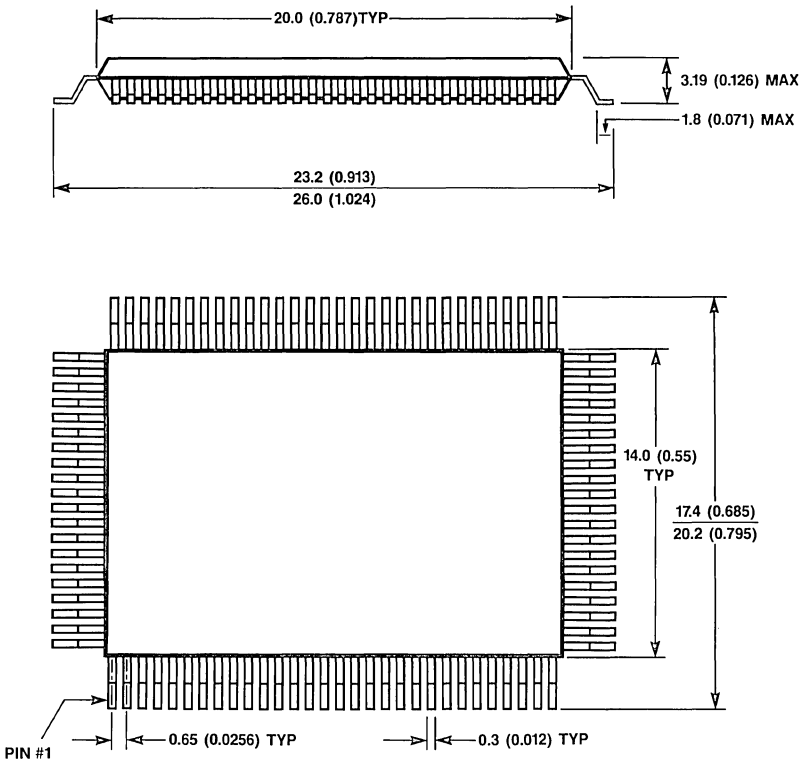
84-PIN PLASTIC LEADED CHIP CARRIER UNIT (mm)



82A303 Absolute Maximum Ratings

Order Number	Package Type Note 1	Remarks
P82C301	PLCC-84	C (Note 2)
P82C302	PLCC-84	C
P82C303	PLCC-68	C
P82A304	PLCC-68	C
P82A305	PLCC—68	C
P82A306	PLCC-68	C
P82C307	PFP	C
CS8230	—	Standard CHIPSet (Note 3)

NOTES
1. PLCC = Plastic Leaded Chip Carrier 84 Pins
2. C = Commercial Range, 0° to 70°C, V_{DD} = 4.75 to 5.25 V
3. CS8230 consists of P82C301, P82C302, P82A303, P82A304, P82A305, P82A306.



DIMENSIONS: mm (in)

100-PIN PLASTIC FLAT PACKAGE
(RECTANGULAR)

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