CHIPS AND TECHNOLOGIES, INC.
3050 ZANKER ROAD, SAN JOSE, CA 95134
408-434-0600

PRELIMINARY SPECIFICATION

CHIPS/280
MODEL 70/80 COMPATIBLE CHIPSET
(16-, 20-, 25-, & 33-MHZ*)

** 33MHZ TIMING WAVEFORMS & T-NUMBERS ARE AVAILABLE IN A SEPARATE DOCUMENT*

AUGUST 9, 1989
CPI022.1/8-89
REV 1.0
STK#10022-002

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Contents

82C321, 82C322, 82C325, 82C223, 82C226, 82C607, 82C451/452 CHIPS/280: Complete IBM PS/2 TM Model 70/80 Compatible CHIPSetTM

- 100% functionally compatible to IBM PS/2TM Models 70/80
- Supports 16, 20, and 25 MHz compatible PS/2TM Models 70/80
- High performance Matched Memory Interface for Micro Channel Memory Adapters at 16, 20 and 25 MHz
- Advanced Page Interleaved Memory Controller with integrated Bad Block Remapping Capability
- Near zero wait states (average 0.5 - 0.7 wait states)

Memory on Local Data Bus

120 ns DRAMs at 16 MHz
100 ns DRAMs at 20 MHz
80 ns DRAMs at 25 MHz

- Integrated Lotus-Intel-Microsoft Memory Specification (LIM EMS 3.2) Memory Controller with 4 register sets, expandable to full LIM EMS 4.0 specification with 8 register sets of 64 mapping registers using the 82C631 EMS mapper chip.
- Supports IBM Matched Memory Cycle and CHIPS Fast Micro Channel Matched Memory Cycle.
- High performance, Fast VGA interface to the 82C451 and 82C452 VGA controllers.
- Asynchronous CPU and DMA state machines.
- PS/2TM Model 70/80 compatible Address Recovery logic.
- Low power, high speed CMOS technology.

CHIPS/280 is a 7-device, enhanced CMOS implementation of most of the system logic necessary to implement personal computers compatible to IBM PS/2TM Model 70/80. CHIPS/280 enables OEMs to offer compatible PS/2TM models 70/80, that are more integrated and superior in performance than IBM's Model 70/80.

CHIPS/280 includes the CS8238 System Logic CHIPSetTM, the 82C607 Multi-Function Controller with Analog Data Separator and 16550 compatible serial port, and the Enhanced Gate-Level Compatible 82C451/452 VGA chip as indicated in Figures 1a and 1b. With these 7 VLSI devices, it requires only 59 additional components plus memory to implement compatible PS/2TM Models 70/80 superior to IBM's models.

SYSTEM LOGIC CS8238 CHIPSET™

The CS8238 System Logic CHIPSet™ consists of the following devices:

Device	Function	Number of Pins
82C321	CPU/Micro Channel Adapter (MCA) Controller	100 PFP
82C322	Page/Interleaved Memory Controller	144 PFP
82C325	Data Buffer	144 PFP
82C223	DMA Controller	84 PLCC or 100 PFP
82C226	System Peripherals Controller	84 PLCC or 100 PFP

82C321 CPU and MCA Controller

The 82C321 CPU and MCA Compatible Controller manages the system timing for the asynchronous 80386 CPU, DMA and MCA cycles. It supports CPU clock speeds 16, 20 and 25 MHz. It supports all Micro Channel Architecture (MCA) compatible cycles including CHIP's proprietary Fast VGA cycle. It includes the state machines for command and control logic signal generation, DMA and refresh logic control. The 82C321 also supports a CHIPS Fast MCA Matched Memory Cycle which can improve accesses to the memory on the MCA channel by up to 33%.

82C322 Page/Interleaved Memory Controller

The 82C322 Page/Interleaved Memory Controller provides an interleaved memory sub-system design with page mode operation. It supports 4 memory banks, with memory configuration ranging from 1MB to 16 MB. While operating in the DOS environment, the memory above 1 MB can be utilized as EMS memory, significantly improving the value of large memory configuration requirements of the OS/2 era. The on-chip EMS logic provides 4 mapping registers. However, with external EMS mapper chip, the full LIM EMS 4.0 specification of 8 register sets of 64 mapping registers can be realized. It interfaces to either static column or page mode DRAMs. The 82C322 supports shadowing of the EPROM into RAM space, allowing faster execution of code. The 82C322 integrates the on-board I/O decode logic and IBM compatible address recovery logic.

82C325 Data Buffer

The 82C325 Data Buffer provides electrical isolation between the Memory Data Bus and the Local Data Bus. Additionally, it performs the latching and bus steering function. The Data Buffer also provides the programmable I/O decode registers for user I/O decoding requirements. It contains the system POS registers, NMI logic, as well as DRAM parity generation and detection logic. 82C607 decode signals, 82C451/82C452 VGA setup and enable signals are also contained in the 82C325.

83C223 DMA Controller

The 82C223 DMA Controller provides 8 DMA channels for slave devices and the Central Arbitration Control Point (CACP) for the entire system. Each DMA Channel has 24-bit addressing capability and can perform 8-bit or 16-bit transfers. It also supports Virtual DMA, wherein DMA channels 0 and 4 can be used to service multiple DMA slaves by multiplexing the DMA channels between the arbitration levels assigned to those slaves. It supports multiple Bus Masters via the CACP arbitrator and control logic. The Bus Arbitration logic includes protection against error conditions like burst mode devices not relinquishing the bus within specified time.

82C226 System Peripherals Controller

The 82C226 System Peripherals Controller integrates PS/2™ Compatible peripherals in one compact package with an optimized bus interface to the Peripheral Bus. It includes two 8259 Programmable Interrupt Controllers, one 8254 compatible timer, two 146818 compatible real-time clocks, 114 bytes of CMOS battery back-up SRAM and one PS/2™ compatible bi-directional Parallel Port.

GRAPHICS

The 82C451 Gate Level compatible VGA provides 100% VGA compatible graphics with backward compatibility to EGA, CGA, MDA and Hercules. In VGA graphics modes, it provides resolutions from 320 x 480 with 16 colors. In VGA text mode, it supports fonts up to 9 x 32. It supports all standard monitors - IBM PS/2™ analog, Multi frequency, EGA, CGA and digital Monochrome. The 82C451 boosts graphics performance with a tightly coupled high performance interface to the CPU and a 16-bit memory interface. The 82C451 is packaged in 144 pin PFP package.

PERIPHERAL SUPPORT

The 82C607 Multi-Function Controller integrates PS/2™ compatible peripherals in one compact package. It includes one 16550 Compatible UART, an Analog Data Separator, POS Registers and Glue logic for a NEC 765A Floppy Disk Controller. The 82C607 is available in 68 pin PLCC package.

SYSTEM OVERVIEW

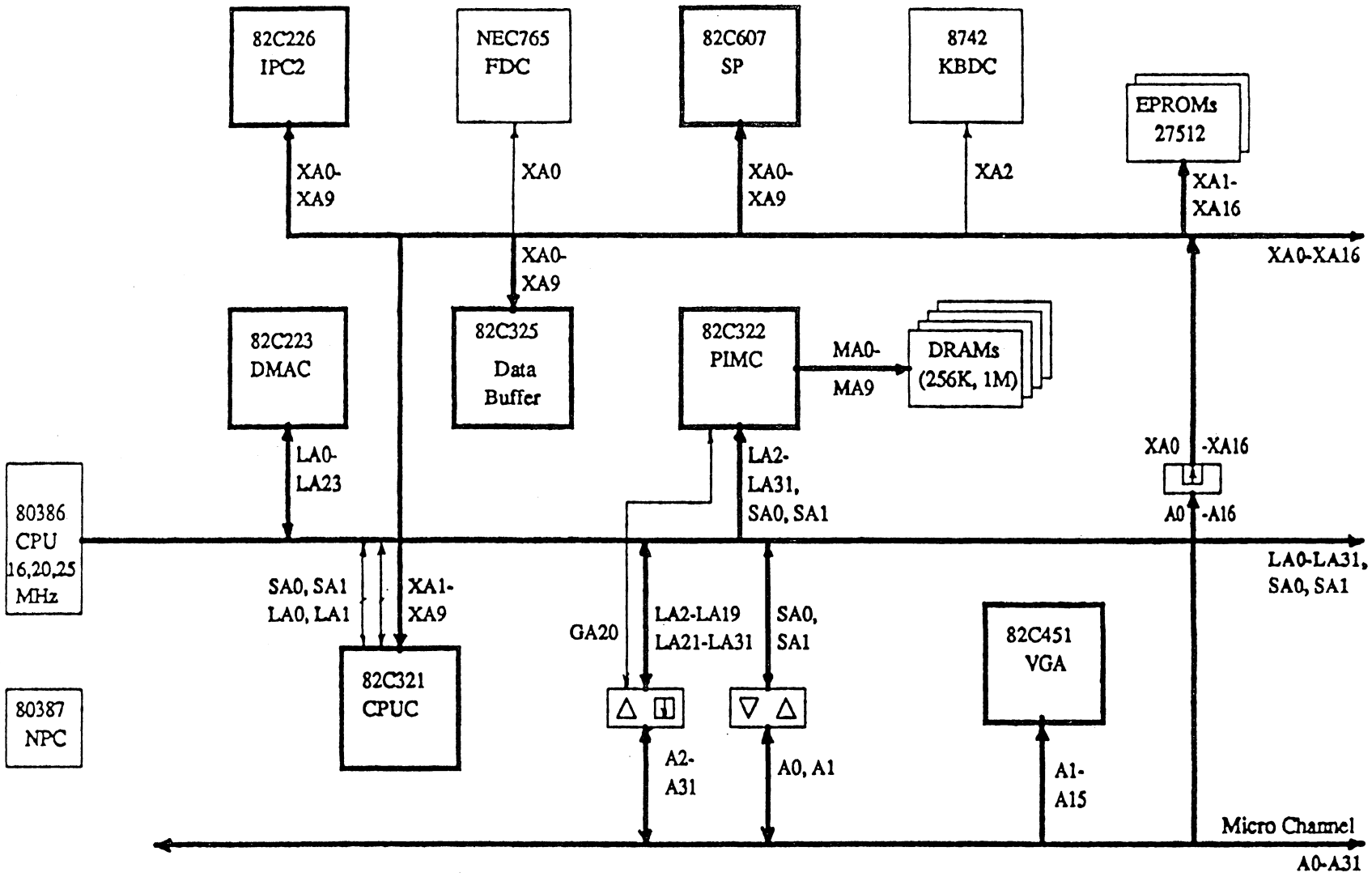
CHIPS/280 is designed to maximize the performance of the 80386 microprocessor by coupling it to a high performance page/interleaved memory sub-system. The maximum page size supported by the CHIPS/280 architecture is 16 KBytes when 1 Mbyte DRAMs are used (16 MB of onboard Memory) and the four way interleaved mode of operation is selected. When executing within a page, the DRAM memory sub-system can execute at the same speed as the processor. To the 386, the memory sub-system appears as a 16 KByte direct mapped cache, using relatively inexpensive DRAMs. When operating at 16, 20 or 25 MHZ, the average waitstate incurred is less than 0.7. Additionally, by using Shadow RAM techniques, the BIOS code can also be executed with near zero wait states.

In addition to the high performance memory interface, CHIPS/280 supports a fast Matched Memory Cycle reducing the access time from 200 ns to 120 ns at 25 MHz. CHIPS proprietary Fast VGA cycle allows VGA I/O accesses to be performed within 187.5 ns @ 16 MHz, 150 ns @ 20 MHz, and 120 ns @ 25 MHz.

Regardless of the CPU speed, the DMA controller operates at 10 MHz. Once the DMA and the peripherals are tuned, for example, with a 1:1 interleaving on the Hard Disk, CHIPS/280 continues to deliver dependable high performance.

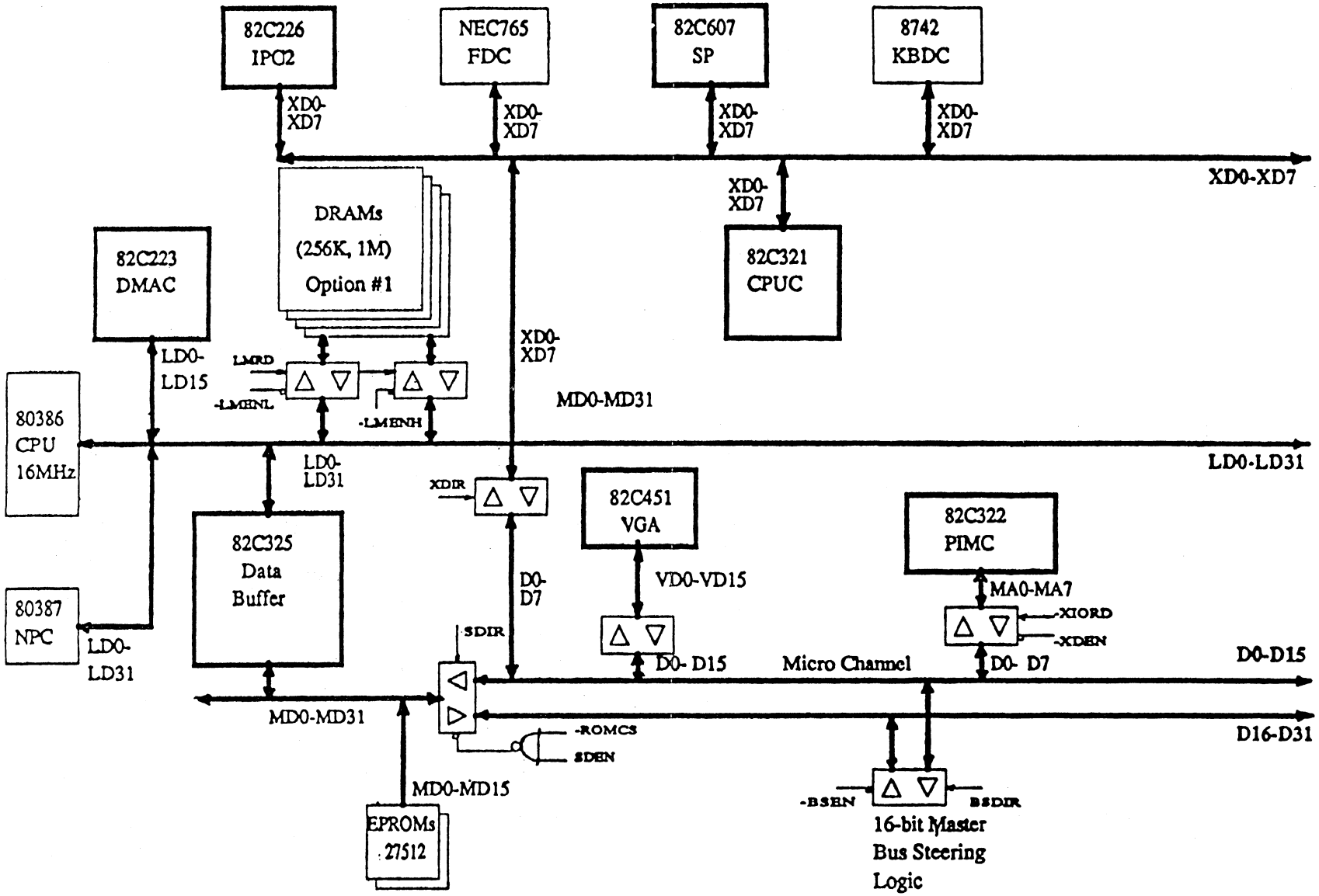
ARCHITECTURE

Figures 1-1 and 1-2 illustrates the Address and Data Bus Architecture.



CHIPS/280 ADDRESS PATHS

Figure 1-1



CHIPS/280 DATA PATHS

Figure 1-2

ADDRESS BUS ARCHITECTURE

The CHIPS/280 supports the following address busses:

- Local Address Bus (LA BUS)
- Memory Address Bus (MA BUS)
- MCA Address Bus (A BUS)
- Peripheral Address BUS (XA BUS)

Local Address Bus (LA <31:0>)

The 80386, the 82C322 Page/Interleaved Memory Controller, and the 82C223 DMA controller share the Local Address Bus. The Local Address Bus is buffered to generate the MCA Address Bus. The buffer used is bi-directional and the direction of the address bus is determined by the polarity of the -MASTER input from the MCA channel.

Memory Address Bus (MA <9:0>)

The lower addresses of the memory address bus (MA <0:7>) are bi-directional. During accesses to the internal configuration registers, these pins are used to program the 82C322. During memory accesses, (MA <0:9>) address outputs contain row and column address information. The memory address lines are derived from the bus master currently in charge, and could be either the CPU, DMA or an external Bus Master that has gained control of the bus.

MCA Address Bus (A<31:0>)

The MCA Address Bus is bi-directional. These are outputs to MCA compatible adapters, when either the CPU or the DMA controller is the bus master. These address lines are driven by the external Bus Masters when they are in control.

XA Address Bus (XA<16:0>)

The XA Address bus is derived from the MCA Address Bus. The address information is latched by the leading edge of -VGACMD. XA<0:15> are derived by latching A<0:15> address lines. XA16 is driven by the 82C322 Page/Interleaved Memory Controller.

DATA BUS ARCHITECTURE

The CHIPS/280 supports the following data busses:

- Local Data Bus (LD BUS)
- Memory Data Bus (MD BUS)
- MCA Data Bus (D BUS)
- Peripheral Data Bus (XD BUS)

Local Data Bus (LD <31:0>)

The Local Data Bus (LD BUS) is shared by the 80386, the 80387, the 82C322(Memory controller) and the 82C223 (DMA Controller). The 80386 BS16# input is strapped high to enable 32-bit accesses. The DMA controller is the only 16 bit device on the local data bus (LD BUS). When accessing the DMA controller, the 82C325 steers the processor data bus information appropriately to the DMA controller. The parity bits (MP <0:3>) are generated by 82C325.

Memory Data Bus (MD<31:0>)

The Memory Data Bus (MD BUS) is driven by the 82C325 Data Buffer. The MD BUS sources the BIOS EPROMS.

MCA Data Bus (D<31:0>)

The MD BUS is buffered by transceivers to generate the MCA Data Bus (D BUS), the direction of which is controlled by SDIR generated by 82C321. These buffers are always enabled (except for ROM accesses) for accessing on-board resources or MCA accesses. The D Bus is used to communicate with the MCA adapters. The D Bus should be tri-stated to prevent MCA adapter cards from accessing BIOS EPROMs.

Peripheral Data Bus (XD <7:0>)

The Peripheral data Bus (XD BUS) is derived from the MCA Data Bus by bi-directional buffers. The Peripheral Data Bus is 8-bits wide (XD<0:7>) in a CHIPS/280 implementation. The XD BUS provides communications to the internal registers of the CHIPS/280 CHIPset™, as well as other on-board peripherals such as the Floppy Disk Controller, Key Board Controller, etc.

The XDIR out of the 82C325 controls the direction of the XD BUS transceivers. XDIR is activated only when the -XDEN signal from the 82C322 Page/Interleaved Memory Controller is in-active. When accessing the internal configuration registers of the 83C322, XDEN is active and XDIR is inactive. The data transfer direction is from the D Bus to XD Bus preventing data bus contention.

Miscellaneous Ports and POS Registers

The CHIPS/280 POS (Programmable Option Select) registers and I/O ports 61, 70, 91, 94, and 3C3 are provided. These ports are distributed in among the CHIPset™, as a result more than one chip may respond for a single port access.

INDEX REGISTERS

CHIPS/280 CHIPSet™ has several additional registers required for programming the various modes of operation that are available. An indexing scheme is used to reduce the I/O ports required for all the registers of the CHIPSet™. Port 22H is used as an Indexing register and Port 23H is used as the Data register. The index value is placed in port 22H and the data to be written to or read from the indexed register is placed in port 23H. Every access to port 23H must be preceded by a write of the index value to port 22H, even if the same register data is accessed again. All reserved bits are set to zero by default and when written to, must be set to zero. Only the registers used in the 82C321, 82C322, and 82C325 are discussed, since the other registers are described in the 82C226, 82C607,8042, 82C223 and 82C451 documentation. Registers R22-R29 are accessed directly (instead of through index registers). Table 1 lists these registers:

Table 1

Reg #	Register Name	Index	Location
R0	Version Register	8DH	82C321
R1	System Speed Select	8EH	82C321
R2	System Option Register	8FH	82C321
R3	Version and Memory Enable	B4	82C322
R4	ROM Configuration	B5H	82C322
R5	Memory Enable Register 1	B6H	82C322
R6	Memory Enable Register 2	B7H	82C322
R7	Reserved Register	B8H	82C322
R8	Memory Type	B9H	82C322
R9	Operating Mode	BAH	82C322
R10	Timing Control	BBH	82C322
R11	EMS Base Address	BCH	82C322
R12	EMS Address Extension 1	BDH	82C322
R13	EMS Address Extension 2	BEH	82C322
R14	EMS Range Address Register	BFH	82C322
R15	Faulty DRAM Address Extension 1	C0H	82C322
R16	Faulty DRAM Address Extension 2	C1H	82C322
R17	Faulty DRAM Base Address 1	C2H	82C322

Table 1 (continued)

Reg #	Register Name	Index	Location
R18	Faulty DRAM Base Address 2	C3H	82C322
R19	Faulty DRAM Base Address 3	C4H	82C322
R20	Faulty DRAM Base Address 4	C5H	82C322
R21	Faulty DRAM Relocation Address	C6H	82C322
R30	Miscellaneous Register	80H	82C325
R31	Programmable I/O Setup #0	81H	82C325
R32	Programmable I/O Decode #0	82H	82C325
R33	Programmable I/O Setup #1	83H	82C325
R34	Programmable I/O Decode #1	84H	82C325
R35	Programmable I/O Setup #2	85H	82C325
R36	Programmable I/O Decode #2	86H	82C325
R37	Upper System ID Byte	87H	82C325

Reg #	Register Name	Address	Location
R22	Split Ram Address Register	E0H	82C322
R23	Split Enable Register	E1H	82C322
R24	Channel Recovery Register(A30-A24)	E2H	82C322
R25	Channel Recovery Register(A23-A16)	E3H	82C322
R26	Channel Recovery Register(A8-A15)	E4H	82C322
R27	Channel Recovery Register(A2-A7)	E5H	82C322
R28	Channel Recovery Register(ARB13-10)	E6H	82C322
R29	Channel Recovery Register(D/C)	E7H	82C322

FEATURES

- Supports 16, 20 and 25 MHz 80386 Processors
- 100% Compatibility with MCA specifications at all CPU speeds
- Programmable wait state option
- Matched Memory Cycle Support
- Fast Matched Memory Cycle Support
- Fast VGA Cycle
- Bus Conversions for 16 and 8-bit devices
- 80387 Interface Logic

FUNCTIONS

The 82C321 MCA/CPU controller performs the following functions in a CHIPS/280 implementation. Figure 1-3 shows the block diagram of 82C321.

- Reset generation
- Bus Cycle Control providing the following:
  * MCA compatible default (I/O and Memory) Cycle (CPU cycle time of 250 ns @ 16 MHz, 250 ns @ 20 MHz, and 240 ns @ 25 MHz).
  * MCA Compatible Matched memory Cycle (CPU Cycle time of 187.5 ns @ 16 MHz, 250 ns @ 20 MHz, and 240 ns @ 25 MHz)
  * Fast Matched memory Cycle (CPU Cycle time of 187.5 ns @ 16 MHz, 150 ns @ 20 MHz, and 120 ns @ 25 MHz)
  * Fast VGA Cycle (CPU cycle time of 187 ns @ 16 MHz, 150 ns @ 20MHz, and 120 ns @ 25 MHz)
- Data bus sizing and steering for CPU, DMA and data bus steering for external bus masters
- MCA bus memory and I/O cycles to 8,16 or 32 bit peripherals
- Waitstate generation logic to provide support for the following:
  * -Slow MCA compatible adapter cards
  * -Slow system board peripherals and index registers.
- 80387 Numeric coprocessor interface logic
- MCA compatible status (S0, S1), Address Decode Latch (-ADL) and Command (-CMD) generation
- GateA20 generation

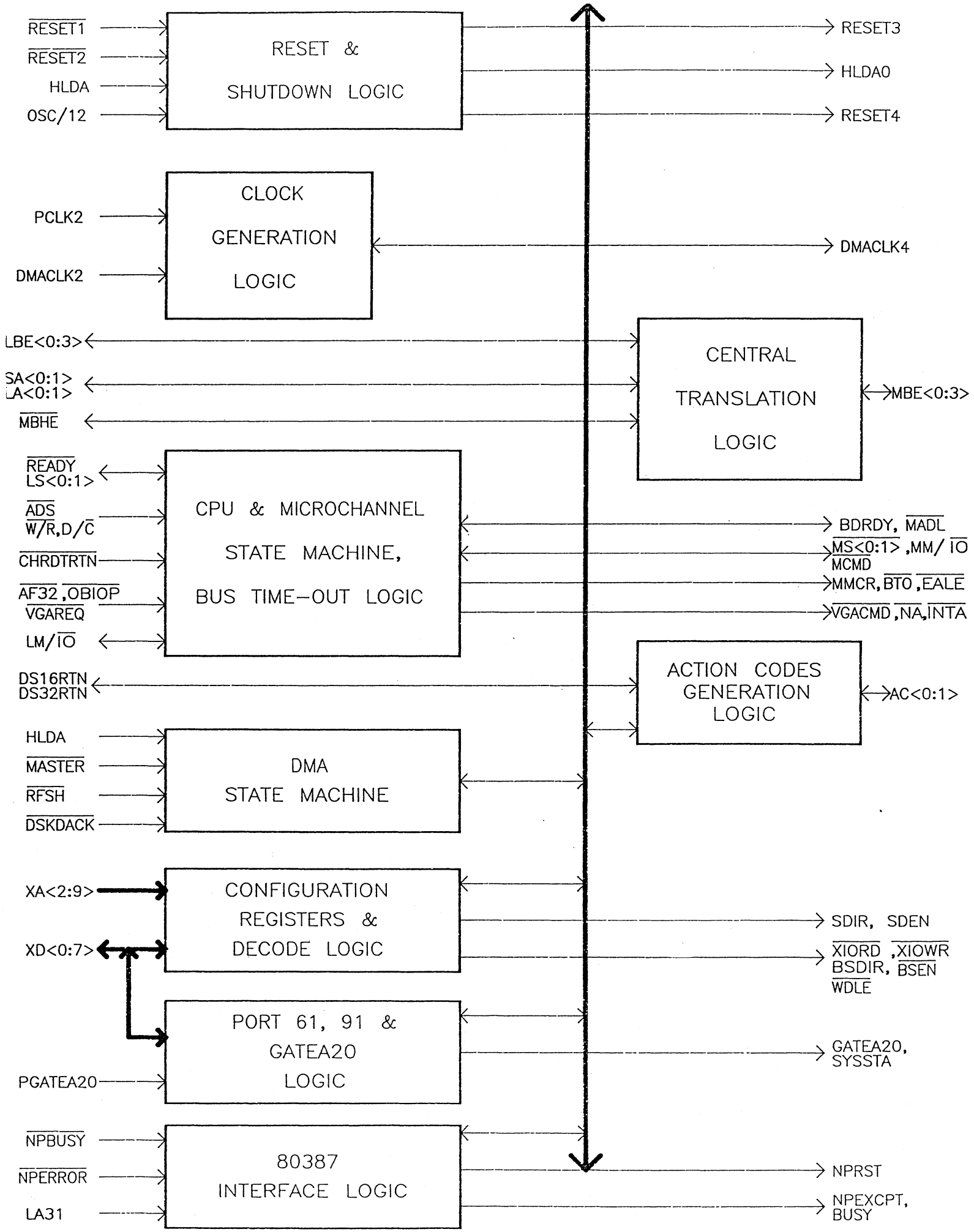


Figure 1.3 82C321 CPU & MicroChannel Controller Block Diagram

1.0 RESET GENERATION LOGIC

The 82C321 receives two reset inputs: - RESET1 and -RESET2. -RESET1 is the Power Good input from the power supply. When -RESET1 is active, the 82C321 activates RESET3 and RESET4 for a system reset. -RESET2 is generated from the 8042 keyboard controller when a warm reset is required. -RESET2 activates RESET3 to the 80386. RESET3 is also activated by the 82C321 when a CPU shutdown condition is detected. Additionally, setting bit 0 in the System Port A (92H) causes RESET3 to be active, after the I/O command goes inactive. RESET3 is held active for at least 128 PCLK2 cycles following the de-activation of -RESET1.

RESET3 is synchronized with respect to PCLK2 to ensure the proper phase between the CPU/DMA state machine and the internal phase of the 80386 Microprocessor. RESET4 performs the system reset function, resetting the 82C322 Page/Interleaved Memory Controller, the 82C223 DMA Controller, the 82C226 Peripheral Controller and the 8742 (or the 8042) key board controller to their default values. RESET3 and RESET4 are held valid for at least 128 PCLK2 cycles, following the deactivation of -RESET1.

The 82C321 generates the NPRESET output to reset the 80387 Numeric Coprocessor. The NPRESET is activated when RESET3 is activated or when port 0F1H is written to. During accesses to port 0F1, the NPRESET is held high for 128 PCLK2 cycles. NPRESET is then forced low for 128 PCLK2 cycles before -READY is returned to the processor. This ensures that the Numeric Coprocessor Reset High and Low time requirements are satisfied.

NOTE: The 80386 deasserts HLDA when RESET3 goes active. This can end a DMA cycle in progress. The 82C321 generates HLDA0 (which goes to 82C223 DMA controller) to correct this problem. If RESET2 and HLDA occurs simultaneously RESET3 is generated, and HLDA0 is not asserted thus blocking the DMA cycle from starting. When RESET3 is completed, HLDA0 is sent to the 82C223 DMA Controller. If the DMA cycle is already in progress and RESET2 becomes active then RESET3 is not asserted until the DMA cycle is completed. The same applies to port 92 RESET operation.

2.0 CPU/DMA STATE MACHINE

The 82C321 supports two state machines, the CPU State Machine and the DMA State Machine. The control logic automatically selects the proper state machine for the CPU or DMA cycles. No clock switching is involved when transitioning from the CPU to the DMA state machine, eliminating clock synchronization delays.

2.1 CPU State Machine

Interface to the 80386 requires interpretation of the 80386 status lines -ADS, M/-IO, D/-C, W/-R during the T1 (non-pipelined) cycle and the synchronization and generation of -READY to the CPU upon the completion of the cycle. The CPU initiates a cycle by driving the -ADS, M/-IO, W/-R and D/-C lines. Upon detecting the start of a new cycle, the 82C321 monitors the -AF32 input to determine if the current access is a local memory cycle or an MCA access. If -AF32 is sampled active, the CPU state machine waits for -READY from the memory controller to terminate the cycle. For all other cycles, (-AF32 inactive), the 82C321 generates the various MCA timing signals including the Matched Memory Cycle, Fast VGA Cycle timing. 82C321 also generates timing signals for Fast Matched Memory cycles. It subsequently generates -READY signal to the CPU to terminate the cycle.

The 82C321 supports 8, 16 and 32-bit transfers between the processor and the MCA I/O or memory adapter cards. The Action Code (AC<1:0>) outputs are used by the 82C325 for bus sizing and conversions.

2.2 MCA Default Cycle

At 16 and 20 MHz operation, two CPU wait states are required for generating the default MCA Cycle. At 25 MHz, three wait states are required in pipeline mode. One more additional wait state is required in non pipeline mode. If delayed sampling of -AF32 is enabled @ 20 or 25 MHz, 3 wait states are required @ 20 MHz, and 4 wait states are required @ 25 MHz. There is always the addition of 1 wait state in the non pipeline mode.

The MCA cycle is initiated when -AF32 is sampled inactive. The status lines -S0, -S1 and M/-IO to the MCA are generated by decoding the -ADS, W/-R, M/-IO and D/-C (when CPU is in control). When The DMA controller is in control, the 82C321 buffers the -LS0, -LS1, LM/-IO to generate the -MS0, -MS1 and MM/-IO outputs to the MCA. When external Master is in control, it drives the -MS0, -MS1, MM/IO inputs and 82C321 passes these inputs on to -LS0, -LS1 and LM/-IO signals respectively.

When the CPU is in control LS0, and LS1 are not asserted during interrupt acknowledge or during second and subsequent bus convert cycles.

When the CPU is in control, the latched status information is made available on the MCA. the 82C321 subsequently generates -ADL and -CMD. The signal timings conform to MCA timing specifications.

When the 82C321 is programmed in 25 or 20 Mhz mode and if the CPU is running at 25 or 20 Mhz, the delayed sampling of -AF32 should be enabled to generate timings conforming to MCA specification. This option is enabled by setting bit 6 in Register R1 (index 8E) to 1. This option when activated delays the sampling of -AF32 by one CLK2 period and also inserts one CPU wait state in all MCA cycles. This also results in delaying all MCA signals by one CLK2 period and also increases the -CMD pulse width by one CLK2.

The 82C321 generates EALE for all MCA accesses . EALE is low at the start of the cycle to allow the processor addresses to flow through to the MCA. EALE is driven high to latch the processor addresses. EALE is de-asserted a minimum of 30 ns after the de-assertion of -ADL to conform to MCA specifications (MCA requires a 30 ns address hold time following the removal of -ADL).

-CHRDYRTN is sampled by the 82C321 to determine if the current cycle can be completed within the default 200 ns timing. If -CHRDYRTN is active, the 82C321 activates -READY at the start of T2 or T2P to terminate the cycle. -CHRDYRTN is a "NANDED" function of all the CDCHRDY <1:8>, DMARDY, MEMRDY and VGARDY signals. If -CHRDYRTN is sampled inactive, then additional wait states are introduced.

DS16RTN and DS32RTN are sampled by the 82C321 to determine the data size of the accessed device. If DS32RTN and DS16RTN are sampled active, then the 82C321 assumes the current access is to a 32-bit device. If DS32RTN is inactive and DS16RTN is active, then the current access is to a 16-bit device. If both DS32RTN and DS16RTN are sampled inactive, then an 8-bit device is assumed. The 82C321 monitors these inputs to generate the corresponding action codes to the 82C325 for bus sizing and conversion. For example, if the current access is a 32-bit access from a CPU to an 8-bit device, the 82C321 generates the appropriate control signals to enable four back to back cycles, before generating -READY to the CPU to terminate the cycle.

The 82C321 receives the On Board I/O Peripheral (-OBIOP) signal, when the I/O address is less than 03FFH. It is used to determine if the current access is to the local devices and the peripheral devices. The 82C321 considers the Timer, Serial Port, Diskette Controller, Interrupt Controller, Real Time Clock, CMOS RAM and Keyboard Controller as Peripheral I/O devices.

All I/O addresses that are below 03FFH and are not peripheral devices are considered as on board devices. The -OBIOP is active from 0 to 03FFH. The 82C321 generates -XIORD and -XIOWR signals for all I/O accesses, and they are valid for the duration -CMD1 is valid. The CPU cycle time and -CMD1 pulse width for on board I/O and peripherals varies with the frequency of operation and are listed below, where cycle time and pulse width are in nsec and frequency in Mhz.

ITEMS	ON BOARD DEVICES			PERIPHERAL DEVICES		
Frequency (MHz)	**16**	**20**	**25**	**16**	**20**	**25**
Cycle time (ns)	437.5	400	360	562.5	550	520
-CMD pulse (ns)	312.5	275	260	437.5	425	420
Wait states	5	6	7	5	9	11

NOTE: The above numbers refer to the CPU in the pipeline mode, and when the delayed sampling of -AF32 option is enabled at 20 and 25 MHz.

2.3 DMA State Machine

The DMA State machine is driven by the DMACLK2 input from the 82C223 DMA controller. It operates asynchronously to the CPU state machine. The DMA state machine monitors the HLDA and -MASTER inputs to determine if it should generate the control signals for the current access. Control is passed to the DMA state machine when HLDA is active and -MASTER is inactive. When the 82C321 detects valid inputs on -LS0, -LS1 and LM/-IO, it generates -ADL and -CMD. The status and address information are allowed to flow through to the MCA. -CMD is held valid for the duration of the cycle. If the current access is to an I/O device, the 82C321 activates the -XIORD or -XIOWR.

The 82C321 does not generate EALE for normal DMA cycles, not requiring bus conversion. EALE is generated when the DMA accesses an 8-bit device, wherein two 8-bit bus convert cycles are required. EALE is used to latch and maintain the address for the second cycle. -READY is activated to the DMA controller after the completion of the second cycle. During Refresh cycles -READY is generated by 321.

If -CHRDYRTN is sampled inactive, then additional wait states are introduced.

If DS16RTN is sampled active by the 82C321, then 16-bit transfer is assumed and no bus conversion cycles are performed. If DS16RTN is sampled inactive, then an 8-bit device is assumed the 82C321 performs the necessary bus steering and conversions.

3.0 MASTER CYCLES

The 82C321 provides complete support for external bus masters to access global resources on the system board. The bus master in control provides the required address, status and command signals.

The Bus Master requests control of MCA by activating the -PREEMPT line. The Central Arbitration Control Point (CACP) raises the ARB/-GNT line signifying the start of an arbitration cycle. The Master drives its arbitration level on to the 4 ARB pins in response to a high level on the ARB/-GNT line. If another device requests the bus, it drives its priority level on the ARB <3:0> pins. Each competing device compares the level it is driving on the pins with the levels already on the pins. If the device priority is higher than what is being presented on the bus, that device is declared the winner. If the device sees a higher priority on the bus than it is asserting, then it is declared a looser.

At the end of arbitration cycle, ARB/-GNT is driven low, indicating the end of the arbitration cycle and the winner of the arbitration process raises its -PREMPT line.

The Bus Master can access system board peripherals or memory via the 82C321. Two basic cycles are supported:

1. Accessing local memory controlled by 82C322
2. Accessing on-board peripherals

3.1 Local Memory Access

The Bus Master in control of the MCA, drives valid addresses -MS0, -MS1 and -MM/-IO status lines, -ADL and -CMD signals on the MCA for the desired memory access. The 82C322 and the 82C321 receive -MS0, -MS1 and MM/-IO from the MCA. The 82C322 monitors the address and status information being presented to determine if the address requested resides in its memory space, and if so, it asserts the -RAS, -CAS and -WE signals to the DRAMs. 82C322 drives the MEMRDY signal inactive at the start of the cycle and activates it at the end of the cycle. The -MEMRDY signal is factored into the CHRDYRTN (Note: The MCA receives CHRDYRTN and the 82C321 receives -CHRDYRTN) signal. The -MASTER samples the CHRDYRTN signal and if inactive extends the cycle. The MASTER initiated memory access is terminated 60 ns(minimum) after CHRDYRTN is sampled active.

The 82C322, in response to memory requests from the MCA drives -AF32 active. External Bus Masters should monitor the -DS32RTN,s and -DS16RTN lines to determine the data sizing of the current access and perform the necessary bus steering.

If the current bus master is 16-bits (as determined by the polarity of MTR32 input), the 82C321 generates the Action Codes to perform the necessary bus steering.

3.2 On-Board Peripherals

The Bus Master in control can access the on board peripherals, except peripherals residing in 00 to 0FFH address space (This is a programmable option, where the 82C223 could be programmed for MASTER to access DMA registers). It requires CPU intervention to access the DMA controller, the interrupt controller and other on-board peripherals residing below 0FFH. The Bus Master asserts valid address, status and control signals to access on board peripherals. The 82C321 samples -MS0, -MS1,-MM/IO,-ADL,-CMD inputs from the MCA. The 82C322 asserts -OBIOP signal to 82C321. The 82C321 generates the appropriate -XIORD or -XIOWR signals to the selected I/O peripherals (For all I/O cycles -XIORD or -XIOWR is generated). -CMD1 is used to gate the -XIORD and -XIOWR signals. -XIORD or -XIOWR are also generated when accessing programmable I/O ports PGMP0-2 (defined in 82C325).

Additionally, for Master cycles the 82C321 de-asserts BDRDY output at the start of the cycle. The BDRDY is factored into the -CHRDYRTN logic. When BDRDY goes active the -CHRDYRTN is sampled active and subsequently, the cycle is terminated.

When accessing 8-bit devices, DS16RTN and DS32RTN (inputs to the 82C321, the MCA receives -DS16RTN and -DS32RTN) are both sampled inactive. The 82C321 generates the appropriate Action Codes to perform the necessary bus steering operations. The MASTER samples the -DS16RTN and -DS32RTN to determine the data sizing of the current transaction. The MASTER performs the necessary bus conversion cycles.

4.0 Bus Conversion

The 82C321 provides a means for the system to perform 32 or 16-bit transfers to 16 or 8-bit devices. The Conversion Logic will detect when a conversion is necessary, signal the Wait State Control Logic to assert wait states to the CPU, and perform the conversion by manipulating the SA1, SA0 and -BHE output pins. During a bus conversion cycle, the CPU is held in a wait condition, with -READY inactive. The 82C321 determines the number of conversion cycles to be performed for the access, and generates the correct action codes and address information for each of the convert cycles.

For example, if a 32 bit access is performed to a 16-bit device, the 82C321 will detect DS32RTN inactive and DS16RTN active. It will perform two bus convert cycles. The sequence of events for the bus convert process, when the processor is in control, are described as follows. Refer to Figure 1-4.

1. The 82C321 samples -AF32 after detecting a valid cycle. If -AF32 is sampled inactive, then a non-local memory access is assumed.

2. EALE is low to allow the processor addresses to flow through to the MCA. It is driven high to latch the processor address and maintain it for the duration of the bus convert cycle. EALE is driven low in the middle of the last bus convert cycle, ensuring 30 ns address hold time following the de-activation of -ADL.

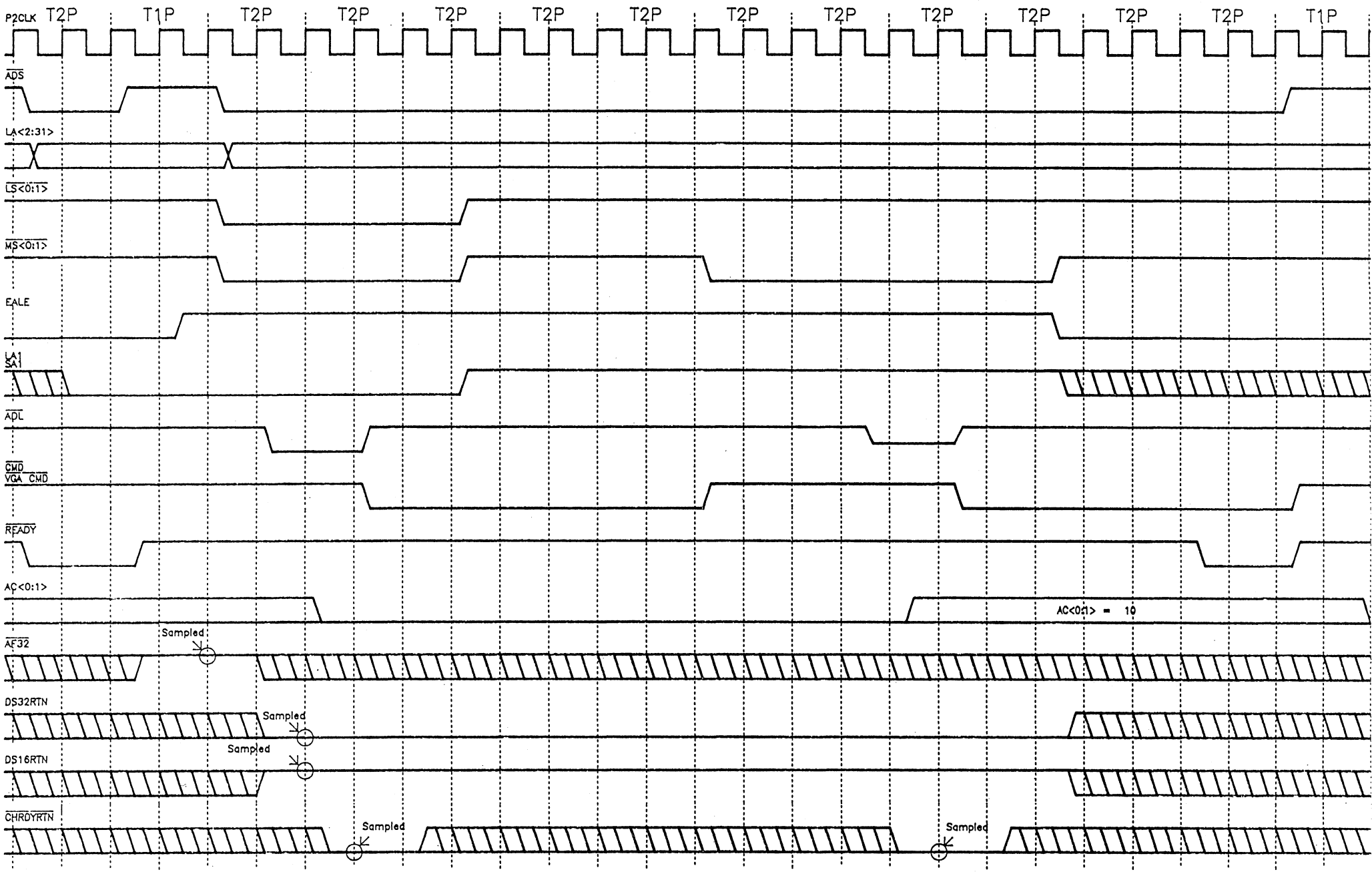


Figure 1.4 CPU Bus Convert Cycle

32 bit access to 16 bit device, 25 MHz Mode (AF32 option enabled)

3. It then samples DS16RTN and DS32RTN to determine if the current access is to an 8, 16 or 32-bit device. The BE<0:3> informs the 82C321 if the current access is a 32, 16 or an 8 bit access. Bus conversion cycles are performed for the following cases:

   a. 32-bit access to an 8 or 16-bit device
   b. 16-bit access to an 8-bit device
   c. 24-bit access to 8 or 16-bit device
   d. 16-bit cross word (BE1 & BE2 active) to 16-bit device.

If DS16RTN is sampled active and DS32RTN sampled inactive, and BE<3:0> are active, then two bus convert cycles are performed. -S0, -S1, -ADL and -CMD are asserted for each cycle, and removed at the end of the cycle. The SA0, SA1 are manipulated to access the correct locations. Example, when performing 32-bit access to 16-bit EPROMs, the SA1 is zero for the first access and one for the subsequent access.

At the completion of the last bus convert cycle, the -READY is generated to the processor to terminate the cycle.

5.0 MATCHED MEMORY CYCLES

Matched Memory Cycles are allowed only for 16 or 32 bit Slave Devices and are only permitted when the CPU is in control. Matched Memory cycles allow for efficient data transfer between memory cards residing on the MCA and the system processor.

Matched Memory Cycle output to the MCA is active only when the CPU is in control. It is generated by HLDA (Hold Acknowledge, -MMC is inversion of HLDA). When HLDA is active, either when DMA or an external Bus Master is in control of the MCA, -MMC is inactive, indicating to the slave device that no matched memory cycles will be performed.

Matched Memory Cycles require one wait state at 16 MHz 20 Mhz, or 25 Mhz when enabled.The adapters residing on the MCA have to request a MMC (Matched Memory Cycle) on a cycle by cycle basis.

On the MCA, the address and the status information become available at the beginning of an MCA cycle. The 82C321 activates -MMC output, when the CPU is in control of the bus. The Adapter card should monitor the -MMC output to determine if it can initiate a Matched Memory Cycle By asserting -MMCR.

When the 82C321 samples MMCR active (high), it activates -MMMCMD. The -MMMCMD informs the adapter cards that data is valid on the Bus. The trailing edge indicates the end of the cycle.

The Matched Memory cycle can be extended by asserting -CHRDYRTN. The Matched Memory Cycle can be disabled or enabled by programming the register R2(index 8F). When disabled(bit 0 of R2 = 0) the default cycles are performed(250 ns @ 16Mhz, 250 ns @ 20MHz, and 240ns @ 25 Mhz), when enabled(bit 0 = 1) Matched Memory cycles are performed(187.5ns @ 16 Mhz,150ns @ 20 Mhz and 120 ns @ 25 Mhz)

6.0 FAST VGA CYCLE

The cycle time for normal VGA I/O accesses is the default cycle time (250 ns @ 16 MHz, 250 ns @ 20 MHz, and 240 ns @ 25 MHz). The 82C321 supports a special fast protocol for the VGA I/O accesses to cut down VGA I/O cycle time. Two pins, -VGAREQ and -VGACMD are reserved for this purpose. The VGA will request a fast cycle with -VGAREQ signal and -VGACMD provides the strobe. The s
fast VGA cycle can be activated by enabling the generation of VGAREQ on the 82C451/452, and enabling the fast VGA cycle on the 82C321 by setting bit 1 in R2 register (Index 8F).

When the fast VGA cycle is enabled, the 82C321 samples -VGAREQ and if -VGAREQ is active, 82C321 performs fast VGA cycles. During fast VGA cycles, -CMD1 and -ADL are not generated but status -MSO, -MS1, and -VGACMD are generated. The cycle time for fast VGA cycles is 187.5 ns @ 16 MHz, 150 ns @ 20 MHz and 120 ns @ 25 MHz (AF32 option disabled). When delayed, AF32 option is enabled @ 20 and 25 MHz. The cycle time for fast VGA cycle is 200 ns @ 20 MHz and 160 ns @ 25 MHz.

The option of fast VGA cycles are not restricted to VGA accesses only. If the -VGAREQ and -VGACMD timings are met any I/O device can run a fast cycle. The Fast VGA cycle can be extended by activating CHRDYRTN.

7.0 NUMERIC COPROCESSOR INTERFACE

Incorporated on the 82C321 is the circuitry to interface the 80387 Numeric Coprocessor to the 80386. The circuitry handles the decoding required for selecting and resetting the numeric coprocessor. The 82C321 also handles -NPBUSY and -ERROR signals from the 80387.

The 82C321 automatically recognizes the presence of the 80387, using a mechanism similar to the 80386 numeric coprocessor detection logic. It samples ERROR output of the 80387 on the falling edge of reset to detect the presence or absence of the 80387.

It supports two methods of -READY generation

1. The 82C321 generates -READY for all numeric coprocessor accesses. The bit 5 of System Speed Register R1 should be set to 0 for this option.

2. The -READY of the 80387 can be used to generate the -READY for numeric coprocessor cycles. This option provides better performance for numeric operations as the number of wait states for NP cycles can be controlled. In order to use this option bit-5 of Register R1 should be set to 1 and also the READY interface circuit as suggested by the manufacturer of 80387 should be implemented. The READY generated by the interface circuit is connected to the CPU READY through a tristate buffer which is enabled when the input signal (which is READY of interface circuit) is present.

Miscellaneous Ports: The 82C321 responds to various miscellaneous ports such as port 61, 92, and 94. The details are listed at the end of this manual.

8.0 82C321 PIN DESCRIPTIONS

CLOCKS

Symbol	Type	PGA	PFP	Description
CPUCLK2	I	26	79	CPU CLOCK 2 input from the 82C322) Memory Controller or from an external clock source, having a maximum frequency of twice the rated frequency of the 80386 processor clock. It is referred to as PCLK2 throughout this document.
DMACLK2	I	63	62	DMA CLOCK2 input from the 82C223 DMA Controller (20MHz). This clock input is used for the DMA state machine.
DMACLK4	O	6	38	DMA CLOCK4 output is used to drive the Keyboard controller clock. It is half the frequency of DMACLK2 and has a duty cycle of approximately 50%.
OSC/12	I	38	4	OSCILLATOR CLOCK /12 is the 1.19 MHz TTL level clock input from the 82C322.

CONTROL

Symbol	Type	PGA	PFP	Description
-RESET1	I	5	35	RESET1 is an active low input generated by the power good signal of the power supply. When low, it activates RESET3 and RESET4.
-RESET2	I	89	36	RESET2 is an active low input(8042) generated from the keyboard controller for a "warm reset" not requiring the system power to be shut off. It forces a CPU reset by activating RESET3.

CONTROL (continued)

Symbol	Type	PGA	PFP	Description
RESET4	O	72	84	RESET4 is an active high output used to reset the MCA, 82C226, 8042 keyboard controller, and the 82C322 memory controller. It is synchronized with the processor clock.
RESET3	O	27	81	RESET3 is an active high output to the 80386 when RESET1 or RESET2 is active. It is also activated when a shut-down condition in the CPU is detected or when I/O port 92H, bit 0 is set from zero to one.

CPU INTERFACE

Symbol	Type	PGA	PFP	Description
-READY	I/O	68	76	READY is an open drain output, and is driven low to terminate the current CPU or DMA cycle after -CHRDYRTN is low. When -AF32 is sampled active, then it is an input from the 82C322. It is connected to the 80386 -READY pin and is normally inactive.
-LS0	I/O	18	63	LOCAL STATUS active low.
-LS1	I/O	64	64	The local status signals, when output, are used by the 82C223 DMA controller during DMA register accesses, CPU or MASTER cycles. These signals are inputs during DMA operation. Pull up resistors of 10K Ohms are required for these signals.

CPU INTERFACE (continued)

Symbol	Type	PGA	PFP	Description
LM/-IO	I/O	94	69	Local MEMORY INPUT/OUTPUT when high, indicates a memory access. When low, it indicates an I/O access. It is used to generate memory and I/O signals for the system. It is output for MASTER cycles and input for CPU and DMA cycles. A pull up resistor of 10K Ohms is required for this signal.
-MBHE	I/O	10	47	BYTE HIGH ENABLE is an active low signal which indicates the transfer of data on the upper byte of a 16 bit data word. It is an input during DMA and MASTER cycles, and an output during CPU cycles. A pull up resistor of 10K Ohms is required for this signal.
-LBE0	I/O	23	74	LOCAL BYTE ENABLE 0 is an active low input from the 80386 CPU indicating data transfer on the lowest byte. It i s an output during DMA and MASTER cycles for the 82C322 Memory Controller.
-LBE1	I/O	67	73	LOCAL BYTE ENABLE 1 is an active low input from the 80386 CPU indicating data transfer on the second lowest byte. It is an output during DMA and MASTER cycles for the 82C322 Memory Controller.
-LBE2	I/O	22	72	LOCAL BYTE ENABLE 2 is an active low input from the 80386 CPU indicating data transfer on the second highest byte. It is an output during DMA and MASTER cycles for the 82C322 Memory Controller.

CPU INTERFACE (continued)

Symbol	Type	PGA	PFP	Description
-LBE3	I/O	66	71	LOCAL BYTE ENABLE 0 is an active low input from the 80386 CPU indicating data transfer on the highest byte. It is an output during DMA and MASTER cycles for the 82C322 Memory Controller.
-ADS	I	24	75	ADDRESS STATUS is an active low signal from the 80386 CPU indicating the initiation of a CPU cycle.
W/-R	I	21	70	WRITE/READ is input from the CPU. When low, it indicates a write cycle. When high, it indicates a read cycle.
D/-C	I	65	68	DATA/CONTROL is input from the CPU. When high, it indicates a data transfer. When low, it indicates a control transfer.
-INTA	O	98	11	INTERRUPT ACKNOWLEDGE is an active low output to the interrupt controller of the 82C226 (IPC2), in response to an interrupt request.

MCA INTERFACE

Symbol	Type	PGA	PFP	Description
BDRDY	O	42	13	BOARD READY is an active high output. When low it indicates a local device not-ready condition leading to wait state generation via the MCA -CHRDYRTN signal, to external MASTERs. When high it allows termination of the current local cycle.

MCA INTERFACE (continued)

Symbol	Type	PGA	PFP	Description
-CHRDYRTN	I	41	10	CHANNEL READY RETURN is an active low input. It is derived from NANDing the -CD CHRDY inputs from all the MCA connectors, and other on board ready signals (like DMASRDY from 82C223, MEMRDY from 82C322 etc.).
-MADL	O	75	93	ADDRESS DECODE LATCH is an active low output. It controls the address latches used to hold the addresses during bus cycles. This signal is inactive for Matched Memory Cycles.
EALE	O	76	96	EXTERNAL ADDRESS LATCH ENABLE is an active high output used to latch the LA2-LA31 address lines (from CPU), to the A2-A31 lines on the MCA.
-MBE0 -MBE1 -MBE2 -MBE3 -MS0 -MS1	I/O I/O I/O I/O I/O I/O	56 9 91 55 29 95	46 45 44 43 85 86	M BUS STATUS lines are active low. These lines are output for CPU, DMA and Refresh cycles and input for MASTER cycles.
-CMD1	O	74	89	M BUS COMMAND is active low, indicating when data is valid on the data bus. The trailing edge indicates the end of a cycle. It is output for CPU, DMA and Refresh cycles, and input for MASTER cycles. This signal could be used by the slaves to latch the address on the MCA bus.

MCA INTERFACE (continued)

Symbol	Type	PGA	PFP	Description
-MMMCMD	O	54	39	M BUS MATCHED MEMORY COMMAND is an active low output signal,indicating that data is valid on the data bus for matched memory cycles. Valid address has to be latched on the leading edge. It is output for CPU cycles only.
MMCR	I	8	42	MATCHED MEMORY CYCLE REQUEST is an active high input from the MCA logic from 32 bit slaves requesting a matched memory cycle.
MTR32	I/O	57	48	M BUS TRANSLATE 32 is an active high signal. It is low output for CPU, DMA and Refresh cycles, and input for MASTER cycles. When a 16-bit MASTER (or DMA) is active the MTR32 is tristated, and remains high hence a 10K Ohm pull up resistor is required to make MTR32 tristate active high. If a 32 bit MASTER is active, the MTR32 pin is tristated (but goes high due to pull up), the MASTER drives MTR32 low.

MCA INTERFACE (continued)

Symbol	Type	PGA	PFP	Description
DS16RTN	I	40	8	DATA SIZE 16 RETURN is an active high input. It is derived from "NAND"ing the -CDDS16 inputs from all the MCA connectors,and other on board DS16 signals (like DMADS16 from the 82C223,VGADS16 from 82C322 etc.). If only DS16RTN is high, it indicates a 16-bit data transfer request. If DS16RTN and DS32RTN are high, it indicates a 32-bit data transfer request.
DS32RTN	I	82	9	DATA SIZE 32 RETURN is an active high input It is derived from NANDing the - -CD DS32 inputs from all the MCA connectors DS32RTN indicates a 32-bit data transfer request.
-BTO	I	62	59	BUS TIME-OUT is an active low input from the DMA controller, indicating that a bus time out has occurred and the current I/O cycle should be terminated. It terminates -XIORD or -XIOWR signal.
SA0 SA1	I/O I/O	97 33	94 95	ADDRESS LINES SA0, SA1 These lines are output for CPU and DMA cycles and are latched. They are buffered to generate the MCA address lines A0, and A1. They are input for Master cycles.
LA0 LA1	I/O I/O	17 92	60 61	LOCAL ADDRESS LINES LA0, LA1. CPU and MASTER cycles to the 82C223 DMA Controller, and input for DMA, and Refresh cycle from the DMA Controller.

MCA INTERFACE (continued)

Symbol	Type	PGA	PFP	Description
LA31	I	71	82	LOCAL ADDRESS LINE LA31 is input from the 80386 for CPU cycles to identify 80387 accesses. It should be pulled up with a 4.7K Ohm resistor.
-LBHE	I/O	20	67	LOCAL BTYE HIGH ENABLE from the 82C223 DMA controller, used to generate action codes. -LBHE is an output during CPU cycles generated by decoding -LBE<0:3>.
SYSSTA	O	83	12	SYSTEM STATUS is an active high output indicating a system disk access.

DMA INTERFACE

Symbol	Type	PGA	PFP	Description
HLDA	I	70	80	HOLD ACKNOWLEDGE is an active high input generated by the CPU, relinquishing the bus to the DMA controller or to an external MASTER.

DMA INTERFACE (continued)

Symbol	Type	PGA	PFP	Description
HLDAO	O	32	92	HLDAO is active high output generated by 321 in response to HLDA input from CPU. This output goes to HLDA of 82C223. This makes sure that HLDA to the 82C223 is not deasserted (until the DMA cycle is complete) when CPU is reset.
-MASTER	I	16	58	MASTER is an active low input indicating that a MASTER device on the MCA is in control of the system.
-RFSH	I	34	97	REFRESH is an active low input from the DMA controller initiating a system refresh cycle. This input is registered in bit 4 of Port 61.
-DSKDACK	I	61	57	DISK CONTROLLER DMA ACKNOWLEDGE from the DMA Controller is an active low input. This introduces additional wait states when accessing the floppy disk controller during DMA operations.

MEMORY CONTROL

Symbol	Type	PGA	PFP	Description
-AF32	I	30	88	AF32 is an active low input from the 82C322 Memory Controller, indicating a 32 bit local DRAM access, and 82C322 generates ready for the CPU.
-OBIOP	I	28	83	ON BOARD I/O PORT is an active low input from the 82C322 Memory controller, indicating I/O access in the address range 0-3FF.
PGATEA20	I	53	37	PGATE A20 input active high from the 8042 Keyboard controller. This is ORred with bit 1 of Port 92 to generate GA20 signal to 322.
GATEA20	O	73	87	GATE A20 output to the 82C322 memory controller. When low, forces the LA20 line low and when high, it propagates the CPU A20 line. It is used to keep address under 1Mb in DOS environments. It is high for DMA and MASTER cycles. It is OR of GATEA20 input and bit 1 of Port 92. The actual gating of A20 is done in the memory Controller 82C322.

BUS INTERFACE

Symbol	Type	PGA	PFP	Description
-XIORD	O	11	49	X BUS I/O READ is an active low output strobe directing an I/O port to place data on the data bus.
-XIOWR	O	12	50	X BUS I/O WRITE is an active low strobe directing an I/O port to accept data from the data bus.

BUS INTERFACE (continued)

Symbol	Type	PGA	PFP	Description
XD0 XD1 XD2 XD3 XD4 XD5 XD6 XD7	I/O I/O I/O I/O I/O I/O I/O I/O	4 51 3 50 2 88 48 47	33 32 31 30 29 26 25 24	X DATA BUS bits <7:0> to access internal registers of the 82C321.
XA2 XA3 XA4 XA5 XA6 XA7 XA8 XA9	I I I I I I I I	43 44 85 100 45 86 46 87	16 17 18 19 20 21 22 23	X ADDRESS lines <2:9> to access the internal registers of the 82C321. These lines are also used to determine the address range, and introduce appropriate wait states during I/O cycles.
-BSEN	O	80	5	BUS STEERING ENABLE is an active low output, used by the MCA bus steering logic to enable a 16 bit Master to access the upper word of channel slaves. It is active when a 16-bit MASTER is accessing the upper word (when SA1 = 1).
-WDLTH	O	58	51	WRITE DATA LATCH ENABLE is an active low output, used by the 82C325 Data Buffer during CPU cycles, to meet the hold time for MCA write cycles. When high allows data to pass through. This signal is low when -CMD1 is low during CPU cycles, and is high during DMA/MASTER cycles.

BUFFER CONTROL

Symbol	Type	PGA	PFP	Description
SDIR	O	81	7	MCA DATA BUS DIRECTION output. A low sets the data path from the MCA to the MD bus. A high sets the data path from the MD bus to the MCA.
SDEN	O	39	6	Presently not used.
AC1 AC0	O O	60 14	5 54	ACTION CODE is a two bit encoded output for bus size control and byte assembly operations performed in the 82C325 Data Buffer.

COPROCESSOR INTERFACE

Symbol	Type	PGA	PFP	Description
-NPBUSY	I	77	98	NUMERICAL PROCESSOR BUSY is an active low input from the NPC, indicating that it is currently executing a command. It is used to generate the BUSY signal to the CPU. A 4.7K Ohm pull up resistor is required on this signal.
-NPERROR	I	35	99	NUMERIC PROCESSOR ERROR is an active low input from the NPC indicating that an unmasked error condition exists. A 4.7K Ohm pull up resistor is required on this signal.
NPRESET	O	36	100	NUMERICAL PROCESSOR RESET is an active high reset to the 80387. It is active when RESET3 is active or when a write operation is made to Port 0F1H. In the later case, it is active for a pre-defined period.

COPROCESSOR INTERFACE (continued)

Symbol	Type	PGA	PFP	Description
NPEXCPT	O	78	1	NUMERICAL PROCESSOR EXCEPTION is an active low output to the 82C226 IPC2. It is connected to the -IRQ13 line in a PS/2™ environment.

VGA INTERFACE

-VGAREQ	I	52	34	VIDEO GRAPHICS ADAPTER REQUEST is an active low input from the 82C451 VGA Controller, requesting a Fast VGA cycle. The 82C321 should be enabled to sample this input.
-VGACMD	O	15	56	VIDEO GRAPHICS ADAPTER COMMAND is an active low Fast VGA command indicating data transfer. During default cycles, -VGACMD is generated identical to CMD1. When fast VGA cycle is in progress only -VGACMD is generated. No -CMD1 is generated. This is also used as latching signal to drive XA <0:15> from MCA address bus.

POWER SUPPLIES

Symbol	PGA	PFP	Description
VDD	84 7 13 93 31 37	2 14 41 52 65 91	Power Supply
VSS	79 99 1 49 90 59 19 69 96 25	3 15 27 28 40 53 66 77 78 90	Ground

Table 2 lists the programming registers that are located on the 82C321 chip.

Table 2

Reg #	Register Name	Index	Location
R0	Version Register	8DH	82C321
R1	System Speed Select	8EH	82C321
R2	System Option Register	8FH	82C321

82C321 Register Descriptions

Version Register R0:

Index Register Port: 22H
Data Register Port: 23H
Index: 8DH (Read Only)

Bits	Value	Function
1,0		82C321 version number (R)
	0,0	Initial version
	0,1	Reserved
	1,1	Reserved
2-7		Reserved

System Speed Select Register R1:

Index Register Port: 22H
Data Register Port: 23H
Index: 8EH

Bits	Value	Function
1,0		Processor clock select (R/W)
	0,0	16MHz
	0,1	20 MHz
	1,0	25 MHz
	1,1	Reserved
2,3		Reserved
4		Indicates presence of 80387 Numeric coprocessor following power up.
	1	80387 Numeric coprocessor installed.
	0	80387 Numeric coprocessor not installed.
5		Math Ready
	1	Numeric coprocessor generates Ready. (Default)
	0	82C321 generates Ready

System Speed Select Register R1: (continued)

Bits	Value	Function
6		This bit enables the delayed sampling of -AF32 signal used when the CPU clock is at 20 or 25 MHz. Setting of this bit delays the sampling of -AF32 by one CLK2 and also inserts one wait state in all bus cycles. It also delays generation of all MCA signals by one CLK2 cycle. -CMD pulse width increases by one CLK2.
	1 0	Enabled (Default) Disabled
7		Reserved

System Option Select Register R2:

Index Register Port: 22H
Data Register Port: 23H
Index: 8FH

Bit	Value	Function
0		Matched Memory Cycle Timing select (R/W). The default = 0 = 250 ns cycles at 16 MHz, 250ns cycles @ 20 Mhz and 240 at 25 MHz. When set to one, the cycles are as follows: 187.5ns @ 16 MHz, 150ns @ 20 MHz and 120ns at 25 MHz.
	0 1	Matched Memory Cycle disabled. (Default) Matched Memory Cycle enabled.
1		VGA Enable bit (R/W). When this bit is set to 1, it enables a fast VGA cycle. The cycle may be extended by using the CHRDY.
	0 1	Disabled fast VGA cycle. (default) Enabled (Enables a fast VGA cycle. The cycle may be extended by using the CHRDY.
2		Data Ready Extend (R/W). When this bit is set to one it inserts one wait state after the 82C321 samples CHRDY active. It provides extended data set-up time for read cycles only.
	0 1	Data Ready extend disabled. Data Ready extend enabled. (Default)
3-7		Reserved

82C321 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	-	7.0	V
Input Voltage	V_I	-0.5	VCC + 0.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{OP}	-25º	85º	C
Storage Temperature	T_{STG}	-40º	125º	C
Maximum Power Dissapation		-	TBD	

NOTE: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C321 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	VCC	4.75	5.25	V
Ambient Temperature	T_A	0º	70º	C

82C321 DC Characteristics

Operating Conditions: T_A =0ºC to 70ºC, VCC = 4.75 to 5.25V

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}	-0.5	+1.5	V
Input High Voltage	V_{IH}	+1.2	VCC+0.5	V
Output Low Voltage	V_{OL}	-	+0.45	V (Note 1)
Output High Voltage	V_{OH}	2.4	-	V (Note 1)
Input Leakage Current $0<V_{IN}<V_{CC}$	I_{IL}	-10	+10	uA
Power Supply Current @ 16MHz	I_{CC}	TBD	-	mA
Output High-Z Leakage Current $0.45<V_{OUT}<V_{CC}$	I_{OZ1}	-10	-10	uA

Note 1: I_{OL} = 8mA and I_{OH} = -8mA for -MADL, -CMD1, -MMMCMD, and -VGACMD
I_{OL} = 4mA and I_{OH} = -4mA for all other output pins

CLOCKS	Min	Max	Unit	Notes
t100 PCLK2 period	31		ns	
t101 PCLK2 low time	9		ns	At 2V
t102 PCLK2 high time	9		ns	At 2V
t103 PCLK2 rise time		8	ns	0.8 to VCC -0.8V
t104 PCLK2 fall time		8	ns	VCC -0.8 to -0.8V
t105 DMACLK2 period	50		ns	
t106 OSC/12 period	840		ns	
t107 DMACLK2 low time	12		ns	At 2V
t108 DMACLK2 high time	16		ns	At 2V
t109 DMACLK2 rise time		8	ns	0.8 to VCC -0.8V
t110 DMACLK2 fall time		8	ns	VCC -0.8 to -0.8V

RESET TIMINGS	Min	Max	Unit	Notes
t111 -RESET2 pulse width	3CLK2			
t112 RESET3 active delay from PCLK2		29	ns	
t113 RESET3, RESET4 inactive delay from PCLK2		36	ns	
t114 -RESET1,-RESET2 set-up time to PCLK2	31.5		ns	
t115 RESET4, RESET3 pulse width		128	PCLK2	

(T_A = 0°C to 70°C, VCC = 5V + 5%, A.C. load = 85pf)

CPU CYCLES:

INPUT REQUIREMENTS	Min	Max	Unit	Notes
t120 -AF32 setup to PCLK2	10		ns	
t121 -AF32 hold from PCLK2	5		ns	
t123 -DS16RTN ,DS32RTN setup to PLCK2	11		ns	
t124 -DS16RTN, DS32RTN hold from EALE*	5		ns	
t125 -CHRDYRTN setup to PCLK2	10		ns	
t126 -CHRDYRTN hold from PCLK2	10		ns	
t127 -READY setup to PCLK2	10		ns	
t128 -READY hold from PCLK2	8		ns	
t129 -ADS setup to PCLK2	22		ns	
t130 -ADS hold from PCLK2	6		ns	
t131 LM/-IO setup to PCLK2	22		ns	
t132 LM/-IO hold from PCLK2	6		ns	
t133 -LBE<0:3>, LA31 setup to PCLK2	26		ns	
t134 -LBE<0:3>, LA31 hold from PCLK2	4		ns	
t135 W/-R setup to PCLK2	22		ns	
t136 W/-R hold from PCLK2	6		ns	
t137 D/-C setup to PCLK2	22		ns	
t138 D/-C hold from PCLK2	6		ns	
t139 MMCR setup to PCLK2	10		ns	
t140 MMCR hold from PCLK2	10		ns	
t143 HLDA setup to PCLK2**	10		ns	
t151 -OBIOP setup to PCLK2	10		ns	

INPUT REQUIREMENTS (continued)	Min	Max	Unit	Notes
t155 -VGAREQ setup to PCLK2	10		ns	
t156 -VGAREQ hold from PCLK2	10		ns	

OUTPUT DELAYS:	Min	Max	Unit	Notes
t160 -MS0,-MS1,-LS0,-LS1 active from PCLK2		30	ns	
t161 -MS0,-MS1,-LS0,-LS1 inactive from PCLK2	5	25	ns	
t162 SA<1:0> valid delay from BE<0:3>		40	ns	
t163 -MADL active delay from PCLK2		22	ns	
t164 -MADL inactive delay from PCLK2		30	ns	
t165 -CMD1 active delay from PCLK2		27	ns	
t166 -CMD1 inactive delay from PCLK2		25	ns	
t167 -XIORD,-XIOWR active from PCLK2		40	ns	
t168 -XIORD,-XIOWR inactive from PCLK2		40	ns	
t169 SDIR active delay from PCLK2		45	ns	
t170 SDIR inactive delay from PCLK2		45	ns	
t171 -READY active delay from PCLK2		31	ns	
t172 -READY inactive delay	4	25	ns	
t173 EALE active from PCLK2		45	ns	
t174 EALE inactive from PCLK2	9	35	ns	
t176 AC<1:0> active delay from PCLK2		34	ns	
t177 AC<1:0> inactive from PCLK2		40	ns	
t178 -INTA active delay from PCLK2		40	ns	
t179 -INTA inactive delay from PCLK2		40	ns	

OUTPUT DELAYS: (continued)		Min	Max	Unit	Notes
t180	-WDLTH active delay from PCLK2		50	ns	
t181	-WDLTH inactive delay from PCLK2		50	ns	
t182	-MBE<3:0> active delay from BE<3:0>		50	ns	
t183	-LBHE, -MBHE active delay from BE<3:0> valid		50	ns	
t185	-VGACMD active delay from PCLK2		30	ns	
t186	-VGACMD inactive delay from PCLK2		30	ns	
t187	MTR32 active delay from HLDA		30	ns	
t188	MTR32 inactive delay from HLDA		30	ns	
t189	-MMMCMD active from PCLK2		20	ns	
t190	-MMMCMDinactive from PCLK2		20	ns	
t191	HLDAO active from HLDA		6	PCLK2	
t192	HLDAO inactive from HLDA		30	ns	

ACCESS TO INTERNAL REGISTERS		Min	Max	Unit	Notes
t200	GATEA20 delay from rising edge of XIOWR (Register bit to output pin)		50	ns	
t201	GATEA20 active delay from PGATEA20		40	ns	
t202	GATEA20 inactive delay from PGATEA20		40	ns	
t203	Valid read data from -XIORD active		50	ns	
t204	Read data invalid from -XIORD inactive		50	ns	
t205	SYSSTA active from -XIOWR		25	ns	
t206	SYSSTA inactive from -XIOWR		25	ns	

DMA CYCLES :

INPUT REQUIREMENTS	Min	Max	Unit	Notes
t210 -LS0,-LS1 active setup to DCLK2	35		ns	
t211 - LS0,-LS1 hold from DCLK2	15		ns	
t212 LA<0:23> setup to DCLK2	15		ns	
t213 LA<0:23> hold from DCLK2	5		ns	
t214 -LBHE setup to DCLK2	35		ns	
t216 DS16RTN,DS32RTN setup to DCLK2	21		ns	
t218 CHRDYRTN setup to DCLK2	10		ns	
t219 CHRDYRTN hold from DCLK2	10		ns	
t220 LM/IO setup to DCLK2	10		ns	
t221 LM/IO hold from DCLK2	5		ns	

OUTPUT DELAYS (continued)	Min	Max	Unit	Notes
t230 -MS0,-MS1,MM/-IO valid delay from -LS0,-LS1,LM/-IO active		30	ns	
t231 -MS0,-MS1,MM/-IO inactive delay from DMACLK2		30	ns	
t232 SA<1:0> delay from LA<1:0> valid		30	ns	
t253 -MBE,LBE<0:3> active delay from LA0, LA1, BHE		34	ns	
t254 -MBE, LBE<0:3> inactive delay from LA0, LA1, BHE		25	ns	
t255 -VGACMD active delay from DCLK2		40	ns	
t256 -VGACMD inactive delay from DCLK2		40	ns	
t257 -CMD1 active from DCLK2	8	30	ns	
t275 -CMD1 inactive from DCLK2		30	ns	
t258 -MADL active from DCLK2	5	30	ns	

OUTPUT DELAYS (continued)	Min	Max	Unit	Notes
t259 -MADL inactive from DCLK2		30	ns	
t260 EALE active from DCLK2		30	ns	
t262 EALE inactive from DCLK2		30	ns	
t263 AC<0:1> active delay from DS16/32RTN		34	ns	
t264 AC<0:1> inactive delay from DCLK2		40	ns	
t267 SDIR active delay from LS0, LS1		35	ns	
t268 SDIR inactive delay from CMD inactive		40	ns	
t269 -XIOWR active delay from DCLK2		40	ns	
t270 -XIOWR inactive delay from DCLK2		40	ns	
t271 -XIORD active delay from DCLK2		40	ns	
t272 -XIORD inactive delay from DCLK2		40	ns	
t273 -READY active delay from DCLK2		30	ns	
t274 -READY inactive delay from DCLK2		30	ns	
t276 -MBHE valid from LBHE valid		40	ns	

EXTERNAL MASTER:	Min	Max	Unit	Notes
t280 -LS0,-LS1,-LM/-IO valid delay from -MS0, -MS1, MM/-IO active		25	ns	
t281 -LS0, -LS1, -LM/-IO inactive delay from -MS0, -MS1, MM/-IO inactive		25	ns	
t282 LA0 valid delay from SA0, SA1 H to L		25	ns	
t283 LA0 inactive delay from SA0, SA1 L to H		25	ns	
t284 BSEN active delay from DS32RTN		18	ns	
t285 BSEN inactive delay from -ADL		25	ns	
t286 BDRDY inactive delay from -ADL		19	ns	
t288 -VGACMD active delay from -CMD1 active		20	ns	

EXTERNAL MASTER: (continued)		Min	Max	Unit	Notes
t289	-VGACMD inactive from -CMD1 inactive		20	ns	
t290	-XIORD active delay from -CMD1 active		25	ns	
t291	-XIORD inactive delay from -CMD1 inactive		25	ns	
t292	-XIOWR active delay from -CMD1 active		25	ns	
t293	-XIOWR inactive delay from -CMD1 inactive		25	ns	
t294	-CMD1 active to BDRDY active (for peripheral devices)	8	9	DCLK2	
t295	-CMD1 active to BDRDY active (for non peripheral devices)	1	2	DCLK2	

Numeric Coprocessor Interface		Min	Max	Unit	Notes
t296	-NPEXCPT active delay from NPBUSY inactive		25	ns	
t297	-NPEXCPT inactive delay from -XIOWR		25	ns	
t298	NPRST active delay from PCLK2		30	ns	
t299	NPRST pulse width		128	PCLK2	

NOTES:

1. The -OBIOP signal should be held active throughout the cycle.
2. The DSKDACK signal is an input (given by 82C223 DMA controller) to indicate 82C321 to introduce additional wait states in the DMA cycle for floppy disk controller accesses.
3. The -RFSH and -BTO are asynchronous inputs.

* The signal should be held active until EALE goes low.
** These are provided for testing purposes only.

(T_A = 0oC to 70oC, VCC = 5V + 5%, A.C. load = 85pf)

CLOCKS	Min	Max	Unit	Notes
t100 PCLK2 period	25		ns	
t101 PCLK2 low time	8		ns	At 2V
t102 PCLK2 high time	8		ns	At 2V
t103 PCLK2 rise time		8	ns	0.8 to VCC -0.8V
t104 PCLK2 fall time		8	ns	VCC -0.8 to -0.8V
t105 DMACLK2 period	50		ns	
t106 OSC/12 period	840		ns	
t107 DMACLK2 low time	12		ns	At 2V
t108 DMACLK2 high time	16		ns	At 2V
t109 DMACLK2 rise time		8	ns	0.8 to VCC -0.8V
t110 DMACLK2 fall time		8	ns	VCC -0.8 to -0.8V

RESET TIMINGS	Min	Max	Unit	Notes
t111 -RESET2 pulse width	3CLK2			
t112 RESET3 active delay from PCLK2		23	ns	
t113 RESET3, RESET4 inactive delay from PCLK2		36	ns	
t114 -RESET1,-RESET2 set-up time to PCLK2	25		ns	
t115 RESET4, RESET3 pulse width		128	PCLK2	

CPU CYCLES:

INPUT REQUIREMENTS	Min	Max	Unit	Notes
t120 -AF32 setup to PCLK2	10		ns	
t121 -AF32 hold from PCLK2	5		ns	
t123 -DS16RTN ,DS32RTN setup to PLCK2	10		ns	
t124 -DS16RTN, DS32RTN hold from EALE*	5		ns	
t125 -CHRDYRTN setup to PCLK2	10		ns	
t126 -CHRDYRTN hold from PCLK2	10		ns	
t127 -READY setup to PCLK2	10		ns	
t128 -READY hold from PCLK2	8		ns	
t129 -ADS setup to PCLK2	20		ns	
t130 -ADS hold from PCLK2	6		ns	
t131 LM/-IO setup to PCLK2	20		ns	
t132 LM/-IO hold from PCLK2	6		ns	
t133 -LBE<0:3>, LA31 setup to PCLK2	18		ns	
t134 -LBE<0:3>, LA31 hold from PCLK2	4		ns	
t135 W/-R setup to PCLK2	20		ns	
t136 W/-R hold from PCLK2	6		ns	
t137 D/-C setup to PCLK2	20		ns	
t138 D/-C hold from PCLK2	6		ns	
t139 MMCR setup to PCLK2	10		ns	
t140 MMCR hold from PCLK2	10		ns	
t143 HLDA setup to PCLK2**	10		ns	
t151 -OBIOP setup to PCLK2	10		ns	

INPUT REQUIREMENTS (continued)	Min	Max	Unit	Notes
t155 -VGAREQ setup to PCLK2	10		ns	
t156 -VGAREQ hold from PCLK2	10		ns	

OUTPUT DELAYS:	Min	Max	Unit	Notes
t160 -MS0,-MS1,-LS0,-LS1 active from PCLK2		26	ns	
t161 -MS0,-MS1,-LS0,-LS1 inactive from PCLK2	5	25	ns	
t162 SA<1:0> valid delay from BE<0:3>		36	ns	
t163 -MADL active delay from PCLK2		22	ns	
t164 -MADL inactive delay from PCLK2		30	ns	
t165 -CMD1 active delay from PCLK2		18	ns	
t166 -CMD1 inactive delay from PCLK2		25	ns	
t167 -XIORD,-XIOWR active from PCLK2		40	ns	
t168 -XIORD,-XIOWR inactive from PCLK2		40	ns	
t169 SDIR active delay from PCLK2		45	ns	
t170 SDIR inactive delay from PCLK2		45	ns	
t171 -READY active delay from PCLK2		24	ns	
t172 -READY inactive delay	4	25	ns	
t173 EALE active from PCLK2		54	ns	
t174 EALE inactive from PCLK2	9	35	ns	
t176 AC<1:0> active delay from PCLK2		34	ns	
t177 AC<1:0> inactive from PCLK2		40	ns	
t178 -INTA active delay from PCLK2		40	ns	
t179 -INTA inactive delay from PCLK2		40	ns	

OUTPUT DELAYS: (continued)		Min	Max	Unit	Notes
t180	-WDLTH active delay from PCLK2		50	ns	
t181	-WDLTH inactive delay from PCLK2		50	ns	
t182	-MBE<3:0> active delay from BE<3:0>		50	ns	
t183	-LBHE, -MBHE active delay from BE<3:0> valid		50	ns	
t185	-VGACMD active delay from PCLK2		30	ns	
t186	-VGACMD inactive delay from PCLK2		30	ns	
t187	MTR32 active delay from HLDA		30	ns	
t188	MTR32 inactive delay from HLDA		30	ns	
t189	-MMMCMD active from PCLK2		20	ns	
t190	-MMMCMDinactive from PCLK2		20	ns	
t191	HLDAO active from HLDA		6	PCLK2	
t192	HLDAO inactive from HLDA		30	ns	

ACCESS TO INTERNAL REGISTERS		Min	Max	Unit	Notes
t200	GATEA20 delay from rising edge of XIOWR (Register bit to output pin)		50	ns	
t201	GATEA20 active delay from PGATEA20		40	ns	
t202	GATEA20 inactive delay from PGATEA20		40	ns	
t203	Valid read data from -XIORD active		50	ns	
t204	Read data invalid from -XIORD inactive		50	ns	
t205	SYSSTA active from -XIOWR		25	ns	
t206	SYSSTA inactive from -XIOWR		25	ns	

DMA CYCLES :

INPUT REQUIREMENTS	Min	Max	Unit	Notes
t210 -LS0,-LS1 active setup to DCLK2	35		ns	
t211 - LS0,-LS1 hold from DCLK2	15		ns	
t212 LA<0:23> setup to DCLK2	15		ns	
t213 LA<0:23> hold from DCLK2	5		ns	
t214 -LBHE setup to DCLK2	35		ns	
t216 DS16RTN,DS32RTN setup to DCLK2	21		ns	
t218 CHRDYRTN setup to DCLK2	10		ns	
t219 CHRDYRTN hold from DCLK2	10		ns	
t220 LM/IO setup to DCLK2	10		ns	
t221 LM/IO hold from DCLK2	5		ns	

OUTPUT DELAYS (continued)	**Min**	**Max**	**Unit**	**Notes**
t230 -MS0,-MS1,MM/-IO valid delay from -LS0,-LS1,LM/-IO active		30	ns	
t231 -MS0,-MS1,MM/-IO inactive delay from DMACLK2		30	ns	
t232 SA<1:0> delay from LA<1:0> valid		30	ns	
t253 -MBE,LBE<0:3> active delay from LA0, LA1, BHE		34	ns	
t254 -MBE, LBE<0:3> inactive delay from LA0, LA1, BHE		25	ns	
t255 -VGACMD active delay from DCLK2		40	ns	
t256 -VGACMD inactive delay from DCLK2		40	ns	
t257 -CMD1 active from DCLK2	8	30	ns	
t275 -CMD1 inactive from DCLK2		30	ns	
t258 -MADL active from DCLK2	5	30	ns	

OUTPUT DELAYS (continued)	Min	Max	Unit	Notes
t259 -MADL inactive from DCLK2		30	ns	
t260 EALE active from DCLK2		30	ns	
t262 EALE inactive from DCLK2		30	ns	
t263 AC<0:1> active delay from DS16/32RTN		34	ns	
t264 AC<0:1> inactive delay from DCLK2		40	ns	
t267 SDIR active delay from LS0, LS1		35	ns	
t268 SDIR inactive delay from CMD inactive		40	ns	
t269 -XIOWR active delay from DCLK2		40	ns	
t270 -XIOWR inactive delay from DCLK2		40	ns	
t271 -XIORD active delay from DCLK2		40	ns	
t272 -XIORD inactive delay from DCLK2		40	ns	
t273 -READY active delay from DCLK2		30	ns	
t274 -READY inactive delay from DCLK2		30	ns	
t276 -MBHE valid from LBHE valid		40	ns	

EXTERNAL MASTER:	Min	Max	Unit	Notes
t280 -LS0,-LS1,-LM/-IO valid delay from -MS0, -MS1, MM/-IO active		25	ns	
t281 -LS0, -LS1, -LM/-IO inactive delay from -MS0, -MS1, MM/-IO inactive		25	ns	
t282 LA0 valid delay from SA0, SA1 H to L		25	ns	
t283 LA0 inactive delay from SA0, SA1 L to H		25	ns	
t284 BSEN active delay from DS32RTN		18	ns	
t285 BSEN inactive delay from -ADL		25	ns	
t286 BDRDY inactive delay from -ADL		19	ns	
t288 -VGACMD active delay from -CMD1 active		20	ns	

EXTERNAL MASTER: (continued)		Min	Max	Unit	Notes
t289	-VGACMD inactive from -CMD1 inactive		20	ns	
t290	-XIORD active delay from -CMD1 active		25	ns	
t291	-XIORD inactive delay from -CMD1 inactive		25	ns	
t292	-XIOWR active delay from -CMD1 active		25	ns	
t293	-XIOWR inactive delay from -CMD1 inactive		25	ns	
t294	-CMD1 active to BDRDY active (for peripheral devices)	8	9	DCLK2	
t295	-CMD1 active to BDRDY active (for non peripheral devices)	1	2	DCLK2	

Numeric Coprocessor Interface		Min	Max	Unit	Notes
t296	-NPEXCPT active delay from NPBUSY inactive		25	ns	
t297	-NPEXCPT inactive delay from -XIOWR		25	ns	
t298	NPRST active delay from PCLK2		25	ns	
t299	NPRST pulse width		128	PCLK2	

NOTES:

1. The -OBIOP signal should be held active throughout the cycle.
2. The DSKDACK signal is an input (given by 82C223 DMA controller) to indicate 82C321 to introduce additional wait states in the DMA cycle for floppy disk controller accesses.
3. The -RFSH and -BTO are asynchronous inputs.

* The signal should be held active until EALE goes low.
** These are provided for testing purposes only.

CLOCKS	Min	Max	Unit	Notes
t100 PCLK2 period	20		ns	
t101 PCLK2 low time	7		ns	At 2V
t102 PCLK2 high time	7		ns	At 2V
t103 PCLK2 rise time		7	ns	0.8 to VCC -0.8V
t104 PCLK2 fall time		7	ns	VCC -0.8 to -0.8V
t105 DMACLK2 period	50		ns	
t106 OSC/12 period	840		ns	
t107 DMACLK2 low time	16		ns	At 2V
t108 DMACLK2 high time	16		ns	At 2V
t109 DMACLK2 rise time		16	ns	0.8 to VCC -0.8V
t110 DMACLK2 fall time		16	ns	VCC -0.8 to -0.8V

RESET TIMINGS	Min	Max	Unit	Notes
t111 -RESET2 pulse width	3CLK2			
t112 RESET3 active delay from PCLK2		18	ns	
t113 RESET3, RESET4 inactive delay from PCLK2		36	ns	
t114 -RESET1,-RESET2 set-up time to PCLK2	20		ns	
t115 RESET4, RESET3 pulse width		128	PCLK2	

(T_A = 0oC to 70oC, VCC = 5V + 5%, A.C. load = 85pf)

CPU CYCLES:

INPUT REQUIREMENTS	Min	Max	Unit	Notes
t120 -AF32 setup to PCLK2	10		ns	
t121 -AF32 hold from PCLK2	5		ns	
t123 -DS16RTN ,DS32RTN setup to PLCK2	3		ns	
t124 -DS16RTN, DS32RTN hold from EALE*	5		ns	
t125 -CHRDYRTN setup to PCLK2	10		ns	
t126 -CHRDYRTN hold from PCLK2	10		ns	
t127 -READY setup to PCLK2	10		ns	
t128 -READY hold from PCLK2	8		ns	
t129 -ADS setup to PCLK2	10		ns	
t130 -ADS hold from PCLK2	4		ns	
t131 LM/-IO setup to PCLK2	10		ns	
t132 LM/-IO hold from PCLK2	4		ns	
t133 -LBE<0:3>, LA31 setup to PCLK2	10		ns	
t134 -LBE<0:3>, LA31 hold from PCLK2	4		ns	
t135 W/-R setup to PCLK2	10		ns	
t136 W/-R hold from PCLK2	10		ns	
t137 D/-C setup to PCLK2	10		ns	
t138 D/-C hold from PCLK2	10		ns	
t139 MMCR setup to PCLK2	10		ns	
t140 MMCR hold from PCLK2	10		ns	
t143 HLDA setup to PCLK2**	10		ns	
t151 -OBIOP setup to PCLK2	10		ns	

INPUT REQUIREMENTS (continued)	Min	Max	Unit	Notes
t155 -VGAREQ setup to PCLK2	10		ns	
t156 -VGAREQ hold from PCLK2	10		ns	

OUTPUT DELAYS:	Min	Max	Unit	Notes
t160 -MS0,-MS1,-LS0,-LS1 active from PCLK2		24	ns	
t161 -MS0,-MS1,-LS0,-LS1 inactive from PCLK2	5	25	ns	
t162 SA<1:0> valid delay from BE<0:3>		22	ns	
t163 -MADL active delay from PCLK2		22	ns	
t164 -MADL inactive delay from PCLK2		30	ns	
t165 -CMD1 active delay from PCLK2		29	ns	
t166 -CMD1 inactive delay from PCLK2		25	ns	
t167 -XIORD,-XIOWR active from PCLK2		40	ns	
t168 -XIORD,-XIOWR inactive from PCLK2		40	ns	
t169 SDIR active delay from PCLK2		45	ns	
t170 SDIR inactive delay from PCLK2		45	ns	
t171 -READY active delay from PCLK2		20	ns	
t172 -READY inactive delay	4	25	ns	
t173 EALE active from PCLK2		30	ns	
t174 EALE inactive from PCLK2	0	35	ns	
t176 AC<1:0> active delay from PCLK2		34	ns	
t177 AC<1:0> inactive from PCLK2		40	ns	
t178 -INTA active delay from PCLK2		40	ns	
t179 -INTA inactive delay from PCLK2		40	ns	

OUTPUT DELAYS: (continued)		Min	Max	Unit	Notes
t180	-WDLTH active delay from PCLK2		50	ns	
t181	-WDLTH inactive delay from PCLK2		50	ns	
t182	-MBE<3:0> active delay from BE<3:0>		50	ns	
t183	-LBHE, -MBHE active delay from BE<3:0> valid		50	ns	
t185	-VGACMD active delay from PCLK2		30	ns	
t186	-VGACMD inactive delay from PCLK2		30	ns	
t187	MTR32 active delay from HLDA		30	ns	
t188	MTR32 inactive delay from HLDA		30	ns	
t189	-MMMCMD active from PCLK2		20	ns	
t190	-MMMCMDinactive from PCLK2		20	ns	
t191	HLDAO active from HLDA		6	PCLK2	
t192	HLDAO inactive from HLDA		30	ns	

ACCESS TO INTERNAL REGISTERS		Min	Max	Unit	Notes
t200	GATEA20 delay from rising edge of XIOWR (Register bit to output pin)		50	ns	
t201	GATEA20 active delay from PGATEA20		40	ns	
t202	GATEA20 inactive delay from PGATEA20		40	ns	
t203	Valid read data from -XIORD active		50	ns	
t204	Read data invalid from -XIORD inactive		50	ns	
t205	SYSSTA active from -XIOWR		25	ns	
t206	SYSSTA inactive from -XIOWR		25	ns	

DMA CYCLES :

INPUT REQUIREMENTS	Min	Max	Unit	Notes
t210 -LS0,-LS1 active setup to DCLK2	35		ns	
t211 - LS0,-LS1 hold from DCLK2	15		ns	
t212 LA<0:23> setup to DCLK2	15		ns	
t213 LA<0:23> hold from DCLK2	5		ns	
t214 -LBHE setup to DCLK2	35		ns	
t216 DS16RTN,DS32RTN setup to DCLK2	21		ns	
t218 CHRDYRTN setup to DCLK2	10		ns	
t219 CHRDYRTN hold from DCLK2	10		ns	
t220 LM/IO setup to DCLK2	10		ns	
t221 LM/IO hold from DCLK2	5		ns	

OUTPUT DELAYS (continued)	Min	Max	Unit	Notes
t230 -MS0,-MS1,MM/-IO valid delay from -LS0,-LS1,LM/-IO active		30	ns	
t231 -MS0,-MS1,MM/-IO inactive delay from DMACLK2		30	ns	
t232 SA<1:0> delay from LA<1:0> valid		30	ns	
t253 -MBE,LBE<0:3> active delay from LA0, LA1, BHE		34	ns	
t254 -MBE, LBE<0:3> inactive delay from LA0, LA1, BHE		25	ns	
t255 -VGACMD active delay from DCLK2		40	ns	
t256 -VGACMD inactive delay from DCLK2		40	ns	
t257 -CMD1 active from DCLK2	8	30	ns	
t275 -CMD1 inactive from DCLK2		30	ns	
t258 -MADL active from DCLK2	5	30	ns	

OUTPUT DELAYS (continued)	Min	Max	Unit	Notes
t259 -MADL inactive from DCLK2		30	ns	
t260 EALE active from DCLK2		30	ns	
t262 EALE inactive from DCLK2		30	ns	
t263 AC<0:1> active delay from DS16/32RTN		34	ns	
t264 AC<0:1> inactive delay from DCLK2		40	ns	
t267 SDIR active delay from LS0, LS1		35	ns	
t268 SDIR inactive delay from CMD inactive		40	ns	
t269 -XIOWR active delay from DCLK2		40	ns	
t270 -XIOWR inactive delay from DCLK2		40	ns	
t271 -XIORD active delay from DCLK2		40	ns	
t272 -XIORD inactive delay from DCLK2		40	ns	
t273 -READY active delay from DCLK2		30	ns	
t274 -READY inactive delay from DCLK2		30	ns	
t276 -MBHE valid from LBHE valid		40	ns	

EXTERNAL MASTER:	Min	Max	Unit	Notes
t280 -LS0,-LS1,-LM/-IO valid delay from -MS0, -MS1, MM/-IO active		25	ns	
t281 -LS0, -LS1, -LM/-IO inactive delay from -MS0, -MS1, MM/-IO inactive		25	ns	
t282 LA0 valid delay from SA0, SA1 H to L		25	ns	
t283 LA0 inactive delay from SA0, SA1 L to H		25	ns	
t284 BSEN active delay from DS32RTN		18	ns	
t285 BSEN inactive delay from -ADL		25	ns	
t286 BDRDY inactive delay from -ADL		19	ns	
t288 -VGACMD active delay from -CMD1 active		20	ns	

EXTERNAL MASTER: (continued)		Min	Max	Unit	Notes
t289	-VGACMD inactive from -CMD1 inactive		20	ns	
t290	-XIORD active delay from -CMD1 active		25	ns	
t291	-XIORD inactive delay from -CMD1 inactive		25	ns	
t292	-XIOWR active delay from -CMD1 active		25	ns	
t293	-XIOWR inactive delay from -CMD1 inactive		25	ns	
t294	-CMD1 active to BDRDY active (for peripheral devices)	8	9	DCLK2	
t295	-CMD1 active to BDRDY active (for non peripheral devices)	1	2	DCLK2	

Numeric Coprocessor Interface		Min	Max	Unit	Notes
t296	-NPEXCPT active delay from NPBUSY inactive		25	ns	
t297	-NPEXCPT inactive delay from -XIOWR		25	ns	
t298	NPRST active delay from PCLK2		20	ns	
t299	NPRST pulse width		128	PCLK2	

NOTES:

1. The -OBIOP signal should be held active throughout the cycle.
2. The DSKDACK signal is an input (given by 82C223 DMA controller) to indicate 82C321 to introduce additional wait states in the DMA cycle for floppy disk controller accesses.
3. The -RFSH and -BTO are asynchronous inputs.

* The signal should be held active until EALE goes low.
** These are provided for testing purposes only.

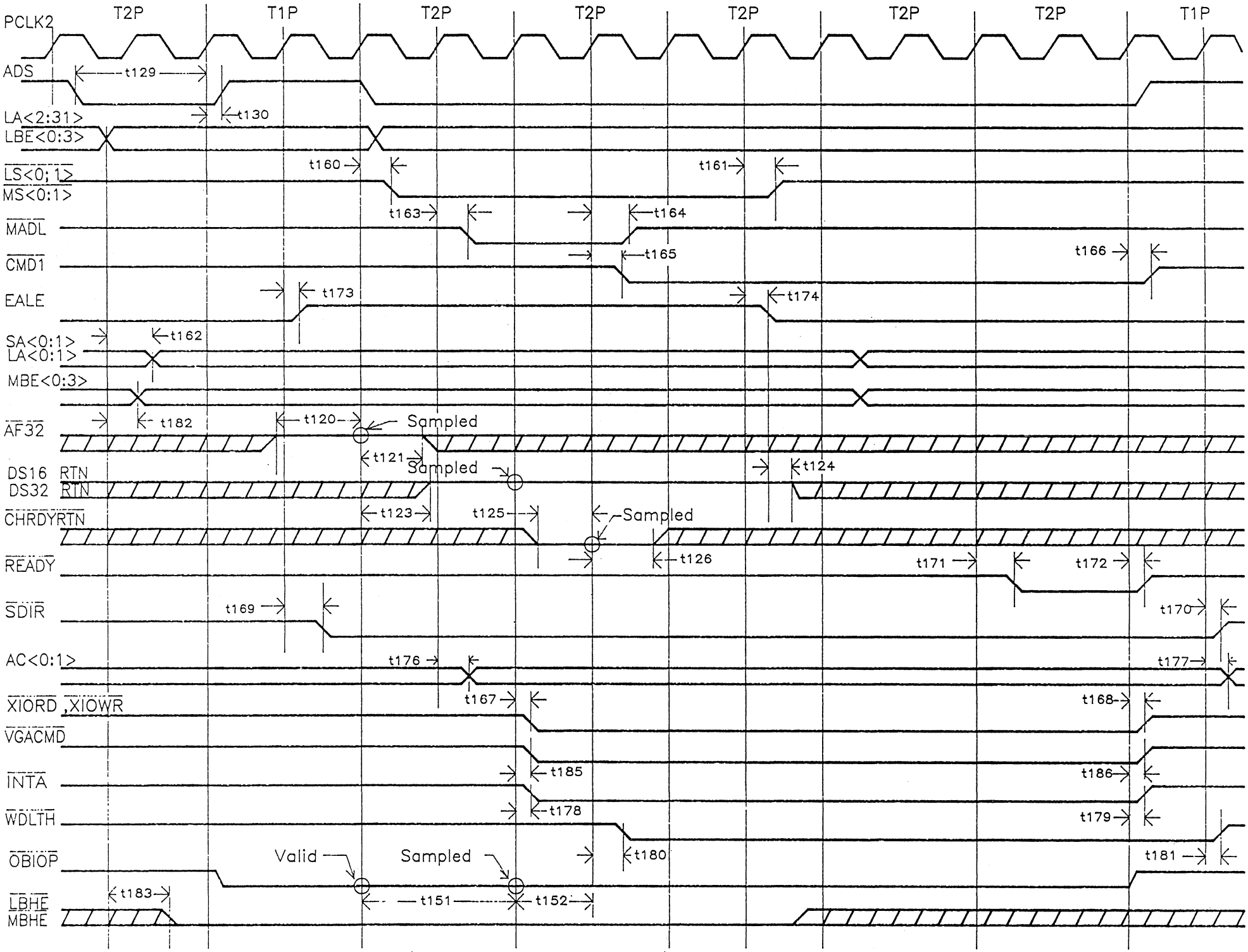


Figure 2.1 25MHz (AF32 Option Enabled) CPU MicroChannel Default Cycle

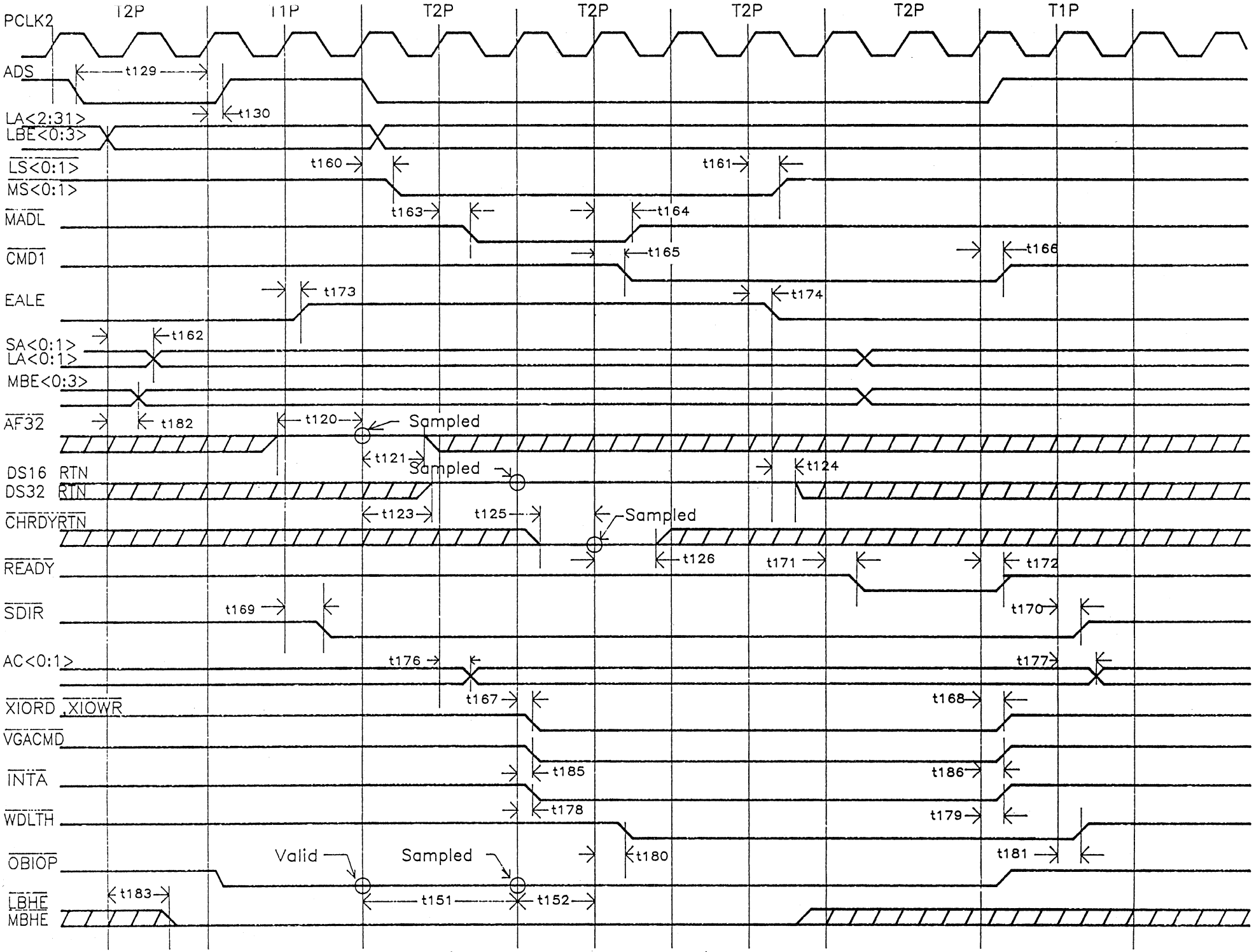


Figure 2.2 20MHz (AF32 Option Enabled) CPU MicroChannel Default Cycle

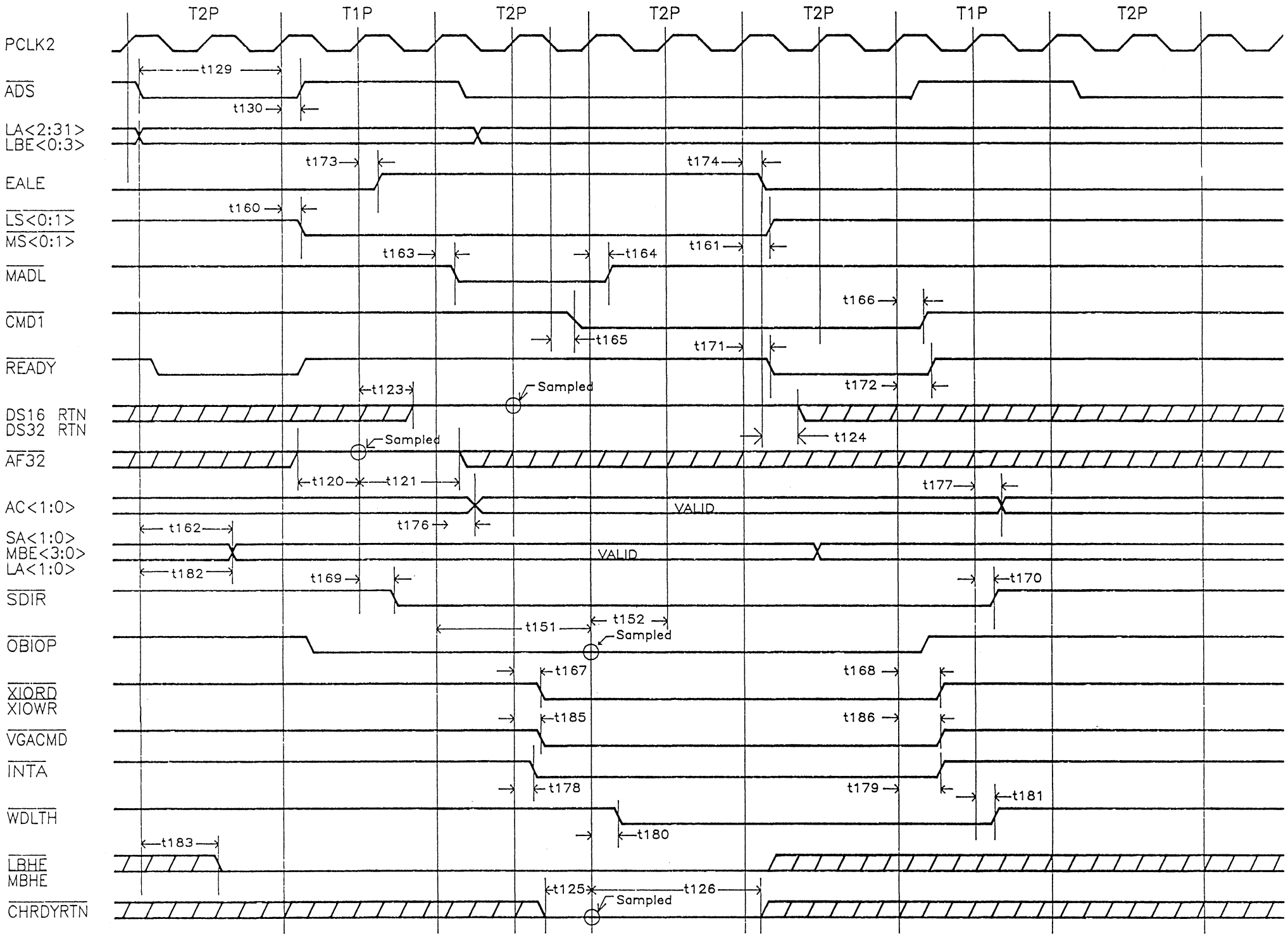


Figure 2.3 16MHz CPU MicroChannel Default Cycle

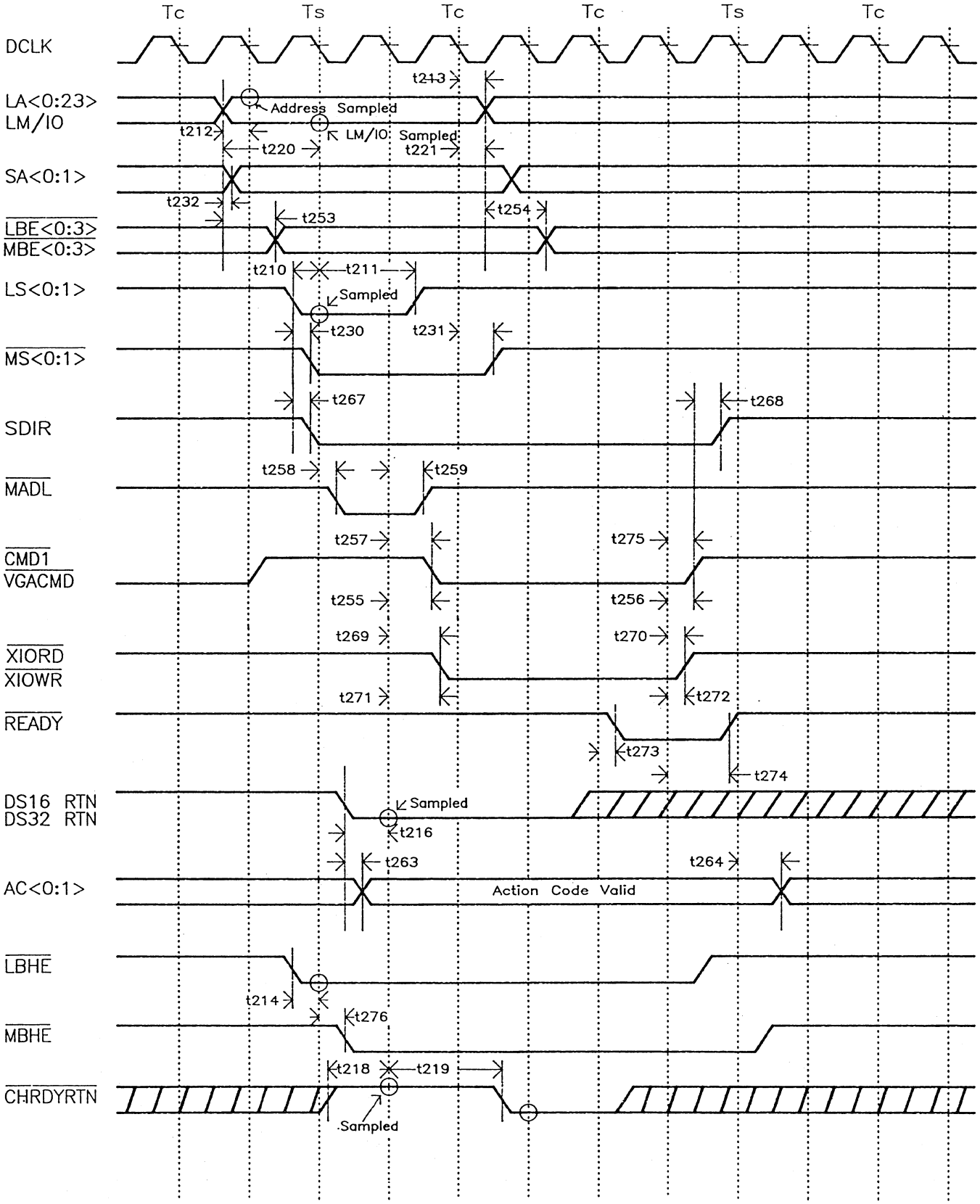


Figure 2.4 82C321 DMA Cycle (1 Wait State)

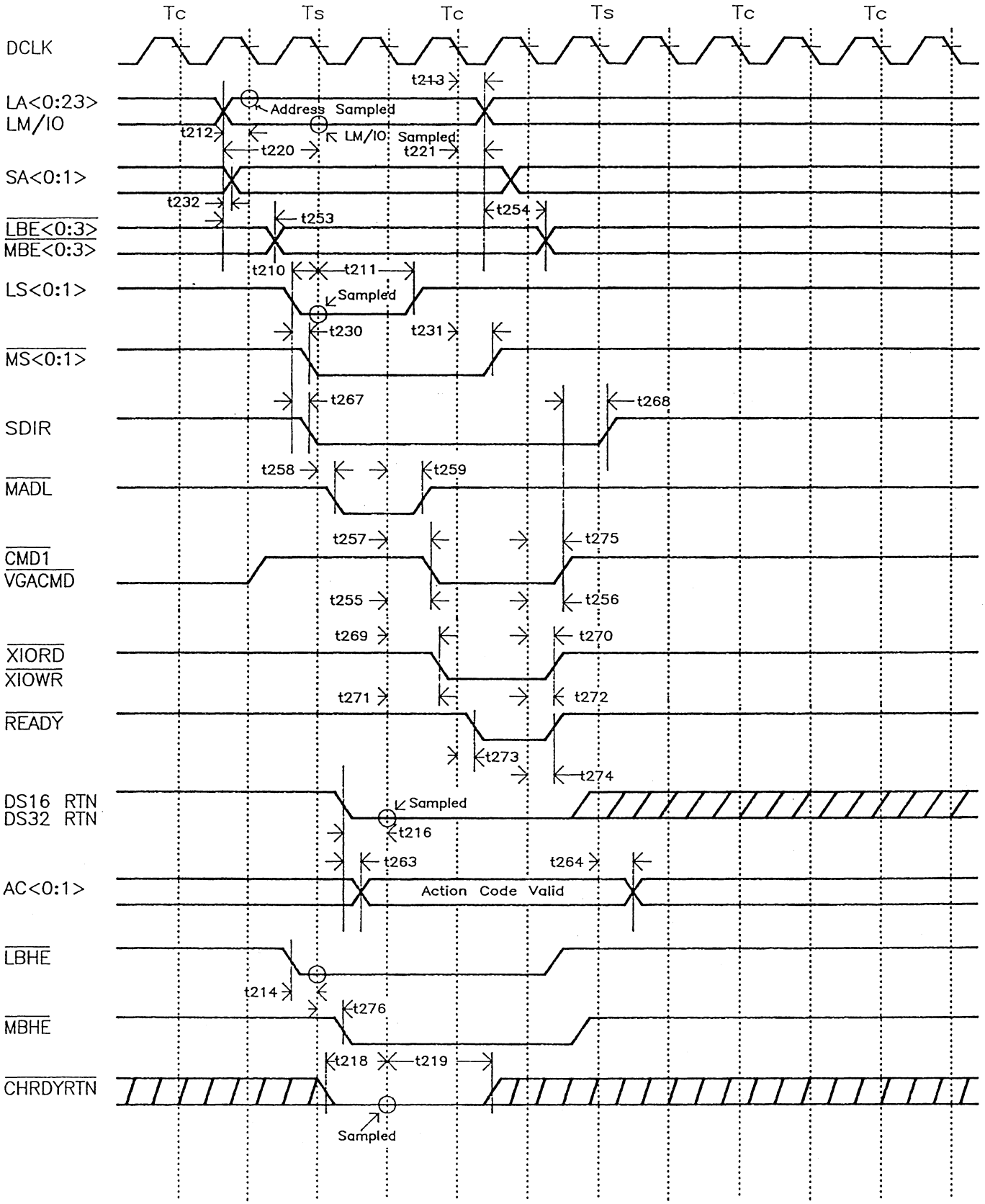


Figure 2.4A 82C321 DMA Cycle (0 Wait State)

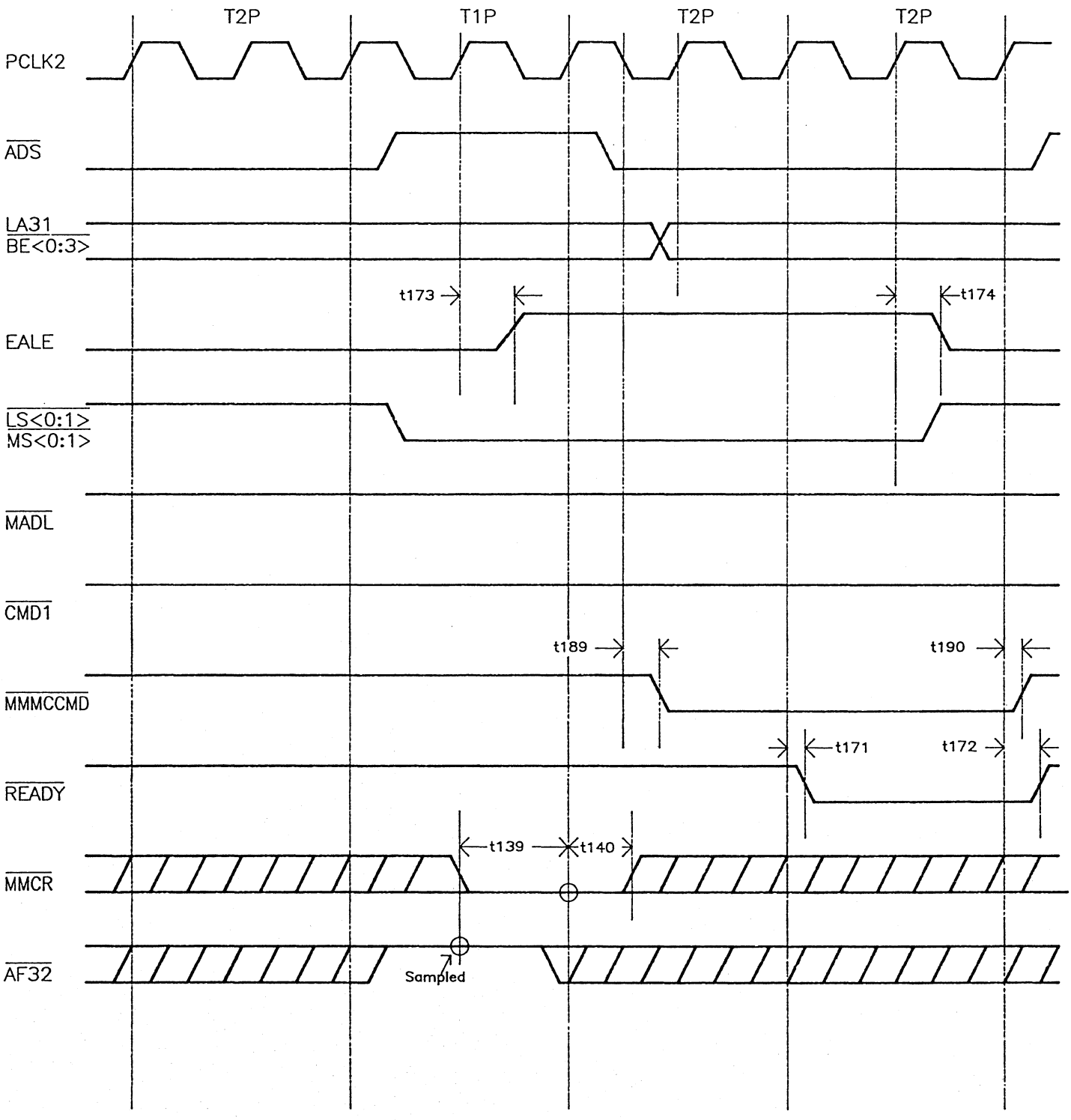


Figure 2.6 16MHz Matched Memory Cycle

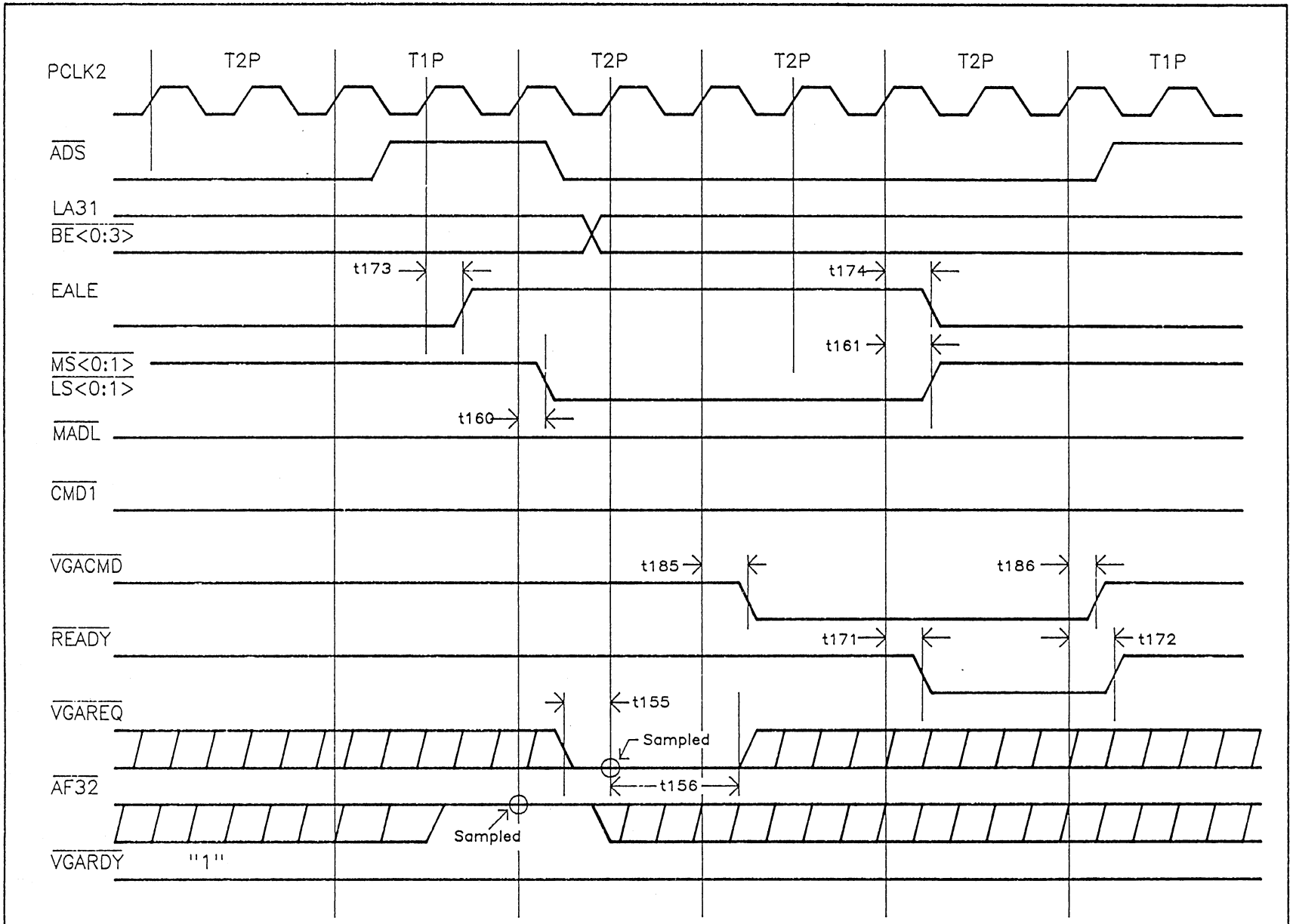


Figure 2.7 20MHz, 25MHz (AF32 Option Enabled) Fast VGA I/O Cycle

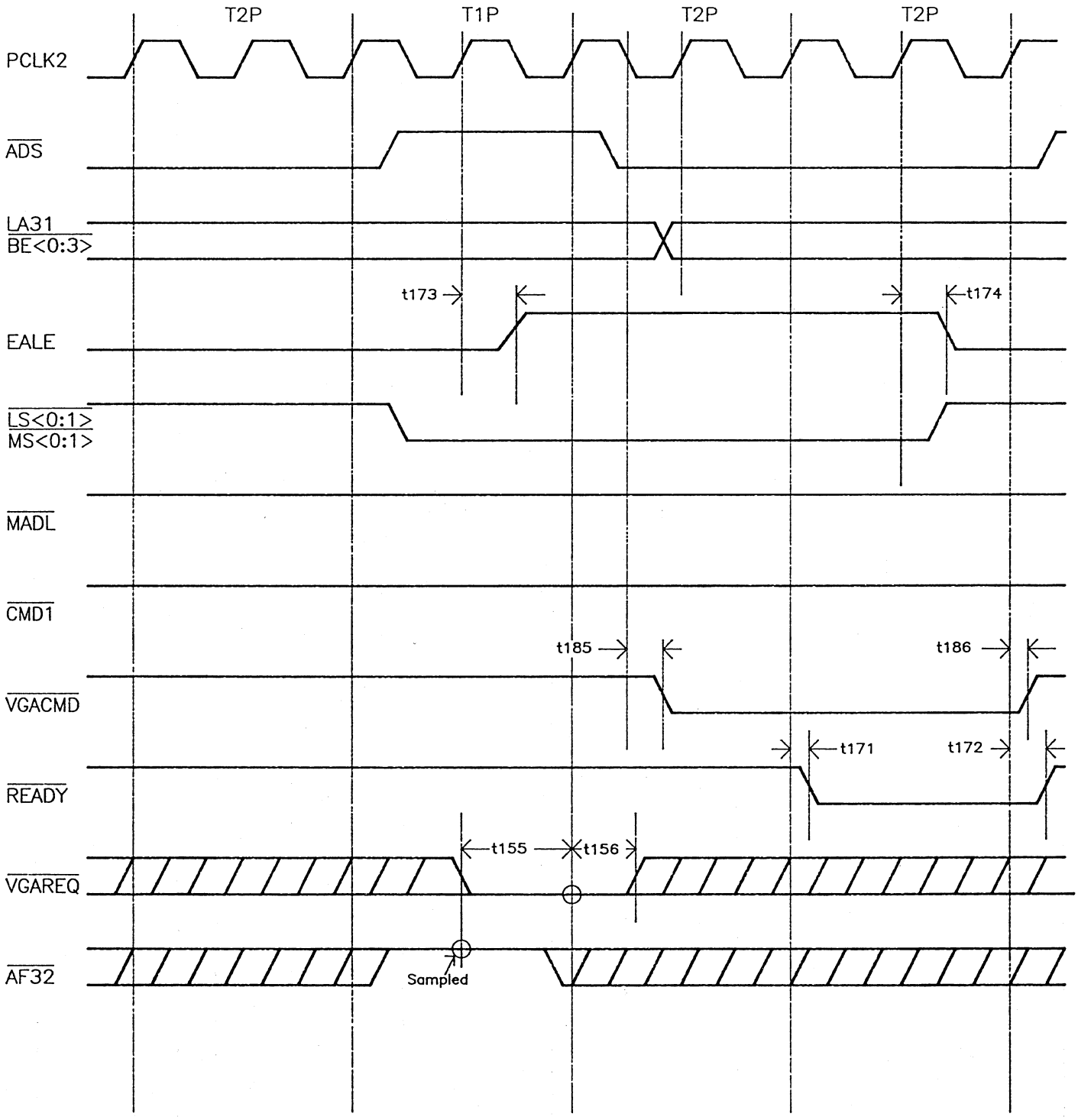


Figure 2.8 16MHz Fast VGA I/O Cycle

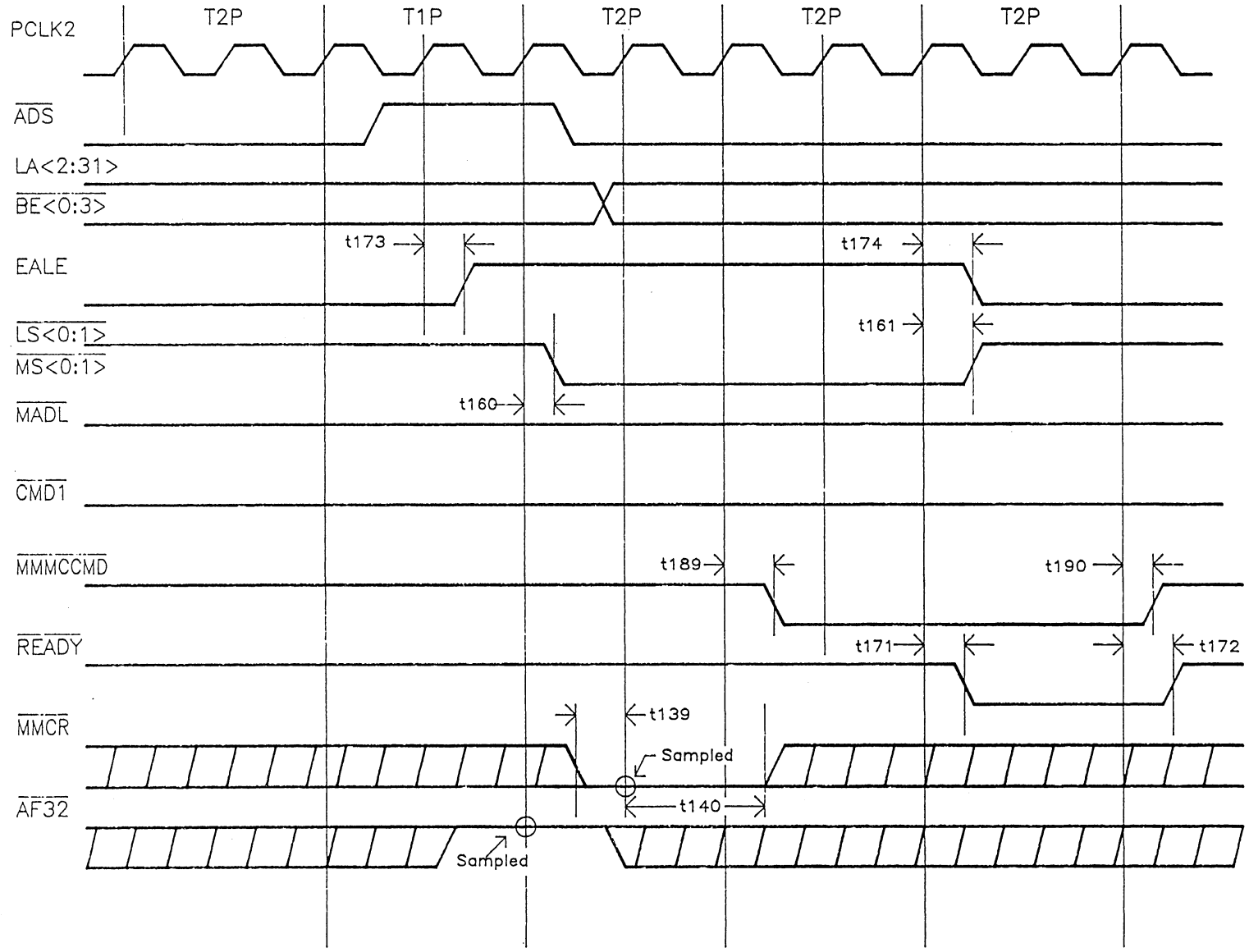


Figure 2.5 20MHz, 25MHz (AF32 Option Enabled) Matched Memory Cycle

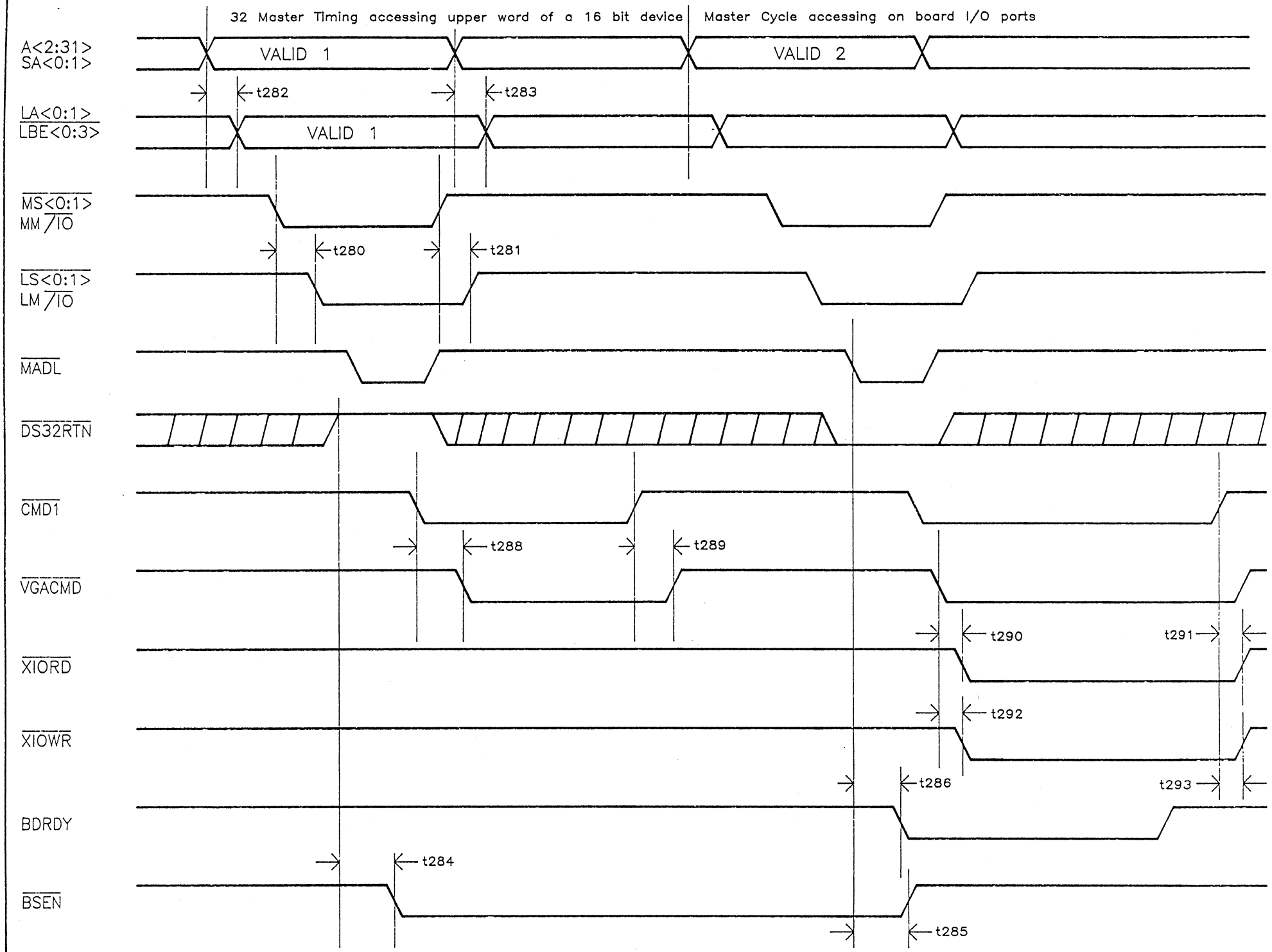


Figure 2.9 Master Timing

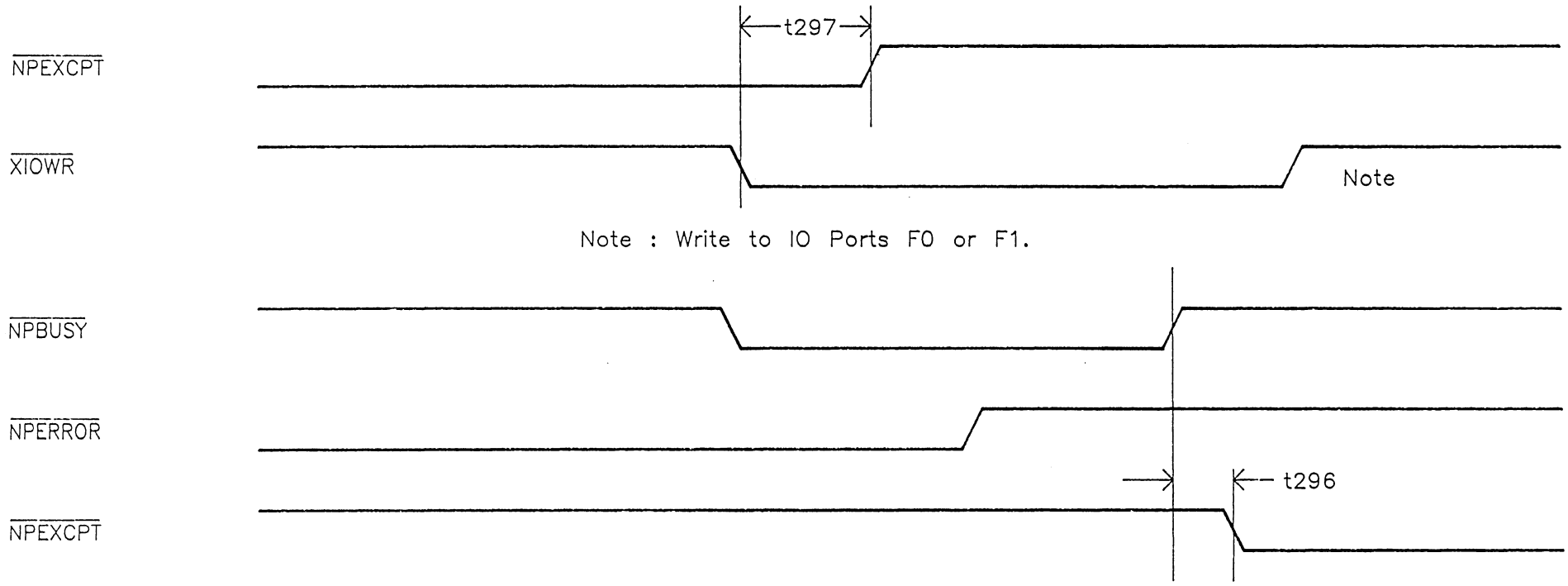


Figure 2.10 Numeric Processor Cycle

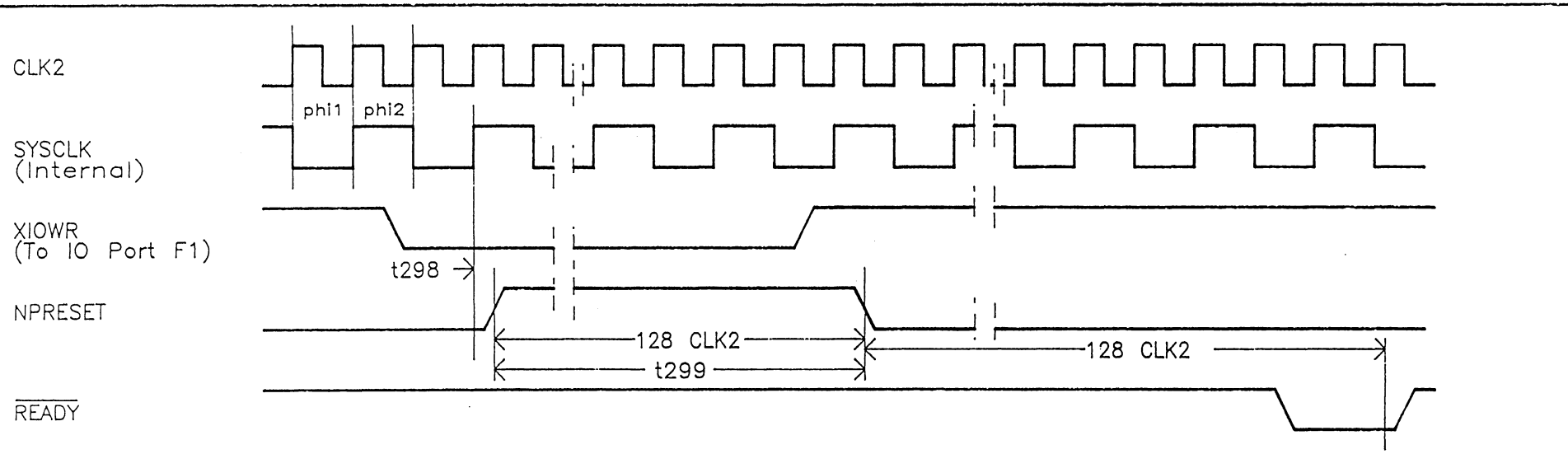


Figure 2.11 Numeric Processor Reset Timing

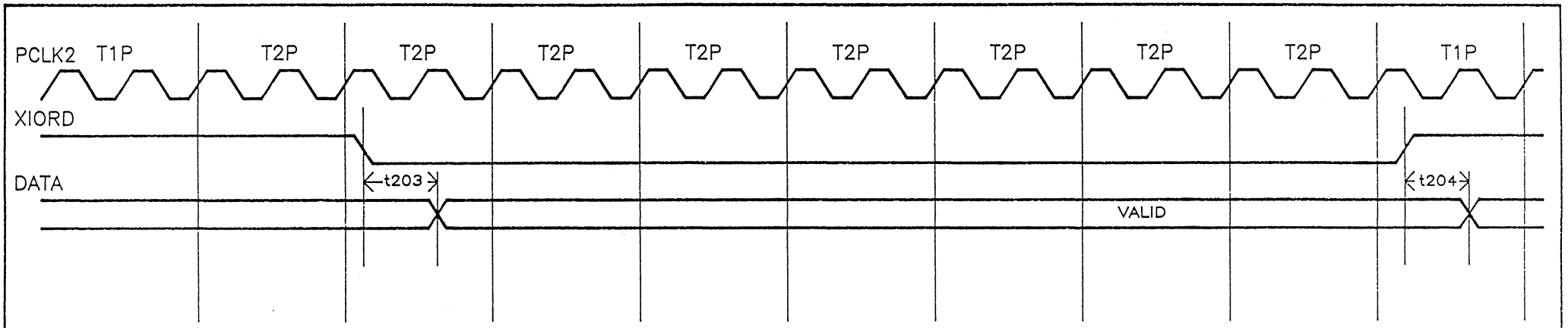


Figure 2.12 Internal Register Access Timing

Note : The number of CPU wait states for register access varies with frequencies, as shown in table below.

Freq.	16MHz	20MHz AF32 Option	25MHz AF32 Option
CPU Cycle Time	437.5 ns	400 ns	360 ns
$\overline{\text{XIORD}}$ Pulse Width	312.5 ns	275 ns	260 ns
CPU Wait States	5	6	7

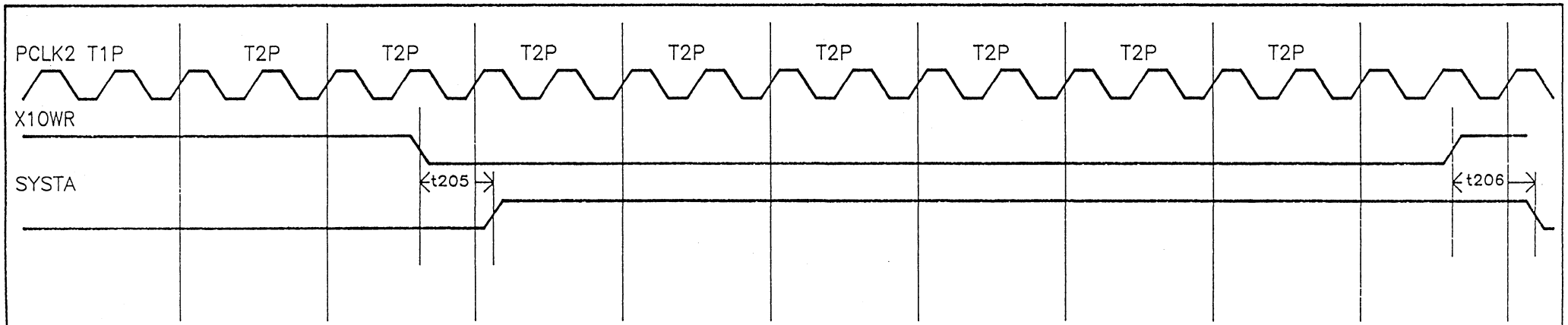


Figure 2.13 SYSTA Timing

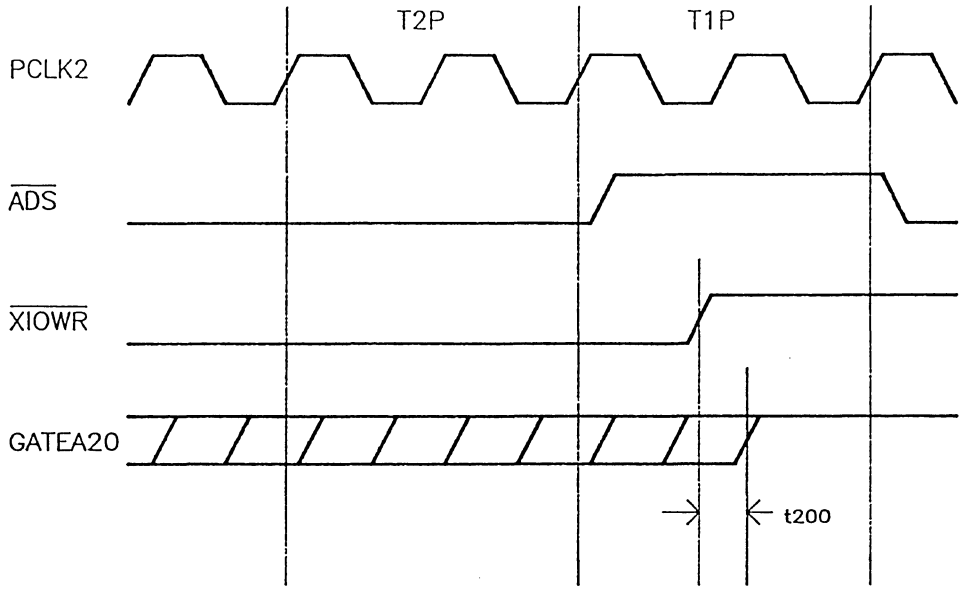


Figure 2.14 MISC. Timing

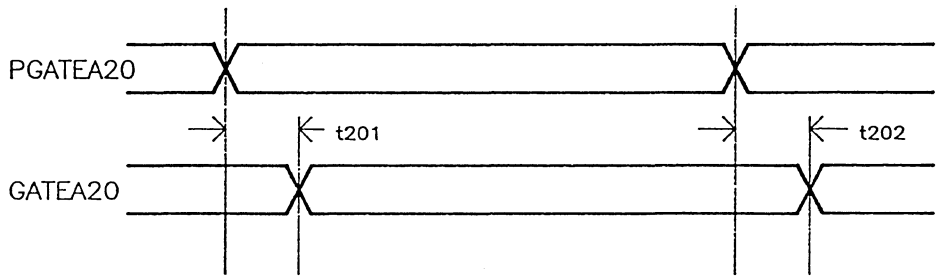


Figure 2.15 GATEA20 Timing

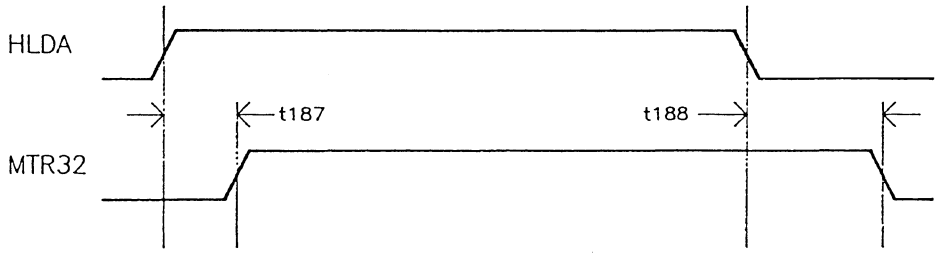


Figure 2.16 MTR32 Timing
(for 16 bit DMA or Master)

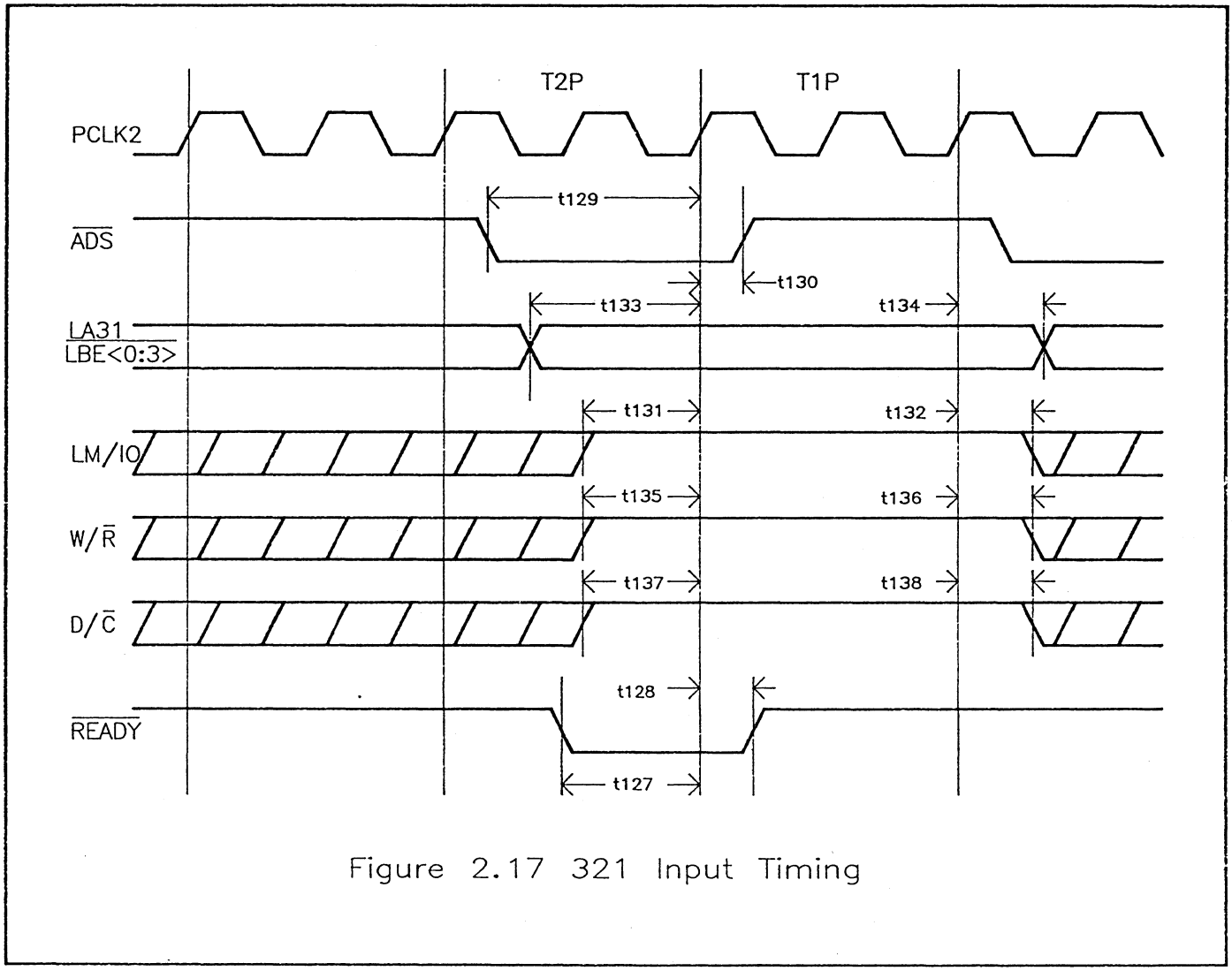


Figure 2.17 321 Input Timing

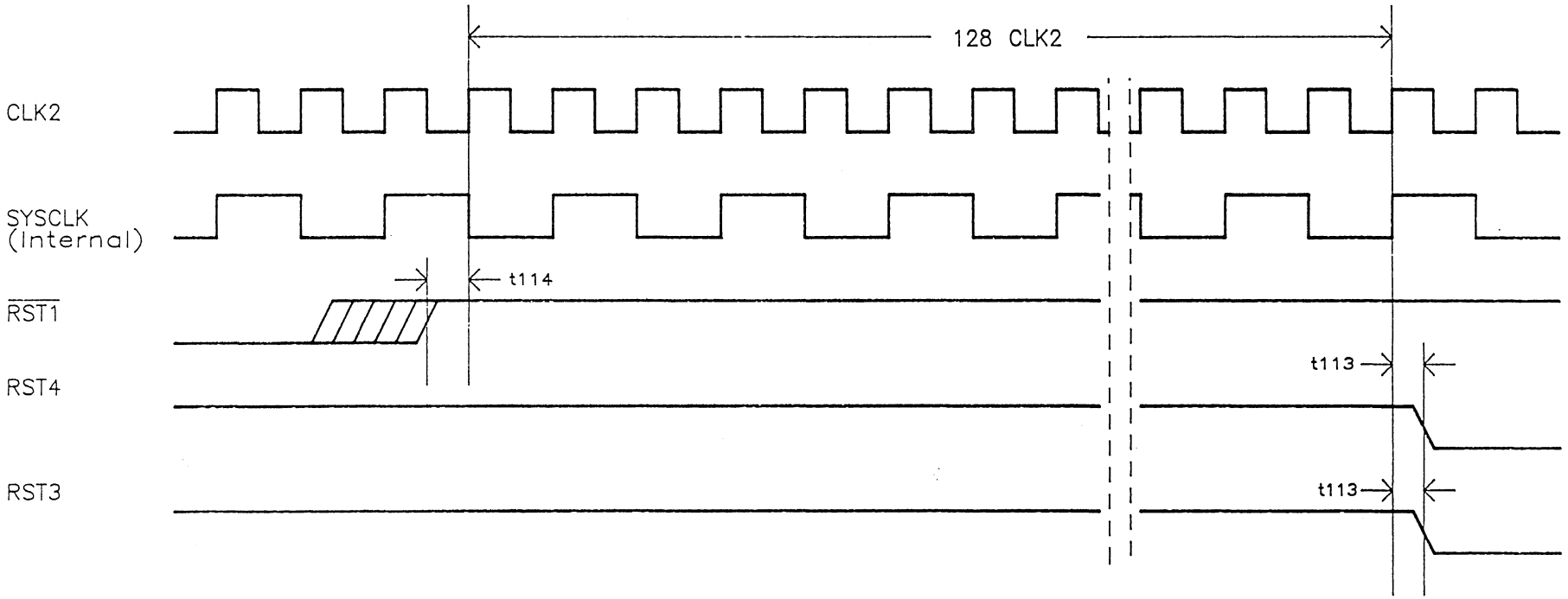


Figure 2.18 Reset 1, Reset 3 and Reset 4 Timing

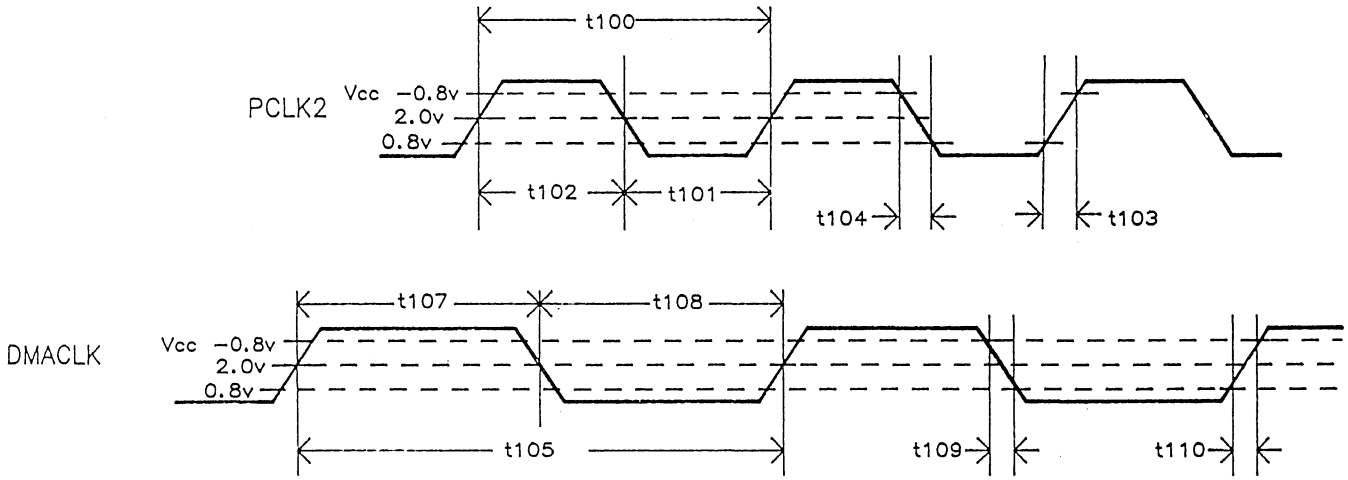


Figure 2.19 Clock Timing

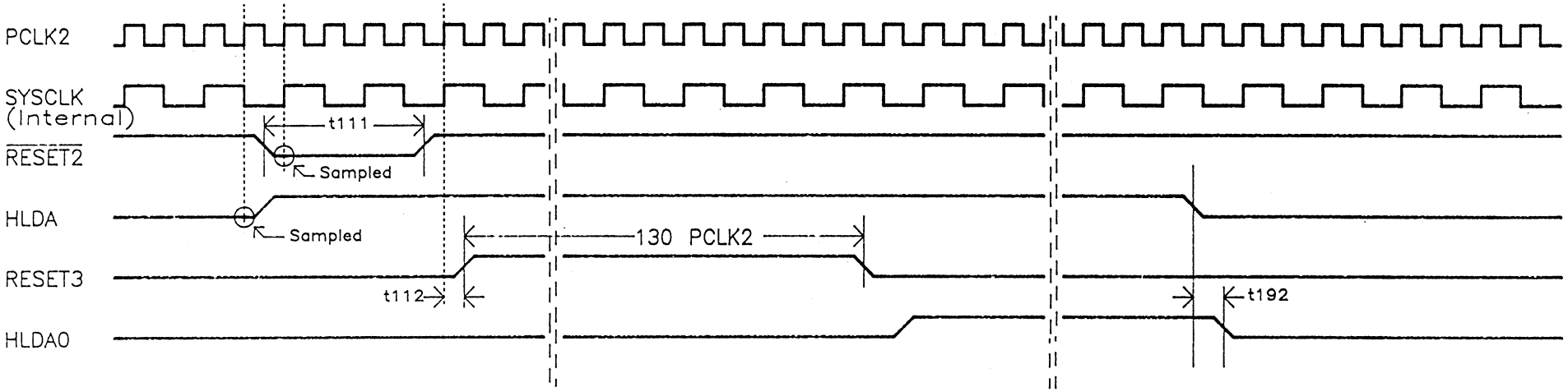


Figure 2.20 RESET2 and HLDA asserted simultaneously

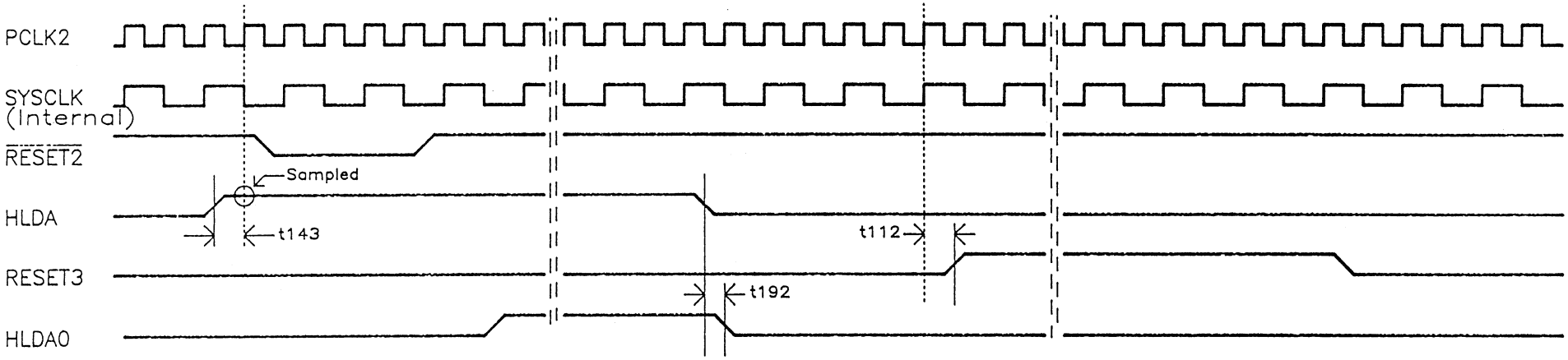


Figure 2.21 RESET2 asserted during HLDA high

NOTE : The 80386 deasserts HLDA when RESET3 goes active, this can end a DMA cycle in progress. The 82C321 generates HLDA0 (which goes to 82C223 DMA controller) to correct this problem. If RESET2 and HLDA occurs simultaneously RESET3 is generated and HLDA0 is not asserted, thus blocking the DMA cycle from starting, when RESET3 is completed, HLDA0 is sent to the 82C223 DMA controller. If the DMA cycle is already in progress and RESET2 becomes active then RESET3 is not asserted until the DMA cycle is completed. The same logic applies to port 92 RESET operation.

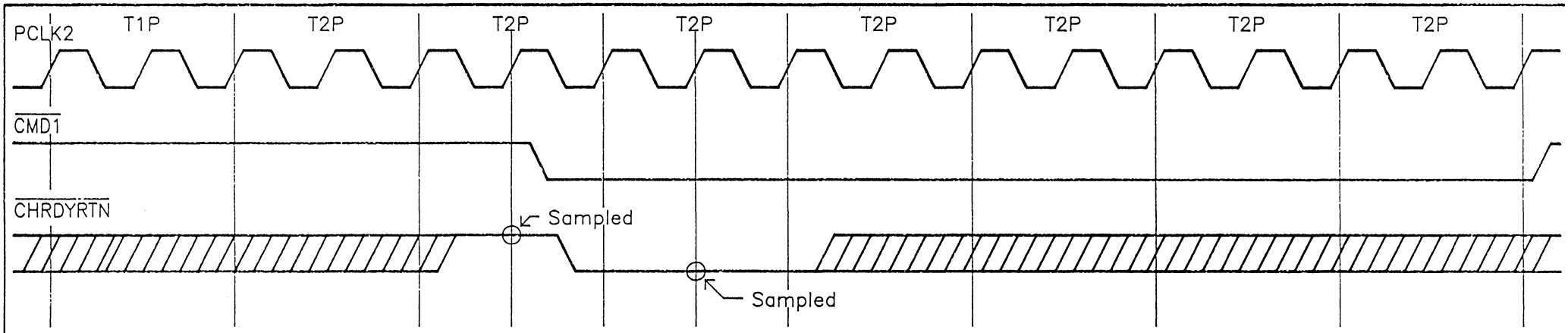


Figure 2.22 25 MHz Synchronous Extended Cycle

Note : The synchronous extended cycle occurs when the CHRDYRTN signal is sampled high in the middle of T2P. The CHRDYRTN signal becomes active (low) after CMD1 becomes active. This is similar to the default cycle except cycle time (hence CMD1 pulse width) increases by two CPU states. For example for 25 MHz the CPU cycle time is 320 nsec, and the default cycle time is 240 nsec.

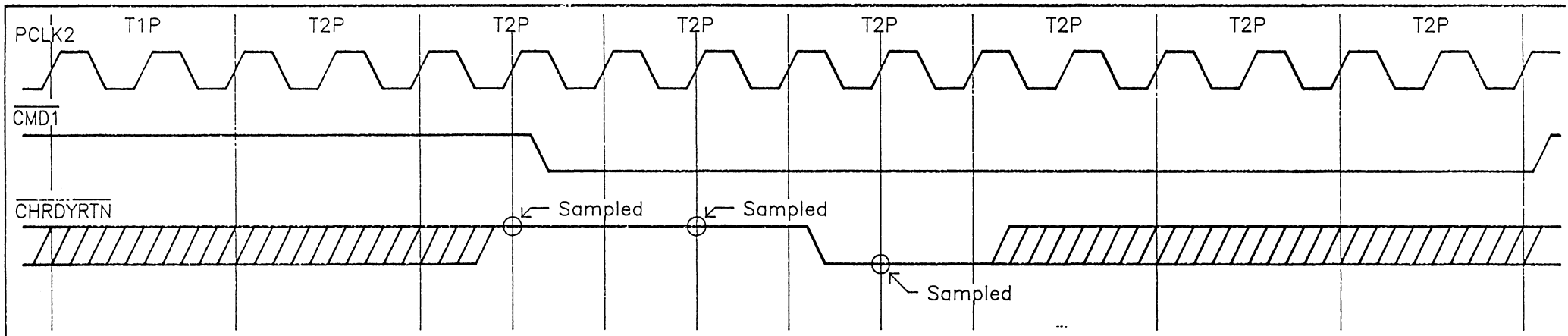
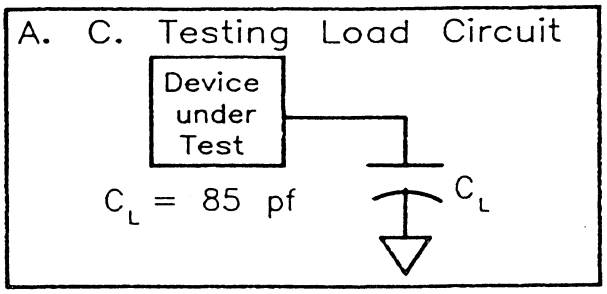


Figure 2.23 25 MHz Asynchronous Extended Cycle

Note : Asynchronous extended cycle occurs when the CHRDYRTN is active (low) asynchronously i.e. not synchronous with the CMD1 as in synchronous extended cycle. The CHRDYRTN is sampled at every T2P until sampled active (low) and the cycle time extends by two CPU states plus the number of CPU states for CHRDYRTN to become active (low). For example at 25 MHz the CHRDYRTN is sampled high at the middle of the second T2P (which introduces two CPU states in the time cycle), and the third T2P, hence the cycle time increases by 3 CPU states (6 PCLK2).


A. C. Testing Load Circuit
Device under Test
C_L = 85 pf
C_L

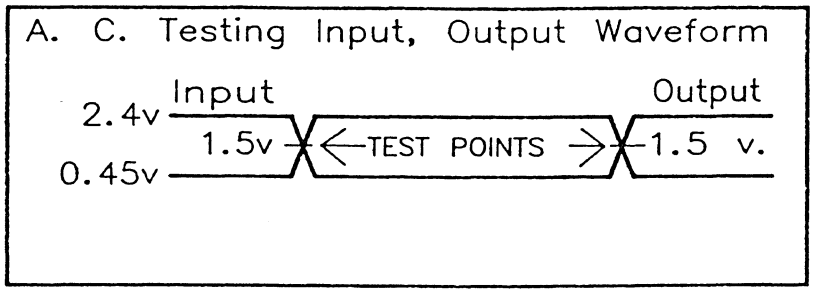
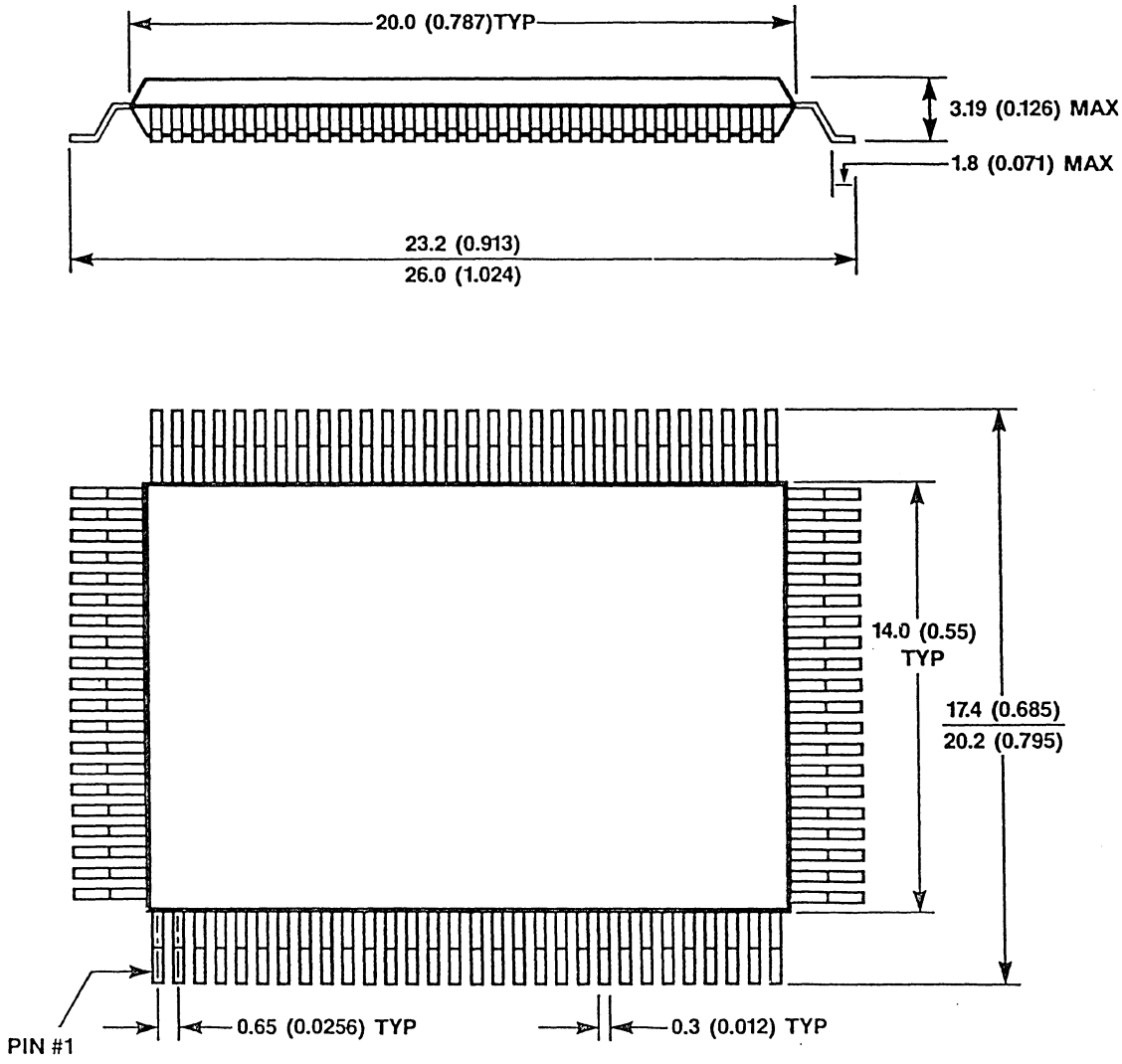

A. C. Testing Input, Output Waveform
Input
Output
2.4v
1.5v
0.45v
TEST POINTS
1.5 v.

Figure 2.24

100-PIN PLASTIC FLAT PACKAGE
(RECTANGULAR)



DIMENSIONS: mm (in)

FEATURES

- Page Mode access including single, two way and four way interleaved memory banks, providing higher performance over conventional DRAM addressing schemes.
- Supports remapping of RAM resident in 640K to 896K area or 512K to 896K area to anywhere from 1MB to 15MB area on 1MB boundaries.
- Supports 256K (x1 or x4), 1M (x1 or x4) DRAMs
- Supports up to 16 MBytes of memory configurable in four banks.
- Shadow RAM feature for efficient Basic Input Output System (BIOS) execution.
- Supports Lotus Intel Microsoft - Expanded Memory System (LIM - EMS 3.2) address translation.
- Supports Page Mode DRAMs
- 16 KB Bad Block remapping for up to four 16K blocks
- Staggered refresh to reduce power supply noise
- Support for external EMS Mapper chip to support the full range of EMS 4.0. specification.
- Wait state generation for local memeory access by CPU, DMAC or External Masters.
- DRAMS locatable on CPU data bus for higher performance.
- EPROM Chip Select Logic.
- On Board I/O Logic and VGA Decode Logic.
- PS/2 (^{TM}) Model 80 compatible Address Recovery Logic.

1.0 Overview

The 82C322 performs the memory control function in a CHIPS/280 implementation of Model 70/80. The 82C322 incorporates a unique interleaved page memory control mechanism that allows fast access to standard page mode DRAMs with near zero wait state operation. The Ready logic function is integrated to allow better synchronization between the 80386 and the memory controller.

In the two way interleaved mode, the average time for memory access is 2.7 cycles (0.7 average wait-states) with 2 banks of DRAMs. In the four way interleaved mode, the average time for memory accesses is 2.5 cycle (0.5 wait states) with 4 banks of DRAMs.

CPU CLOCK	Page/Interleaved 2 Way	4 Way	DRAMS Speed
16 MHz	0.7	0.5	120 ns
20 MHz	0.7	0.5	100 ns
25 MHz	0.7	0.5	80 ns

1.1 Array Configuration

The 82C322 organizes memory as banks of 36 bits, consisting of 32 bits of data and 4 bits of parity information. The 32 bits of data are split into four bytes, with one parity bit per byte. This configuration can be implemented by using four 9-bit wide SIMM DRAMs. The minimum configuration can be a single bank operating in non-interleaved mode up to a maximum of four banks of DRAMs operating in the four way interleaved mode. Since the 82C322 uses a two way/four way interleaving scheme, the DRAMs within a pair of banks must be identical.

1.2 Page/Interleaved Operation

The 82C322 uses a page/interleaved design that is different from most interleaved memory designs. Typical interleaving schemes use two banks of DRAMs with even word addresses on one bank and odd word addresses on the other bank. If memory accesses are sequential, the RAS precharge time of one bank overlaps the access time of the other bank. Typically, programs consist of instruction fetches interspersed with operand accesses. The instruction fetches tend to be sequential and the operand accesses tend to be random.

Figure 3.1 is a sequence diagram for an interleaved memory scheme using two banks 0 and 1. The -RAS signals of the two banks are interleaved so that the -RAS precharge time (TRP) of one bank overlaps the -RAS active time in the other bank. This requires sequential accesses to be alternating between the two banks. For non-sequential accesses, it is possible to get wait states due to a "miss." Typically, this results in a 50% hit ratio.

Figure 3.2 is a sequence diagram of a page-mode DRAM operation. In paged mode DRAMs, once a row access has been made, it is possible to access subsequent column addresses within that row, without the -RAS precharge penalty. However, after a -RAS active timeout, there is a -RAS precharge period which typically occurs every 10 microseconds. Since the -CAS precharge time TCP is small, it is possible to make fast random accesses within a selected row. Typically, page mode access times are half the normal DRAM access times.

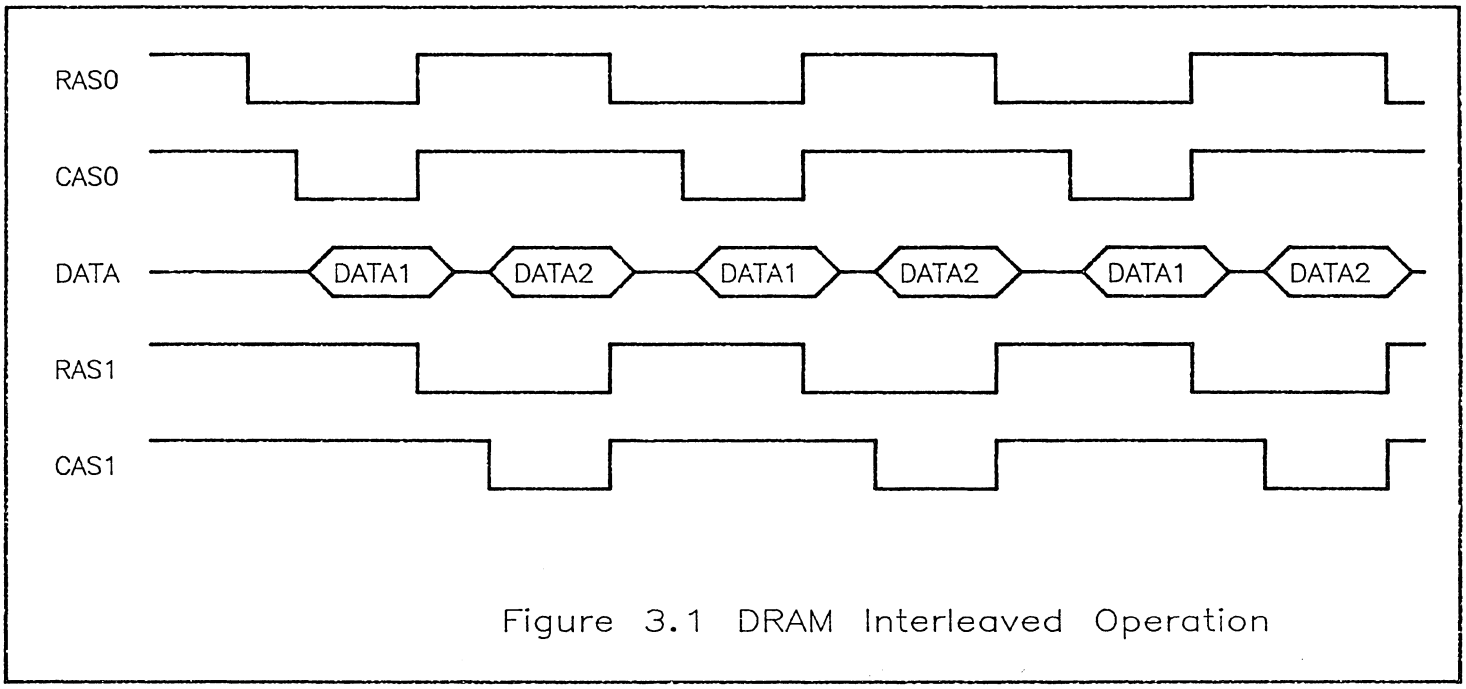


Figure 3.1 DRAM Interleaved Operation

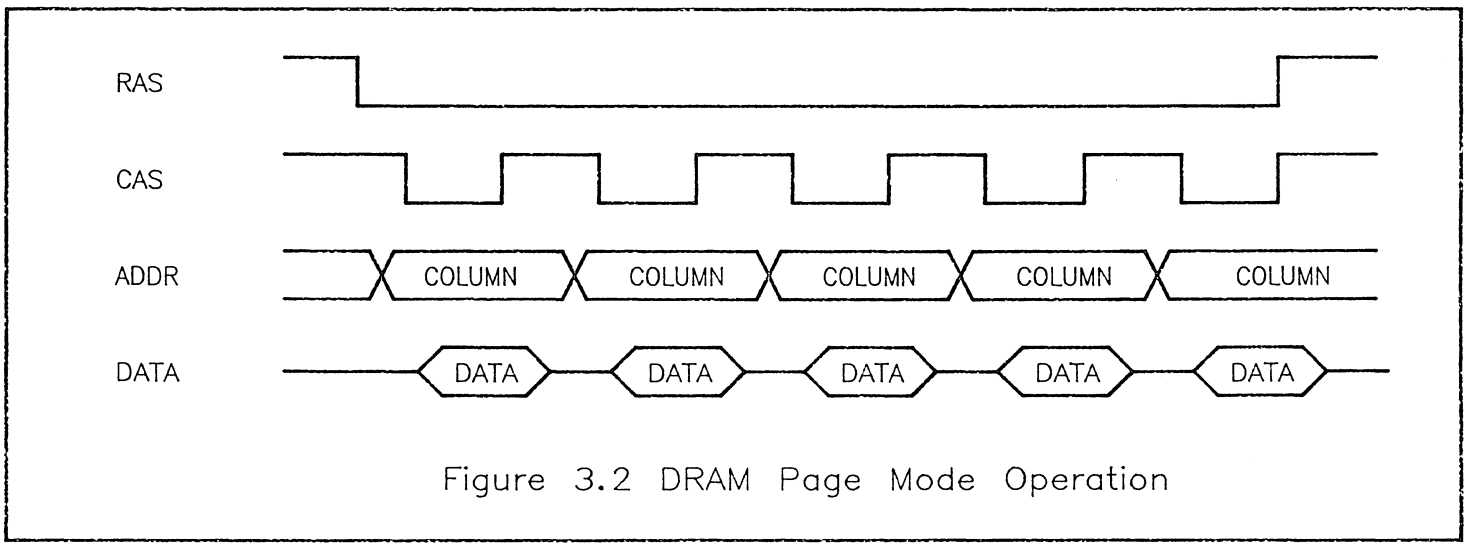


Figure 3.2 DRAM Page Mode Operation

256K X 1 DRAMs are internally configured as 256 rows and 256 columns. If thirty six 256K X 1 bit DRAMs are used to implement a bank, a page would have 256 X 4 bytes (excluding 4 bits for parity) = 1 Kbytes. When 1 MByte DRAMs are used, they are organized as 1024 rows and 1024 columns. For this case the page size would be four times as large i.e. 4KBytes. The maximum page size that can be realized using 1 MBit DRAMs and four way interleave scheme would be four 4KB pages. Thus paged mode DRAMs could be interleaved at 1 Kbyte to 16 Kbyte boundaries. Any access to the currently active -RAS page would occur in a short page access time rather than the normal DRAM access time and any subsequent access could be anywhere in the same 4/8/16 Kbyte boundary (depending upon the type of DRAMs used and the memory configuration), without incurring any penalty due to -RAS precharge. If memory is configured to take advantage of this DRAM organization, significantly better performance can be achieved over conventional interleaving because:

1 Page mode access time is shorter than normal DRAM access time. This allows more time in the DRAM critical paths, to achieve penalty free accesses or 'hits'.

2 The possibility of the next access being fast is significantly higher than in a regular interleaving scheme. This is because instructions and data tend to cluster together by principle of locality of reference. The DRAM -RAS lines for both banks can be held active till the -RAS active time out period, at which time a -RAS precharge for that bank is required. Typical hit ratios higher than 80% are possible using this scheme with the 82C322 memory controller, using the page/interleaved scheme, 120 nano second access time DRAMs can be used at 16 MHz and 100 nano seconds access time DRAMs at 20 MHz.

In a four way interleaved scheme, the page size is doubled, as the memory controller maintains four page registers active at the same time. Four way interleaved memory organization is shown in Figure 3.3. When using 256K DRAMs, the page size is 4K (4 sequential 1 Kbyte pages) bytes. The 1 MBit DRAMs support 1024 bit rows. The 82C322 Memory Controller takes advantage of the increased row size, and the resulting page size is 16K Bytes.

2.0 FUNCTIONAL DESCRIPTION

Figure 3.4 is a block diagram of the 82C322 memory controller. It consists of the following sub-modules:

- EPROM and DRAM control logic
- Refresh Logic
- System Control logic
- Memory Mapping and Refresh logic
- EMS Address Translation Logic
- MCA Channel Check Recovery Logic
- Configuration registers

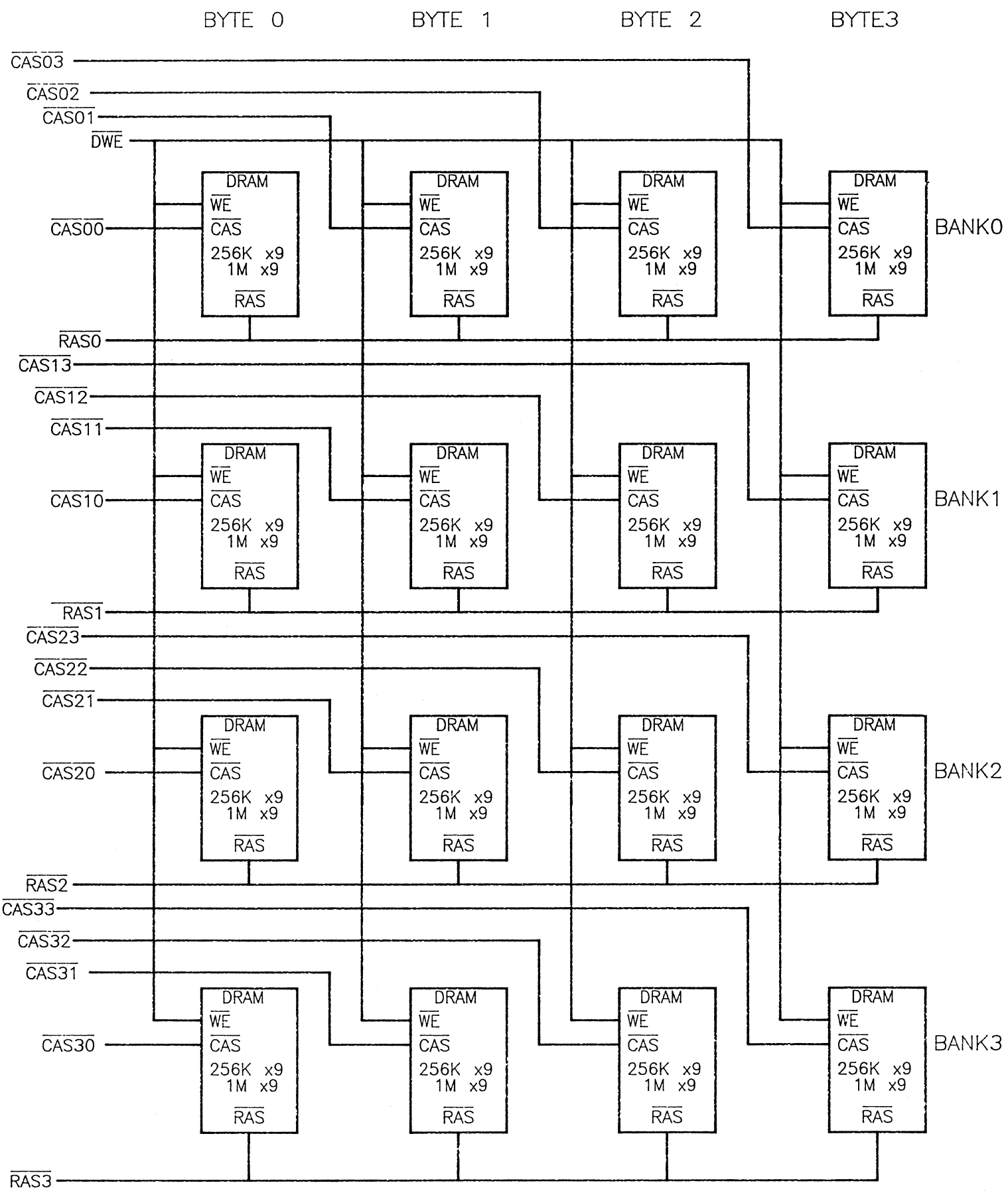


Figure 3.3 DRAM Organization

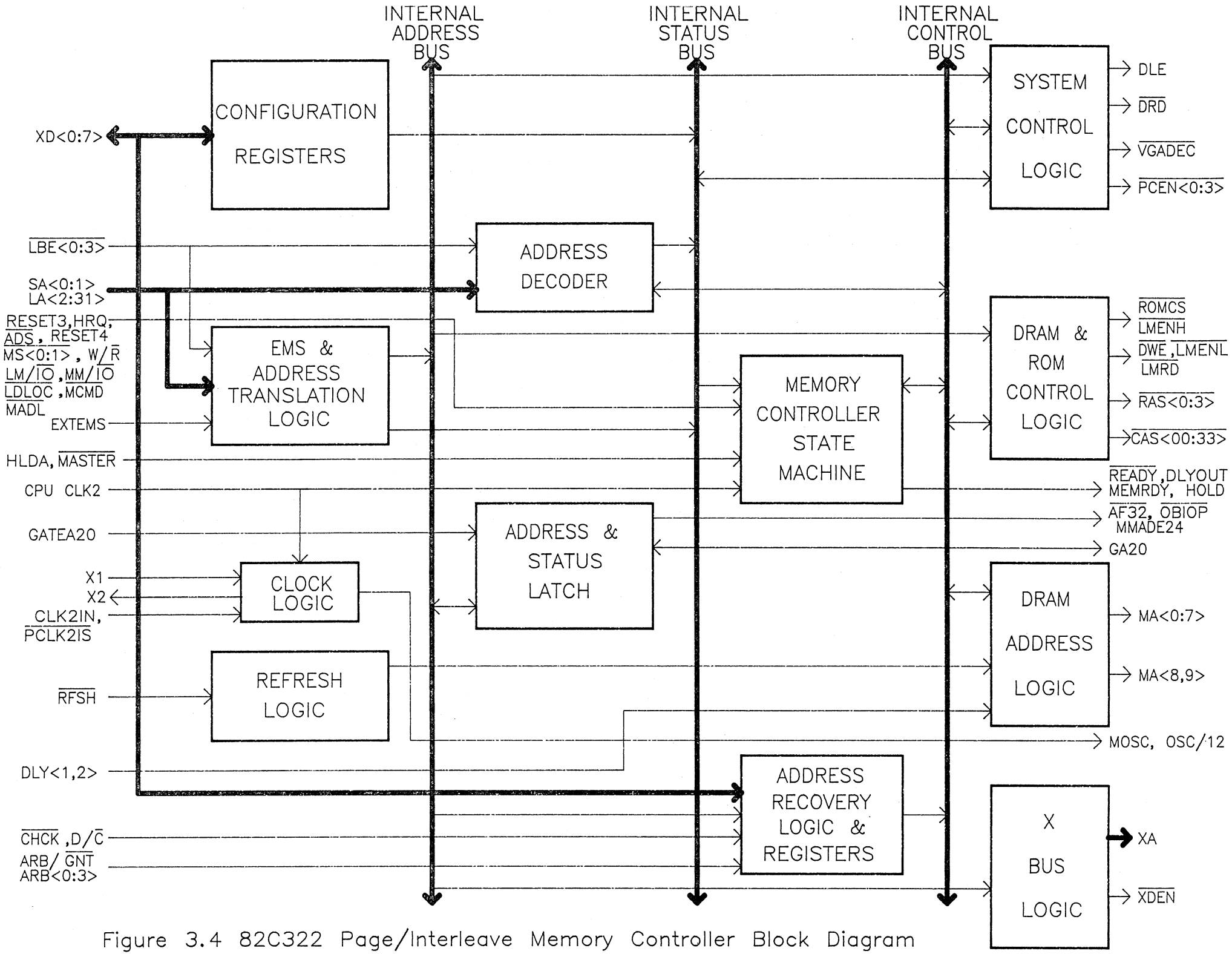


Figure 3.4 82C322 Page/Interleave Memory Controller Block Diagram

2.1 EPROM and DRAM Control Logic

The EPROM and DRAM control logic in the 82C322 is responsible for the generation of the -RAS, -CAS and -MWE signals for DRAM accesses and the generation of -ROMCS for EPROM accesses. This sub-module also generates -READY to the CPU upon completion of the desired local memory operation. The appropriate number of wait states are inserted, as programmed by software (or by default) in the wait state register of the 82C322.

2.2 Memory Access State Machines and Arbitration

The 82C322 supports memory requests from CPU, DMA, External Bus Masters and refresh requests. These accesses are arbitrated based on HLDA, -MASTER and -RFSH inputs. There are three state machines controlling each type of accesses. The CPU cycle state machine controls memory accesses requested by the CPU controller. The DMA and external Bus Master requests are handled by the DMA state machine. The refresh control state machine controls DRAM refresh operation.

The refresh state machine is in control when -RFSH is active. When HLDA is active then the DMA state machine is in control. The only difference between DMA accesses (HLDA active and -MASTER inactive) and an access from an external Bus Master (HLDA and -MASTER both active) is that for DMA accesses, with external EMS disabled,the "GA20" is an output (A20 is an input), while for Master cycles, with external EMS disabled the "GA20" is an input,while A20 is an output. When external EMS is enabled A20 is input and GA20 is tristated. In all other cases, the CPU cycle state machine is in control for valid DRAM addresses as defined by the memory map in the configuration registers. The arbitration is not preemptive in that the current access is terminated before relinquishing the control.

2.3 CPU Accesses

The 82C322 is tightly coupled to the 80386 processor. It has an integrated bus controller, that constantly monitors the processor address and control lines. When it receives valid address and status information from the processor, it decodes the addresses and accordingly generates -ROMCS or -OBIOP or initiates a DRAM memory cycle.

When 82C322 receives addresses to program its internal registers, it generatres -XDEN to enable input data via MA<0:7> lines. In all other cases MA<0:7> and MA<8:9> lines are used for providing row and column address information to the DRAMS.

The 82C322 allows only the CPU to initiate page mode accesses. It maintains four page registers, called active page registers, which store the page address of the most recently accessed DRAM pages of the two/four way interleaved banks. Accesses to active pages are called "hits' and are completed without additional wait states.

The 82C322 supports either one, two or four banks. Each bank has an active page register associated with it; the number of active pages vary with the amount of installed memory. In a single bank non-interleaved configuration, only one active register is in use. For each active page register in use, the corresponding -RAS stays asserted from the previous access. If the address stored in the active page register does not match the row address of the current access, then it is a "miss" cycle, and the -RAS line for that bank is de-asserted and activated following the RAS pre-charge time.

For CPU initiated access, the 82C322 monitors the processor address and status lines. When a valid memory request is detected, it activates -AF32 to the 82C321. The 82C321, when it samples -AF32 active, idles till the memory controller generates -READY to terminate the cycle. -RAS is maintained active if the current access is to an active page. If "page Hit" is not detected, then it de-asserts -RAS. After the programmed RAS pre-charge time, -RAS is asserted to select a new page. Appropriate -CAS and -WE signals are also generated. At the completion of the DRAM cycle, the 82C322 generates -READY back to the processor and the 82C321 to terminate the cycle.

2.4 DMA/Master Access

DMA and Master cycles are identical. The only difference is that for Master initiated requests, with external EMS disabled the 82C322 uses GA20 as input and A20 as an output For DMA cycles with external EMS disabled , A20 is an input and GA20 is an output. When external EMS enabled , for both DMA and MASTER cycles A20 is an input and GA20 is tristated. For all other cycles, the "GA20" is an output.

DMA/Master accesses are initiated by asserting HLDA. All the active -RAS lines are de-asserted on the low to high transition of HLDA. The DMA controller drives valid address and status information on the LA <0:23>, -LS0, -LS1 and LM/-IO outputs. The 82C322 receives -MS0, -MS1 and LM/-IO. The address and status information are decoded by the 82C322 to determine if it is an access to a memory location mapped by the 82C322. It uses the falling edge of -MADL to activate -RAS for the selected memory bank. As a result, the DMA cycle is always a non-page mode or conventional access to DRAMs.

For read cycles, -CAS is activated using DLY input (if external delay line mode is selected. If not selected, the internal delay lines are used for -RAS, -CAS generation). For write cycles, -CAS is activated by the later of -CMD or DLY2 input. -RAS is de-asserted the programmed delay after the assertion of -CAS (-CAS to -RAS delay is programmable in intervals of 0.5 PCLK2 cycles). -CAS is terminated following the de-activation of -CMD.

For DMA cycles, the 82C322 uses -MEMRDY to extend the cycle. -MEMRDY is driven inactive at the beginning of the cycle. It is driven active at the completion of the cycle. -MEMRDY is factored into the -CHRDYRTN logic and the 82C321 provides the ready signal. DRAM requests will not coincide with a refresh cycle already in progress, since the 82C223 provides the arbitration.

2.5 Refresh Cycles

Refresh cycles are initiated when the 82C322 samples HLDA and -RFSH active. All active RAS lines are driven high following the low to high transition on HLDA input. The 82C223 DMA controller generates the valid refresh address and status information for a refresh cycle. The 82C322 activates -RAS0 and -RAS3 following the falling edge of -CMD. -RAS1 and -RAS2 are activated after some delay which is dictated by the delay line (internal or external). All the -RAS lines are driven high following the de-activation of -CMD input.

The default refresh cycle is 200 ns. The refresh cycle can be extended by the -MEMRDY output from the 82C322. The 82C322 activates -MEMRDY following the falling edge of -MS0 or -MS1. It is deactivated following the activation of -MCMD. The 82C321 monitors -MEMRDY (it monitors -CHRDYRTN. Since -MEMRDY is factored into -CHRDYRTN logic, it indirectly samples -MEMRDY). When -CHRDYRTN is sampled active, the 82C223 DMA controller removes the -RFSH input at the end of the TC state. During refresh cycle 321 generates -READY.

2.6 RAS Time Out

When using Page Mode DRAMs, the maximum RAS low pulse width specification will be maintained. For most DRAMs, this is 10 microseconds (although some DRAMs have 30 to 100 micro seconds limit). The 82C322 maintains timers for each bank to ensure that the data integrity is maintained. RAS is de-asserted for each bank when its counter times out at about 10 microsecond intervals.

3.0 System Control Logic

The 82C322 allows users to locate the DRAMs on the Processor Local Data Bus. When DRAMs are located on the local data bus, it generates -LMRD, -LMENL and -LMENH for controlling the external data transceivers to channel the DRAM data to the processor. The 82C322 generates -
DRD and DLE to the 82C325 Data Buffer. The 82C325 uses the -DRD signal to determine memory data transfer direction (when Bus Master is reading the memory) and DLE to latch the data from the DRAMs during a memory operation. The 325 uses the latched data to generate parity bits during write operations.

Additionally, the 82C322 generates -XDEN during accesses to the internal registers of the 82C322. It is used to enable the XD0-7 lines onto the MA0-7 lines from an external buffer, for accessing the internal registers of the 82C322. -AF32 is issued by the 82C322 state machine. It is active for local memory accesses and meets the set up and hold times with respect to PROCCLK for the 82C321.

The 82C322 incorporates on-chip decode circuitry to generate -OBIOP (on board I/O) -VGADEC signal which connects directly to 82C451/52 VGA controller.

The -VGADEC signal is activated when:

1. A19 address line is high
2. A<20:31> address lines are low

When CPU is the bus master, this signal is latched with an internally generated ALE signal. When DMA or other bus masters are in control, this signal is latched by -MCMD input.

The On Board I/O Peripheral Decode (-OBIOPB) output is activated when A<15:10> address lines and M/IO input are all low. -OBIOP is not active for INTA cycles or DMA I/O accesses for address 0. When CPU is the bus master, -OBIOP is latched by an internally generated ALE signal. When DMA or an external master is in control, it latches on the high to low transition of -CMD.

3.1 Memory Mapping

The 82C322 has an extensive set of memory mapping registers for various memory organizations. The registers are discussed in section "Configuration Registers". Through the memory mapping logic, it is possible to map RAM that overlaps the EPROM and VIDEO area (640Kbyte - 896Kbyte assuming RAM split at 640K)) to the top of the 1 Mbyte area, as shown in Figure 3.5. Hence, for 1 Mbyte of on board RAM, the software can address it from 0 to 640 Kbytes and from 896Kbyte to 1.256Mbytes. The EPROM can be addressed from the 896 Kbyte area to the 1 Mbyte area.If the split is at 512K in the system RAM, then the RAM from 512K to 896K can be mapped from 1MB to 1.384Mbytes.

For normal mode of operation, only one bank of DRAMs may be used. However, for the page/interleaved mode of operation, RAM bank pairs must be used. If only one bank is present and the 322 configured in page/interleave mode then the memory works in page mode only.

3.2 Shadow RAM Feature

For efficient execution of BIOS, it is preferable to execute BIOS code through RAM rather than through slower EPROMs. The 82C322 provides the Shadow RAM feature, which if enabled, allows the BIOS code to be executed from system RAM resident at the same physical address as the BIOS EPROM. The software should transfer code stored in the BIOS EPROMs to the system RAM, before enabling the shadow RAM feature. This feature significantly improves the performance in BIOS-call intensive applications. Performance improvements as high as 300 to 400% have been observed in benchmark tests on the shadow RAM. The shadow RAM feature is invoked by copying the contents of BIOS EPROM to the same physical address(i.e. read the BIOS EPROM and write it to the same address)and disabling the ROM by writing 0 in bit 1 of Split Enable Register R23(I/O port E1).This bit disables the generation of -ROMCS for address range E0000-FFFFF on the system board, but does not disable any ROM on the option/adapter card.

If more than 1 Mbyte of system RAM exists, it is mapped as shown in Figure 3.6, if the shadow RAM feature has not been invoked. This means that RAM in the 640 Kbyte to 1 Mbyte area cannot be accessed. If the shadow RAM feature is used, then the RAM is mapped as shown in Figure 3.7, overlapping or Shadowing the EPROM area. In both cases, for accesses beyond the 1 Mbyte address range, the processor is switched from real to protected mode by the BIOS.

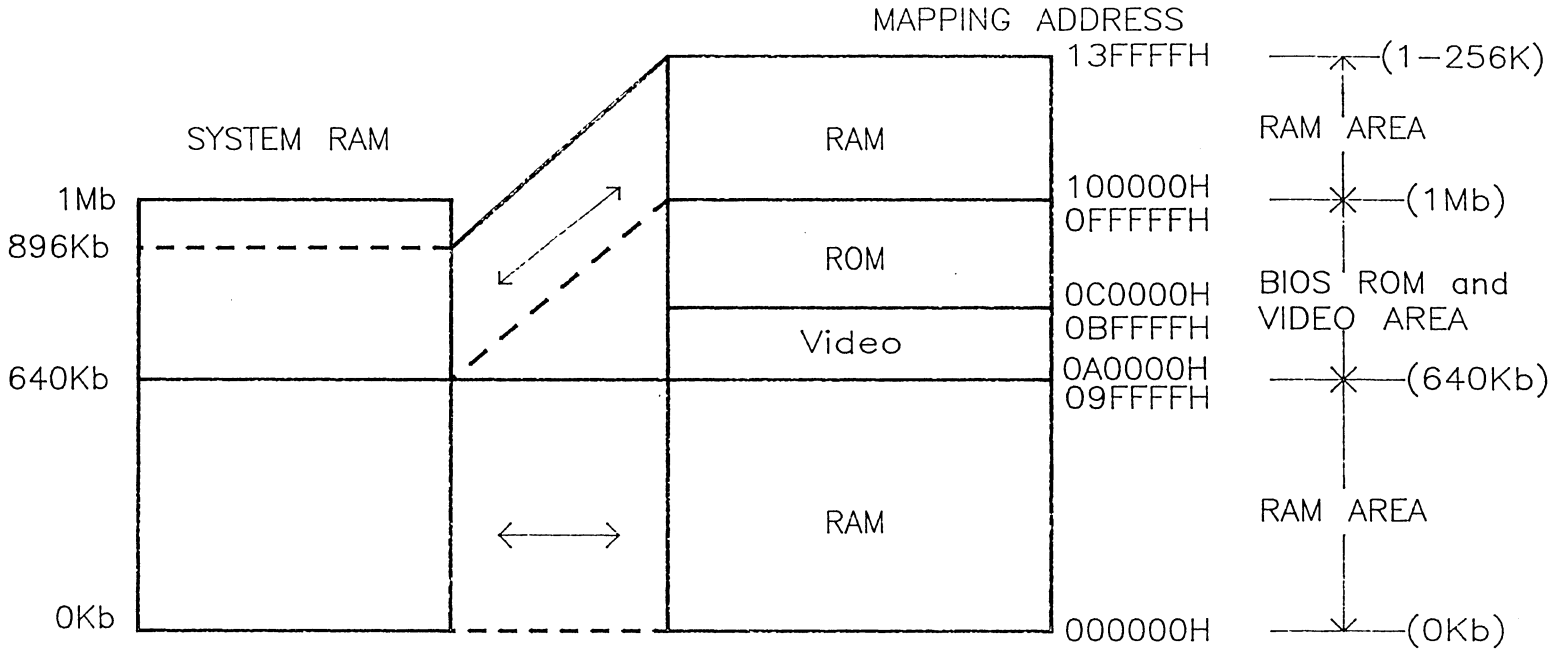


Figure 3.5 System RAM/ROM Mapping for 1MB System RAM

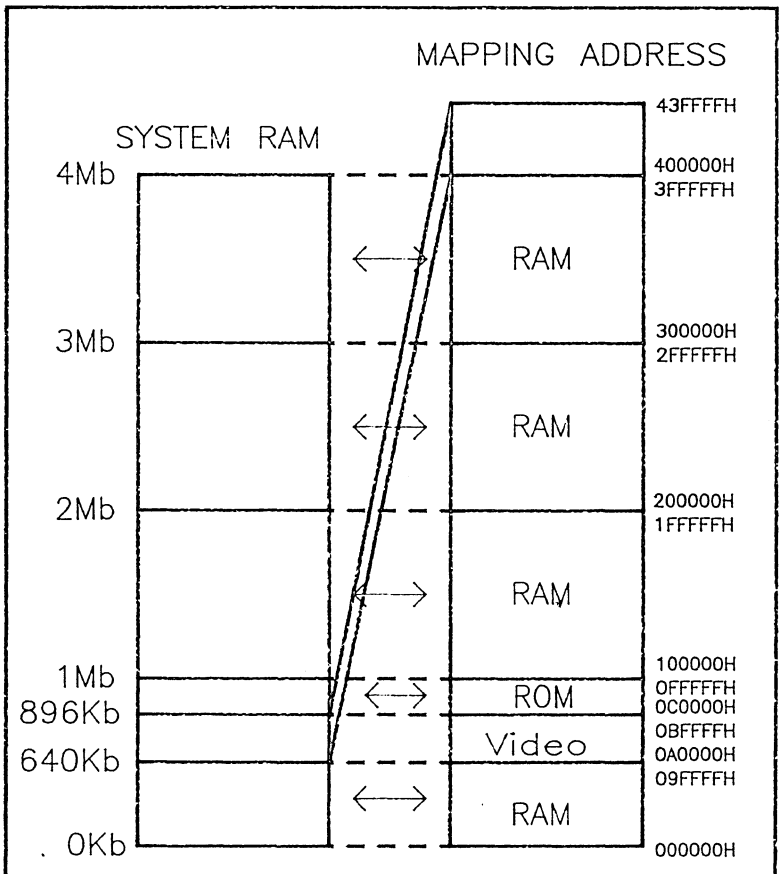


Figure 3.6 RAM/ROM Mapping Without Shadow RAM (More Than 1MB of RAM)

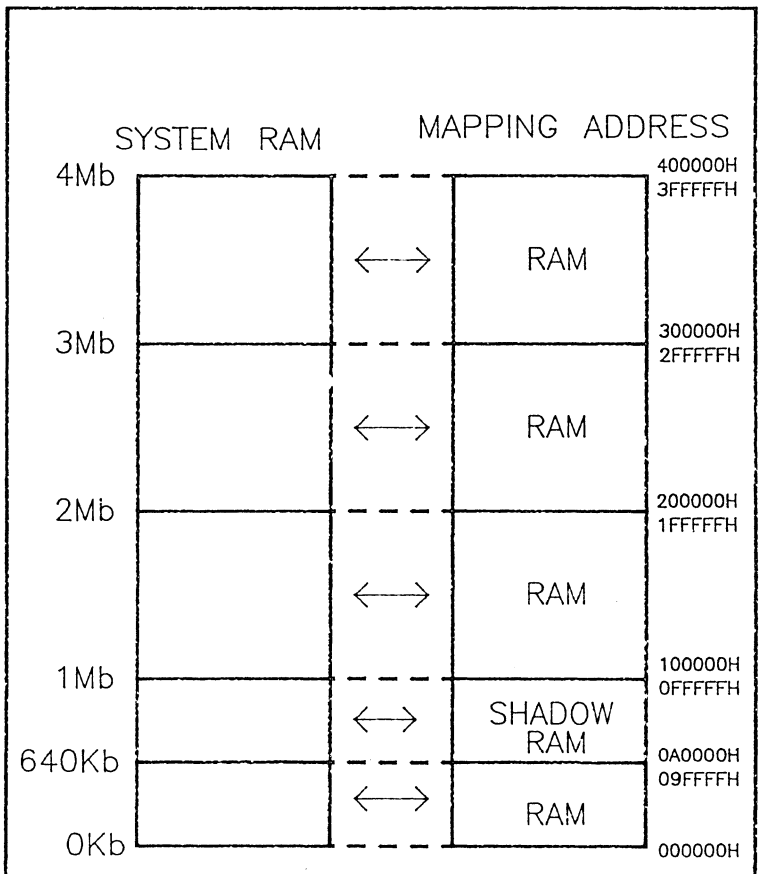


Figure 3.7 RAM Mapping with Shadow RAM (More Than 1MB of RAM)

3.3 EMS Address Translation Logic

Expanded Memory System or EMS is a memory mapping scheme used to map a 64 Kbyte block of memory in the EPROM area D0000H - DFFFFH to anywhere in the 1 Mbyte - 16 Mbyte area. This 64 Kbyte memory block is segmented into four 16 Kbyte pages. Through a translation table, each 16 Kbyte segment can be mapped any where in the 1 Mbyte to 16 Mbyte area. Since the 82C322 uses an on chip translation table in the EMS mode, address lines A14 to A22 are translated by the appropriate EMS mapping register. Hence, this scheme does not require switching between user and protected mode. Figure 3.8 shows the EMS organization with a possible translation scheme. It is possible for the 82C322 to map this 16Kbyte block to anywhere in the 0 to 16 Mbyte area. However, it is desirable to map this block above the 1 Mbyte area in order to not use the RAM space in the 0 to 640 Kbyte area. Although the EMS scheme translates the 64 Kbyte block in the D0000H - DFFFFH area, it is possible to select a 64 Kbyte block from the C0000H-CFFFFH or C4000H-D3FFFH or C8000H-D7000H or CC000H-DBFFFH as described in register R11.

External EMS mapper 82C631 could be used along with 82C322 for full implementation of EMS-LIM 4.0. In order to use the EMS mapper chip, the EXTERNAL EMS pin on 82C322 should be low and the internal EMS should not be needed at the same time.

3.4 16KB Memory Bad Block Remapping

The 82C322 supports Bad Block remapping registers that allow system BIOS to relocate up to 4 16KB defective blocks to any contiguous 64K memory segment. When the bad blocks are addressed, the 82C322 translates the addresses to access good memory blocks.

Refer to "16KB Faulty DRAM Relocation Registers" description for programming information.

3.5 System Board Memory Configuration

The Split Enable Register allows the first physical 1MB RAM to be split at 640K or 512K (depending on bit 2 of E1). The upper 384K or 256K (i.e 512K to 896K or 640K to 896K)can be re-mapped any where from 1MB to 15 MB on Mega Byte boundary, as specified in the Split RAM Address Register.

In a DOS environment, the VGA and BIOS EPROMs occupy the upper 384KB address space. When using a DRAM memory configuration greater than or equal to 1MB, there is an over lap of ROM and DRAM address space, beyond 640K. The 384K of DRAM space is not being utilized. This address space can be used in two ways.

1. The Split Enable Register and the Split Address Register can be used to perform the split (bit 3 in Split Enable Register R23 = 0) and to remap the 256K or 384K DRAM address any where from 1MB to 15 MB on Mega Byte boundaries.

2. The 384 KB of DRAMs can be used to shadow the BIOS EPROMs, whereby, the BIOS code is executed out of the DRAMs as opposed to the slower EPROMs. This is done by first copying the contents of the BIOS to the same physical address location. Then the Bit 1 (ROM ENABLE) of the Split Enable Register is set to 0 to disable the generation of -ROMCS. When BIOS code is subsequently accessed, they are retrieved from the DRAMs, rather than the slower EPROMs.

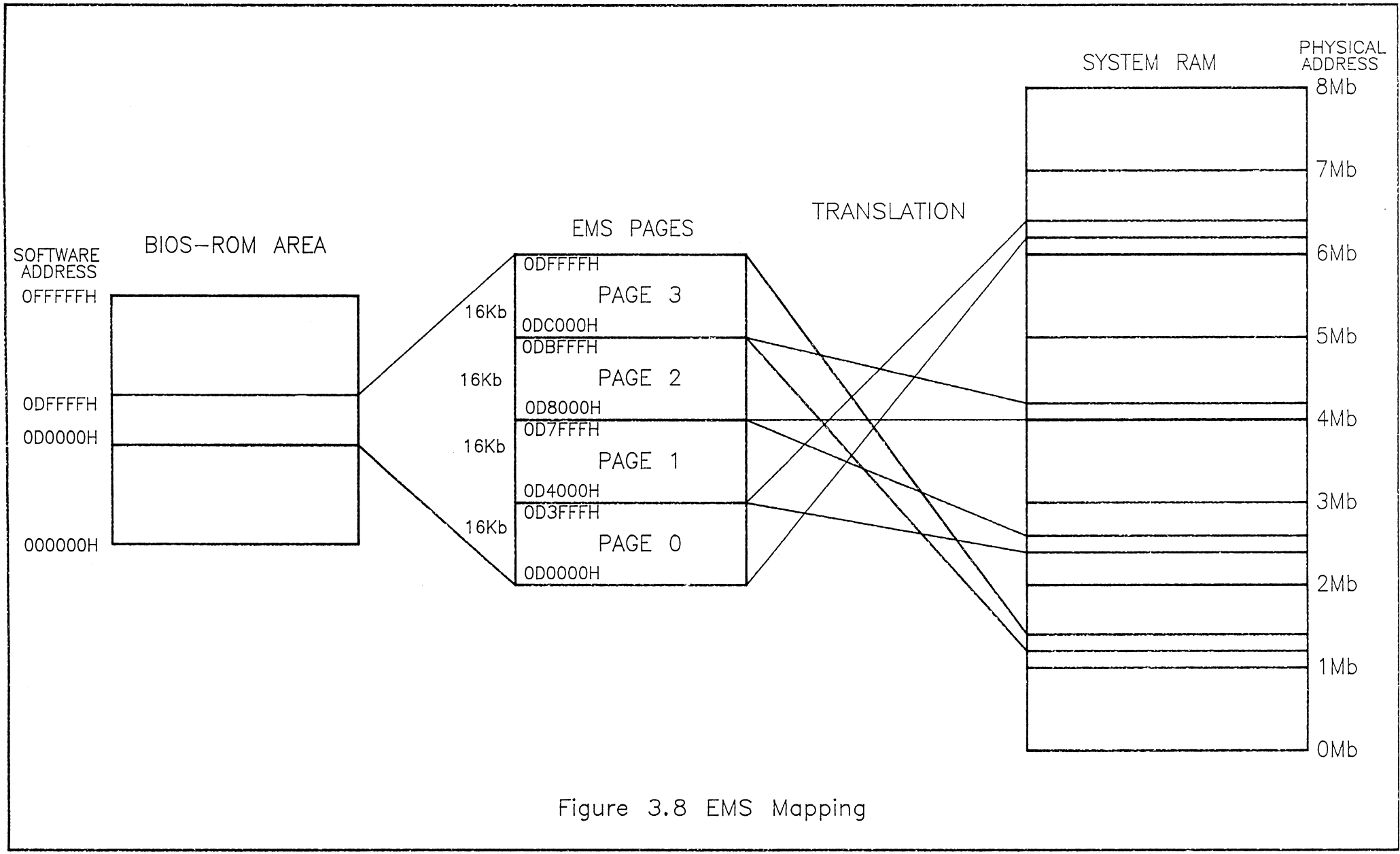


Figure 3.8 EMS Mapping

When the shadow RAM is enabled the memory between 640K (or 512k depending on SP640 bit , bit 3 in R23) and 896K is not used. The 82C322 provides Registers R4, R5 and R6 to shadow RAM the address range A0000 to DFFFF selectively, so that the RAM area below 896K could be used for shadowing. For Example it is desired to shadow RAM the address range C0000H to DFFFFH which is on the system board ROM. The steps for shadowing the the RAM are as follows:

a. Set bit 3 of R23(port E1) to 1 (disable the split)

b. Read the EPROM and write it to the same physical address(transfer the EPROM code to shadow RAM).

c. Set bits 4 and 5 of R4(index B5) to 1 (enable shadow RAM).

d. Set all bits of R6 to 1 (Enable shadow RAM).

This procedure shadows the EPROM area on the system board and it does not shadow any ROM on the adapter card (like ROM on the disk controller). To shadow any ROM on the adapter the procedure is the same as described above except that there should not be any ROM on the system board in that address range.

Registers R5 and R6 allows us to partially shadow RAM on a 16K boundary. The parts of memory which are not enabled cannot be used. The 82C322 also allows us to write protect the shadow RAM(bits 6 and 7 in R4) in the address range C0000H-DFFFFH.

3.6 Address Recovery Logic

Whenever there is a catastrophic error such as a parity error on the MCA, the addresses and control information of the command executed before the error was flagged (by -CHCK active) are latched in the 82C322. This information will be useful for diagnostic purposes. The address lines A2 to A30, M/IO, ARB/GNT, ARB10-ARB13 and D/-C signals are latched in these registers.

3.7 Memory Configurations

It is possible to use 1M bit or 256K bit DRAMs for system memory using the CHIPS/280 CHIPSet™. Possible configurations for on board memory are listed in Table 3.1. Each bank is 32 bits wide plus four bits for parity.

3.8 Parity Handling: The parity check enable bit is bit 0 in the Split Enable Register. If this bit is 0 (default) the parity checking is enabled. Bits 2 and 3 (Enable Parity and Channel check) of I/O port 61 should be 0 to enable the parity. When Parity error occurs (the 325 checks the parity) bit 7 of I/O Port (61) is set and the 325 generates a NMI to the CPU. The parity is cleared by toggling(write 1 and then 0)the bit 0 in Split Enable Register and also toggling (write 1 and then 0) bits 2 and 3 in I/O Port 61. The parity clearing routine will be a part of NMI rotine normally resident in the BIOS.

Table 3.1

	DRAM TYPE				TOTAL	EMS
	BANK0	BANK1	BANK2	BANK3	MEMORY	RANGE
1	0	0	0	0	disable	0
2	256K	0	0	0	1 Mb	0
3	1M	0	0	0	4Mb	1Mb to 4Mb
4	256K	256K	0	0	2Mb	1Mb to 2Mb
5	1M	1M	0	0	8Mb	1Mb to 8Mb
6	256K	256K	256K	0	3Mb	1Mb to 3Mb
7	256K	256K	1M	0	6Mb	1Mb to 6Mb
8	1M	1M	1M	0	12Mb	1Mb to 6Mb
9	256K	256K	256K	256K	4Mb	1Mb to 12Mb
10	256K	256K	1M	1M	10Mb	1Mb to 10Mb
11	1M	1M	1M	1M	16Mb	1Mb to 16Mb
12	256K	1M	0	0	5M	1Mb to 5Mb

Page/interleaving is possible for only those combinations with similar pairs of DRAMs. In table 3.1, page/interleaving is possible with combinations 4,5,9,10, and 11. For combination 6 and 8 bank 0 and 1 works in page/interleave mode and bank 2 works only in page mode.

4.0 CLOCKS AND CONTROL

Symbol	Type	PGA	PFP	Description
CLK2IN	I	99	16	CLOCK 2 INPUT is the TTL level input from a crystal oscillator having twice the rated frequency of the 80386 processor clock.
-PCLK2IS	I	68	67	PROCESSOR CLOCK 2 INPUT SELECT is internally pulled up. When high, CPU CLK2 is an output. When low, it is an input.
CPUCLK2	I/O	49	15	PROCESSOR CLOCK 2 is the MOS level clock output for the 80386 and 82C321 CPU controller, when -PCLK2IS is high. It is an input when -PCLK2IS is low, making it suitable for multi-processing environments.
X1	I	14	68	CRYSTAL 1 is the input from the 14.31818 MHz crystal.
X2	O	114	69	CRYSTAL 2 is the output to the 14.31818 MHz crystal.
MOSC	O	69	71	OSCILLATOR is the 14.31818 MHz TTL level system clock output. This signal is buffered before driving the MCA OSC line.
OSC/12	O	115	70	OSCILLATOR divided by 12 is the 1.19318 MHz clock output, used by the 82C321 CPU controller and 82C226 Integrated Peripherals Controller.

RESET4	I	90	134	RESET 4 is the active high reset input from the 82C321. It resets the configuration registers to their default values. When active, RAS<0:3> and CAS<00:31> remain high.
-RFSH	I	65	59	REFRESH is an active low input for DRAM refresh control from the 82C223 DMA Controller. It initiates a refresh cycle for the DRAMs.
-MS0 -MS1	I I	39 132	133 132	STATUS input lines from the M Bus are active low. These lines are monitored to detect the start of a cycle. The 82C321 drives these pins for CPU, DMA and Refresh cycles. For MASTER cycles, these signals are driven by the MASTER residing on the Micro Channel.
LM/- I/O	I	95	4	CPU MEMORY I/O input signal. When high it indicates a CPU memory cycle and when low, it indicates a CPU I/O cycle.
-ADS	I	97	10	ADDRESS STATUS is an active low input from the 80386 CPU indicating the initiation of a CPU cycle.
HRQ	I	112	60	HOLD REQUEST is the active high, asynchronous input from the 82C223 DMA Controller.
HOLD	O	98	12	HOLD is the active high, synchronized hold request output to the 80386 CPU in response to HRQ
HLDA	I	139	13	HOLD ACKNOWLEDGE is an active high input from the CPU. It is used to distinguish between CPU and non-CPU cycles.

CLOCKS AND CONTROL (continued)

-MASTER	I	40	135	MASTER is an active low input from the 82C223 DMA controller, indicating that an external master is in control of the MCA.
W/-R	I	137	5	Write/-Read is an input from the 80386 CPU. When high, it indicates a CPU write operation and when low it indicates a CPU read operation.
SA0 SA1	I I	35 34	123 122	SYSTEM ADDRESS LINES SA<0,1> are address inputs from the 82C321 for CPU and DMA cycles. They are input from the buffered MCA address lines A0, A1 for MASTER cycles.
-READY	I/O	47	11	READY is the system ready signal to the CPU. It is an active low output, after requested local DRAM data transfer is completed. It is an input for all other cycles. Ready is also used by 82C321 to indicate that the memory cycle is completed.
-AF32	O	38	129	AF32 is an active low output asserted on local memory (DRAM) cycles. It is high for all other cycles. This signal is sampled by the 82C321. Pull up of 10K is suggested.
LA2 LA3 LA4 LA5 LA6 LA7 LA8	I I I I I I I	52 100 101 142 53 102 54	21 22 23 24 25 26 27	LOCAL ADDRESS input lines A <2:31> from the CPU or 82C322 DMA controller (A<2:23>) or MASTER, through a buffer.

CLOCKS AND CONTROL (continued)

LA9	I	55	28	
LA10	I	103	29	
LA11	I	143	30	
LA12	I	104	31	
LA13	I	56	32	
LA14	I	144	33	
LA15	I	105	34	
LA16	I	57	35	
LA17	I	58	38	
LA18	I	2	39	
LA19	I	59	40	
LA20	I/O	107	41	
LA21	I	3	42	
LA22	I	60	43	
LA23	I	4	44	
LA24	I	108	45	
LA25	I	61	46	
LA26	I	5	47	
LA27	I	62	48	
LA28	I	109	49	
LA29	I	6	50	
LA30	I	7	51	
LA31	I	63	52	

CLOCKS AND CONTROL (continued)

-LBE0 -LBE1 -LBE2 -LBE3	I I I I	138 46 96 45	9 8 7 6	BYTE ENABLES <0:3> are active low inputs from the CPU for transfer of data on the four different bytes of the 32 bit data word. These lines are driven by the 82C321 for DMA and MASTER cycles.
MMADE24	I/O	64	58	M BUS MEMORY ADDRESS 24 is an active high output when LA24-LA31 address lines are all low. It is low for extended 32 bit addressing and is an input during DMA, Refresh and MASTER cycles. An external pull-up resistor of 10K is required. During MASTER cycles -AF32 will not be generated if MMADE24 is low.
-MCMD	I	89	131	M BUS COMMAND is an active low command signal input. It indicates the duration of data transfer activity and is used to write to the internal registers of the 82C322.
-MADL	I	87	124	M BUS ADDRESS DECODE LATCH is an active low input used to latch valid addresses and status for DMA, MASTER and Refresh Cycles.
XA16	O	19	83	X ADDRESS LINE 16 is the three-state XA16 address line for the local I/O bus. The XA0 through XA15 address lines are generated externally.
-XDEN	O	135	142	X DATA BUS ENABLE is an active low output that enables the transceiver between the X Data Bus and the MA<0:7> lines.

ADDRESS RECOVERY INTERFACE

Symbol	Type	PGA	PFP	Description
-CHCK	I	113	66	CHANNEL CHECK is an active low input signal from the MCA indicating a catastrophic error on the channel such as parity error. It is used to latch the address and status of the MCA.
D/-C	I	44	3	DATA/COMMAND is an input from the 80386 CPU. When high it indicates a data transfer and when low, it indicates a command transfer. It is latched when -CHCK is active.
ARB/-GNT	I	11	61	ARBITRATE/GRANT is an input from the MCA. When high, it indicates that channel arbitration is in progress. When low, it indicates that the requesting MASTER/DMA device with highest priority has been granted the channel. It is latched when -CHCK is active.
ARB0 ARB1 ARB2 ARB3	I I I I	66 12 13 67	62 63 64 65	ARBITRATION lines <0:3> are input from the MCA, supporting 16 priority levels. These lines are latched when -CHCK is active

Local Memory Interface

Symbol	Type	PGA	PFP	Description
-ROMCS	O	74	84	ROM CHIP SELECT is an active low chip select output to the BIOS EPROMs. It can be also connected to the output enable pin of the EPROMs. It is activated for the address range C0000-FFFFFH. If the ROMEN bit in E1 is disabled then -ROMCS is activated in the address range C0000-DFFFFH.
-RAS0 -RAS1 -RAS2 -RAS3	O O O O	75 21 20 119	88 87 86 85	ROW ADDRESS STROBES 3 to 0 are active low inputs used as RAS signals to the DRAMs for selecting different banks. -RAS3 selects the highest bank and -RAS0 selects the lowest bank. These signals should be buffered and line terminated with 33 Ohm resistors to reduce ringing before driving the DRAM RAS lines.
-CAS00 -CAS01 -CAS02 -CAS03 -CAS10 -CAS11 -CAS12 -CAS13 -CAS20 -CAS21 -CAS22 -CAS23 -CAS30 -CAS31 -CAS32 -CAS33	O O O O O O O O O O O O O O O O	30 82 81 125 122 77 76 24 124 28 80 123 79 27 26 78	111 110 107 106 96 95 94 93 105 104 103 102 101 100 99 98	COLUMN ADRESS STROBES are active low outputs used to individually select the four bytes of DRAMs of each bank. These signals should be line terminated with 33 OHM resistors to reduce ringing before driving the DRAM -CAS lines.

Local Memory Interface (continued)

Symbol	Type	PGA	PFP	Description
-LDLOC	I	41	136	LOCAL DRAM LOCATION is input to indicate the location of system DRAM. When low, the DRAMs are on the M Data Bus and when high, the DRAMs are on the L Data Bus (CPU Data Bus).
-LMRD	O	73	82	LOCAL MEMORY READ is an active low output for DRAM read cycles, used to set the direction of the transreceiver data paths when the DRAMs are on the Local Data Bus (LD Bus).
-LMENL	O	118	81	LOCAL MEMORY LOW WORD ENABLE is an active low signal for DRAM cycles, when located on the LD Bus. It is used to enable the low word, LD<0:15> between the CPU and DRAMs.
-LMENH	O	18	80	LOCAL MEMORY HIGH WORD ENABLE is an acive low signal for DRAM cycles, when located on the LD Bus. It is used to enable the high word, LD<16:31> between the CPU and DRAMs.
-DWE	O	25	97	DRAM WRITE ENABLE is an active low output for DRAM write enable.
DLE	O	94	2	DATA LATCH ENABLE is an active high output used to enable the local memory data buffer latch in the 82C325.

Local Memory Interface (continued)

-DRD	O	93	143	DATA READ is an active low output used to transfer data from the memory bus (MD Bus) to the CPU bus (LD Bus) in the 82C325. If high, it sets the data path from the CPU bus to the memory bus. If low, it sets the data path from the memory bus to the CPU bus.
DLYOUT	O	72	79	DELAY LINE OUT is an active high output to the delay line for generating the DRAM control signals during DMA or MASTER cycles if the external delay line is enabled.
DLY1 DLY2	I I	17 117	78 77	Delay IN 1, 2 are active high inputs from the first and second taps on the delay line used to generate DRAM control signals during DMA or MASTER cycles if the external delay line is enabled.
MA0 MA1 MA2 MA3 MA4 MA5 MA6 MA7	I/O I/O I/O I/O I/O I/O I/O I/O	129 86 33 85 128 32 84 31	121 120 119 118 117 116 115 114	MULTIPLEXED DRAM ADDRESS lines <MA0:MA7>. These lines should be buffered and line 75 terminated with Ohm resistors before driving the DRAM address lines. They are address (output) for DRAM cycles and become data lines for 82C322 I/O cycles. As data lines, they are used in conjunction with an external transceiver, to communicate with the internal registers of the 82C322.

Local Memory Interface (continued)

MA8 MA9	O O	127 83	113 112	M BUS ADDRESS line <MA8,MA9>. These lines should be buffered and line terminated with 75 Ohm resistors before driving the upper two DRAM address lines.
-PCEN0 -PCEN1 -PCEN2 -PCEN3	O O O O	134 42 92 133	141 140 139 138	PARITY CHECK ENABLES <0:3> are active low outputs. They are individually activated, when parity is enabled for 8, 16, 24 or 32 bit local DRAM accesses.
MEMRDY	O	71	76	MEMORY READY is an active high output, indicating that the local memory has successfully completed a memory transfer. This signal is used to generate the CHRDYRTN used by external MASTERS or the 82C321 during DMA cycles. MEMRDY is also generated during extended refresh cycles.
-EXTEMS	I	16	75	EXTERNAL EMS is an active low input indicating that external EMS mapping will be performed. This feature is useful when a large number of EMS mapped tasks are to be performed simultaneously.

MISCELLANEOUS

GA20	I/O	10	57	ADDRESS line 20 is the gated A20 bit which is controlled by GATEA20. With External EMS disabled It is output for CPU and DMA cycles and input for MASTER cycles. When external EMS is enabled, GA20 is tristated during DMA/MASTER cycles.

Symbol	Type	PGA	PFP	Description
GATEA20	I	88	130	GATE ADDRESS 20 is an input used to force A20 low when GATEA20 is low. When high it propagates CPU A20 on to the A20 line. It is used to keep address under 1Mb in DOS environments. It is high for DMA and MASTER cycles.
-OBIOP	O	91	137	ON BOARD I/O PORT is an active low output for all on board I/O accesses. It is active when LA15 through LA10 are all zero and M/IO is low. It is high for interrupt acknowledge cycles and for DMA I/O transfers when the address is 0.
VGADEC	O	70	74	VIDEO GRAPHICS ADAPTER DECODE is an active high output, indicating address lines A31 through A20 to be zero and A19 equal to one.

POWER SUPPLIES

Symbol	PGA	PFP	Description
VDD	136 140	1 18	Power Supply
	110 15 116 120 130 43	54 72 73 90 126 144	
VSS	141 1 106 111 121 29 126 131 48	14 19 20 36 37 55 56 91 92 108 109 127 128	Ground
NC	50 51 8 9 22 23 36 37	17 53 89 125	Not Connected

5.0 Configuration Registers

There are twenty seven configuration and diagnostics registers in the 82C322, R3 - R29. Registers R3 - R29 are accessed through I/O ports 22H and 23H normally found in the interrupt controller module of the 82C206 IPC. Registers R22 - R29 are accessed directly. An indexing scheme is used to reduce the number of I/O addresses required to access all of the index registers needed to configured and control the memory controller. Port 22H is used as an index register that points to the required data value accessed through port 23H. A write of the index value for the required data is performed to location 22H. This is then decoded and controls the multiplexers gating the appropriate register to the output bus. Every access to port 23H must be preceded by a write of the index value to port 22H even if the same data register is being accessed again. All bits marked as Reserved are set to zero by default and must be maintained that way during write operations.

Reg #	Register Name	Index	Location
R3	Version and Memory Enable	B4	82C322
R4	ROM Configuration	B5H	82C322
R5	Memory Enable Register 1	B6H	82C322
R6	Memory Enable Register 2	B7H	82C322
R7	Reserved Register	B8H	82C322
R8	Memory Type	B9H	82C322
R9	Operating Mode	BAH	82C322
R10	Timing Control	BBH	82C322
R11	EMS Base Address	BCH	82C322
R12	EMS Address Extension 1	BDH	82C322
R13	EMS Address Extension 2	BEH	82C322
R14	EMS Range Address Register	BFH	82C322
R15	Faulty DRAM Address Extension 1	C0H	82C322
R16	Faulty DRAM Address Extension 2	C1H	82C322
R17	Faulty DRAM Base Address 1	C2H	82C322
R18	Faulty DRAM Base Address 2	C3H	82C322

Reg #	Register Name	Index	Location
R19	Faulty DRAM Base Address 3	C4H	82C322
R20	Faulty DRAM Base Address 4	C5H	82C322
R21	Faulty DRAM Relocation Address	C6H	82C322

Reg #	Register Name	Address	Location
R22	Split Ram Address Register	E0H	82C322
R23	Split Enable Register	E1H	82C322, 82C325
R24	Channel Recovery Register(A30-A24)	E2H	82C322
R25	Channel Recovery Register(A23-A16)	E3H	82C322
R26	Channel Recovery Register(A8-A15)	E4H	82C322
R27	Channel Recovery Register(A2-A7)	E5H	82C322
R28	Channel Recovery Register(ARB13-10)	E6H	82C322
R29	Channel Recovery Register(D/C)	E7H	82C322

Version and Memory Enable Register R3

Index register port: 22H
Data register port: 23H
Index: B4H

Bits	Value	Function
0	0 1	Address map RAM on system board in 00000H-1FFFFH area. Address is on the Micro Channel Address is on the system board and is put out by the 82C322 Memory Controller (default).
1	0 1	Address map RAM on system board in 20000H-3FFFFH area. Address is on the Micro Channel Address is on the system board and is put out by the 82C322 Memory Controller (default).
2	0 1	Address map RAM on system board in 40000H-5FFFFH area. Address is on the Micro Channel Address is on the system board and is put out by the 82C322 Memory Controller (default).
3	0 1	Address map RAM on system board in 60000H-7FFFFH area. Address is on the Micro Channel Address is on the system board and is put out by the 82C322 Memory Controller (default).
4	0 1	Address map RAM on system board in 80000H-9FFFFH area. Address is on the Micro Channel Address is on the system board and is put out by the 82C322 Memory Controller (default).
5,6	0 0 Rest	82C322 Version number initial Reserved
7	0	Memory controller identifier bit (Reserved). 82C322 Page/Interleaved Memory Controller

ROM Configuration register R4:

Index register port: 22H
Data register port: 23H
Index: B5

Bits	Value	Function
0-3		Reserved
4	 1 0	Enable Shadow RAM at D0000H-DFFFFH. Disable ROM. Shadow RAM enabled (default) at D0000H - DFFFFH Disable Shadow RAM at D0000H-DFFFFH.
5	 1 0	Enable Shadow RAM at C0000H-CFFFFH. Disable ROM Shadow RAM enabled (default) at C0000H - CFFFFH Disable Shadow RAM at C0000H-CFFFFH.
6	1 0	Write protect Shadow RAM at D0000H-DFFFFH. Read/Write enabled (default) For RAM at D0000H-DFFFFH
7	1 0	Write protect Shadow RAM at C0000H-CFFFFH. Read/Write enabled (default) For RAM at C0000H-CFFFFH

Memory Enable Register 1 R5

Index register port: 22H
Data register port: 23H
Index: B6H

Bits	Value	Function
0		Enable Shadow RAM at B0000H-B3FFFH.
	0	Disable (default) - Disable Shadow RAM at B0000H-B3FFFH
	1	Enable - Enable Shadow RAM at B0000H-B3FFFH
1		Enable Shadow RAM at B4000H-B7FFFH.
	0	Disable (default) - Disable Shadow RAM at B4000H-B7FFFH
	1	Enable - Enable Shadow RAM at B4000H-B7FFFH
2		Enable Shadow RAM at B8000H-BBFFFH.
	0	Disable (default) - Disable Shadow RAM at B8000H-BBFFFH
	1	Enable - Enable Shadow RAM at B8000H-BBFFFH
3		Enable Shadow RAM at BC000H-BFFFFH.
	0	Disable (default) - Disable Shadow RAM at BC000H-BFFFFH
	1	Enable - Enable Shadow RAM at BC000H-BFFFFH
4		Enable Shadow RAM at A0000H-A3FFFH.
	0	Disable (default) - Disable Shadow RAM at A0000H-A3FFFH
	1	Enable - Enable Shadow RAM at A0000H-A3FFFH
5		Enable Shadow RAM at A4000H-A7FFFH.
	0	Disable (default) - Disable Shadow RAM at A4000H-A7FFFH
	1	Enable - Enable Shadow RAM at A4000H-A7FFFH
6		Enable Shadow RAM at A8000H-ABFFFH.
	0	Disable (default) - Disable Shadow RAM at A8000H-ABFFFH
	1	Enable - Enable Shadow RAM at A8000H-ABFFFH
7		Enable Shadow RAM at AC000H-AFFFFH.
	0	Disable (default) - Disable Shadow RAM at AC000H-AFFFFH
	1	Enable - Enable Shadow RAM at AC000H-AFFFFH

Memory Enable Register 2 R6

Index register port: 22H
Data register port: 23H
Index: B7H

Bits	Value	Function
0		Enable Shadow RAM at C0000H-C3FFFH.
	0	Disable (default) - Disable Shadow RAM at C0000H-C3FFFH
	1	Enable - Enable Shadow RAM at C0000H-C3FFFH
1		Enable Shadow RAM at C4000H-C7FFFH.
	0	Disable (default) - Disable Shadow RAM at C4000H-C7FFFH
	1	Enable - Enable Shadow RAM at C4000H-C7FFFH
2		Enable Shadow RAM at C8000H-CBFFFH.
	0	Disable (default) - Disable Shadow RAM at C8000H-CBFFFH
	1	Enable - Enable Shadow RAM at C8000H-CBFFFH
3		Enable Shadow RAM at CC000H-CFFFFH.
	0	Disable (default) - Disable Shadow RAM at CC000H-CFFFFH
	1	Enable - Enable Shadow RAM at CC000H-CFFFFH
4		Enable Shadow RAM at D0000H-D3FFFH.
	0	Disable (default) - Disable Shadow RAM at D0000H-D3FFFH
	1	Enable - Enable Shadow RAM at D0000H-D3FFFH
5		Enable Shadow RAM at D4000H-D7FFFH.
	0	Disable (default) - Disable Shadow RAM at D0000H-D3FFFH
	1	Enable - Enable Shadow RAM at D0000H-D3FFFH
6		Enable Shadow RAM at D8000H-DBFFFH.
	0	Disable (default) - Disable Shadow RAM at D8000H-DBFFFH
	1	Enable - Enable Shadow RAM at D8000H-DBFFFH
7		Enable Shadow RAM at DC000H-DFFFFH.
	0	Disable (default) - Disable Shadow RAM at DC000H-DFFFFH
	1	Enable - Enable Shadow RAM at DC000H-DFFFFH

Reserved Register R7

Index register port: 22H
Data register port: 23H
Index: B8H

Bits	Function
0,7	Reserved

Memory Type Register R8

Index register port: 22H
Data register port: 23H
Index: B9H

Bits	Value	Function
0	1 0	Fast time out enable. This bit if enabled, causes -RAS precharge during I/O or idle cycles. Fast time out disabled no RAS precharge during I/O or idle cycle (default)
1	 1 0	Vary -RAS precharge time, valid only if bit 0 = 1. 1 = 5 CPU CLK2 cycles. (default) 3 = CPU CLK2 cycles.

2:7 These bits contain DRAM bank and size information as listed below:

D7	D6	D5	D4	D3	D2	Bank0	Bank1	Bank2	Bank3
1	0	0	0	0	0	256Kb			
1	0	1	0	0	0	256Kb	256Kb		
1	0	1	1	0	0	256Kb	256Kb	256Kb	
1	0	1	1	0	1	256Kb	256Kb	256Kb	256Kb
1	0	1	1	1	0	256Kb	256Kb	1Mb	
1	0	1	1	1	1	256Kb	256Kb	1Mb	1Mb
0	1	1	0	0	0	256Kb	1Mb		
1	1	0	0	0	0	1Mb			
1	1	1	0	0	0	1Mb	1Mb		
1	1	1	1	1	0	1Mb	1Mb	1Mb	
1	1	1	1	1	1	1Mb	1Mb	1Mb	1Mb

Operating Mode Register R9

Index register port: 22H
Data register port: 23H (R/W)
Index: BAH

Bits	Value	Function
0		Reserved
1,2		Additional DRAM read access wait states. If bit 6 is set to 1 these bits are valid and provide additional wait states for read accesses for both page and non page mode.
	2 1 0 0 0 1 1 0 1 1	Extra Wait States / Total Wait States 0 / 1 1 / 2 2 / 3 RESERVED
3		EMS memory access wait states.
	0	0 No wait states introduced during
	1	1 (Default) Additional wait states introduced for EMS access.
4		EMS enable bit.
	0	Disabled (default) Disables the on chip EMS operation
	1	Enabled Enables the on chip EMS operation
5		DRAM write access wait states. If set to 0, accesses
	0	Accesses have 0 wait states
	1	Accesses have 1 wait state (default)
6		DRAM read access wait states. If set to 0, accesses
	0	Accesses have 0 wait states.
	1	Accesses have 1 wait state (default)
7		Page/Interleaved mode enable.
	0	Disables the page/interleaved mode, allowing usage of normal mode for the DRAMs.
	1	Enables page/interleaved mode for the DRAMs (default). It is recommemded to use the page interleave mode.

Timing Control Register R10

Index register port: 22H
Data register port: 23H
Index: BBH

Bits	Value	Function
0:1		Reserved
2	1 0	Memory Ready bit -MRDY generated to 82C321 during DMA/MASTER DRAM cycles.(default) -MRDY not generated to 82C321 during DMA/MASTER DRAM cycles.
3	1 0	Internal delay line for generation of contol signals Internal delay line is used to generate CAS for DRAMs during DMA/MASTER operations cycles. (default) External delay line is used to generate CAS for DRAMs during DMA/MASTER operations cycles.
4,5		These bits control the RAS hold time from CAS active for DMA or MASTER cycles.
	5,4 0 0 0 1 1 0 1 1	**Period** 2 CPU CLK2 cycles (Default) 2.5 CPU CLK2 cycles (Use this option for 25 MHZ CLK) 3 CPU CLK2 cycles 3.5 CPU CLK2 cycles
6	1 0	Refresh wait states. -MRDY generated during refresh cycles. (default) No -MRDY is generated during refresh cycles.
7	0 1	Column address setup time to -CAS, for DMA/MASTER cycles when internal delay line is used. Delay is 1/2 CPU CLK2. Delay is 1 CPU CLK2, ifinternal delay line is used. (Set this bit to 1 when CPU CLK IS 25 MHZ).

EMS Base Address Register R11

Index register port: 22H
Data register port: 23H (R/W)
Index: BCH

Bits	Function
0-3	These bits are used for the EMS page register I/O base address. The bits are encoded as follows, with unused combinations being reserved:

3,2,1,0	I/O Base
0 0 0 0	208H/209H
0 0 0 1	218H/219H
0 1 0 1	258H/259H
0 1 1 0	268H/269H
1 0 1 0	2A8H/2A9H
1 0 1 1	2B8H/2B9H
1 1 1 0	2E8H/2E9H

7-4	These bits are used for selecting the expanded memory base addresses. They are encoded as follows, with all unused combinations being reserved:

7,6,5,4	EMS Base Addresses
0 0 0 0	C0000H, C4000H, C8000H, CC000H
0 0 0 1	C4000H, C8000H, CC000H, D0000H
0 0 1 0	C8000H, CC000H, D0000H, D4000H
0 0 1 1	CC000H, D0000H, D4000H, D8000H
0 1 0 0	D0000H, D4000H, D8000H, DC000H

EMS Address Extension Register-1 R12

Index register port: 22H
Data register port: 23H
Index: BDH

Bits	Function
0:2	EMS Page 1 address extension bits. These bits correspond to address lines A21:A23
3	Reserved
4:6	EMS Page 0 address extension bits. These bits correspond to address lines A21:A23
7	Reserved

EMS Address Extension Register-2 R13

Index register port: 22H
Data register port: 23H
Index: BEH

Bits	Function
0:2	EMS Page 3 address extension bits. These bits correspond to address lines A21:A23
3	Reserved
4:6	EMS Page 2 address extension bits. These bits correspond to address lines A21:A23
7	Reserved

EMS Range Address Register R14

Index register port: 22H
Data register port: 23H
Index: BFH

Bits	Value	Function
0,1		Reserved
2	 0 1	This bit is used to enable the RAS time-out counter for page mode operation. The counter is disabled (Default) The counter is enabled
3	 0	External EMS enable Disable (default)
4-7		These bits are used to set the EMS memory space according to the following coding:
7,6,5,4		EMS Memory Size
0 0 0 1		1 Mbyte to top of system memory (16Mb max)
0 0 1 0		2 Mbyte to top of system memory (16Mb max)
0 0 1 1		3 Mbyte to top of system memory (16Mb max)
0 1 0 0		4 Mbyte to top of system memory (16Mb max)
0 1 0 1		5 Mbyte to top of system memory (16Mb max)
0 1 1 0		6 Mbyte to top of system memory (16Mb max)
0 1 1 1		7 Mbyte to top of system memory (16Mb max)
1 0 0 0		8 Mbyte to top of system memory (16Mb max)
1 0 0 1		9 Mbyte to top of system memory (16Mb max)
1 0 1 0		10 Mbyte to top of system memory (16Mb max)
1 0 1 1		11 Mbyte to top of system memory (16Mb max)
1 1 0 0		12 Mbyte to top of system memory (16Mb max)
1 1 0 1		13 Mbyte to top of system memory (16Mb max)
1 1 1 0		14 Mbyte to top of system memory (16Mb max)
1 1 1 1		15 Mbyte to top of system memory (16Mb max)

Faulty DRAM Address Extension Register 1 R15

Index register port: 22H
Data register port: 23H
Index: C0H

Bits	Function
0:2	Address extension bits for remapping 16Kb of bad DRAM in Page 1. The bits correspond to A21:A23
3	Reserved
4:6	Address extension bits for remapping 16Kb of bad DRAM in Page 0. The bits correspond to A21:A23
7	Reserved

Faulty DRAM Address Extension Register 2 R16

Index register port: 22H
Data register port: 23H
Index: C1H

Bits	Function
0:2	Address extension bits for remapping 16Kb of bad DRAM in Page 3. The bits correspond to A21:A23
3	Reserved
4:6	Address extension bits for remapping 16Kb of bad DRAM in Page 2. The bits correspond to A21:A23
7	Reserved

Faulty DRAM Base Address Register 1 R17

Index register port: 22H
Data register port: 23H
Index: C2H

Bits	Value	Function
0:6		Base address for remapping 16Kb of bad DRAM in Page 0. Bits 0 through 6 correspond to A14:A20
7	1 0	Enables the remapping of 16Kb for Page 0. Disables the remapping of 16KB for Page 0 (default)

Faulty DRAM Base Address Register 2 R18

Index register port: 22H
Data register port: 23H
Index: C3H

Bits	Value	Function
0:6		Base address for remapping 16Kb of bad DRAM in Page 1. Bits 0 through 6 correspond to A14:A20
7	1 0	Enables the remapping of 16Kb for Page 1. Disables the remapping of 16Kb for Page 1. (default)

Faulty DRAM Base Address Register 3 R19

Index register port: 22H
Data register port: 23H
Index: C4H

Bits	Value	Function
0:6		Base address for remapping 16Kb of bad DRAM in Page 2. Bits 0 through 6 correspond to A14:A20
7	 0	Enables the remapping of 16Kb for Page 2. Disables the remapping of 16Kb for Page 2. (default)

Faulty DRAM Base Address Register 4 R20

Index register port: 22H
Data register port: 23H
Index: C5H

Bits	Value	Function
0:6		Base address for remapping 16Kb of bad DRAM in Page 3. Bits 0 through 6 correspond to A14:A20
7	1 0	Enables the remapping of 16Kb for Page 3. Disables the remapping of 16Kb for Page 3. (default)

Faulty DRAM Relocation Address Register R21

Index register port: 22H
Data register port: 23H
Index: C6H

Bits	Function
0:7	These bits specify the base address corresponding to address lines A16:A23 of the 64Kb block where the four 16Kb bad DRAM pages will be remapped.

The following registers are used to define the memory setup features and are accessed directly through I/O ports (PS/2 TM compatible).

Split Ram Address Register R22

I/O Port Address : E0H

Bits	Functions
0:3	These bits specify the address which define the starting location of high portion of the first 1MB of active memory(portion of memory beyond the split). When SPLITEN = 0 (bit 3 in Memory Encoding Reg.),the address determines the starting location of the memory beyond the split(after 640K or 512K depending on the value of SP640 bit in the Memory Encoding Reg.). The bits correspond to address lines A20 - A23. The starting location can be any where from 1MB to 15MB on 1MB boundary. These bits may not be set to 0 unless SPLITEN = 1 (inactive).
4:7	Reserved

Split Enable Register R23

I/O Port Address : E1H

Bits	Value	Functions
0	 1 0	Parity Check Enable Bit. (82C325 also responds to this bit). Enables parity check on system board RAM. Disables Parity on the system board RAM (default)
1	 1 0	ROM Enable Bit. This bit is used to control generation of -ROMCS in the address range E0000- FFFFF. ROM is enabled Default.(-ROMCS is generated) ROM is disabled(-ROMCS is not generated).
2	 0	SP640 Bit. This bit determines where the first active 1MB block of RAM is split. The split is at 640K i.e the 640K of the first 1MB of memory is mapped into the first 640k of address space (0H-9FFFFH). The rest of 384K can be disabled (SPLITEN = 1) or mapped (SPLITEN = 0) as defined by Split Address Register. When the RAM is mapped using the split address register, only the RAM in the range 640-896K is relocated. The top 128K of the RAM (896k-1Mb) is not remapped. The RAM is split at 512K (instead of 640K). The remaining 384K can be disabled or mapped as describe earlier. (default)
3	 0 1	SPLITEN bit. This bit enables the portion of memory beyond the split. Enabled (default) Disabled
4:7		Reserved

The following registers R24 -R29 (I/O address E2 to E7) are used to obtain information when a serious system error (such as parity error) has occured on the microchannel bus. These registers are used in the channel check recovery logic. The registers hold the address bits A2-A30, and other bus control signals.

Registers	I/O Port	Bits	Contents
R24	E2	2:7	Address lines A24 - A30
R25	E3	0:7	Address lines A16 - A23
R26	E4	0:7	Address lines A8 - A15
R27	E5	2:7 1 0	Address lines A2 - A7 M/IO ARB/GNT
R28	E6	0:3 4:7	ARB10 - ARB13 Reserved
R29	E7	0 1:7	D/C Reserved

82C322 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	-	7.0	V
Input Voltage	V_I	-0.5	VCC + 0.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{OP}	-25o	85o	C
Storage Temperature	T_{STG}	-40o	125o	C
Maximum Power Dissapation		-	0.70	W

NOTE: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C322 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	VCC	4.75	5.25	V
Ambient Temperature	T_A	0o	70o	C

82C322 DC Characteristics

Operating Conditions: T_A =0oC to 70oC, VCC = 4.75 to 5.25V

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}	-0.5	1.8	V
Input High Voltage	V_{IH}	1.2	VCC+0.5	V
Output Low Voltage	V_{OL}	-	0.45	V (Note 1)
Output High Voltage	V_{OH}	2.4	-	V (Note 1)
Input Leakage Current $0<V_{IN}<V_{CC}$	I_{IL}	-30	+30	uA
Power Supply Current @ 25MHz	I_{CC}	-	100	mA
Output High-Z Leakage Current $0.45<V_{OUT}<V_{CC}$	I_{OZ1}	-70	+1.5	uA

Note 1: I_{OL} = 8mA and I_{OH} = -8mA for LD data bus and data bus MPO:3, NMI.
I_{OL} = 4mA and I_{OH} = -4mA for all other output pins.

CPU CYCLES:

INPUT REQUIREMENTS	Min	Max	Units	Notes
t354 LM/-IO setup from PCLK2	15		ns	
t355 LM/-IO hold from PCLK2	10		ns	
t356 -ADS setup from PCLK2	15		ns	
t357 -ADS hold from PCLK2	4		ns	
t362 -W/-R setup from PCLK2	15		ns	
t363 -W/-R hold from PCLK2	10		ns	
t367 -READY setup from PCLK2	10		ns	
t368 -READY hold from PCLK2	4		ns	
t369 LA<2:31> setup from PCLK2	20		ns	
t370 LA<2:31> hold from PCLK2	24		ns	
t371 LBE<0:3> setup from PCLK2	15		ns	
t372 -LBE<0:3> hold from PCLK2	24		ns	
t373 D/-C setup from PCLK2	15		ns	
t374 D/-C hold from PCLK2	10		ns	
t379 GATEA20 setup from PCLK2	25		ns	
t380 GATEA20 hold from PCLK2	10		ns	

OUTPUT DELAYS	Min	Max	Unit	Notes
t309 -AF32 active from address valid		45	ns	
t310 -AF32 inactive from address invalid		32	ns	
t311 -READY active delay from PCLK2		31	ns	
t312 -READY inactive delay from PCLK2	8	23	ns	
t313 -DRD active delay from PCLK2		40	ns	

OUTPUT DELAYS (continued)	Min	Max	Unit	Notes
t314 -DRD inactive delay from PCLK2	10	30	ns	
t315 DLE active delay from-CASi		10	ns	
t316 DLE inactive delay from -CASi		4.5	ns	
t317 -GA20 valid from CPU <A20> valid		20	ns	
t319 -DWE active delay from PCLK2	10	28	ns	
t320 -DWE inactive delay from PCLK2	0	21	ns	
t321 -CASi active delay from PCLK2(page md,CPU)	8	26	ns	
t322 -CASi inactive delay from PCLK2(page md,CPU)	7	30	ns	
t323 -RASi active delay from PCLK2(Page md,CPU)	8	28	ns	
t324 -RASi inactive delay from PCLK2(page md,CPU)	0	44	ns	
t325 -RASi precharge time		122	ns	
t337 PCEN<0:3> active from PCLK2		40	ns	
t340 DLE inactive delay from PCLK2	0	30	ns	
t346 Row address valid from PCLK2		40	ns	
t347 Column address valid from PCLK2	0	40	ns	
t348 Column address invalid from PCLK2	10	35	ns	
t349 -LMRD active delay from -CAS		35	ns	
t350 -LMRD inactive delay from -CAS		35	ns	
t381 -LEMNH(L) active delay from PCLK2		40	ns	
t382 -LEMNH(L) inactive delay from PCLK2		40	ns	
t388 Row address setup to -RASi	2		ns	
t389 Row address hold from -RASi	1		ns	
t390 Column address setup to -CASi	0		ns	

DMA CYCLES:

INPUT REQUIREMENTS	Min	Max	Unit	Notes
t352 MS<0:1> setup from -ADL(DMA/MSTR)	10		ns	
t353 MS<0:1> hold from -ADL(DMA/MSTR)	10		ns	
t364 SA<0:1> setup from -ADL(DMA/MSTR)	15		ns	
t365 SA<0:1> hold from -ADL(DMA/MSTR)	10		ns	
t358 HRQ setup from PCLK2	10		ns	
t359 HRQ hold from PCLK2	20		ns	

OUTPUT DELAYS	Min	Max	Unit	Notes
t303 DLYOUT active delay from RASi (non-page, external delay, DMA/MSTR)	0	8	ns	
t304 DLYOUT active inactive delay from RASi (non-page/DMA)	0	20	ns	
t305 Column address stable from DLY1 (non-page/DMA)	0	27	ns	
t306 Column address hold from DLY1 (non-page/DMA)	0	30	ns	
t307 -CASi active delay from DLY2 (non-page/DMA)	0	30	ns	
t328 -RAS <0:3> inactive delay from HLDA (for DMA, RFSH and MASTER cycles)	5	25	ns	
t333 -MRDY active from status active		50	ns	
t334 -MRDY inactive from CMD active		35	ns	
t335 -RASi inactive from PCLK2(DMA/MSTR)	10	50	ns	
t338 CAS<0:3> active from PCLK2 (non page mode internal delay option, DMA, MSTR)		40	ns	
t339 CAS<0:3> inactive from -CMD (non page mode internal delay option DMA, MSTR)		35	ns	
t341 HOLD active delay from PCLK2		30	ns	
t345 -RAS active from -ADL(DMA/MSTR)		44	ns	
t394 LA address to Row address delay (DMA/MSTR)		35	ns	

OUTPUT DELAYS (continued)	Min	Max	Unit	Notes
t395 -MWE active from ADL active		24	ns	
t396 -MWE inactive from ADL inactive		40	ns	

REFRESH CYCLES	Min	Max	Unit	Notes
t329 -RAS <0,3> active from -CMD(rfsh)		30	ns	
t330 -RAS <0,3> inactive from -CMD(rfsh)		25	ns	
t331 -RAS <1,2> active from PCLK2(rfsh)		35	ns	
t332 -RAS <1,2> inactive from PCLK2(rfsh)		40	ns	

REGISTER ACCESSES	Min	Max	Unit	Notes
t343 -XDEN active from -CMD active		30	ns	
t344 -XDEN inactive from -CMD active		30	ns	

MISCELLANEOUS:		Min	Max	Unit Notes
t326 -ROMCS active from PCLK2		30	ns	
t327 -ROMCS inactive from PCLK2		25	ns	
t342 MMADE24 active from PCLK2		30	ns	
t386 -OBIOP active delay from PCLK2		30	ns	
t387-OBIOP inactive from PCLK2		30	ns	
t375 ARB/-GNT set up to PCLK2	15		ns	
t376 ARB/-GNT hold from PCLK2	30		ns	
t377 ARB<0:3> setup to PCLK2	15		ns	
t378 ARB<0:3> hold from PCLK2	30		ns	

(T_A = 0°C to 70°C, VCC = 5V + 5%, A.C. load = 85pf)

CLOCKS	Min	Max	Units	Notes
t400 PCLK2 period	31		ns	
t401 PCLK2 low time	9		ns	At 2V
t402 PCLK2 high time	9		ns	At 2V
t403 PCLK2 rise time		8	ns VCC	0.8 to -0.8 V
t404 PCLK fall time		8	ns 0.8V	VCC -0.8 to

CPU CYCLES:

INPUT REQUIREMENTS	Min	Max	Units	Notes
t354 LM/-IO setup from PCLK2	15		ns	
t355 LM/-IO hold from PCLK2	10		ns	
t356 -ADS setup from PCLK2	15		ns	
t357 -ADS hold from PCLK2	4		ns	
t362 -W/-R setup from PCLK2	15		ns	
t363 -W/-R hold from PCLK2	10		ns	
t367 -READY setup from PCLK2	10		ns	
t368 -READY hold from PCLK2	4		ns	
t369 LA<2:31> setup from PCLK2	20		ns	
t370 LA<2:31> hold from PCLK2	24		ns	
t371 LBE<0:3> setup from PCLK2	15		ns	
t372 -LBE<0:3> hold from PCLK2	24		ns	
t373 D/-C setup from PCLK2	15		ns	
t374 D/-C hold from PCLK2	10		ns	
t379 GATEA20 setup from PCLK2	25		ns	
t380 GATEA20 hold from PCLK2	10		ns	

CPU CYCLES:

OUTPUT DELAYS	Min	Max	Units	Notes
t309 -AF32 active from address valid		45	ns	
t310 -AF32 inactive from address invalid		32	ns	
t311 -READY active delay from PCLK2		25	ns	
t312 -READY inactive delay from PCLK2	8	23	ns	
t313 -DRD active delay from PCLK2		40	ns	

CPU CYCLES:

OUTPUT DELAYS (continued)	Min	Max	Unit	Notes
t314 -DRD inactive delay from PCLK2	10	30	ns	
t315 DLE active delay from-CASi		10	ns	
t316 DLE inactive delay from -CASi		4.5	ns	
t317 -GA20 valid from CPU <A20> valid		20	ns	
t319 -DWE active delay from PCLK2	10	28	ns	
t320 -DWE inactive delay from PCLK2	0	21	ns	
t321 -CASi active delay from PCLK2(page md,CPU)	8	26	ns	
t322 -CASi inactive delay from PCLK2(page md,CPU)	7	30	ns	
t323 -RASi active delay from PCLK2(Page md,CPU)	8	28	ns	
t324 -RASi inactive delay from PCLK2(page md,CPU)	0	44	ns	
t325 -RASi precharge time		97	ns	
t337 PCEN<0:3> active from PCLK2		40	ns	
t340 DLE inactive delay from PCLK2	0	30	ns	
t346 Row address valid from PCLK2		40	ns	
t347 Column address valid from PCLK2	0	40	ns	
t348 Column address invalid from PCLK2	10	35	ns	
t349 -LMRD active delay from -CAS		35	ns	
t350 -LMRD inactive delay from -CAS		35	ns	
t381 -LEMNH(L) active delay from PCLK2		40	ns	
t382 -LEMNH(L) inactive delay from PCLK2		40	ns	
t388 Row address setup to -RASi	8		ns	
t389 Row address hold from -RASi	15		ns	
t390 Column address setup to -CASi	0		ns	

DMA CYCLES:

INPUT REQUIREMENTS	Min	Max	Unit	Notes
t352 MS<0:1> setup from -ADL(DMA/MSTR)	10		ns	
t353 MS<0:1> hold from -ADL(DMA/MSTR)	10		ns	
t364 SA<0:1> setup from -ADL(DMA/MSTR)	15		ns	
t365 SA<0:1> hold from -ADL(DMA/MSTR)	10		ns	
t358 HRQ setup from PCLK2	10		ns	
t359 HRQ hold from PCLK2	20		ns	

OUTPUT DELAYS	Min	Max	Unit	Notes
t303 DLYOUT active delay from RASi (non-page, external delay, DMA/MSTR)	0	8	ns	
t304 DLYOUT active inactive delay from RASi (non-page/DMA)	0	20	ns	
t305 Column address stable from DLY1 (non-page/DMA)	0	27	ns	
t306 Column address hold from DLY1 (non-page/DMA)	0	30	ns	
t307 -CASi active delay from DLY2 (non-page/DMA)	0	30	ns	
t328 -RAS <0:3> inactive delay from HLDA (for DMA, RFSH and MASTER cycles)	5	25	ns	
t333 -MRDY active from status active		50	ns	
t334 -MRDY inactive from CMD active		35	ns	
t335 -RASi inactive from PCLK2(DMA/MSTR)	10	50	ns	
t338 CAS<0:3> active from PCLK2 (non page mode internal delay option, DMA, MSTR)		40	ns	
t339 CAS<0:3> inactive from -CMD (non page mode internal delay option DMA, MSTR)		35	ns	
t341 HOLD active delay from PCLK2		30	ns	
t345 -RAS active from -ADL(DMA/MSTR)		44	ns	
t394 LA address to Row address delay (DMA/MSTR)		35	ns	

OUTPUT DELAYS (continued)	Min	Max	Unit	Notes
t395 -MWE active from ADL active		24	ns	
t396 -MWE inactive from ADL inactive		40	ns	

REFRESH CYCLES	Min	Max	Unit	Notes
t329 -RAS <0,3> active from -CMD(rfsh)		30	ns	
t330 -RAS <0,3> inactive from -CMD(rfsh)		25	ns	
t331 -RAS <1,2> active from PCLK2(rfsh)		35	ns	
t332 -RAS <1,2> inactive from PCLK2(rfsh)		40	ns	

REGISTER ACCESSES	Min	Max	Unit	Notes
t343 -XDEN active from -CMD active		30	ns	
t344 -XDEN inactive from -CMD active		30	ns	

MISCELLANEOUS	Min	Max	Unit	Notes
t326 -ROMCS active from PCLK2		30	ns	
t327 -ROMCS inactive from PCLK2		25	ns	
t342 MMADE24 active from PCLK2		30	ns	
t386 -OBIOP active delay from PCLK2		30	ns	
t387-OBIOP inactive from PCLK2		30	ns	
t375 ARB/-GNT set up to PCLK2	15		ns	
t376 ARB/-GNT hold from PCLK2	30		ns	
t377 ARB<0:3> setup to PCLK2	15		ns	
t378 ARB<0:3> hold from PCLK2	30		ns	

CLOCKS	Min	Max	Units	Notes
t400 PCLK2 period	25		ns	
t401 PCLK2 low time	8		ns	At 2V
t402 PCLK2 high time	8		ns	At 2V
t403 PCLK2 rise time		8	ns VCC	0.8 to -0.8 V
t404 PCLK fall time		8	ns 0.8V	VCC -0.8 to

CPU CYCLES:

INPUT REQUIREMENTS	Min	Max	Units	Notes
t354 LM/-IO setup from PCLK2	15		ns	
t355 LM/-IO hold from PCLK2	10		ns	
t356 -ADS setup from PCLK2	15		ns	
t357 -ADS hold from PCLK2	4		ns	
t362 -W/-R setup from PCLK2	15		ns	
t363 -W/-R hold from PCLK2	10		ns	
t367 -READY setup from PCLK2	10		ns	
t368 -READY hold from PCLK2	4		ns	
t369 LA<2:31> setup from PCLK2	20		ns	
t370 LA<2:31> hold from PCLK2	24		ns	
t371 LBE<0:3> setup from PCLK2	15		ns	
t372 -LBE<0:3> hold from PCLK2	24		ns	
t373 D/-C setup from PCLK2	15		ns	
t374 D/-C hold from PCLK2	10		ns	
t379 GATEA20 setup from PCLK2	25		ns	
t380 GATEA20 hold from PCLK2	10		ns	

OUTPUT DELAYS	Min	Max	Unit	Notes
t309 -AF32 active from address valid		45	ns	
t310 -AF32 inactive from address invalid		32	ns	
t311 -READY active delay from PCLK2		20	ns	
t312 -READY inactive delay from PCLK2	8	23	ns	
t313 -DRD active delay from PCLK2		40	ns	

OUTPUT DELAYS (continued)	Min	Max	Unit	Notes
t314 -DRD inactive delay from PCLK2	10	30	ns	
t315 DLE active delay from-CASi		10	ns	
t316 DLE inactive delay from -CASi		4.5	ns	
t317 -GA20 valid from CPU <A20> valid		20	ns	
t319 -DWE active delay from PCLK2	10	28	ns	
t320 -DWE inactive delay from PCLK2	0	21	ns	
t321 -CASi active delay from PCLK2(page md,CPU)	8	26	ns	
t322 -CASi inactive delay from PCLK2(page md,CPU)	7	30	ns	
t323 -RASi active delay from PCLK2(Page md,CPU)	8	28	ns	
t324 -RASi inactive delay from PCLK2(page md,CPU)	0	44	ns	
t325 -RASi precharge time		77	ns	
t337 PCEN<0:3> active from PCLK2		40	ns	
t340 DLE inactive delay from PCLK2	0	30	ns	
t346 Row address valid from PCLK2		40	ns	
t347 Column address valid from PCLK2	0	40	ns	
t348 Column address invalid from PCLK2	10	35	ns	
t349 -LMRD active delay from -CAS		35	ns	
t350 -LMRD inactive delay from -CAS		35	ns	
t381 -LEMNH(L) active delay from PCLK2		40	ns	
t382 -LEMNH(L) inactive delay from PCLK2		40	ns	
t388 Row address setup to -RASi	13		ns	
t389 Row address hold from -RASi	15		ns	
t390 Column address setup to -CASi	0		ns	

(T_A = 0°C to 70°C, VCC = 5V + 5%, A.C. load = 85pf)

DMA CYCLES:

INPUT REQUIREMENTS	Min	Max	Unit	Notes
t352 MS<0:1> setup from -ADL(DMA/MSTR)	10		ns	
t353 MS<0:1> hold from -ADL(DMA/MSTR)	10		ns	
t364 SA<0:1> setup from -ADL(DMA/MSTR)	15		ns	
t365 SA<0:1> hold from -ADL(DMA/MSTR)	10		ns	
t358 HRQ setup from PCLK2	10		ns	
t359 HRQ hold from PCLK2	20		ns	

OUTPUT DELAYS	Min	Max	Unit	Notes
t303 DLYOUT active delay from RASi (non-page)	0	8	ns	
t304 DLYOUT active inactive delay from RASi (non-page)	0	20	ns	
t305 Column address stable from DLY1 (non-page)	0	27	ns	
t306 Column address hold from DLY1 (non-page)	0	30	ns	
t307 -CASi active delay from DLY2 (non-page)	0	30	ns	
t328 -RAS <0:3> inactive delay from HLDA (for DMA, RFSH and MASTER cycles)	5	25	ns	
t333 -MRDY active from status active		50	ns	
t334 -MRDY inactive from CMD active		35	ns	
t335 -RASi inactive from PCLK2(DMA/MSTR)	10	50	ns	
t338 CAS<0:3> active from PCLK2 (non page mode internal delay option, DMA, MSTR)		40	ns	
t339 CAS<0:3> inactive from -CMD (non page mode internal delay option DMA, MSTR)		35	ns	
t341 HOLD active delay from PCLK2		30	ns	
t345 -RAS active from -ADL(DMA/MSTR)		44	ns	
t394 LA address to Row address delay (DMA/MSTR)		35	ns	

OUTPUT DELAYS (continued)	Min	Max	Unit	Notes
t395 -MWE active from ADL active		24	ns	
t396 -MWE inactive from ADL inactive		40	ns	

REFRESH CYCLES	Min	Max	Unit	Notes
t329 -RAS <0,3> active from -CMD(rfsh)		30	ns	
t330 -RAS <0,3> inactive from -CMD(rfsh)		25	ns	
t331 -RAS <1,2> active from PCLK2(rfsh)		35	ns	
t332 -RAS <1,2> inactive from PCLK2(rfsh)		40	ns	

REGISTER ACCESSES	Min	Max	Unit	Notes
t343 -XDEN active from -CMD active		30	ns	
t344 -XDEN inactive from -CMD active		30	ns	

MISCELLANEOUS	Min	Max	Unit	Notes
t326 -ROMCS active from PCLK2		30	ns	
t327 -ROMCS inactive from PCLK2		25	ns	
t342 MMADE24 active from PCLK2		30	ns	
t386 -OBIOP active delay from PCLK2		30	ns	
t387 -OBIOP inactive from PCLK2		30	ns	
t375 ARB/-GNT set up to PCLK2	15		ns	
t376 ARB/-GNT hold from PCLK2	30		ns	
t377 ARB<0:3> setup to PCLK2	15		ns	
t378 ARB<0:3> hold from PCLK2	30		ns	

CLOCK	Min	Max	Units	Notes
t400 PCLK2 period	20		ns	
t401 PCLK2 low time	7		ns	At 2V
t402 PCLK2 high time	7		ns	At 2V
t403 PCLK2 rise time		7	ns VCC	0.8 to -0.8 V
t404 PCLK fall time		7	ns 0.8V	VCC -0.8 to

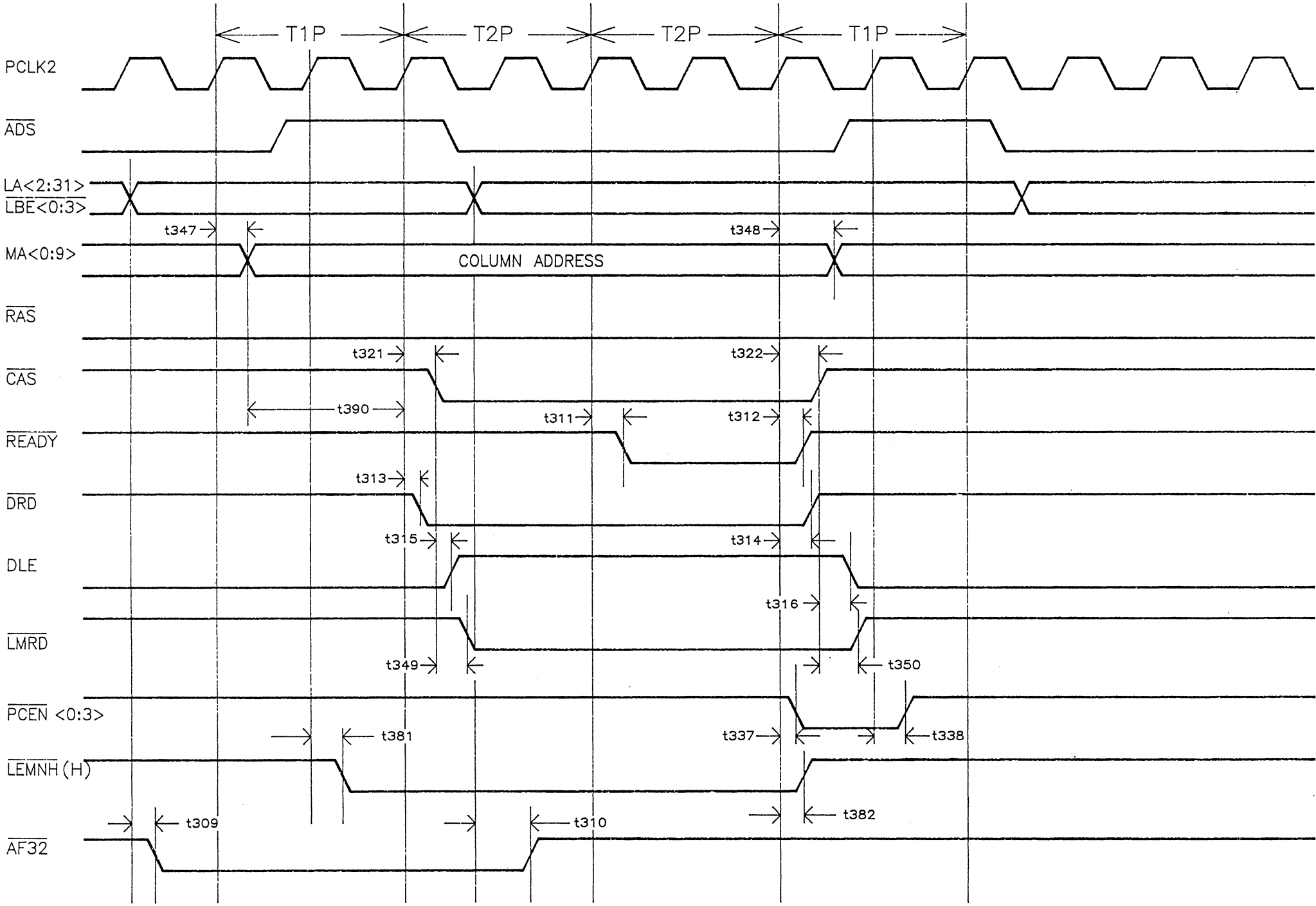


Figure 4.1 Memory on LD Bus, Page Mode, 1 Wait State, Read Hit Cycle

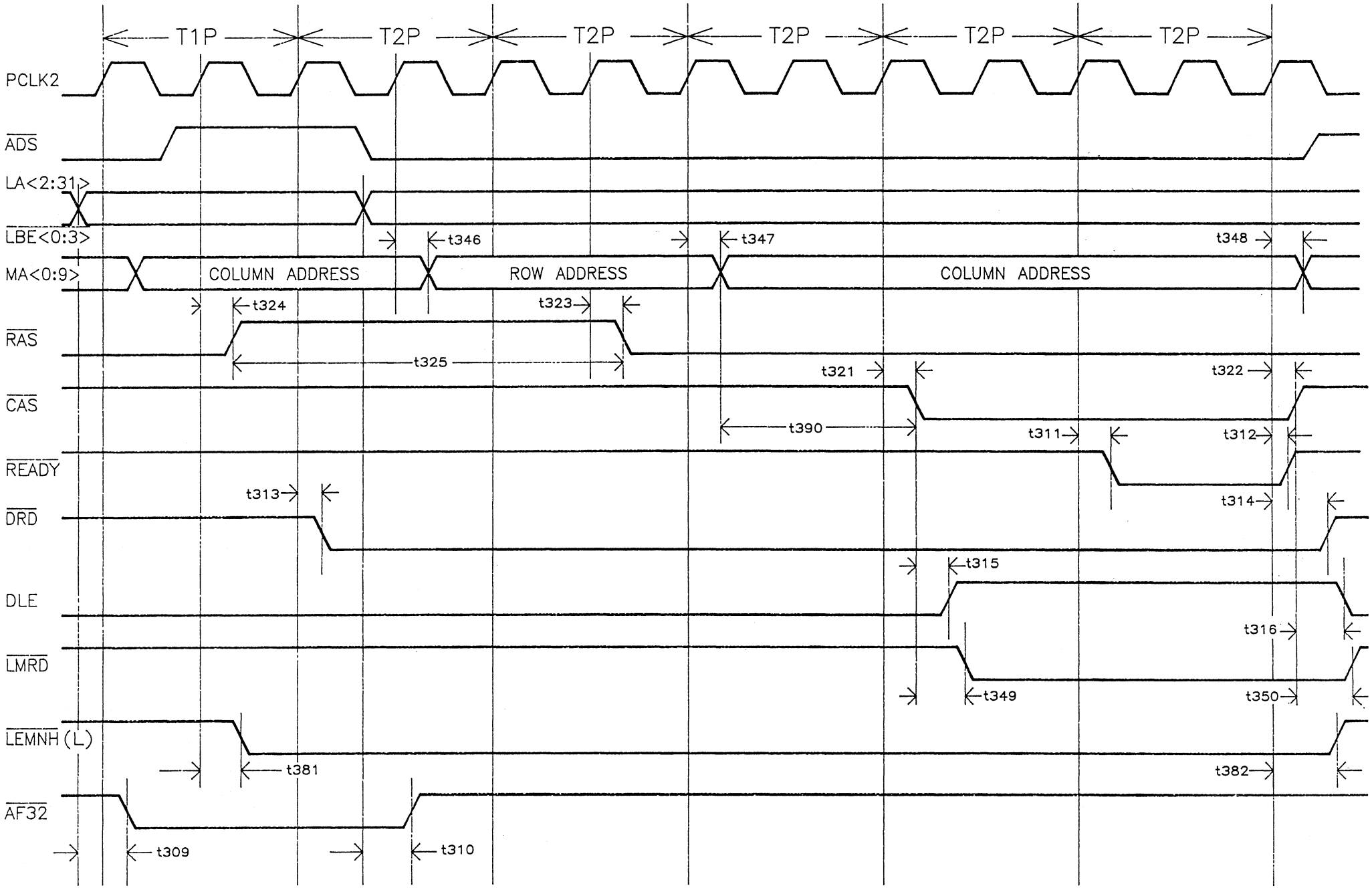


Figure 4.2 Memory on LD Bus, Page Mode, 1 Wait State, Page Miss, Read Cycle

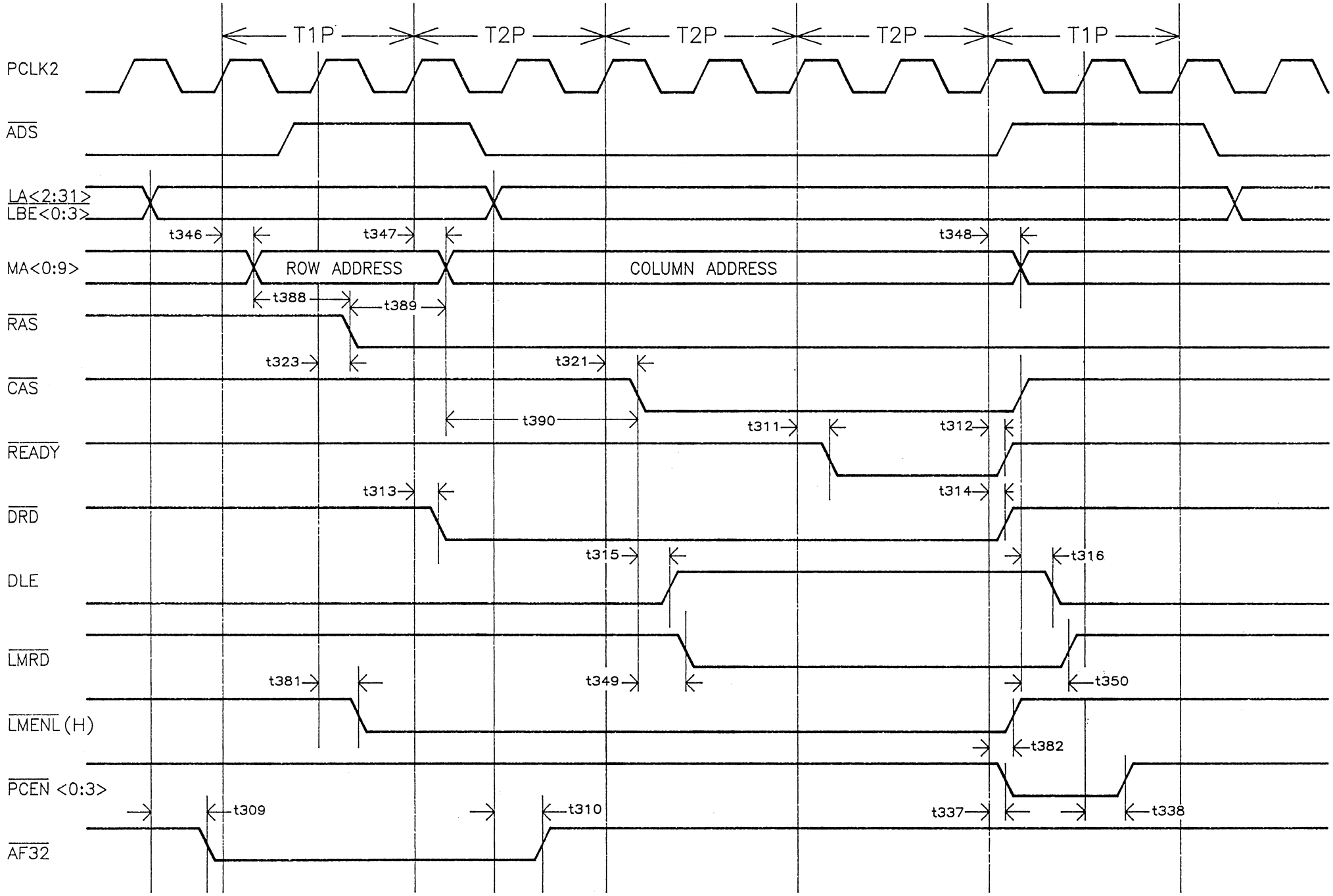


Figure 4.3 Memory on LD Bus, Page Mode, 1 Wait State, RAS High, Read Cycle

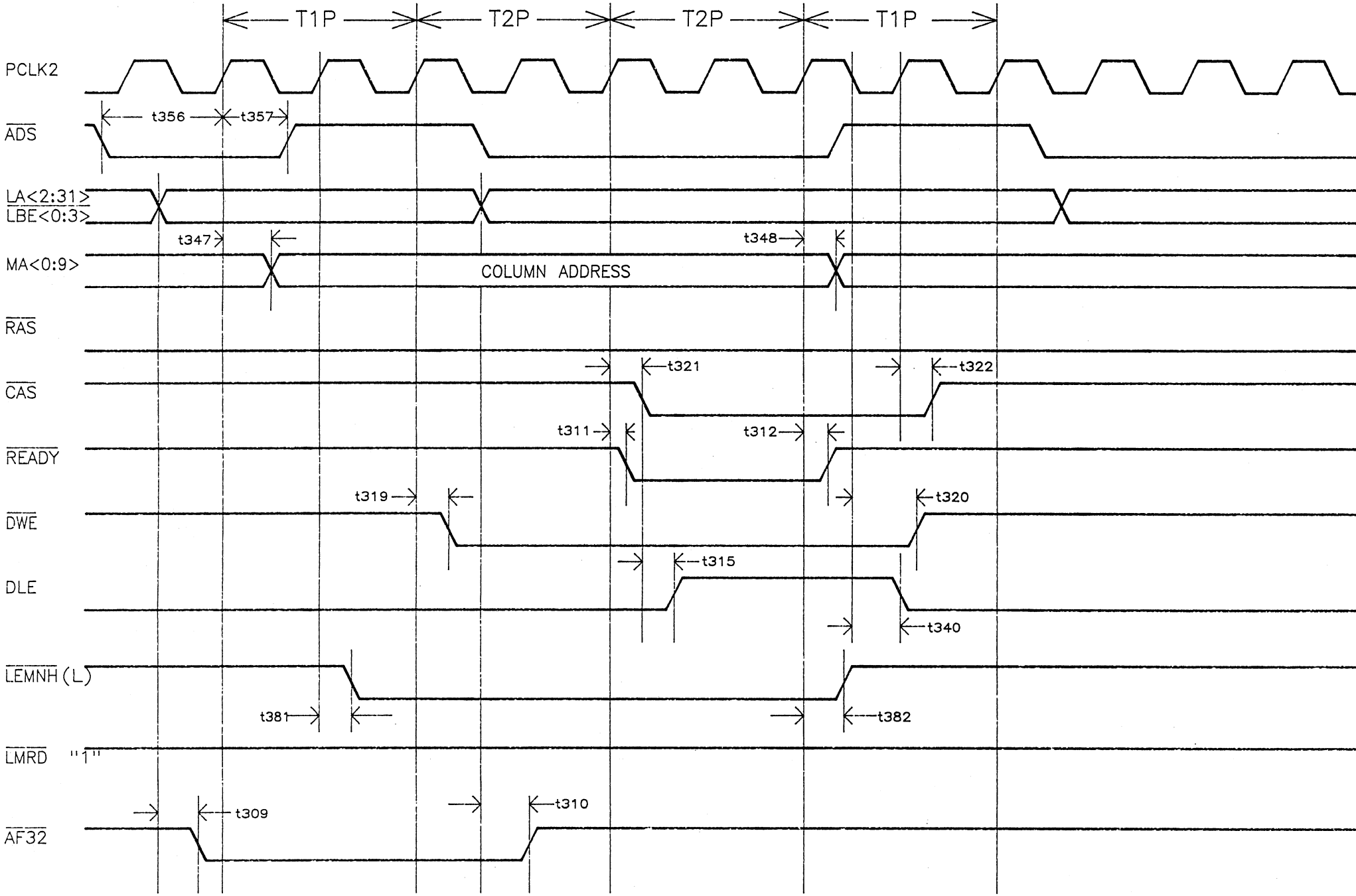


Figure 4.4 Memory on LD Bus, Page Mode, 1 Wait State, Write Hit Cycle

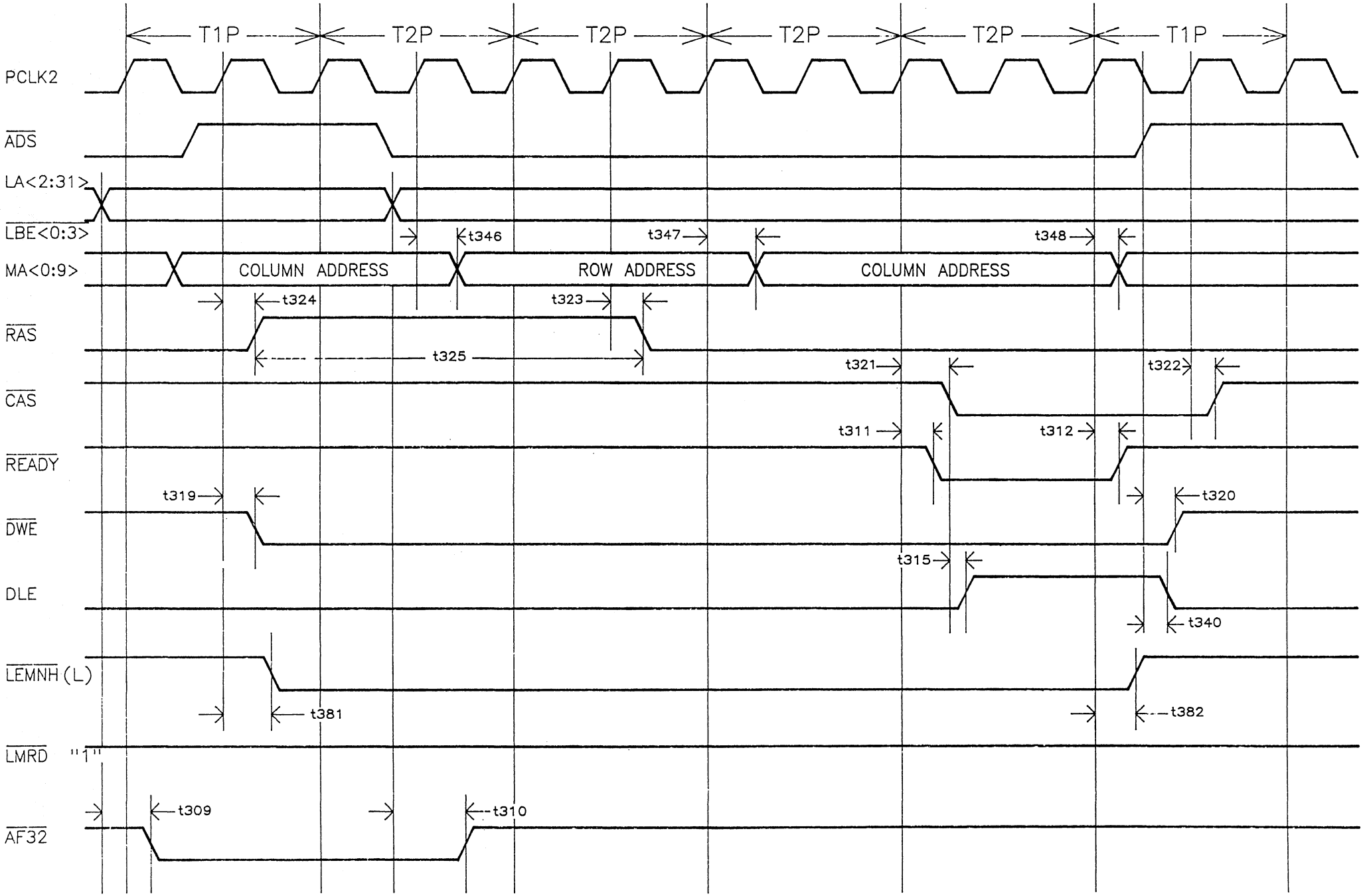


Figure 4.5 Memory on LD Bus, Page Mode, 1 Wait State, Page Miss, Write Cycle

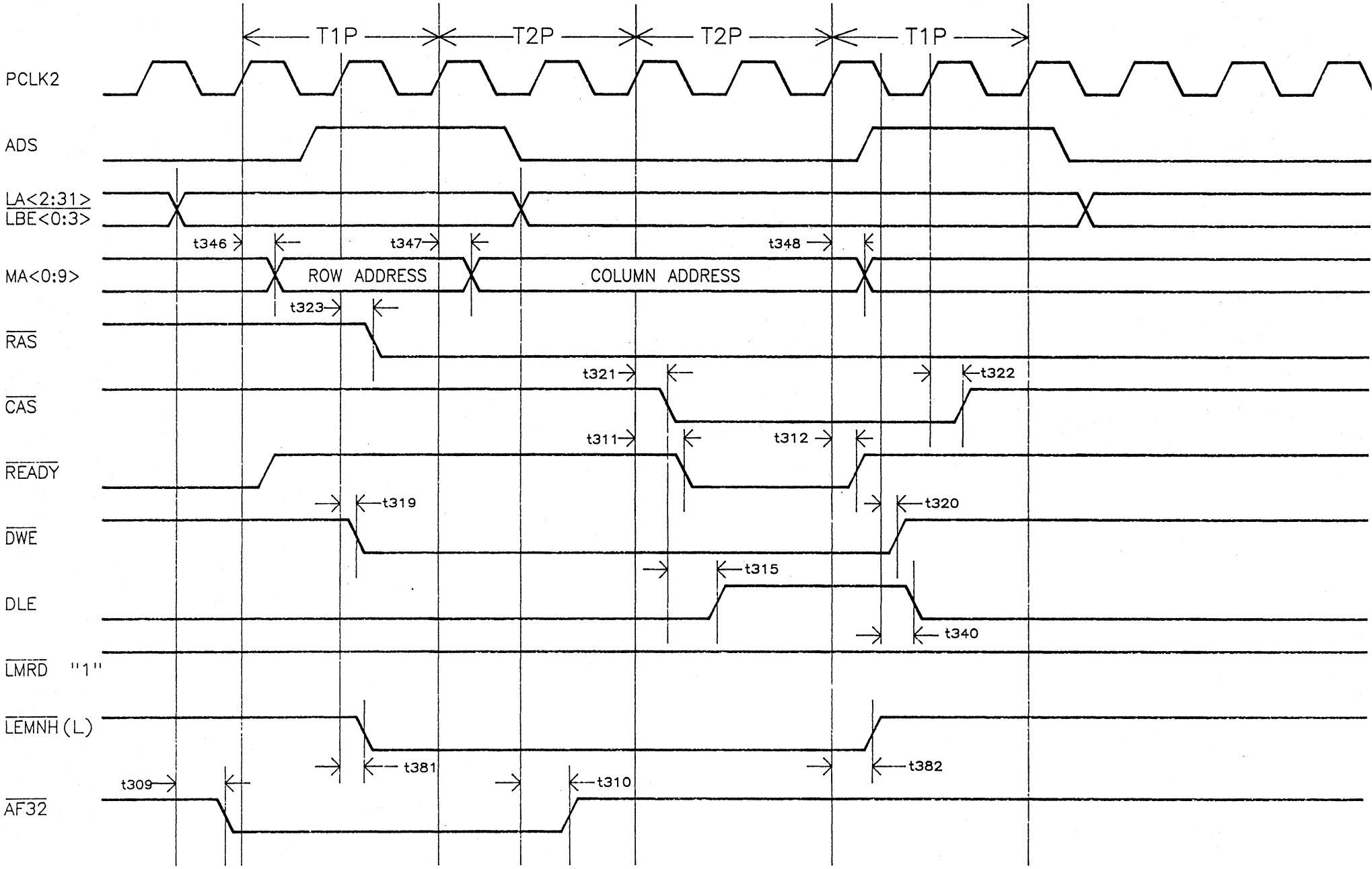
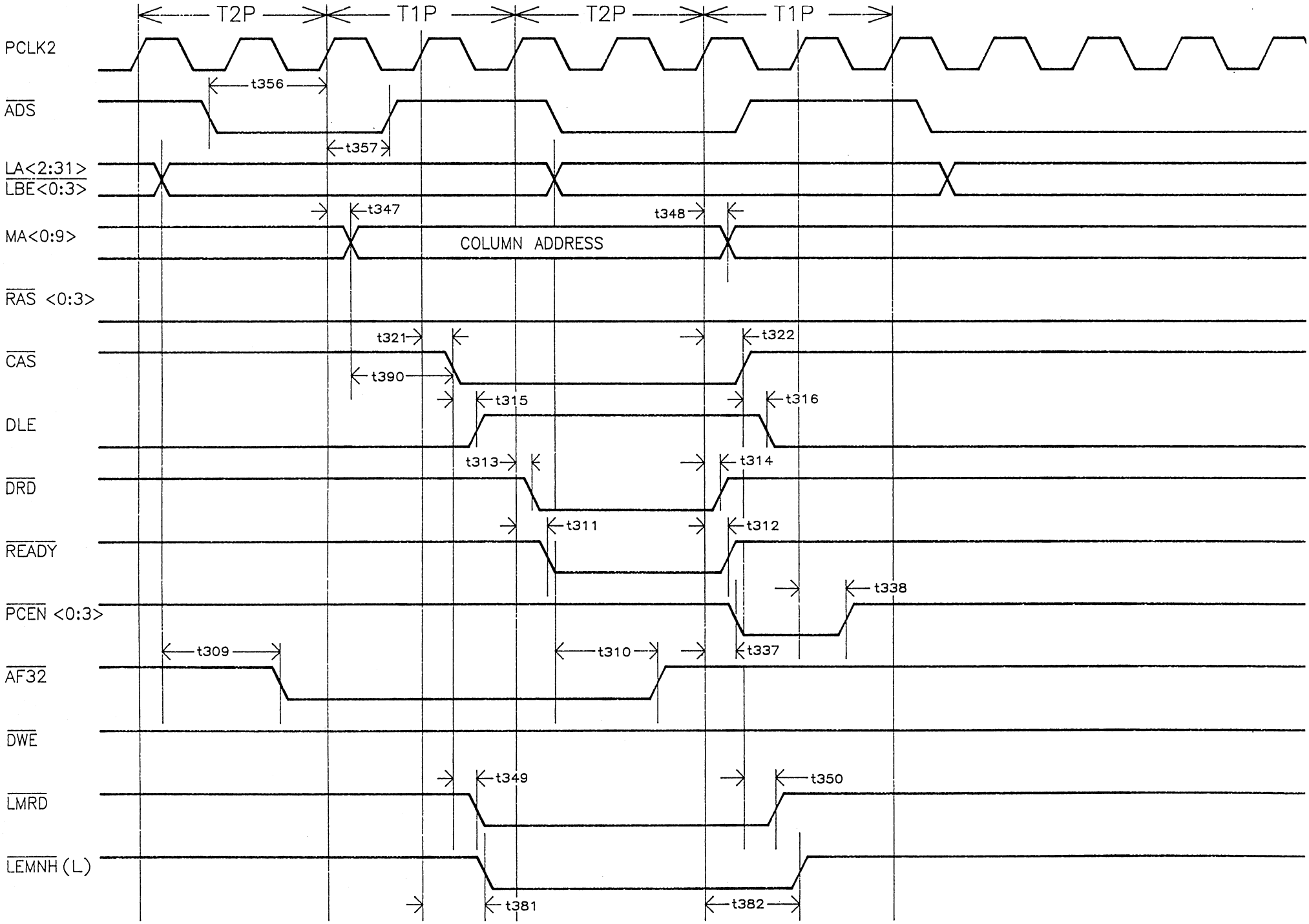


Figure 4.6 Memory on LD Bus, Page Mode, 1 Wait State, RAS High, Write Cycle



NOTE : During T2P 322 decodes address for next cycle, by end of T2P a hit or miss is decided. Assuming 256K DRAM with four way interleaving, during a hit address lines A2–A10 are used as Column address, A11 and A12 are used for Bank decoding.

Figure 4.7 Memory on LD Bus, Page Mode, 0 Wait State, Read Hit Cycle

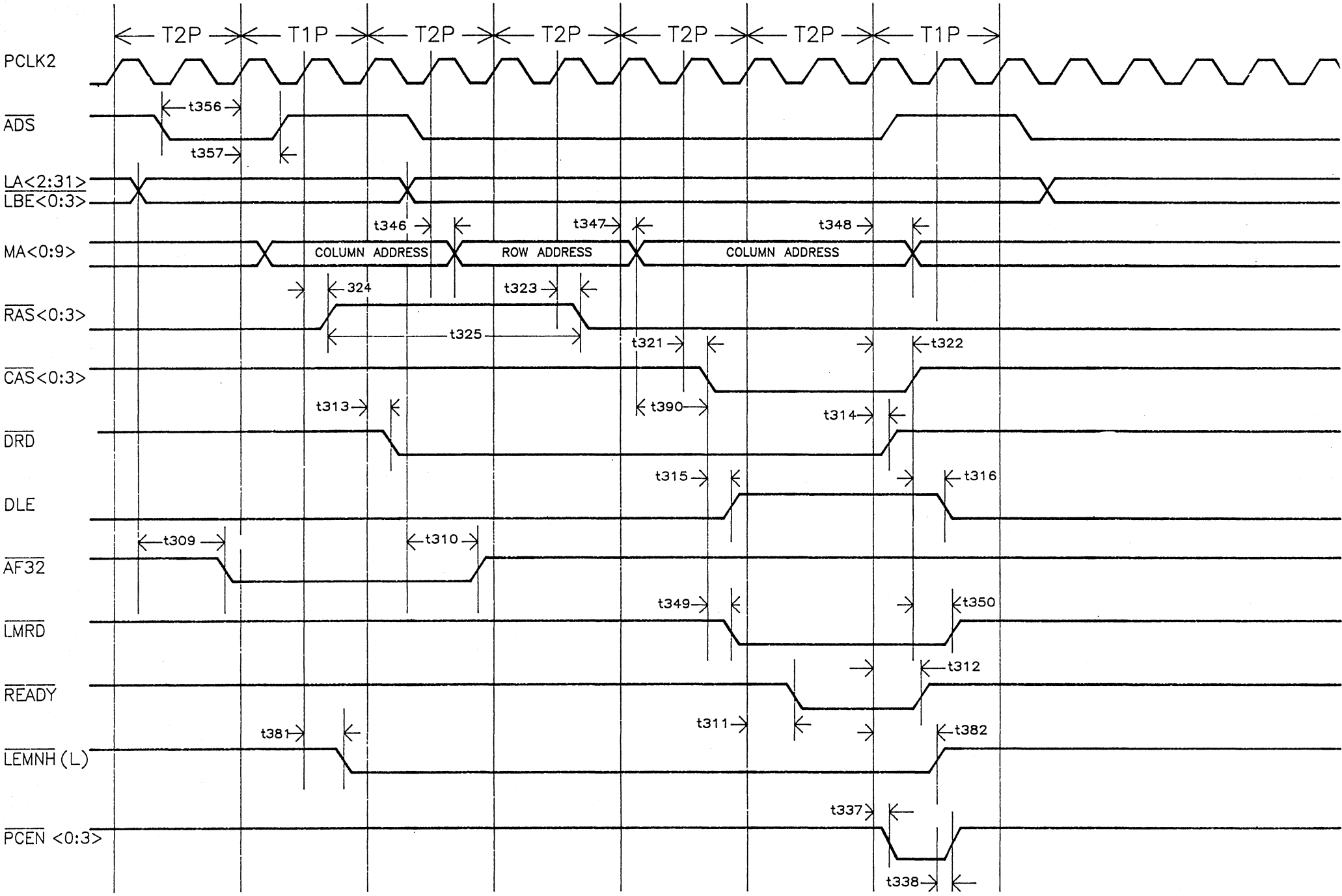


Figure 4.8 Memory on LD Bus, Page Mode, 0 Wait State, Page Miss, Read Cycle

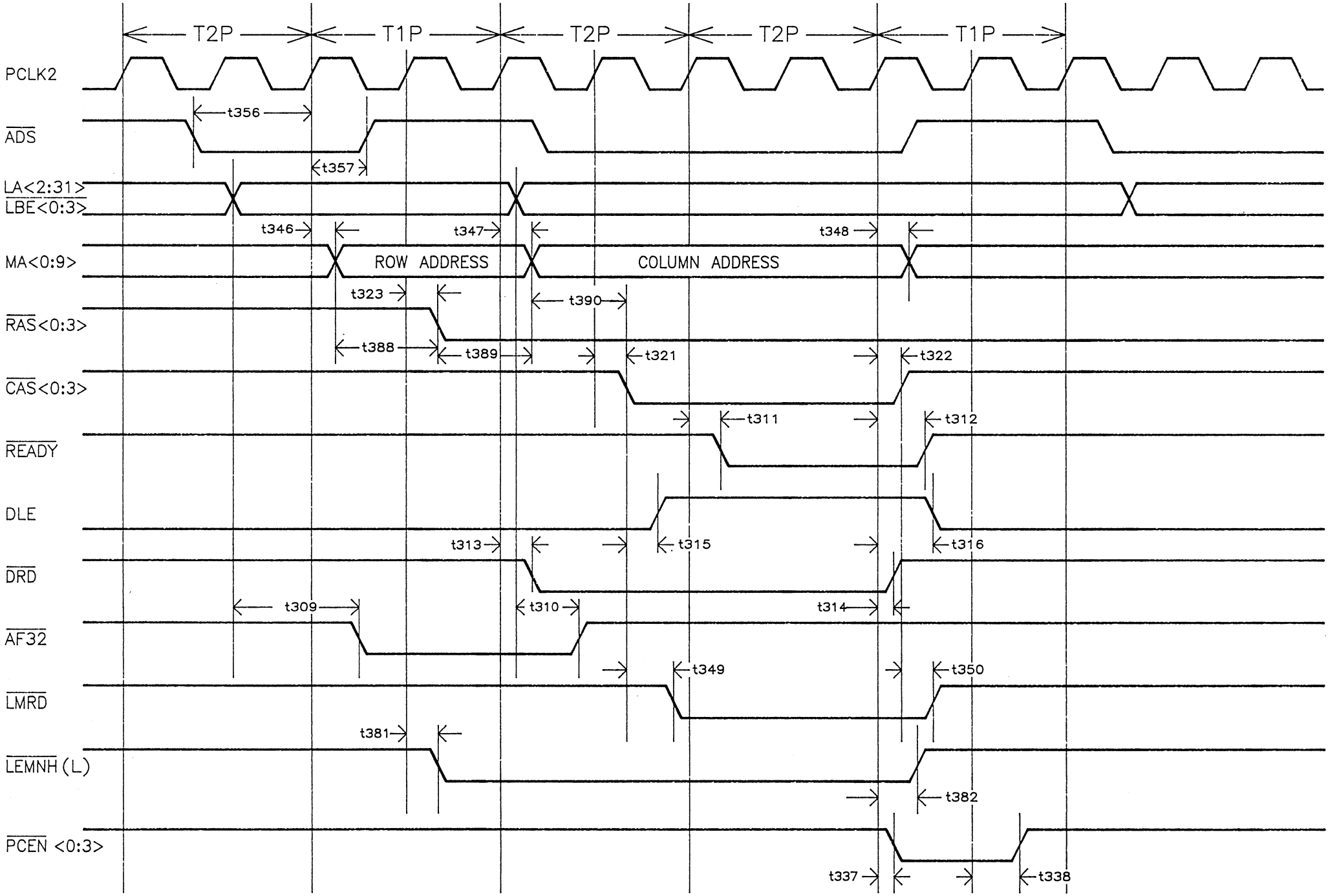


Figure 4.9 Memory on LD Bus, Page Mode, 0 Wait State, RAS High, Read Cycle

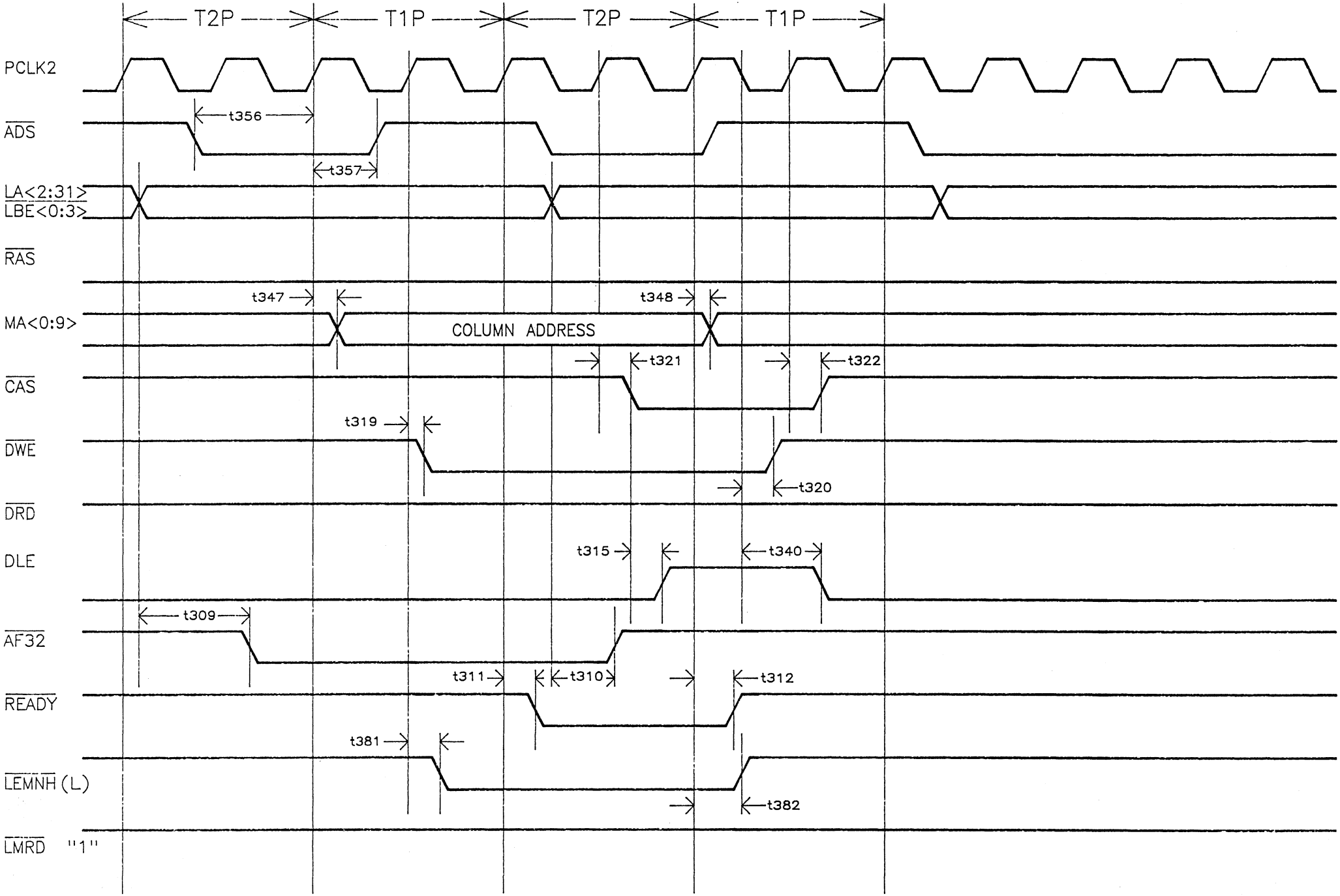


Figure 4.10 Memory on LD Bus, Page Mode, 0 Wait State, Write Hit Cycle

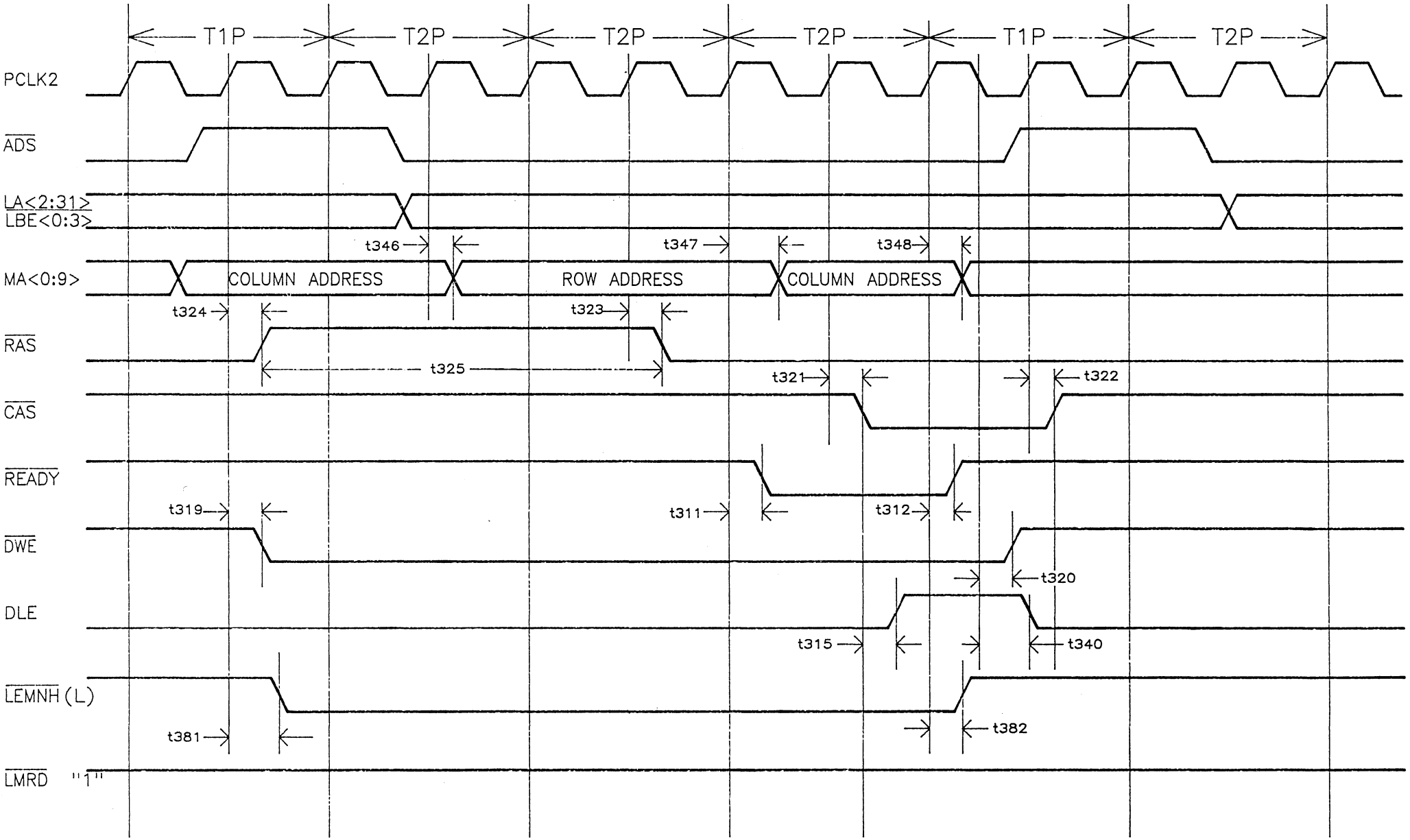


Figure 4.11 Memory on LD Bus, Page Mode, 0 Wait State, Page Miss, Write Cycle

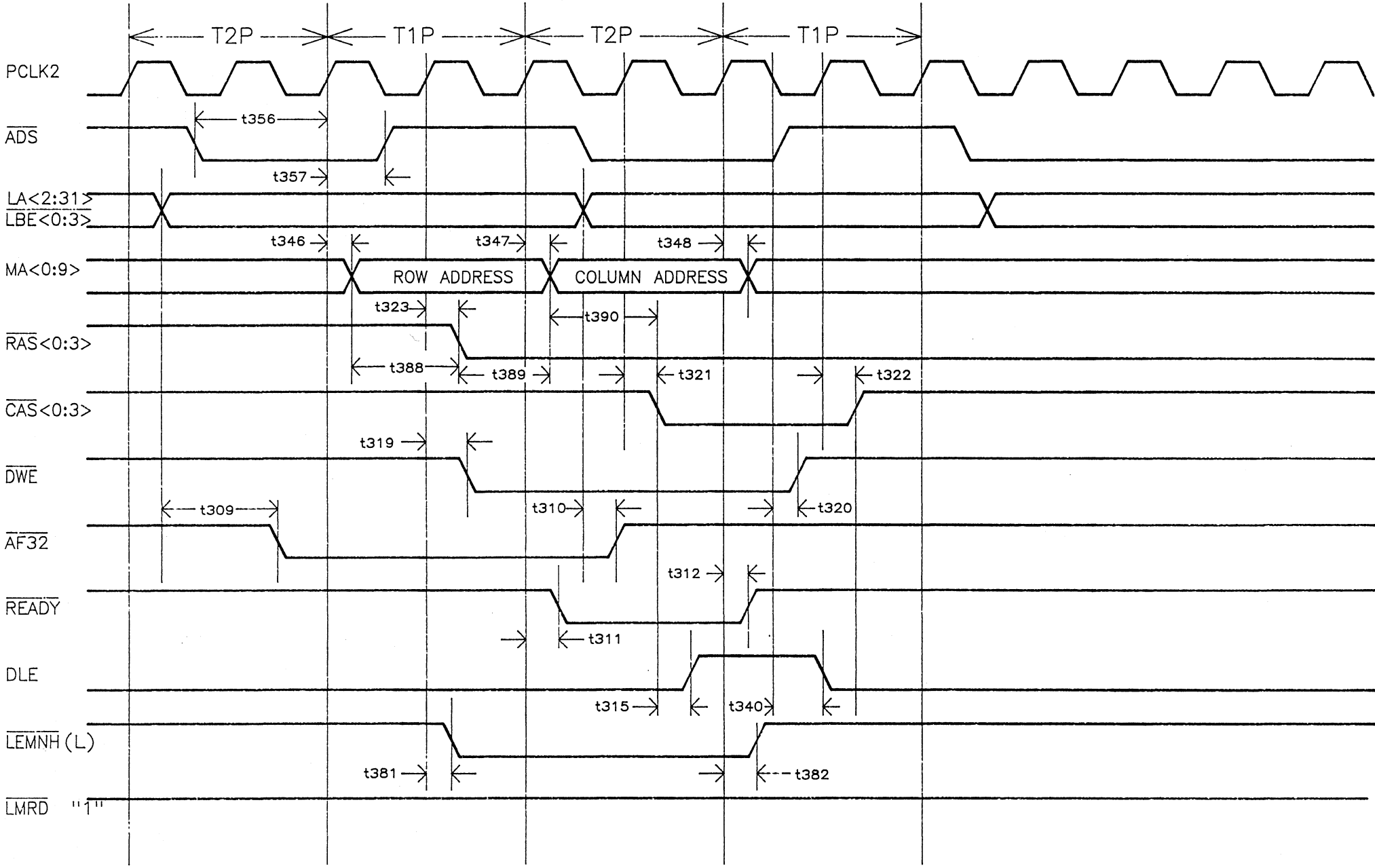


Figure 4.12 Memory on LD Bus, Page Mode, 0 Wait State, RAS High, Write Cycle

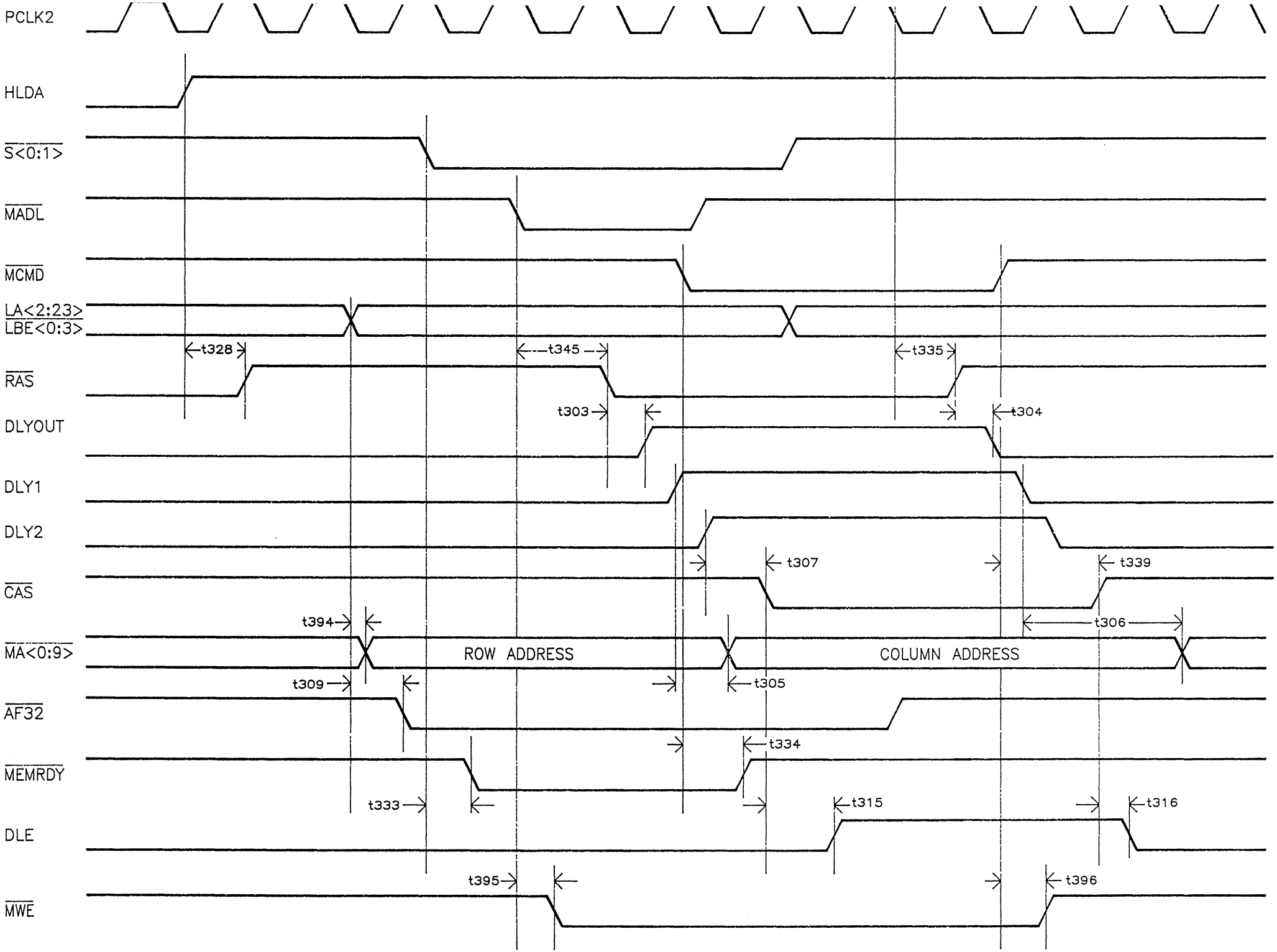


Figure 4.13 DMA/Master Cycle, External Delay line

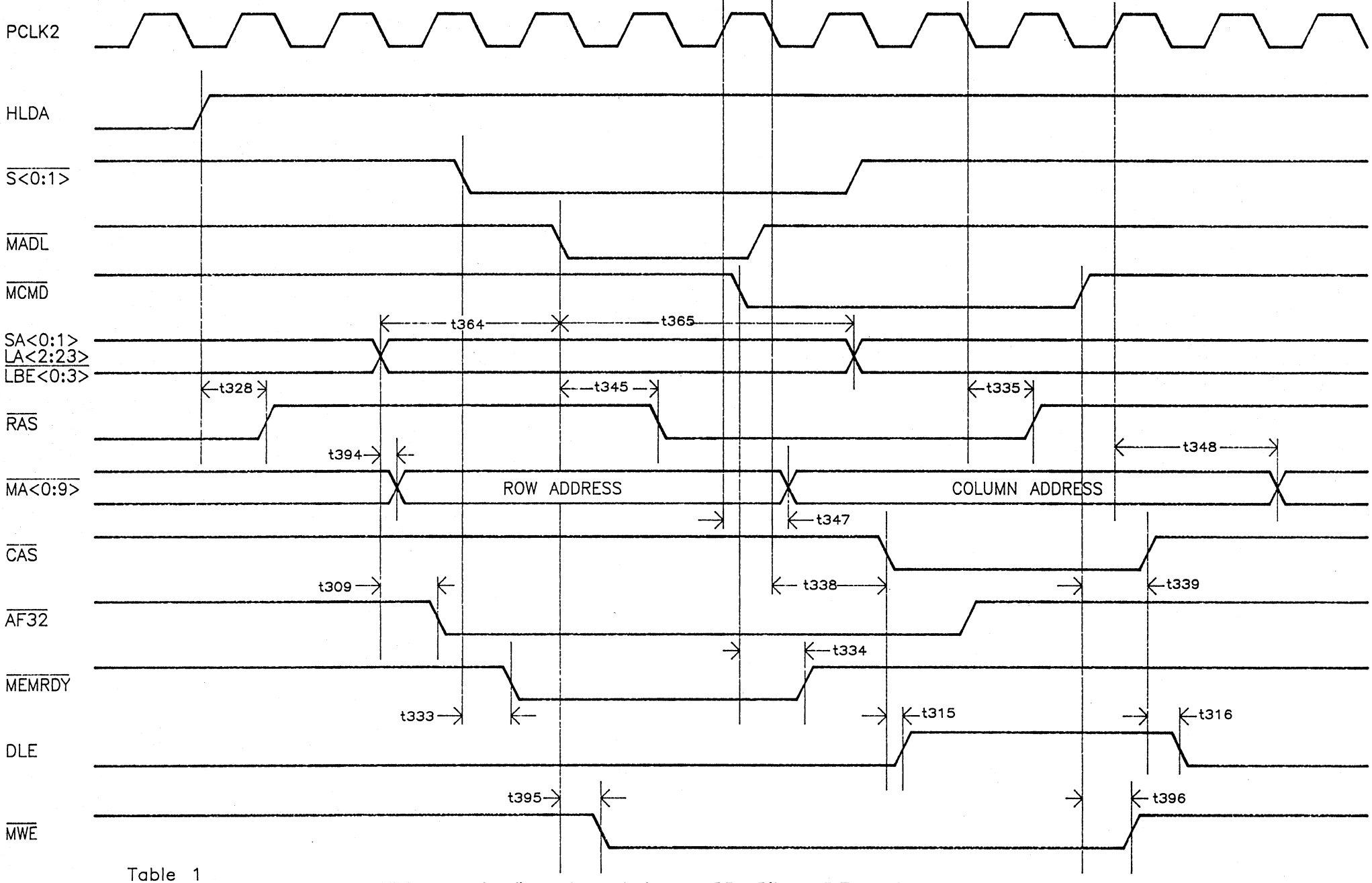


Table 1

Bit 4	Bit 5	CAS active to RAS inactive
0	0	2 CLK2
0	1	2.5 CLK2
1	0	3 CLK2
1	1	3.5 CLK2

NOTE :
1. Configured as Index = BB, Bits 4,5,7 = 0
2. Index Register BB bits 4 and 5 control timing for RAS inactive from CAS active. As shown in table 1.
3. Index Register BB bit 7 controls generation of CAS with respect to Column Address. If bit 7 = 0 CAS gets generated .5 CLK2 later then Column Address. If bit 7 = 1 CAS gets generated 1 CLK2 after Column Address.

Figure 4.14 DMA/Master Cycle, Internal Delay Line

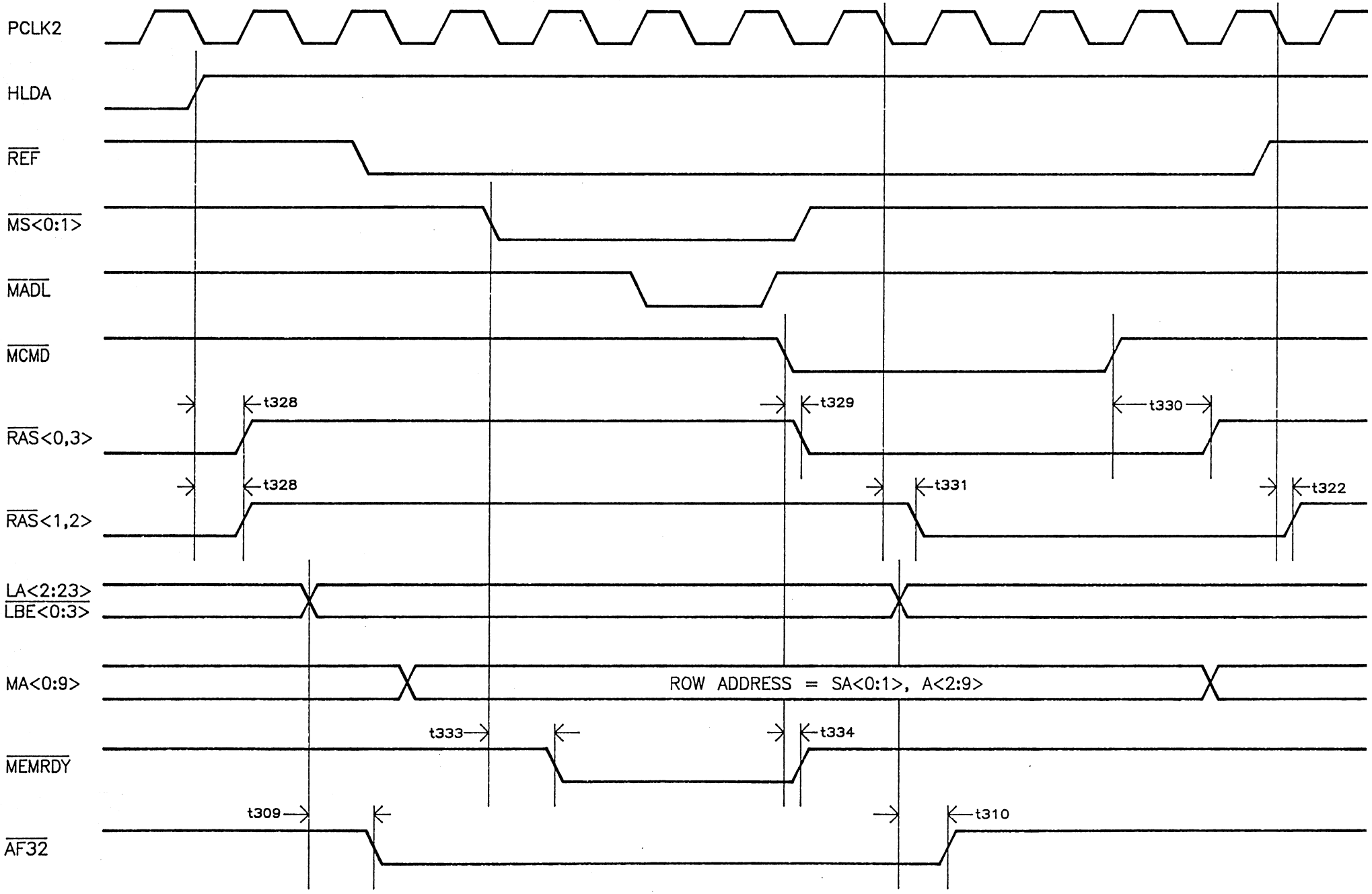


Figure 4.15 Refresh Cycle, Internal Delay Line, 1 Wait State

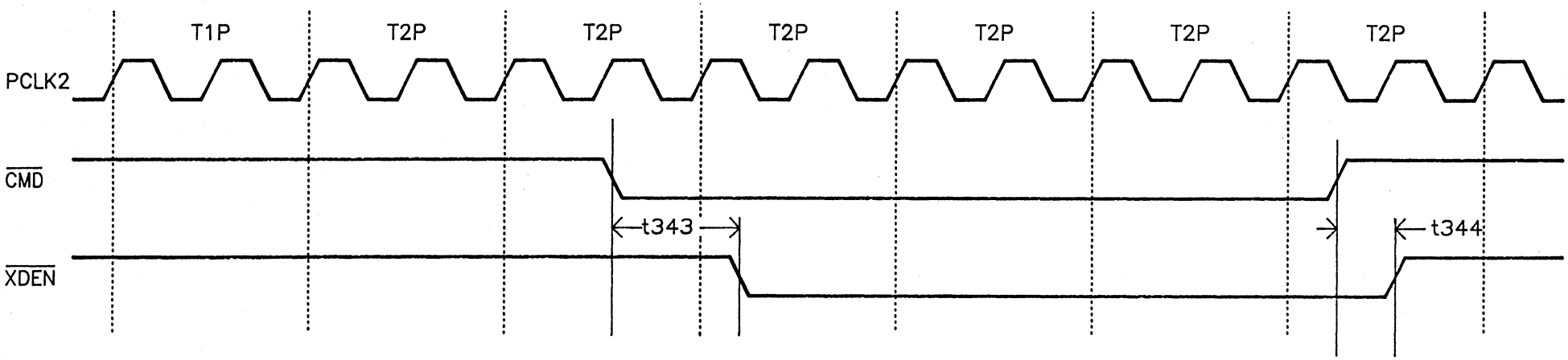


Figure 4.16 XDEN Timing

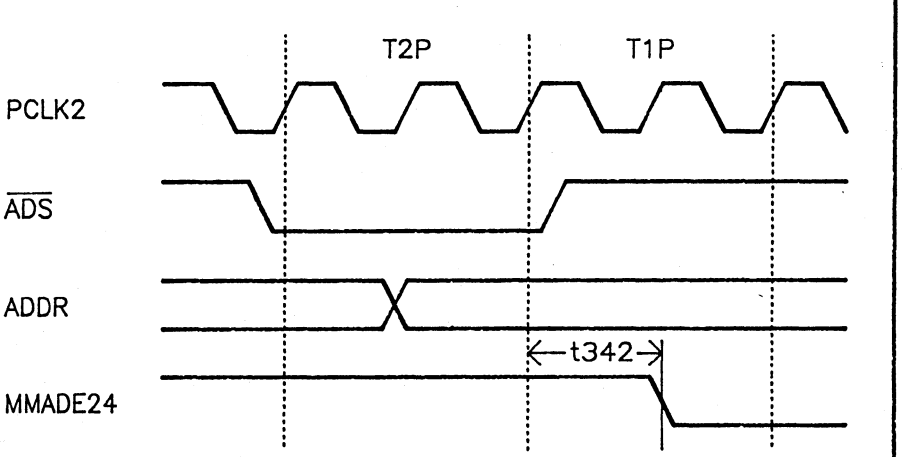


Figure 4.17 MMADE24 Timing

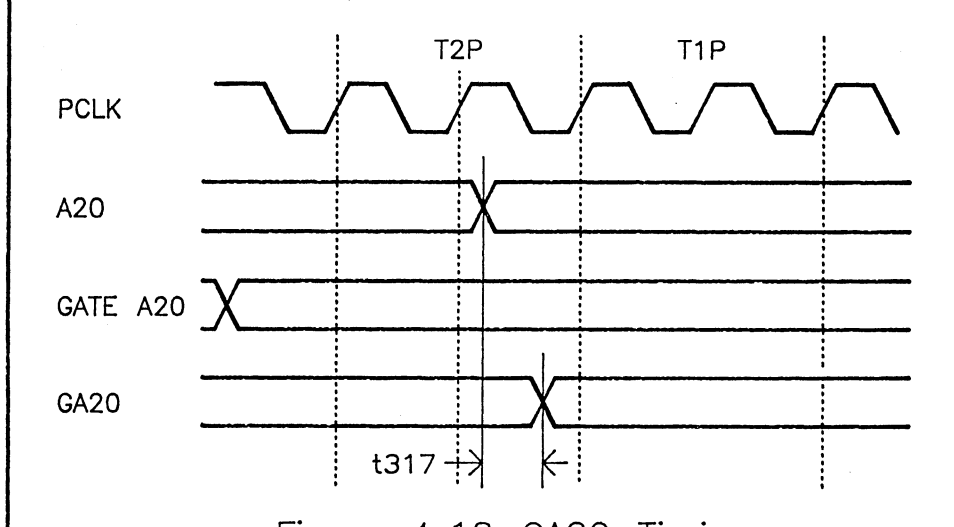
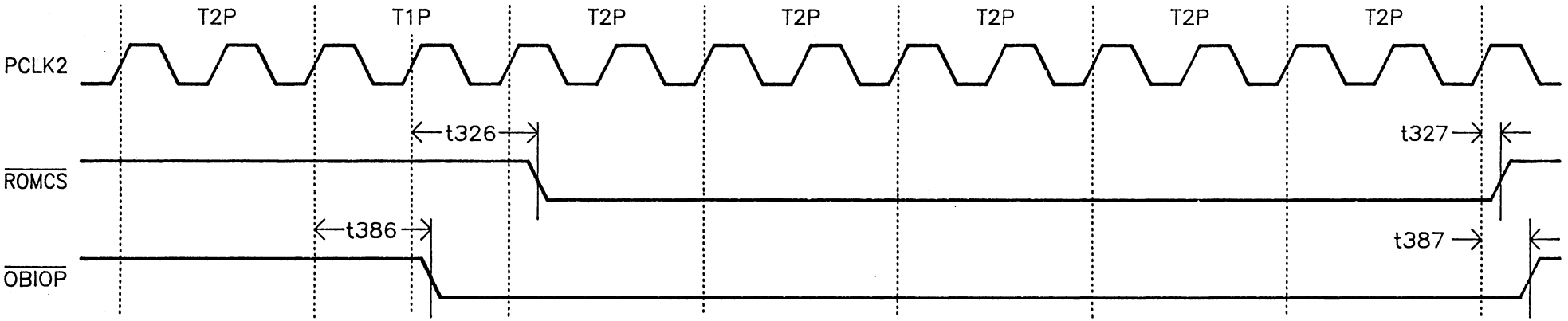


Figure 4.18 GA20 Timing



Note : Assumes a 25 MHz (AF32 option enabled) Microchannel Cycle.

Figure 4.19 ROMCS and OBIOP Generation

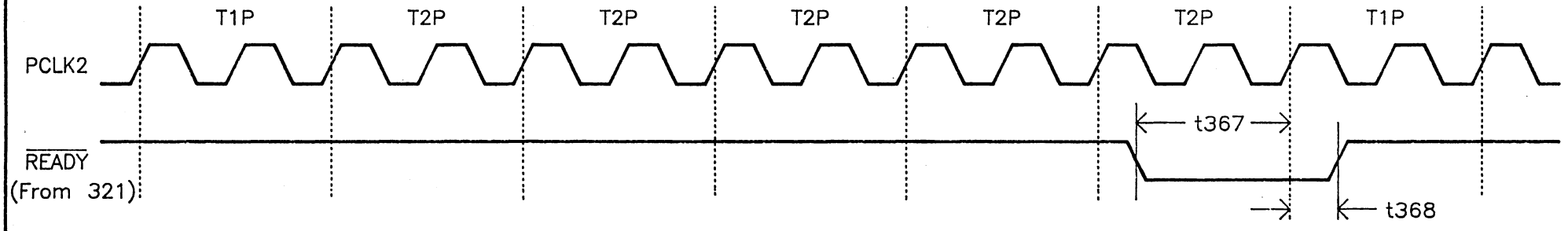


Figure 4.20 READY Sampling by 322

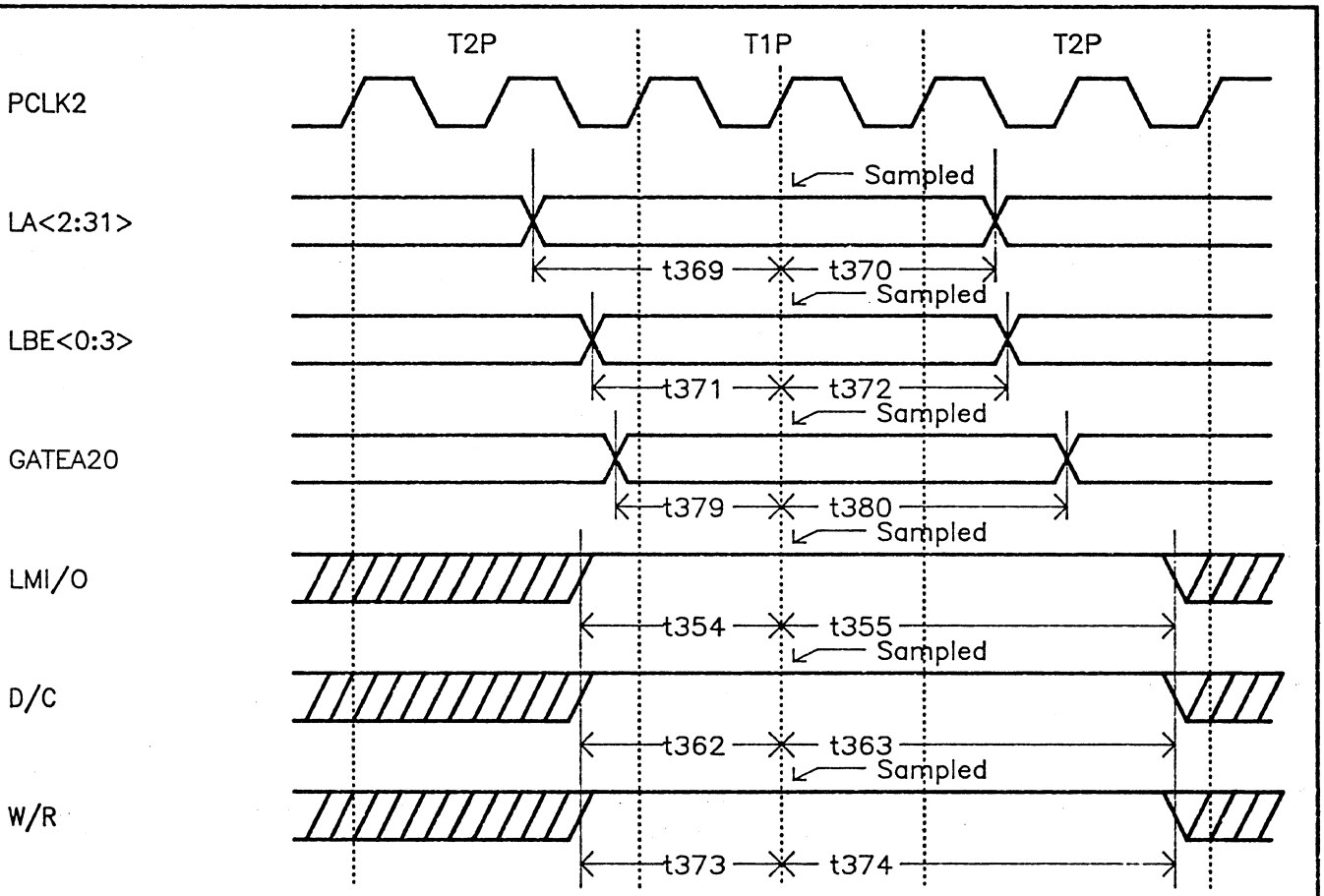


Figure 4.21 Input Waveforms

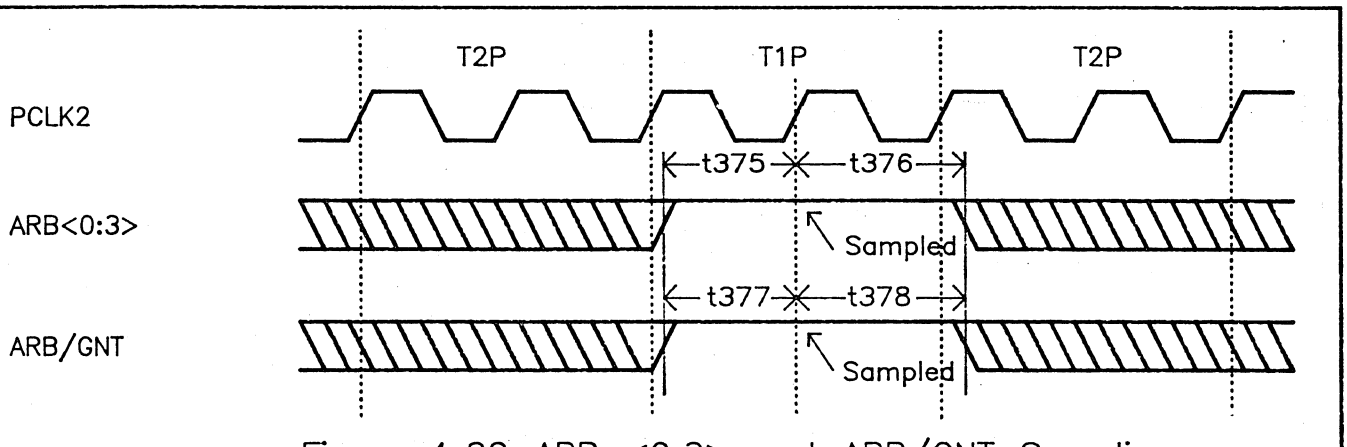


Figure 4.22 ARB <0:3> and ARB/GNT Sampling

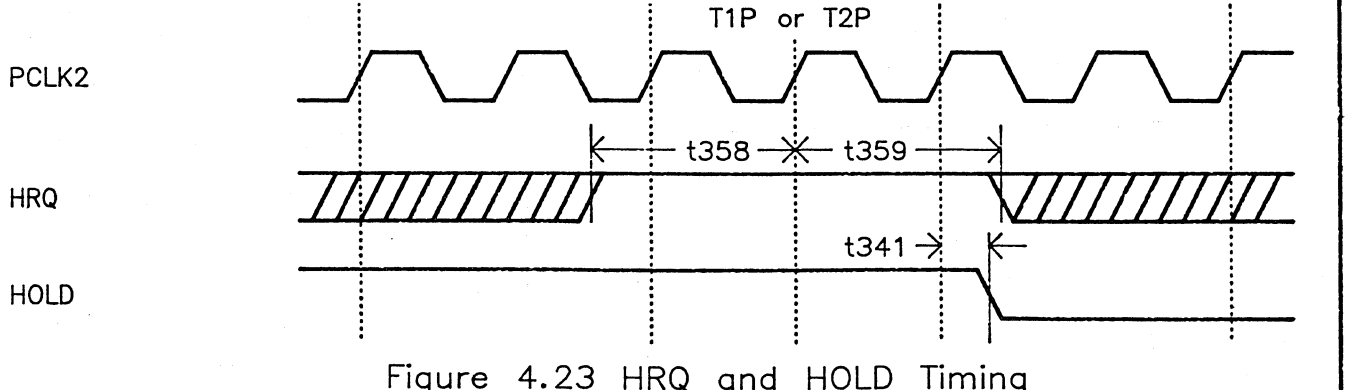


Figure 4.23 HRQ and HOLD Timing

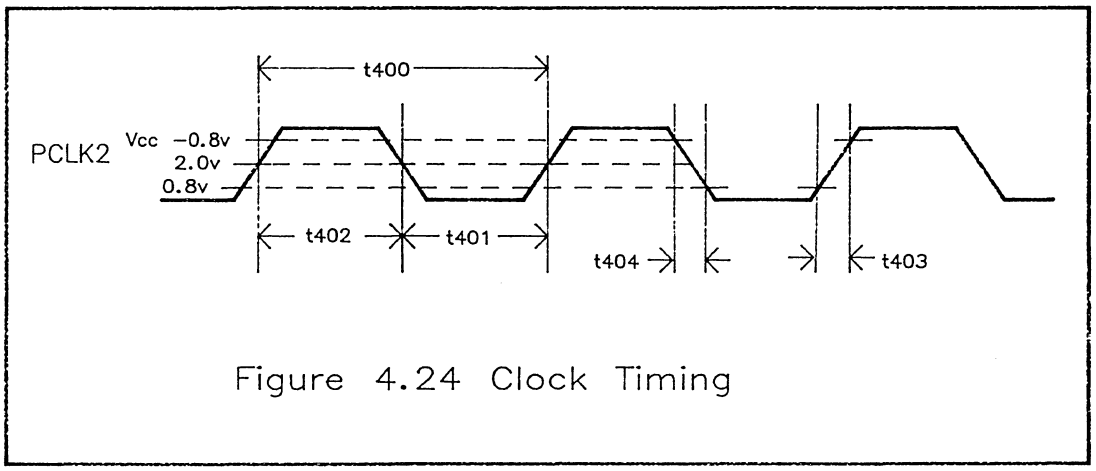
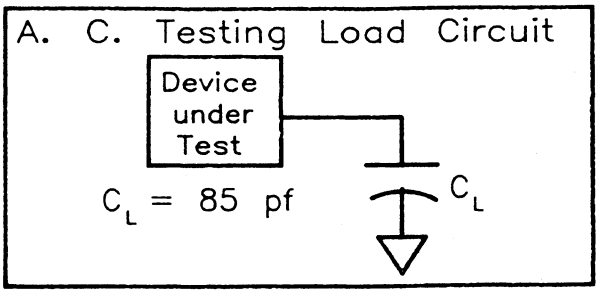


Figure 4.24 Clock Timing


A. C. Testing Load Circuit
Device under Test
C_L = 85 pf
C_L

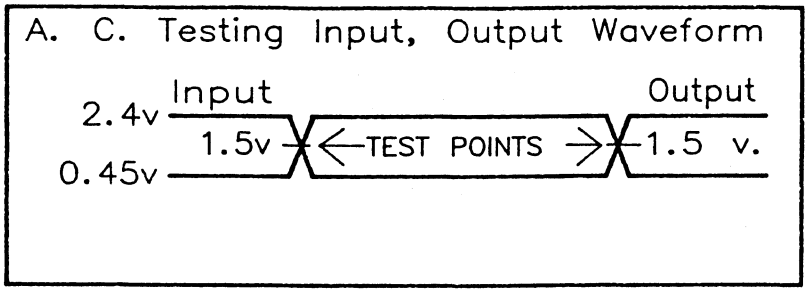
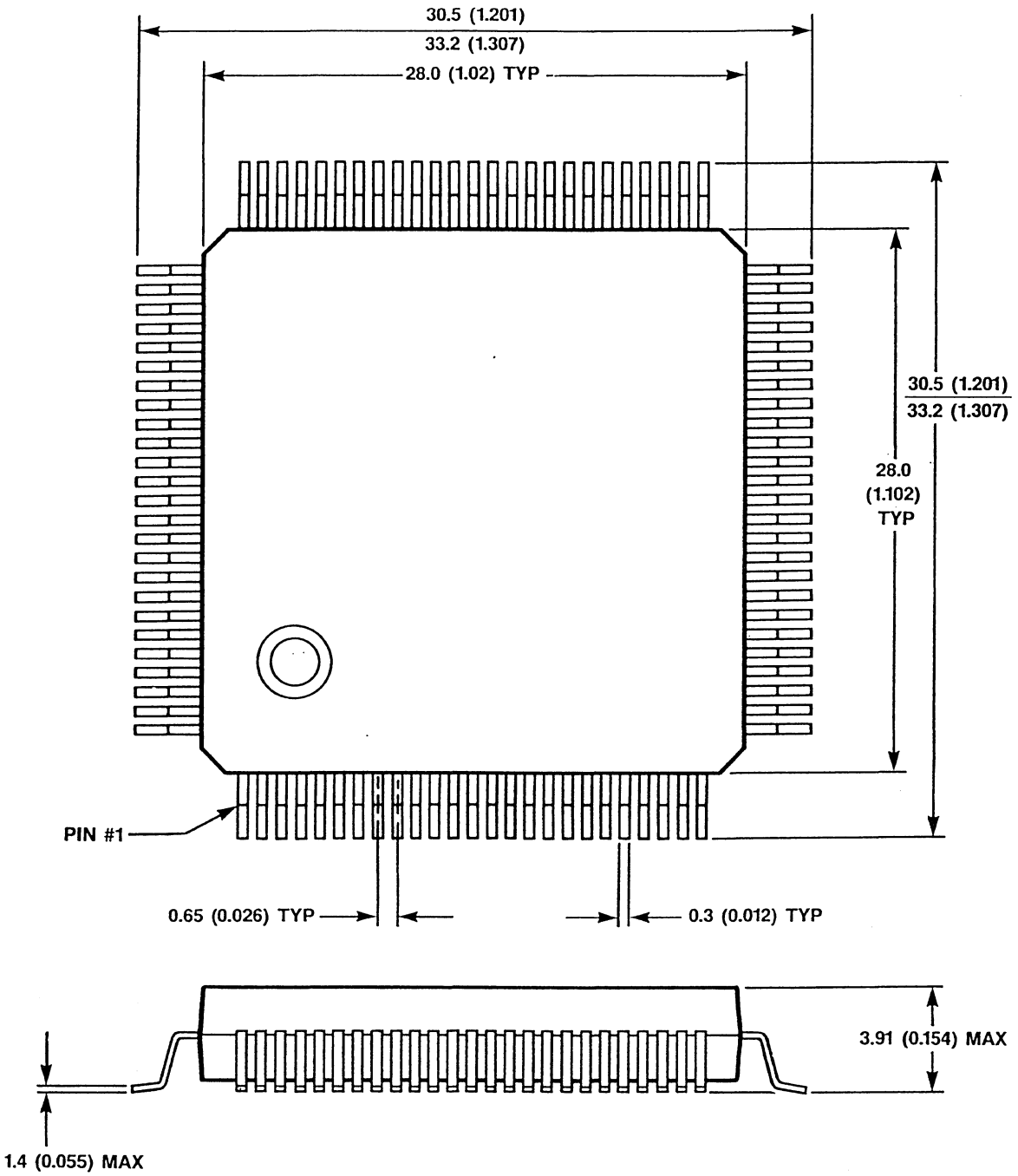

A. C. Testing Input, Output Waveform
Input
Output
2.4v
1.5v
0.45v
TEST POINTS
1.5 v.

Figure 4.25

DIMENSIONS: mm (in)



144 PIN PLASTIC FLAT PACKAGE (SQUARE)

FEATURES

- Bus Conversion logic for 32 bit to 16 or 8 bit data transfers
- Bus Steering for DMA and 16 bit Masters
- Parity generation and detection logic
- User programmable address decode registers and IBM PS/2™ compatible POS registers

FUNCTIONS

The 82C325 Data Buffer performs the following functions in the CHIPS/280 implementation of Model 70/80. Figure 5.1 shows the block diagram of the 82C325 Data buffer. It consists of five modules:

- Data buffers and latches
- Bus conversion logic
- Parity generation/detection logic
- Configuration registers and User programmable decode registers
- Miscellaneous system logic

Data Buffers and Latches

The 82C325 provides the buffering between the CPU data bus (LD0-LD31) and the memory data bus (MD0-MD31). The LD0-LD31 lines sink 4 mA output low currents (I_{OL}). The MD0-MD31 lines sink 8 mA I_{OL}.

Bus Control Logic

The Bus Control unit controls the bus transaction between LD and MD buses. There are two basic types of cycles:

1. CPU/DMA cycles
2. External Master initiated cycles

1.0 CPU/DMA CYCLES

For CPU/DMA (local bus cycles) initiated cycles, bus direction is controlled by AC <1:0>, -DRD, DLE and -VGACMD signals. When CPU or DMA controller is in control of the bus, the data transfer direction, by default, is from the LD to the MD bus. During read cycles, -DRD is active enabling data transfer from the MD to the LD bus for all read operations. When DMA or CPU reads memory on the LD bus or when CPU reads DMA or NP registers, the data path is not from the MD-LD bus. DLE and -VGACMD are used to latch the read data. DLE is used to latch the data for the local memory read cycle and -VGACMD is used for latching data during non-local memory cycles.

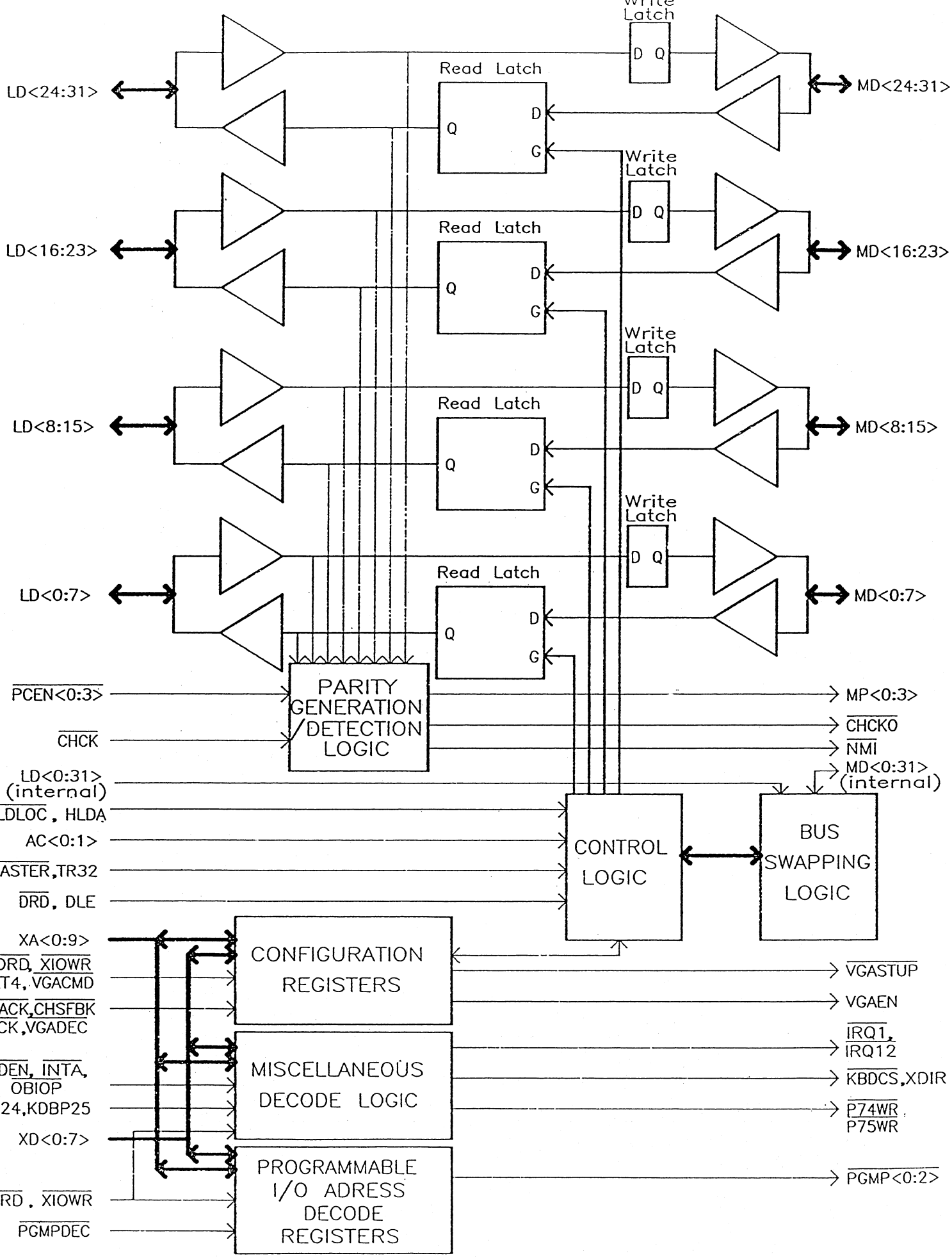


Figure 5.1 82C325 DATA BUFFER Block Diagram

The latch enable signal from the Memory Data bus to the CPU Data bus is controlled by -DRD, HLDA, MTR32, MASTER and the action codes AC <0:1>. Latching occurs on the trailing edge of DLE for DRAM read cycles from the CPU. When the CPU is writing to slaves on the D bus, additional data hold time is provided by internally latching the write data, using -WDLTH. The write data is latched using the leading edge of -WDLTH, to provide between 40 to 61ns of data hold time after -CMD goes inactive. Figure 5.2 is a block diagram showing the data paths for the CHIPS/280 system, with 8, 16 and 32-bit slaves and 16, 32-bit masters.

1.1 External Master Initiated Cycles

When MASTER is in control of the system bus the default data transfer direction is from the MD to the LD bus. The 82C322 activates DRD according to the -LS0, -LS1 and LM/-IO inputs. It is the responsibility of the Master to perform the necessary bus conversion.

1.2 Bus Conversion Logic

The 82C325 provides data bus conversion when the 32 bit CPU reads from or writes to 8 or 16 bit devices. It also provides bus conversion when the 16 bit DMA controller reads from or writes to 8 bit devices. It provides bus steering for the DMA controller and 16-bit Masters, while accessing the upper word of 32-bit slaves. The various paths under CPU, DMA, 16-bit Master and 32-bit Master control are listed in Table 5.1 in conjunction with Figure 5.3. These conversions are controlled by the action codes generated by the 82C321 and other signals such as: HLDA, MASTER, MTR32, -LDLOC.

Table 5.1

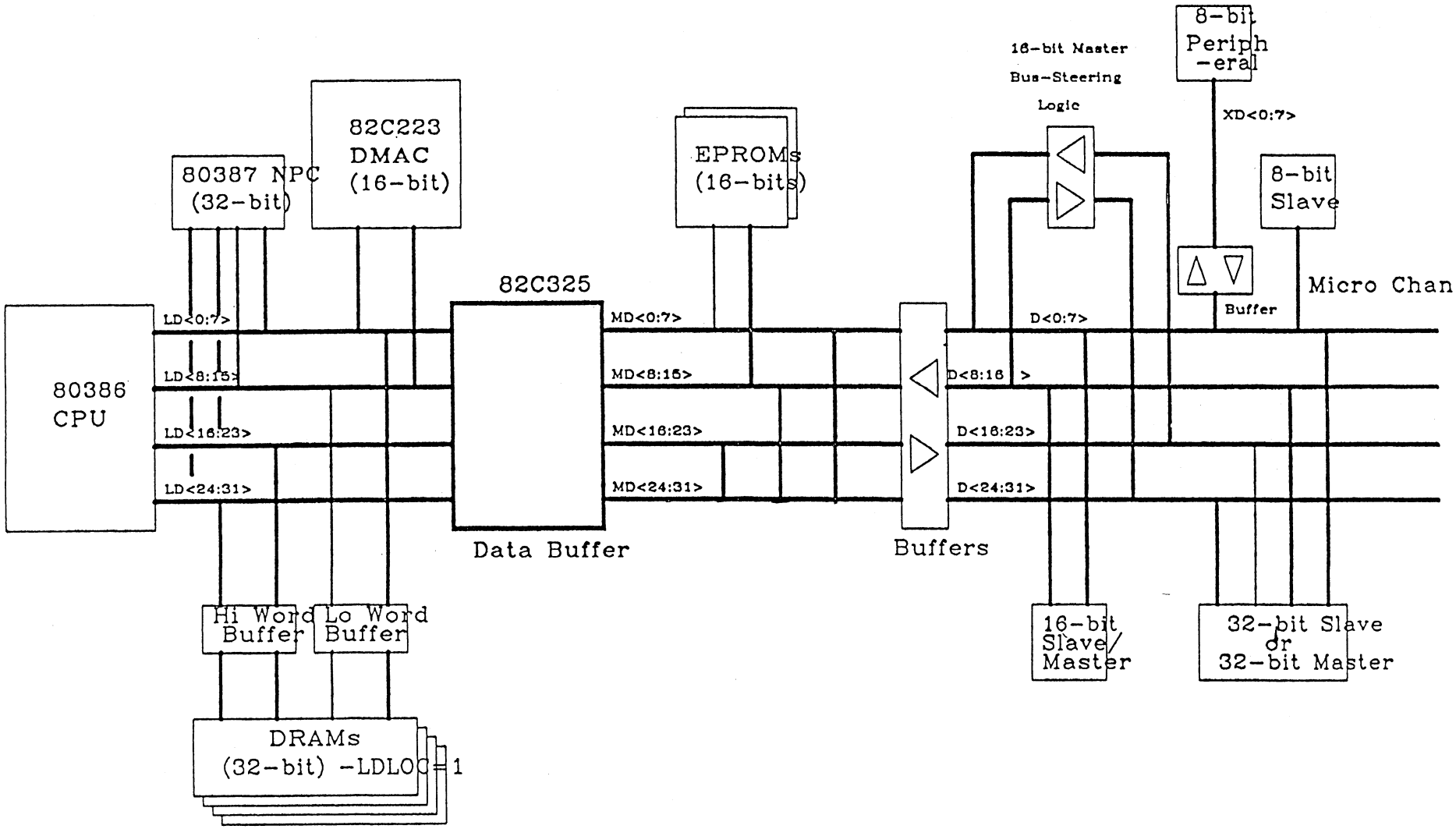
AC1	AC0	Cycle	Operation	Data Path
0	0	CPU	32 bit write	A-B,C-D,E-F,G-H
0	0	CPU	32 bit read	B-A,D-C,F-E,H-G
0	0	CPU	16 bit LO word write	E-F,G-H
0	0	CPU	16 bit LO word read	F-E,H-G
0	0	CPU	8 bit byte 0 write	G-H
0	0	CPU	8 bit byte 0 read	H-G
1	0	CPU	16 bit HI word write	A-J-F,C-K-H
1	0	CPU	16 bit HI word read	F-J-A,H-K-C
0	1	CPU	8 bit byte 1 write	E-L-H
0	1	CPU	8 bit byte 1 read	H-L-E
1	0	CPU	8 bit byte 2 write	C-K-H

Table 5.1 (continued)

AC1	AC0	Cycle	Operation	Data Path
1	0	CPU	8 bit byte 2 read	H-K-C
1	1	CPU	8 bit byte 3 write	A-J-L-H
1	1	CPU	8 bit byte 3 read	H-L-J-A
X	X	CPU	16 bit HI word read from DMA registers	E-J-A,G-K-C
0	0	DMA	16 bit word write	E-F,G-H
0	0	DMA	16 bit word read	F-E,H-G
0	0	DMA	8 bit LO byte write	G-H
0	0	DMA	8 bit LO byte read	H-G
1	0	DMA	32 bit HI word write on the MD bus	E-J-B,G-K-D
1	0	DMA	32 bit HI word read on the MD bus	B-J-E,D-K-G
1	0	DMA	32 bit HI word write on the LD bus	E-J-A,G-K-C
1	0	DMA	32 bit HI word read on the LD bus	A-J-E,C-K-G
0	1	DMA	8 bit HI byte write	E-L-H
0	1	DMA	8 bit HI byte read	H-L-E
0	0	16-bit MSTR	32 bit LO word write 16 bit write on LD bus	F-E, H-G
0	0	16-bit MSTR	32 bit LO word read 16 bit read on LD bus	E-F, G-H
0	1	16-bit MSTR	32 bit HI word write on the LD bus	F-J-A,H-K-C
0	1	16-bit MSTR	32 bit HI word read on the LD bus	A-J-F,C-K-H
0	1	16-bit MSTR	DRAM HI word write on the MD bus	F-J-B,H-K-D

Table 5.1 (continued)

AC1	AC0	Cycle	Operation	Data Path
0	1	16-bit MSTR	DRAM HI word read on the MD bus	B-J-F,D-K-H
1	1	16-bit MSTR	8 bit write to DMA or 82C325 registers	F-E,H-G
1	1	16-bit MSTR	8 bit read from DMA or 82C325 registers	E-F,G-H
1	0	16-bit MSTR	32 bit HI word write to slave on MD bus	F-J-B,H-K-D
1	0	16-bit MSTR	32 bit HI word read to slave on MD bus	B-J-F,D-K-H
0	0	32-bit MSTR	DRAM on LD bus, write	B-A,D-C,F-E,H-G
0	0	32-bit MSTR	DRAM on LD bus, read	A-B,C-D,E-F,G-H
1	1	32-bit MSTR	DMA or 82C325 reg. write	F-E,H-G
1	1	32-bit MSTR	DMA or 82C325 reg. read	E-F,G-H



CHIPS

82C325 Data Paths

FIGURE 5.2

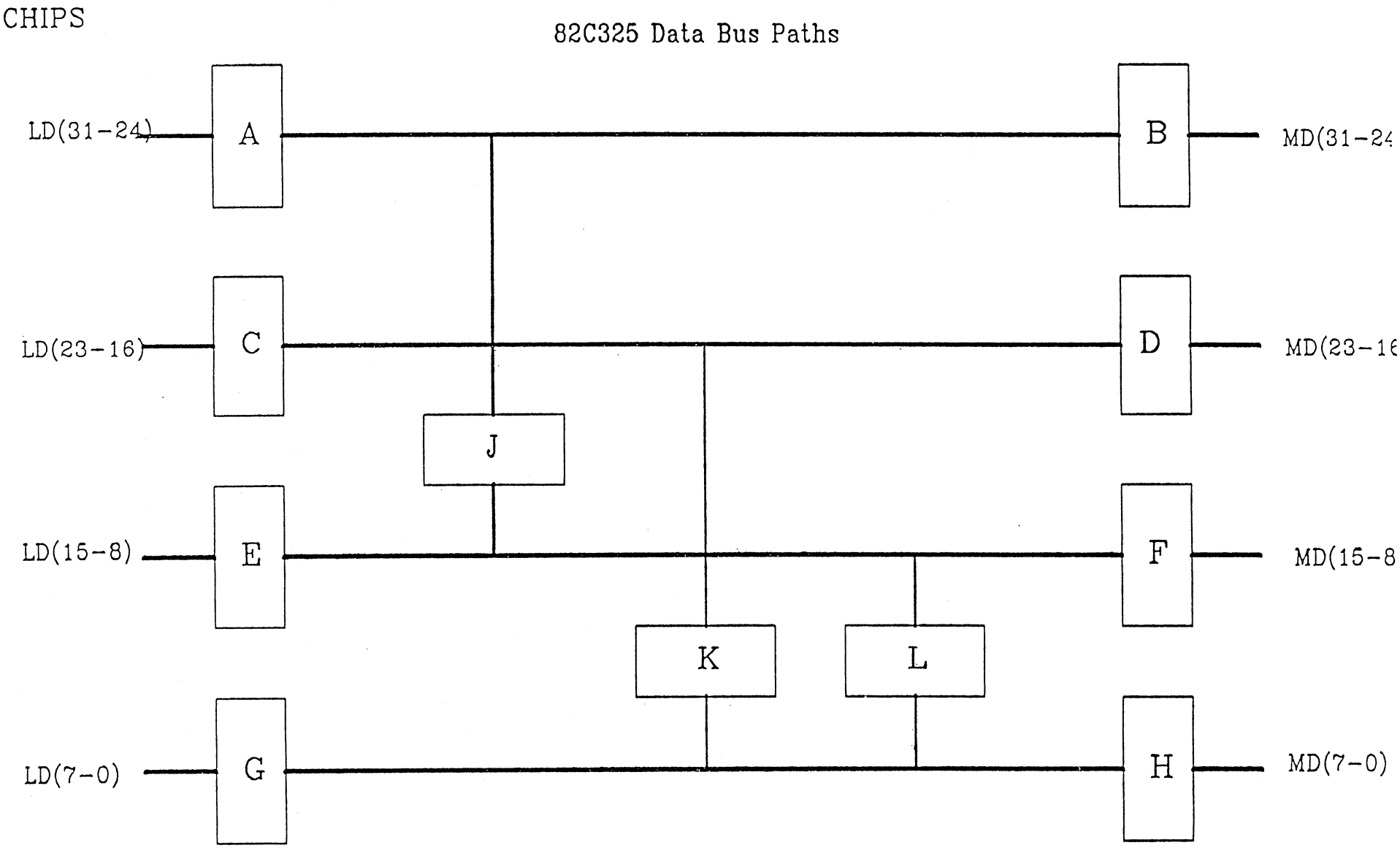

CHIPS
82C325 Data Bus Paths
LD(31-24)
A
B
MD(31-24
LD(23-16)
C
D
MD(23-16
J
LD(15-8)
E
F
MD(15-8
K
L
LD(7-0)
G
H
MD(7-0)

FIGURE 5.3

1.3 Parity Generation/Detection Logic

For local RAM write cycles, the 82C325 generates odd parity (including parity bit) for each of the four bytes of a double word. These valid odd parity bits are written to the bits MP0, MP1, MP2, and MP3 in the local DRAMs. Whenever there are an even number of ones in a byte, the corresponding MP bit will be one. During a local memory read cycle, the 82C325 checks for even parity (including parity bit) for each local DRAM byte read. If the parity is detected as being even, the 82C325 flags a parity error, if the parity error is enabled (Register E1, bit 0 = 1). In order to enable the parity check, the parity check enable bit (bit 2 in port 61) should be 0, and the -PCEN (0:3) lines should be active. The parity check is enabled for each byte whenever the corresponding -PCEN line is active. The -PCEN lines are generated by 82C322 (bit 0 in E1 should be 0) and are used by 82C325.

If the parity error is detected, the -CHCK 0 goes active, which generates -CHCK externally to the MCA and 82C322. The 82C322 uses the -CHCK signal to latch the address caused by the parity error in address recovery logic. If NMI is enabled (port 70, bit 7 = 0) the NMI is generated to the CPU. Whenever a parity error occurs, the parity error is cleared by toggling bit 0 (write 1, and then 0) in E1, and bits 2 and 3 (write 1, and then 0) in port 61. Parity bit outputs MP <0:3> are tristated during read operation.

2.0 ON-CHIP I/O PORTS and DECODE LOGIC

This unit includes the following functionalities:

- NMI Generation
- VGA Signals
- -IRQ1 and IRQ12
- Decoded Signals
- -KBDCS
- PGMP
- -XDIR
- -P74WR and -P75WR

2.1 NMI Generation

If either /CHCK or parity error signal is active and the I/O port 61 bit 3 or bit 2 is enabled, NMI will be generated if it is not masked (I/O Port 70 bit 7 should be set to 0). -CHCKO is activated during a parity error condition. To clear the parity error in the NMI routine, bit 0 of port E1 should be toggled, and then bits 2 and 3 of port 61 should also be toggled.

2.2 VGA Signals

The 82C325 generates -VGASETUP signal when VGA is in the setup mode. When external bus masters want to disable motherboard VGA, they can do so by setting bit 0 in IO Port 3C3 to 0 whereby, VGAEN is deactivated, disabling VGA.If 82C452 VGA is used the VGAEN pin of 82C325 should not be used as 82C452 responds to port 3C# to disable the mother board VGA.

-IRQ1 and IRQ12

The rising edges of the KBDP24 and KBDP25 activates the -IRQ1 and IRQ12 respectively. -IRQ1 connects directly to the 82C226. IRQ12 is buffered by an inverted open collector driver before driving the IRQ12 input on the 82C226. A read from I/O location 60H resets IRQ1 and IRQ12.

2.3 Decoded Signals

This unit also provides on-chip decoding for the following output signals:

-P74WR and -P75WR

The 2K CMOS static RAM uses an indexing scheme. The address of the memory location to be accessed is written to I/O ports P74WR and P75WR. Data is then accessed through IO port 76H. The 82C325 integrates the decode logic for the generation of -74WR and -75WR outputs while the decode logic for -76EN is provided in the 82C226 System Peripheral Controller.

-KBDCS

The 82C325 has on-chip decode logic which monitors the I/O addresses and activates -KBDCS during accesses to the keyboard controller.

-PGMP(0:2)

The 82C325 supports three Universal Decoder outputs. The addresses and the address range that these outputs respond to, can be programmed. These outputs can be used as general purpose decoder for I/O ports. The -PGMP <0:2> can be generated by programming I/O setup registers and I/O decoder register. For example, in order to generate -PGMP0 for a particular I/O address, registers R31 (I/O setup register 0) and R32 (I/O decode register 0) should be programmed. The address lines used for generation of -PGMP <0:2> are XA16 - XA0. If bit 2 of I/O setup register is 0 then the corresponding -PGMP output is generated for the programmed address only if XA10 - XA16 are zeroes. i.e for the I/O address range 0H-3FFH. If -PGMP <0:2> is to be generated for any address range of 0H - FFFFH, the address lines XA16 - X10 could be externally decoded to generate -PGMPDEC to the 82C325, in which case bit 2 of I/O setup register should be 1, in order to factor the -PGMPDEC signal during -PGMP <0:2> decoding. Thus address lines XA10 - XA16 determine the 1K block in 0 - 64K address range and XA0 - XA9 determine the actual address within 1K block. The option is also provided to mask the lower address bits XA0 - XA2, during -PGMP <0:2> decoding. For example, if -PGMP0 is programmed for I/O address 30H, and masking all the lower address bits (XA0 - XA2) will result in -PGMP0 being generated for I/O address 30H - 37H.

The -PGMP <0:2> can be generated for I/O read or I/O write only. Bits 3 and 4 of I/O setup registers are used for this purpose. If bit 3 = 1, then the corresponding -PGMP output is generated whenever there is I/O write operation for the selected I/O address.

-XDIR

The 82C325 generates XDIR to direct data transfers between the XD BUS and the D bus. -XDIR is not generated for programmable I/O ports -PGMP <0:2>.

3.0 82C325 PIN DESCRIPTIONS
CONTROL

Symbol	Type	PGA	PFP	Description
AC1 AC0	I I	71 117	76 77	ACTION CODES input from the 82C321 are used for bus sizing and word, byte assembly operations.
DLE	I	66	62	DATA LATCH ENABLE is an active high input from the 82C322 used to enable the local memory data buffer latch.
-DRD	I	12	63	DATA READ is an active low input from the 82C322 used to transfer data from the local memory data bus to the CPU data bus. If high, it sets the data path from the CPU data bus to the local memory data bus.
-WDLE	I	17	78	WRITE DATA LATCH ENABLE is an active low input from the 82C322 CPU Controller, used to provide the Micro Channel™ data hold time for channel write cycles from the CPU. It is inactive for DMA and MASTER cycles.
-XIORD	I	18	80	X BUS I/O READ is an active low input from the 82C321 for reading internal registers of the 82C325 and is also used for generation of programmable decodes and -XDIR.
-XIOWR	I	72	79	X BUS I/O WRITE is an active low input from the 82C321 for writing to the internal registers of the 82C325 and also used for generation of programmable decodes.

CONTROL (continued)

Symbol	Type	PGA	PFP	Description
-XDEN	I	13	64	X DATA BUS ENABLE is an active low input from the 82C322 Memory Controller and is used to generate the XDIR signal.
XDIR	O	82	110	X DATA BUS DIRECTION CONTROL is an output used to control the direction of the X Data Bus transreceiver. When low, it indicates a read cycle and when high, it indicates a write cycle. this line is normally high.
-INTA	I	11	61	INTERRUPT ACKNOWLEDGE is an active low input from the 82C321 CPU Controller, used to control XDIR to read the interrupt vectors.
MTR32	I	118	81	M BUS TRANSLATE 32 is an active high input, indicating that a 16-bit MASTER or DMA controller is in control of the system. It is use to provide necessary bus steering between the 16-bit MASTER and the upper word of 32-bit slaves.
HLDA	I	112	60	HOLD ACKNOWLEDGE is an active high input from the 80386 CPU, relinquishing the bus to the DMA Controller or MASTER.

CONTROL (continued)

Symbol	Type	PGA	PFP	Description
-LDLOC	I	115	70	LOCAL DRAM LOCATION is an active low input (strap), indicating the presence of DRAMs on the Memory Data Bus. When high, it indicates the presence of DRAMs on the Local Data Bus. It is used to provide the necessary data bus steering control from CPU, DMA Controller or MASTER to the system DRAMs.
RESET4	I	73	82	RESET 4 is the active high system reset from the 82C321. When active, it resets the internal registers of the 82C325 to their default state, all outputs go inactive and the data lines are three-stated.
-MASTER	I	69	71	MASTER is an active low input, asserted when an external master is in control of the Micro Channel. It is used for data buffer direction control.
-VGACMD	I	16	75	VGA COMMAND is an active low input indicating data transfer activity. It is used to latch data in the read latches in 82C325.

ADDRESS LINES

Symbol	Type	PGA	PFP	Description
XA0	I	19	83	X ADDRESS lines XA0 - XA9 are used to communicate with the internal registers of the 82C325.
XA1	I	74	84	
XA2	I	119	85	
XA3	I	20	86	
XA4	I	21	87	
XA5	I	75	88	
XA6	I	24	93	
XA7	I	76	94	
XA8	I	77	95	
XA9	I	122	96	

DATA LINES

Symbol	Type	PGA	PFP	Description
LD0	I/O	65	59	Data lines LD0 - LD31 from the CPU.
LD1	I/O	64	58	
LD2	I/O	10	57	
LD3	I/O	63	52	
LD4	I/O	7	51	
LD5	I/O	6	50	
LD6	I/O	109	49	
LD7	I/O	62	48	
LD8	I/O	5	47	
LD9	I/O	61	46	
LD10	I/O	108	45	
LD11	I/O	4	44	
LD12	I/O	60	43	
LD13	I/O	3	42	
LD14	I/O	107	41	
LD15	I/O	59	40	
LD16	I/O	2	39	
LD17	I/O	57	35	
LD18	I/O	105	34	
LD19	I/O	144	33	
LD20	I/O	56	32	
LD21	I/O	104	31	
LD22	I/O	143	30	
LD23	I/O	103	29	
LD24	I/O	55	28	
LD25	I/O	54	27	
LD26	I/O	102	26	
LD27	I/O	53	25	

DATA LINES (continued)

Symbol	Type	PGA	PFP	Description
LD28	I/O	142	24	
LD29	I/O	101	23	
LD30	I/O	100	22	
LD31	I/O	52	21	

MEMORY DATA LINES

Symbol	Type	PGA	PFP	Description
MD0	I/O	34	122	MEMORY DATA lines MD0 - MD31 from the memory bus.
MD1	I/O	35	123	
MD2	I/O	87	124	
MD3	I/O	38	129	
MD4	I/O	88	130	
MD5	I/O	89	131	
MD6	I/O	132	132	
MD7	I/O	39	133	
MD8	I/O	90	134	
MD9	I/O	40	135	
MD10	I/O	41	136	
MD11	I/O	91	137	
MD12	I/O	133	138	
MD13	I/O	92	139	
MD14	I/O	42	140	
MD15	I/O	134	141	
MD16	I/O	135	142	
MD17	I/O	94	2	
MD18	I/O	44	3	
MD19	I/O	95	4	
MD20	I/O	137	5	
MD21	I/O	45	6	
MD22	I/O	96	7	
MD23	I/O	46	8	
MD24	I/O	138	9	
MD25	I/O	97	10	
MD26	I/O	47	11	
MD27	I/O	98	12	
MD28	I/O	139	13	
MD29	I/O	48	14	
MD30	I/O	49	15	
MD31	I/O	99	16	

PARITY

Symbol	Type	PGA	PFP	Description
MP0 MP1 MP2 MP3	I/O I/O I/O I/O	85 33 86 129	118 119 120 121	MEMORY PARITY bits for the four bytes of the system DRAMs. These lines are input during memory read operations for parity error detection and are output during memory write operations for parity generation.
-CHCK	I	32	116	CHANNEL CHECK is an active low input from the MCA. When active it indicates a catastrophical error on the MCA and must be held low until the interrupt handler resets it. When active, it generates an NMI to the CPU (if enabled).
-CHCKO	O	31	114	CHANNEL CHECK OUTPUT is an active low, output to the -CHCK line on the MCA. It goes active upon detecting a parity error during a system memory read operation. It is used internally, to generate a non-maskable interrupt (if enabled) to the CPU.
-NMI	O	84	115	NON MASKABLE INTERRUPT is an active low, open collector output to the 80386 (if enabled), when either -CHCK is active or - CHCKO is active.
-PCEN0 -PCEN1 -PCEN2 -PCEN3	I I I I	67 113 68 14	65 66 67 68	PARITY CHECK ENABLES <0:3> are active low parity enable inputs from the 82C322. When enabled, these lines individually check the parity of the respective Memory Data bytes.

MISCELLANEOUS SIGNALS

Symbol	Type	PGA	PFP	Description
-OBIOP	I	114	69	ON BOARD I/O PORT is an active low input from the 82C322. In conjunction with XA<0:9>, it is used for complete on board I/O address decoding for the internal registers of the 82C325, the user programmable I/O ports, several peripheral chip select functions and for data bus control.
-DSKDACK	I	70	74	DISK DMA ACKNOWLEDGE is an active low input is used to set the I/O port 091H, bit 0 and for XDIR control.
CDSFBK	I	128	117	CARD SELECTED FEED-BACK is an active low signal. It is asserted when a slave on the system is accessed. Its state is latched in I/O port 091H.
KBDP24	I	79	101	KEYBOARD PORT 2-4 is an active high input from the 8042 keyboard controller providing keyboard interrupts and is used to generate - IRQ1.
KBDP25	I	123	102	KEYBOARD PORT 2-5 is an active high input from the 8042 keyboard controller providing mouse interrupts and is used to generate - IRQ12.
-VGAACK	I	30	111	VIDEO GRAPHICS ADAPTER ACKNOWLEDGE is an active low input from the VGA controller in response to a selected VGA I/O or memory. It is used to set I/O port 091H bit 0 to a one.

MISCELLANEOUS SIGNALS (continued)

Symbol	Type	PGA	PFP	Description
-VGASTUP	O	83	112	VIDEO GRAPHICS ADAPTER SET UP is an active low output during VGA set-up and is the output of I/O port 094H bit 5.
VGAEN	O	127	113	VIDEO GRAPHICS ADAPTER ENABLE is an active high output from I/O port 3C3H bit 0. When low, it disables the VGA subsystem.
-KBDCS	O	80	103	KEYBOARD CHIP SELECT is an active low output, used as the 8042 keyboard controller chip select.
-P74WR	O	28	104	PORT 74 WRITE is an active low output to the lower address (CA0-CA7) latch of the CMOS SRAM.
-P75WR	O	124	105	PORT 75 WRITE is an active low output to the upper address (CA8-CA11) latch of the CMOS SRAM
-IRQ1	O	125	106	INTERRUPT REQUEST 1 is an active low output to the 82C226 IPC in a PS/2™ environment. It is used to generate keyboard interrupts.
-IRQ12	O	81	107	INTERRUPT REQUEST 12 is an active low output to the 82C226 IPC in a PS/2™ environment. It is used to generate mouse interrupts and is an open collector line requiring a 10K pull-up resistor.

MISCELLANEOUS SIGNALS (continued)

-PGMPDEC		I	25	97	PROGRAMMABLE PORT DECODE is an active low input which can be used in programmable I/O address decoding, -PGMP <0:2>.
-PGMP0 -PGMP1 -PGMP2	O O O	78 26 27	98 99 100		PROGRAMMABLE PORT select <0:2> are active general purpose outputs for I/O decoding. The decode address can be programmed in I/O setup, and I/O decode registers.

POWER SUPPLIES

Symbol	PGA	PFP	Description
V_{SS}	1 141 131 126 29 121 111 93 106 - - - -	19 20 36 37 55 56 91 92 108 109 127 128 143	Power Supply
V_{DD}	140 136 43 130 120 116 15 110 58	1 18 38 54 72 73 90 126 144	Ground

Power Supply

NC	50 51 8 9 22 23 36 37	17 53 89 125 - - - -	Not Connected
Not Connected			

4.0 82C325 REGISTER DESCRIPTIONS

Miscellaneous Register R30

Index Register Port: 22H
Data Register Port: 23H
Index: 80H

Bits	Value	Function
0,1		Reserved
2,3		Reserved
4	0	Enable Programmable I/O decode. Default = 0 = disabled Disabled (default)
5	1	I/O port 0070H, bit 7. When this bit is read as 1, it implies that NMI is disabled
6	0 1	Write enable I/O port 03C3H. Write protected (default) When = 0, port 3C3H cannot be written to. Write enabled. When = 1, port 3C3 can be written to.
7	0 1	This bit determines which edge of the -CMD is used to sample -VGAACK signal, and post it in card select feed back register (91). The trailing edge of CMD is used to sample VGAACK (default). The leading edge of CMD is used to sample VGAACK.

Programmable I/O Setup Register-0 R31

Index Register Port: 22H
Data Register Port: 23H
Index: 81H

Bits	Value	Function
0	0	Programmable port address decode bit 8 (default)
1	0	Programmable port address decode bit 9 (default)

Programmable I/O Setup Register-0 R31 (continued)

Bits	Value	Function
2		Programmable port upper address decode (XA10 - XA16).
	0	-OBIOP input is used to decode Programmable port address. i.e. XA10 - XA16 are zeroes. Only XA0-XA9 are used for -PGMP0 output. (Default) The port decode range is 0 - 1K.
	1	-PGMPDEC input is used in conjunction with XA0 - XA9, to generate -PGMP0. The -PGMPDEC input to the 325 is derived by externally decoding XA10 - XA16. The port decode range is 0 - 64K
3		Write enable -PGMP0 bit
	1	When this bit is 1, the -PGMP0 is only generated for I/O write operation. For example when -XIOWR = 0.
	0	When this bit is 0, -XIOWR is not factored in -PGMP0 decoding.(default), -PGMP0 in generated irrespective of -XIOWR.
4		Read enable -PGMP0 bit.
	1	When this bit is 1, the -PGMP0 is generated for I/O read operation only. For example -XIORD = 0.
	0	When this bit is 0, -XIORD is not factored into -PGMP0 decoding. -PGMP0 is generated irrespective of -XIORD.
5-7		Programmable port lower address mask bits (for address bits 0 - 2). Default is all bits unmasked.
	7 6 5	Masked Addresses
	0 0 0	All address bits unmasked (default)
	0 0 1	Address bit 1 masked (don't-care)
	: : :	
	1 1 1	All lower 3 address bits masked (don't-care)

Programmable I/O Decode Register-0 R32

Index Register Port: 22H
Data Register Port: 23H
Index: 82H

Bits	Function
0	Programmable I/O port address decode bit 0
1	Programmable I/O port address decode bit 1
2	Programmable I/O port address decode bit 2
3	Programmable I/O port address decode bit 3
4	Programmable I/O port address decode bit 4
5	Programmable I/O port address decode bit 5
6	Programmable I/O port address decode bit 6
7	Programmable I/O port address decode bit 7

Programmable I/O Setup Register-0 R33

Index Register Port: 22H
Data Register Port: 23H
Index: 83H

Bits	Value	Function
0	0	Programmable port address decode bit 8 (default)
1	0	Programmable port address decode bit 9 (default)

Programmable I/O Setup Register-0 R33 (continued)

Bits	Value	Function
2		Programmable port upper address decode (XA10 - XA16).
	0	-OBIOP input is used to decode Programmable port address. i.e. XA10-XA16 are zeroes. Only XA0 - XA9 are used for -PGMP1 output. (Default) The port decode range is 0 - 1K.
	1	-PGMPDEC input is used in conjunction with XA0 - XA9, to generate -PGMP1. The -PGMPDEC input to the 325 is derived by externally decoding XA10 - XA16. The port decode range is 0 - 64K
3		Write enable -PGMP1 bit
	1	When this bit is 1, the -PGMP1 is only generated for I/O operation. For example when -XIOWR = 0.
	0	When this bit is 0, -XIOWR is not factored in -PGMP1 decoding (default). -PGMP1 in generated irrespective of -XIOWR.
4		Read enable -PGMP1 bit.
	1	When this bit is 1, the -PGMP1 is generated for I/O read operation only. For example -XIORD = 0.
	0	When this bit is 0, -XIORD is not factored into -PGMP1 decoding. -PGMP1 is generated irrespective of -XIORD.
5-7		Programmable port lower address mask bits (for address bits 0 - 2). Default is all bits unmasked.
	7 6 5	Masked Addresses
	0 0 0	All address bits unmasked (default)
	0 0 1	Address bit 1 masked (don't-care)
	: : :	
	1 1 1	All lower 3 address bits masked (don't-care)

Programmable I/O Decode Register-1 R34

Index Register Port: 22H
Data Register Port: 23H
Index: 84H

Bits	Function
0	Programmable I/O port address decode bit 0
1	Programmable I/O port address decode bit 1
2	Programmable I/O port address decode bit 2
3	Programmable I/O port address decode bit 3
4	Programmable I/O port address decode bit 4
5	Programmable I/O port address decode bit 5
6	Programmable I/O port address decode bit 6
7	Programmable I/O port address decode bit 7

Programmable I/O Setup Register-0 R35

Index Register Port: 22H
Data Register Port: 23H
Index: 85H

Bits	Value	Function
0	0	Programmable port address decode bit 8 (default)
1	0	Programmable port address decode bit 9 (default)
2		Programmable port upper address decode (XA10-XA16).
	0	-OBIOP input is used to decode Programmable port address. i.e. XA10-XA16 are zeroes. Only XA0-XA9 are used for -PGMP2 output. (Default) The port decode range is 0 - 1K.
	1	-PGMPDEC input is used in conjunction with XA0-XA9, to generate -PGMP2. The -PGMPDEC input to the 325 is derived by externally decoding XA10 - XA16. The port decode range is 0 - 64K
3		Write enable -PGMP2 bit
	1	When this bit is 1, the -PGMP2 is only generated for I/O operation. For example when -XIOWR = 0.
	0	When this bit is 0, -XIOWR is not factored in -PGMP2 decoding.(default), -PGMP2 in generated irrespective of -XIOWR.
4		Read enable -PGMP2 bit.
	1	When this bit is 1, the -PGMP2 is generated for I/O read operation only. For example -XIORD = 0.
	0	When this bit is 0, -XIORD is not factored into -PGMP2 decoding. -PGMP2 is generated irrespective of -XIORD.
5:7		Programmable port lower address mask bits (for address bits 0 - 2). Default is all bits unmasked.
	7 6 5 0 0 0 0 0 1 : : : 1 1 1	Masked Addresses All address bits unmasked (default) Address bit 1 masked (don't-care) All lower 3 address bits masked (don't-care)

Programmable I/O Decode Register-2 R36

Index Register Port: 22H
Data register port: 23H
Index: 86H

Bits	Function
0	Programmable I/O port address decode bit 0
1	Programmable I/O port address decode bit 1
2	Programmable I/O port address decode bit 2
3	Programmable I/O port address decode bit 3
4	Programmable I/O port address decode bit 4
5	Programmable I/O port address decode bit 5
6	Programmable I/O port address decode bit 6
7	Programmable I/O port address decode bit 7

Higher System ID Byte Register - R37

Index register port: 22H
Data register port: 23H
Index: 87H

This register contains the upper 8 bits of the system ID number and is a read/write register. The contents can be read from the System POS register 1, at location 0101H, under system set-up mode only. The default is FD. The ID bytes varies with the system. For example, the IBM Model 80 at 16 MHz., ID = FE. This information is used by the NMI routine in the BIOS.

5.0 MISCELLANEOUS PORTS and POS REGISTERS:

The system miscellaneous ports and POS registers are located in 82C325 and also distributed among other CHIPsets™. They are listed as follows:

I/O port 60 - A read on this port resets IRQ1 and IRQ12.

I/O Port 61 (Default) Bit Definition

The following shows the bit definition for READ operations and also bits distribution among the CHIPSET™.

Bit	Definition	Location	Default
7	Parity error	82C325	(0=No parity error)
6	Channel check error	82C325	(0=No channel error)
5	Timer 2 output	82C226	
4	Toggles with each Refresh request	82C321	
3	Channel check enable	82C325	(1=disable)
2	Parity check enable	82C325	(1=disable)
1	Speaker data enable	82C325	(0=No speaker data)
0	Timer 2 Gate to speaker	82C325	(0=disable timer 2)

The following is I/O Port 61 bit deinition for WRITE operations and distribution.

Bit	Definition	Location
7	Reset timer 0 output	82C226
6	Reserved	
5	Reserved	
4	Reserved	
3	Channel check enable	82C325
2	Parity check enable	82C325
1	Speaker data enable	82C325, 82C226
0	Timer 2 Gate to speaker	82C325, 82C226

I/O Port 70 Bit Definition

This port is located completely in 82C325.

Bits	Definition	Access	Default
7	NMI mask	Write only	(1=NMI masked)
6-0	RT/CMOS Address	Write/Read	

The bits 0-6 in I/O port 70 is used to access 128 byte of Real time CMOS RAM. When doing I/O operations to RT/CMOS RAM Interrupts should be inhibited. To access the RT/CMOS RAM, OUT to port 70 with the RT/CMOS address to be accessed and then immedietely port 71 should be accessed. If the RT/CMOS is to be written OUT to port 71 with the data and to read the RT/CMOS IN from port 71, data is returned in AL.

I/O Port 91 Bit Definition

This Port is located completely in 82C325.

Bits	Definition	Access	Default
7-1	Not used		
0	Channel acknowledge	Read	(0=No select feedback)

I/O Port 92 Bit Definition.

This port is located in 82C321 and 82C226.

Bit	Definition	Access	Location
7	Fixed disk activity light bit A	Read/write	82C321
6	Fixed disk activity light bit B	Read/Write	82C321
5	Reserved		
4	Watch dog timer status	Read	82C226
3	Security lock latch	Write Read	82C321,82C226 82C321
2	Reserved		
1	Alternate Gate A20 (default = 0)	Read/write	82C321
0	Alternate Hot Reset	Read/Write	82C321

I/O Port 94 Bit Definition

This is located in 82C325 for both read and write. In addition, while writing to bit 7, this bit gets written into 82C321, 82C226 and 82C607.

Bit	Definition	Access	Default
7	System board enable/-setup	R/W	(1=enable)
6	Not used		
5	VGA enable/-setup	R/W	(1=enable)
4-0	Not used		

SYSTEM POS REGISTERS

All the POS registers 100-103 and 3C3 are located in 82C325.

I/O Port 100 bit definition

Bits	Description	Access	Default
7-0	System board ID low byte	R	(=FF)

I/O Port 101

Bits	Description	Access	Default
7-0	System board ID high byte	R	(=FD)

I/O Port 102 Bit definition

Bits	Function	Access	Default
7	PP direction enable	R/W	(0=bi-directional)
6	PP select 1	R/W	
5	PP select 2	R/W	
4	PP enable	R/W	
3	SP select	R/W	
2	SP enable	R/W	
1	Disk enable	R/W	
0	PP, SP, Disk enable	R/W	0 = disable

I/O Port 103 Bit Definition

To access this register bit 3 of port 96 should be a 0 to avoid sending a setup signal to any MCA slot, and bit 7 of port 94 should be 0 to accept setup cycles. After accessing port 103, bit 7 of port 94 should be set back to 1.

PORT 103 is located in 82C325 and provided for compatibility purposese only.

The following is the READ ONLY definition of port 103

Bits	Function	Access	Default
7-4	not used		
3,2	1 MB memory installed in second connector.	R	
	Bits 3, Bit 2 Meaning 0 0 1Mb present 1 1 1Mb absent		
1,0	1 MB memory installed in first connector.	R	
	Bits 1 Bit 0 Meaning 0 0 1Mb present 1 1 1Mb absent		

The following is the WRITE definition of port 103

The port 103 is writable but no activity takes place.

I/O Port 3C3 Bit Definition

This is located in 82C325. If 82C452 VGA is used port 3C3 is also provided in the VGA, in which case the VGAEN pin on 82C325 should not be used on the board.

Bits	Definition	Access	Default
7-1	not used		
0	On board VGA enable	R/W	(1=enable) Enables VGA on the motherboard. (0=disable) Disables the VGA on the motherboard. **Note:** (This is useful when there is a VGA card on the MCA bus.)

82C325 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	-	7.0	V
Input Voltage	V_I	-0.5	VCC + 0.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{OP}	-25º	85º	C
Storage Temperature	T_{STG}	-40º	125º	C
Maximum Power Dissapation		-	0.84	W

NOTE: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C325 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	VCC	4.75	5.25	V
Ambient Temperature	T_A	0º	70º	C

82C325 DC Characteristics

Operating Conditions: T_A =0ºC to 70ºC, VCC = 4.75 to 5.25V

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}	-0.5	1.5	V
Input High Voltage	V_{IH}	2.0	VCC+0.5	V
Output Low Voltage	V_{OL}	-	0.45	V (Note 1)
Output High Voltage	V_{OH}	2.4	-	V (Note 1)
Input Leakage Current $0<V_{IN}<V_{CC}$	I_{IL}	-80	+10	uA
Power Supply Current @ 25MHz	I_{CC}	120		mA
Output High-Z Leakage Current $0.45<V_{OUT}<V_{CC}$	I_{OZ1}	-80	+0.1	uA

Note 1: I_{OL} = 8mA and I_{OH} = -8mA for LD data bus, and data bus MP 0:3, NMI.
I_{OL} = 4mA and I_{OH} = -4mA for all other output pins

CPU CYCLES:

OUTPUT DELAYS		Min	Max	Unit
t501	LD valid to MD valid, -MSTR inactive		22	ns
t502	LD invalid to MD invalid, -MSTR inactive		18	ns
t503	LD to MP delay, -MSTR inactive		30	ns
t504	LD invalid to MP invalid, -MSTR inactive		30	ns
t507	MD, MP active to LD active, MSTR inactive		20	ns
t510	-DRD inactive to LD in Hi-Z -MSTR inactive		30	ns
t513	MD (0-15) active to LD(16-31) active		23	ns
t514	MD (0-15) inactive to LD(16-31) inactive		23	ns
t515	LD(16-31) active to MD(0-15) active		23	ns
t516	LD(16-31) inactive to MD(0-15) inactive		23	ns
t517	MD(0-7) active to LD(8-15) active		23	ns
t518	MD(0-7) inactive to LD(8-15) inactive		23	ns
t519	LD(8-15) active to MD(0-7) active		23	ns
t520	LD(8-15) inactive to MD(0-7) inactive		23	ns
t521	MD(0-7) active to LD(24-31) active		23	ns
t522	MD(0-7) inactive to LD(24-31) inactive		23	ns
t523	LD(24-31) active to MD(0-7) active		23	ns
t524	LD(24-31) inactive to MD(0-7) inactive		23	ns
t525	LD(0-15) active to LD(16-31) active		23	ns
t526	LD(0-15) inactive to LD(16-31) inactive		23	ns
t527	LD(16-31) active to LD(0-15) active		23	ns
t528	LD(16-31) inactive to LD(0-15) inactive		23	ns
t529	LD(0-15) active to MD(16-31) active		23	ns
t530	LD(0-15) inactive to MD(16-31) inactive		23	ns

OUTPUT DELAYS (continued)		Min	Max	Unit
t531	MD(16-31) active to LD(0-15) active		23	ns
t532	MD(16-31) inactive to LD(0-15) inactive		23	ns
t533	MD(0-15) active to MD(16-31) active		23	ns
t534	MD(0-15) inactive to MD(16-31) inactive		23	ns
t535	MD (16-31) active to MD(0-15) active		23	ns
t536	MD (16-31) inactive to MD(0-15) inactive		23	ns

PARITY RELATED OUTPUTS (OUTPUT DELAYS)		Min	Max	Unit
t542	MD(16-31) inactive to MP(2-3) inactive		20	ns
t543	MD(0-15) active to MP(2-3) active		20	ns
t544	MD(16-31) inactive to MP(2-3) inactive		20	ns
t551	-PCEN(0-3) active to -CHCKO active		18	ns
t553	-PCEN(0-3) active to -NMI active (from Hi-Z)		20	ns
t555	-CHCK0 active to -NMI active		20	ns
t574	LD(0-15) to MP(2-3) valid		22	ns
t577	MD(0-15) valid to MP(2-3) valid		30	ns
t578	MD(0-15) invalid to MP(2-3) invalid		36	
t579	LD(0-15) invalid to MP(2-3) invalid		33	ns
t580	LD(0-15) valid to MP(2-3) valid		30	ns

MASTER CYCLES (OUTPUT DELAYS)		Min	Max	Unit
t537	MD invalid to LD invalid , for 32 bit MSTR		20	ns
t538	MD vaild to MP valid, for 32 bit MSTR		30	ns
t539	MD invaild to MP invalid, for 32 bit MSTR		22	ns
t540	-DRD active to LD in Hi-Z for 32 bit MSTR		22	ns

MASTER CYCLES (OUTPUT DELAYS continued)		Min	Max	Unit
t541	-DRD active to MP in Hi-Z for 32 bit MSTR		20	ns
t547	-DRD active to MD(0-7) valid for internal register access by MSTR.		35	ns
t575	-DRD inactive to MD in Hi-Z for 32 bit MSTR		38	ns

MISCELLANEOUS (OUTPUT DELAYS)		Min	Max	Unit
t546	-VGACMD active to LD valid for Register access by CPU.		32	ns
t552	-XIOWR inactive to -CHCKO inactive		20	ns
t554	-XIOWR inactive to -NMI inactive(to Hi-Z)		20	ns
t556	-XA(0-9), -OBIOP valid to -KBDCS active		30	ns
t557	-XA(0-9), -OBIOP invalid to -KBDCS inactive		15	ns
t558	KBDP24 active to -IRQ1 active		15	ns
t559	-XIORD active to -IRQ1 inactive		15	ns
t560	KBDP25 active to -IRQ12 active		15	ns
t561	-XIORD active to -IRQ12 inactive		15	ns
t562	-XIORD, -XIOWR active to XDIR low		15	ns
t563	-XIORD, -XIOWR inactive to XDIR high		15	ns
t564	-XIOWR inactive to -VGASETUP, VGAEN low		20	ns
t565	-XIOWR inactive to VGASETUP VGAEN high		15	ns
t566	-XIOWR active -P74WR, -P75WR active		15	ns
t568	-XIORD, -XIOWR active to -PGMP(0-2) active		15	ns
t569	-XIORD, -XIOWR inactive to -PGMP(0-2) inactive		15	ns
t570	-INTA active to XDIR low		15	ns
t571	-INTA inactive to XDIR high		12	ns

CPU CYCLES:

OUTPUT DELAYS		Min	Max	Unit
t501	LD valid to MD valid, -MSTR inactive		22	ns
t502	LD invalid to MD invalid, -MSTR inactive		18	ns
t503	LD to MP delay, -MSTR inactive		20	ns
t504	LD invalid to MP invalid, -MSTR inactive		18	ns
t507	MD, MP active to LD active, MSTR inactive		20	ns
t510	-DRD inactive to LD in Hi-Z -MSTR inactive		30	ns
t513	MD (0-15) active to LD(16-31) active		23	ns
t514	MD (0-15) inactive to LD(16-31) inactive		23	ns
t515	LD(16-31) active to MD(0-15) active		23	ns
t516	LD(16-31) inactive to MD(0-15) inactive		23	ns
t517	MD(0-7) active to LD(8-15) active		23	ns
t518	MD(0-7) inactive to LD(8-15) inactive		23	ns
t519	LD(8-15) active to MD(0-7) active		23	ns
t520	LD(8-15) inactive to MD(0-7) inactive		23	ns
t521	MD(0-7) active to LD(24-31) active		23	ns
t522	MD(0-7) inactive to LD(24-31) inactive		23	ns
t523	LD(24-31) active to MD(0-7) active		23	ns
t524	LD(24-31) inactive to MD(0-7) inactive		23	ns
t525	LD(0-15) active to LD(16-31) active		23	ns
t526	LD(0-15) inactive to LD(16-31) inactive		23	ns
t527	LD(16-31) active to LD(0-15) active		23	ns
t528	LD(16-31) inactive to LD(0-15) inactive		23	ns
t529	LD(0-15) active to MD(16-31) active		23	ns
t530	LD(0-15) inactive to MD(16-31) inactive		23	ns

OUTPUT DELAYS (Continued)		Min	Max	Unit
t531	MD(16-31) active to LD(0-15) active		23	ns
t532	MD(16-31) inactive to LD(0-15) inactive		23	ns
t533	MD(0-15) active to MD(16-31) active		23	ns
t534	MD(0-15) inactive to MD(16-31) inactive		23	ns
t535	MD (16-31) active to MD(0-15) active		23	ns
t536	MD (16-31) inactive to MD(0-15) inactive		23	ns

PARITY RELATED OUTPUTS (OUTPUT DELAYS)		Min	Max	Unit
t542	MD(16-31) inactive to MP(2-3) inactive		20	ns
t543	MD(0-15) active to MP(2-3) active		20	ns
t544	MD(16-31) inactive to MP(2-3) inactive		20	ns
t551	-PCEN(0-3) active to -CHCKO active		18	ns
t553	-PCEN(0-3) active to -NMI active (from Hi-Z)		18	ns
t555	-CHCK0 active to -NMI active		15	ns
t574	LD(0-15) to MP(2-3) valid		19	ns
t577	MD(0-15) valid to MP(2-3) valid		21	ns
t578	MD(0-15) invalid to MP(2-3) invalid		36	ns
t579	LD(0-15) invalid to MP(2-3) invalid		33	ns
t580	LD(0-15) valid to MP(2-3) valid		19	ns

MASTER CYCLES (OUTPUT DELAYS)		Min	Max	Unit
t537	MD invalid to LD invalid , for 32 bit MSTR		20	ns
t538	MD vaild to MP valid, for 32 bit MSTR		18	ns
t539	MD invaild to MP invalid, for 32 bit MSTR		20	ns
t540	-DRD active to LD in Hi-Z for 32 bit MSTR		20	ns

MASTER CYCLES (OUTPUT DELAYS continued)		Min	Max	Unit
t541	-DRD active to MP in Hi-Z for 32 bit MSTR		20	ns
t547	-DRD active to MD(0-7) valid for internal register access by MSTR.		35	ns
t575	-DRD inactive to MD in Hi-Z for 32 bit MSTR		38	ns

MISCELLANEOUS OUTPUTS (OUTPUT DELAYS)		Min	Max	Unit
t546	-VGACMD active to LD valid for Register access by CPU.		32	ns
t552	-XIOWR inactive to -CHCKO inactive		17	ns
t554	-XIOWR inactive to -NMI inactive(to Hi-Z)		15	ns
t556	-XA(0-9), -OBIOP valid to -KBDCS active		30	ns
t557	-XA(0-9), -OBIOP invalid to -KBDCS inactive		12	ns
t558	KBDP24 active to -IRQ1 active		12	ns
t559	-XIORD active to -IRQ1 inactive		15	ns
t560	KBDP25 active to -IRQ12 active		11	ns
t561	-XIORD active to -IRQ12 inactive		15	ns
t562	-XIORD, -XIOWR active to XDIR low		13	ns
t563	-XIORD, -XIOWR inactive to XDIR high		10	ns
t564	-XIOWR inactive to -VGASETUP, VGAEN low		15	ns
t565	-XIOWR inactive to VGASETUP VGAEN high		15	ns
t566	-XIOWR active -P74WR, -P75WR active		15	ns
t568	-XIORD, -XIOWR active to -PGMP(0-2) active		15	ns
t569	-XIORD, -XIOWR inactive to -PGMP(0-2) inactive		12	ns
t570	-INTA active to XDIR low		12	ns
t571	-INTA inactive to XDIR high		9	ns

CPU CYCLES:

OUTPUT DELAYS		Min	Max	Unit
t501	LD valid to MD valid, -MSTR inactive		22	ns
t502	LD invalid to MD invalid, -MSTR inactive		18	ns
t503	LD to MP delay, -MSTR inactive		20	ns
t504	LD invalid to MP invalid, -MSTR inactive		18	ns
t507	MD, MP active to LD active, MSTR inactive		20	ns
t510	-DRD inactive to LD in Hi-Z -MSTR inactive		30	ns
t513	MD (0-15) active to LD(16-31) active		23	ns
t514	MD (0-15) inactive to LD(16-31) inactive		23	ns
t515	LD(16-31) active to MD(0-15) active		23	ns
t516	LD(16-31) inactive to MD(0-15) inactive		23	ns
t517	MD(0-7) active to LD(8-15) active		23	ns
t518	MD(0-7) inactive to LD(8-15) inactive		23	ns
t519	LD(8-15) active to MD(0-7) active		23	ns
t520	LD(8-15) inactive to MD(0-7) inactive		23	ns
t521	MD(0-7) active to LD(24-31) active		23	ns
t522	MD(0-7) inactive to LD(24-31) inactive		23	ns
t523	LD(24-31) active to MD(0-7) active		23	ns
t524	LD(24-31) inactive to MD(0-7) inactive		23	ns
t525	LD(0-15) active to LD(16-31) active		23	ns
t526	LD(0-15) inactive to LD(16-31) inactive		23	ns
t527	LD(16-31) active to LD(0-15) active		23	ns
t528	LD(16-31) inactive to LD(0-15) inactive		23	ns
t529	LD(0-15) active to MD(16-31) active		23	ns
t530	LD(0-15) inactive to MD(16-31) inactive		23	ns

OUTPUT DELAYS (continued)		Min	Max	Unit
t531	MD(16-31) active to LD(0-15) active		23	ns
t532	MD(16-31) inactive to LD(0-15) inactive		23	ns
t533	MD(0-15) active to MD(16-31) active		23	ns
t534	MD(0-15) inactive to MD(16-31) inactive		23	ns
t535	MD (16-31) active to MD(0-15) active		23	ns
t536	MD (16-31) inactive to MD(0-15) inactive		23	ns

PARITY RELATED OUTPUTS (OUTPUT DELAYS)		Min	Max	Unit
t542	MD(16-31) inactive to MP(2-3) inactive		20	ns
t543	MD(0-15) active to MP(2-3) active		20	ns
t544	MD(16-31) inactive to MP(2-3) inactive		20	ns
t551	-PCEN(0-3) active to -CHCKO active		18	ns
t553	-PCEN(0-3) active to -NMI active (from Hi-Z)		18	ns
t555	-CHCK0 active to -NMI active		15	ns
t574	LD(0-15) to MP(2-3) valid		19	ns
t577	MD(0-15) valid to MP(2-3) valid		21	ns
t578	MD(0-15) invalid to MP(2-3) invalid		36	ns
t579	LD(0-15) invalid to MP(2-3) invalid		33	ns
t580	LD(0-15) valid to MP(2-3) valid		19	ns

MASTER CYCLES (OUTPUT DELAYS)		Min	Max	Unit
t537	MD invalid to LD invalid , for 32 bit MSTR		20	ns
t538	MD vaild to MP valid, for 32 bit MSTR		18	ns
t539	MD invaild to MP invalid, for 32 bit MSTR		20	ns
t540	-DRD active to LD in Hi-Z for 32 bit MSTR		20	ns

MASTER CYCLES (OUTPUT DELAYS continued)		Min	Max	Unit
t541	-DRD active to MP in Hi-Z for 32 bit MSTR		20	ns
t547	-DRD active to MD(0-7) valid for internal register access by MSTR.		35	ns
t575	-DRD inactive to MD in Hi-Z for 32 bit MSTR		38	ns

MISCELLANEOUS (OUTPUT DELAYS)		Min	Max	Unit
t546	-VGACMD active to LD valid for Register access by CPU.		32	ns
t552	-XIOWR inactive to -CHCKO inactive		17	ns
t554	-XIOWR inactive to -NMI inactive(to Hi-Z)		15	ns
t556	-XA(0-9), -OBIOP valid to -KBDCS active		30	ns
t557	-XA(0-9), -OBIOP invalid to -KBDCS inactive		12	ns
t558	KBDP24 active to -IRQ1 active		12	ns
t559	-XIORD active to -IRQ1 inactive		15	ns
t560	KBDP25 active to -IRQ12 active		11	ns
t561	-XIORD active to -IRQ12 inactive		15	ns
t562	-XIORD, -XIOWR active to XDIR low		13	ns
t563	-XIORD, -XIOWR inactive to XDIR high		10	ns
t564	-XIOWR inactive to -VGASETUP, VGAEN low		15	ns
t565	-XIOWR inactive to VGASETUP VGAEN high		15	ns
t566	-XIOWR active -P74WR, -P75WR active		15	ns
t568	-XIORD, -XIOWR active to -PGMP(0-2) active		15	ns
t569	-XIORD, -XIOWR inactive to -PGMP(0-2) inactive		12	ns
t570	-INTA active to XDIR low		12	ns
t571	-INTA inactive to XDIR high		9	ns

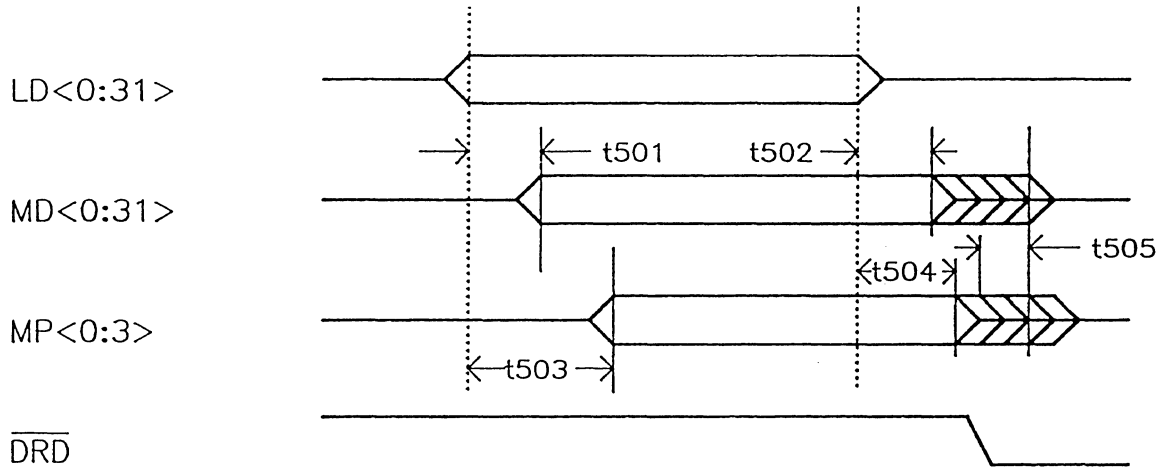


Figure 6.1 CPU Writes to DRAM on MD Bus (DMA Low Word)

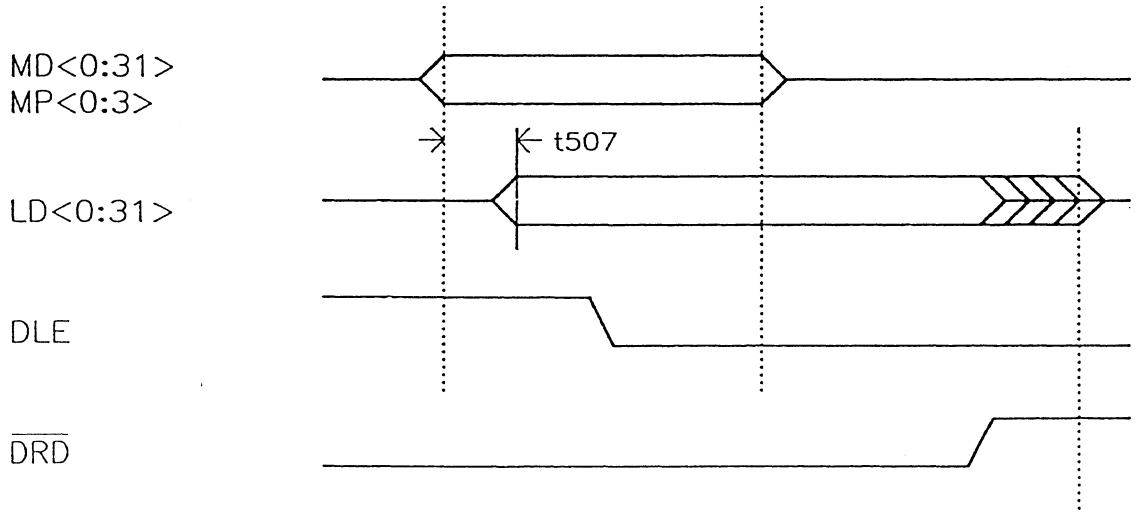


Figure 6.2 CPU Reads DRAM on the MD Bus (DMA Low Word)

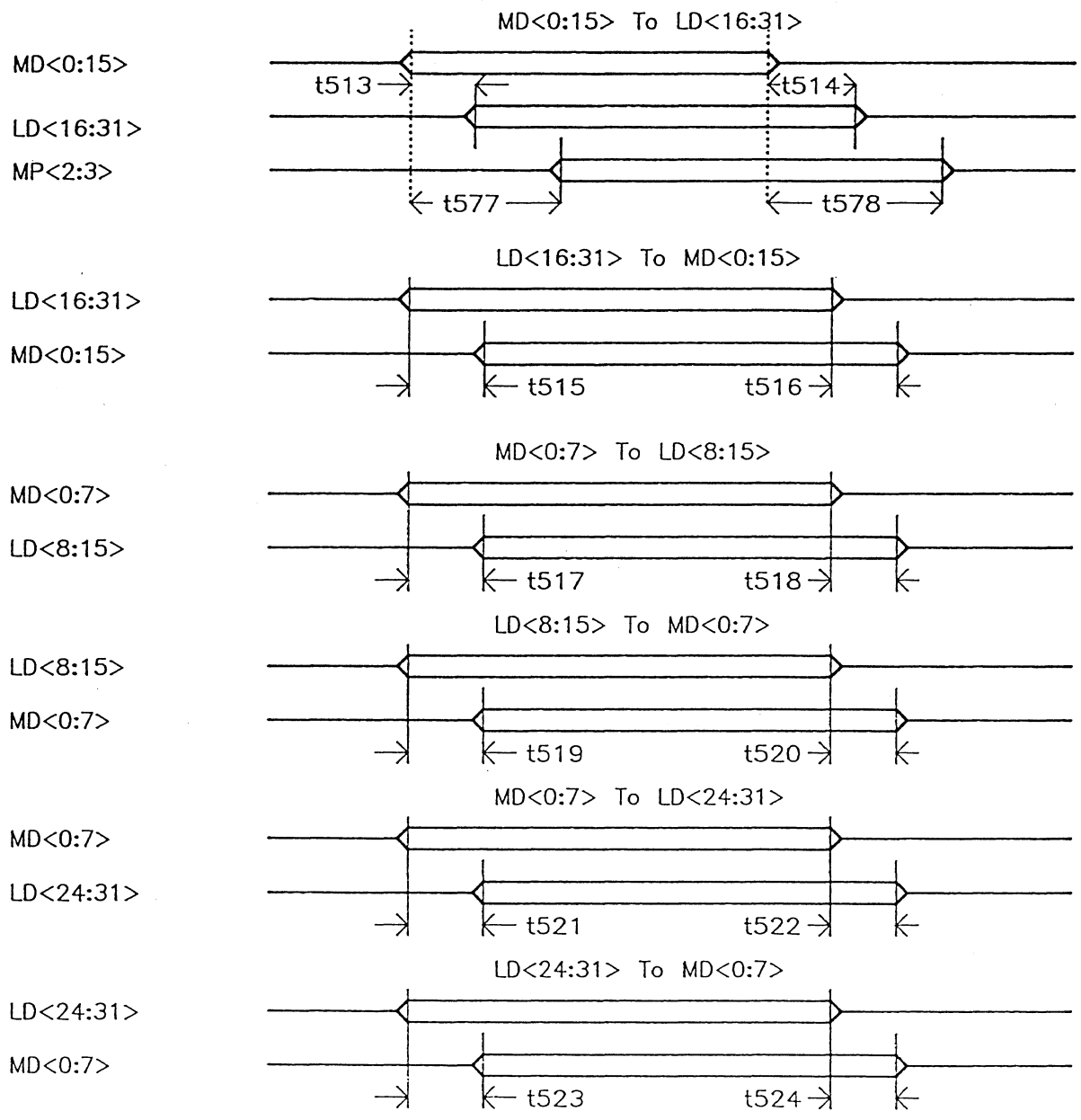


Figure 6.3 Path Propagation Delays

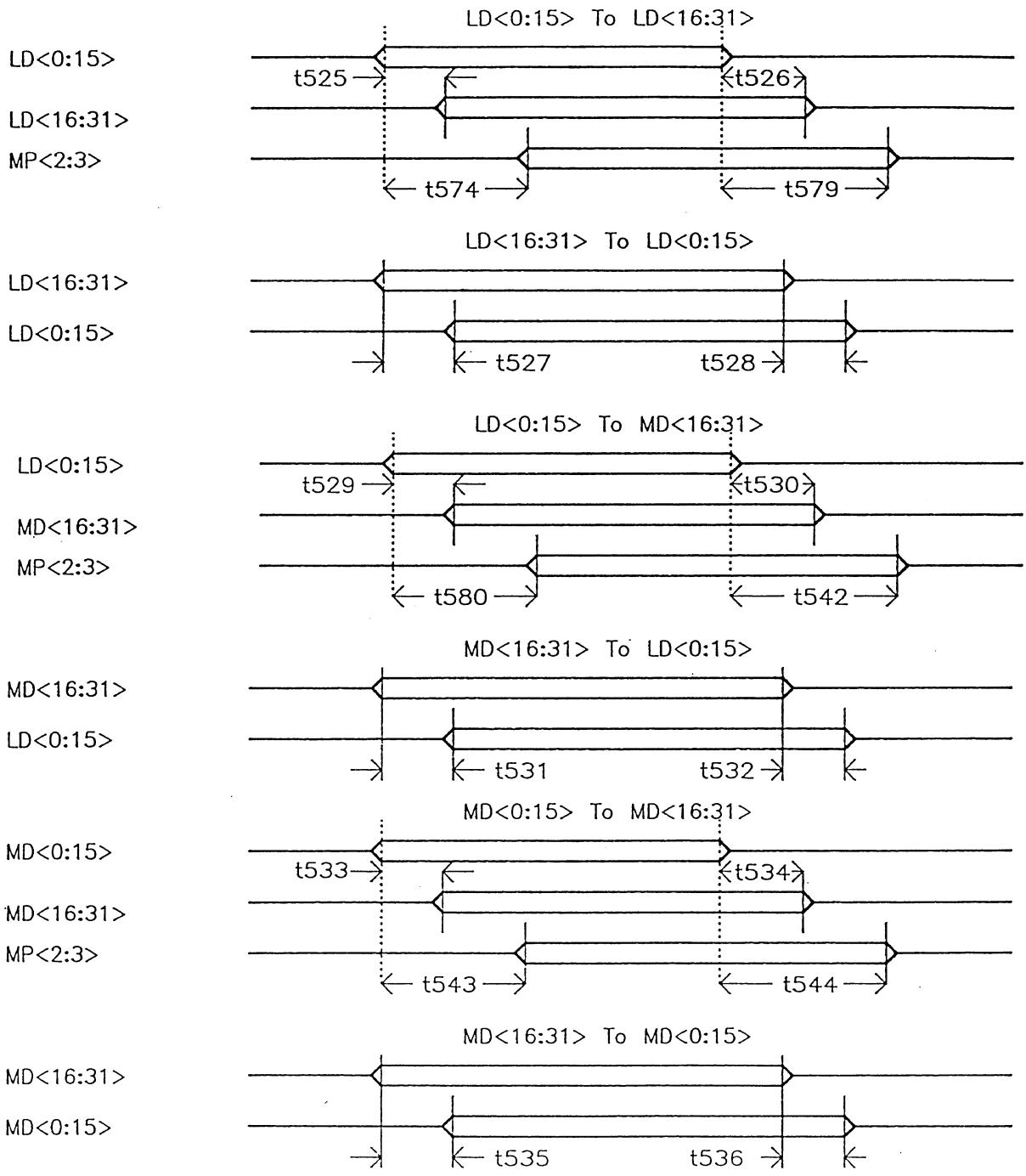


Figure 6.4 Path Propagation Delays

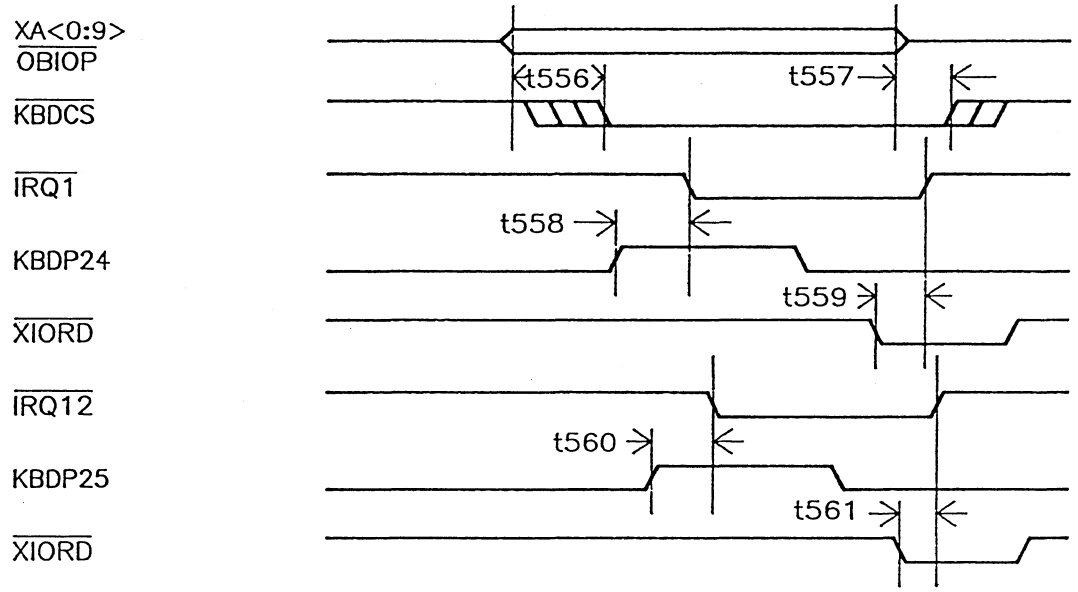


Figure 6.5 IRQ and IRQ12 Timing

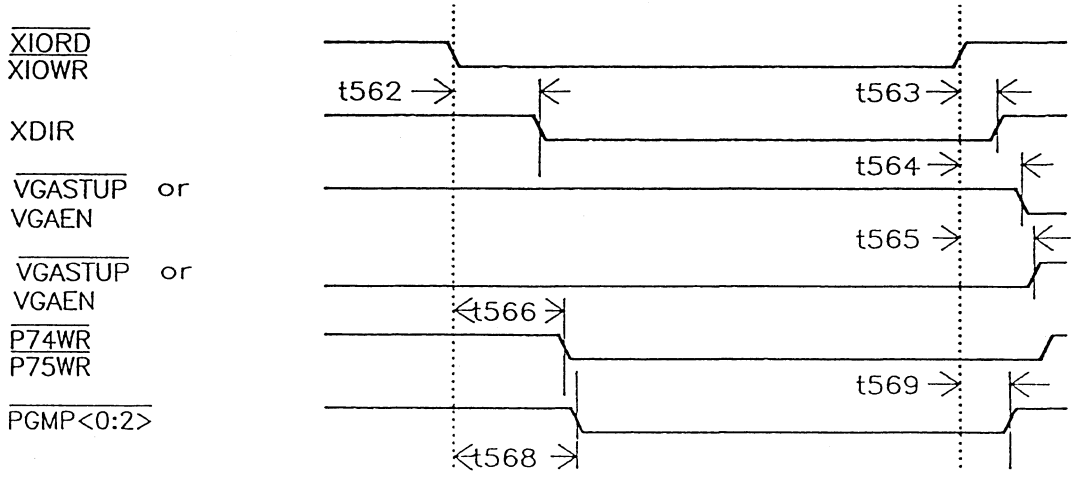


Figure 6.6 Misc. Signal Timing

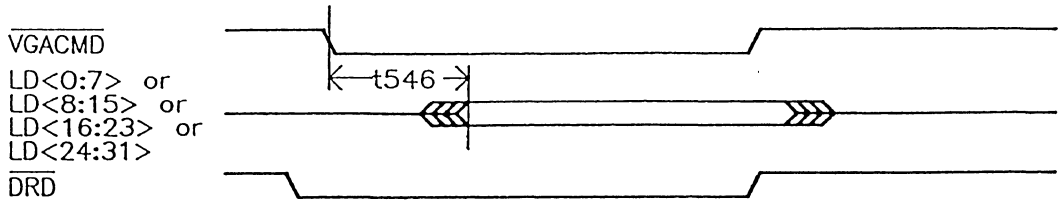


Figure 6.7 Register Access from CPU(Read)

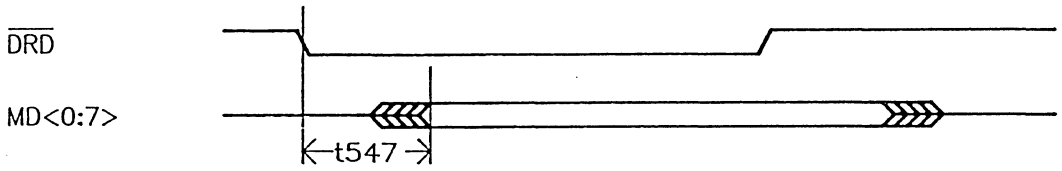


Figure 6.8 Register Access from Master(Read)

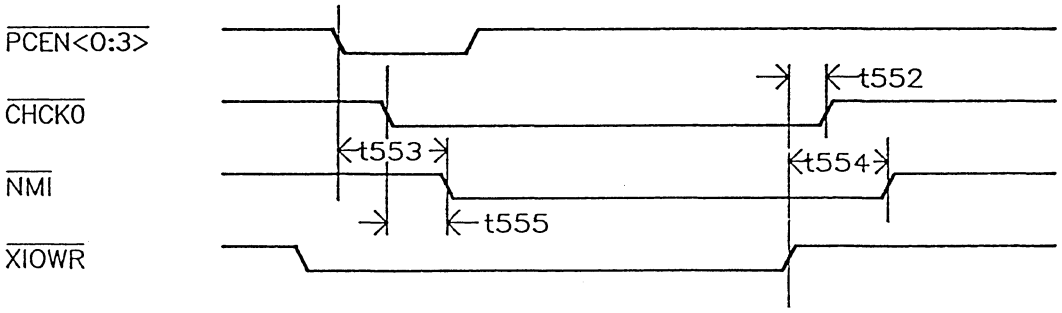


Figure 6.9 NMI and CHCK0 Timing

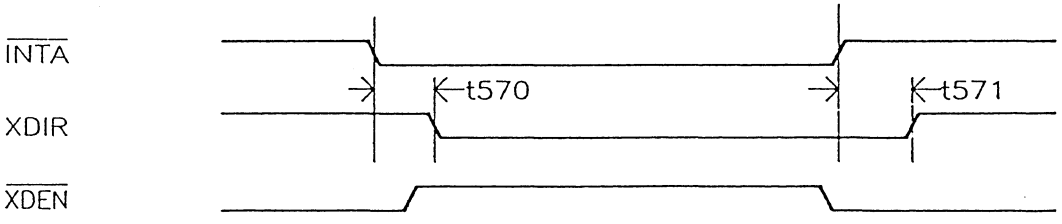


Figure 6.10 XDIR, XDEN and INTA Timing

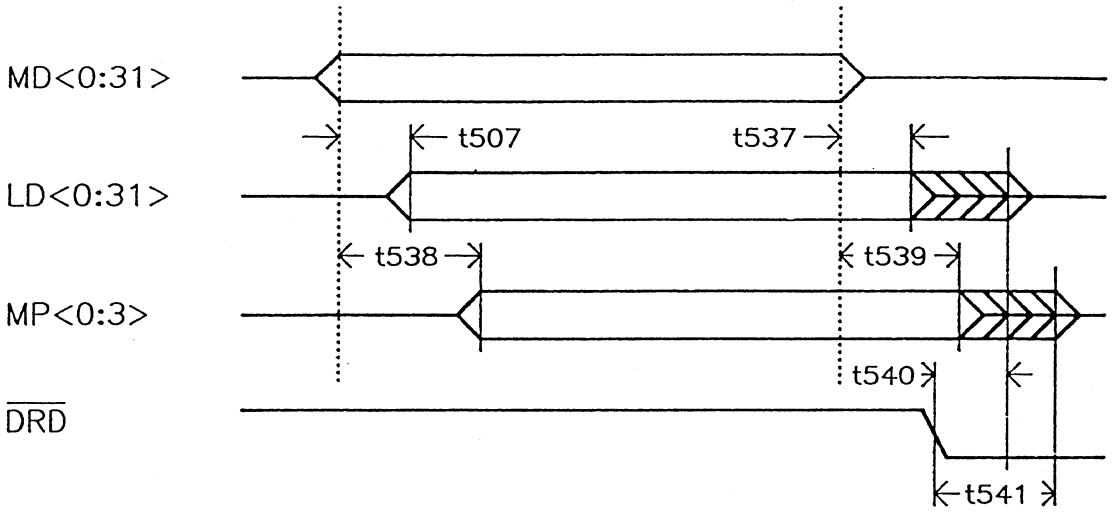


Figure 6.11 32 Bit Master Write to DRAM on LD Bus

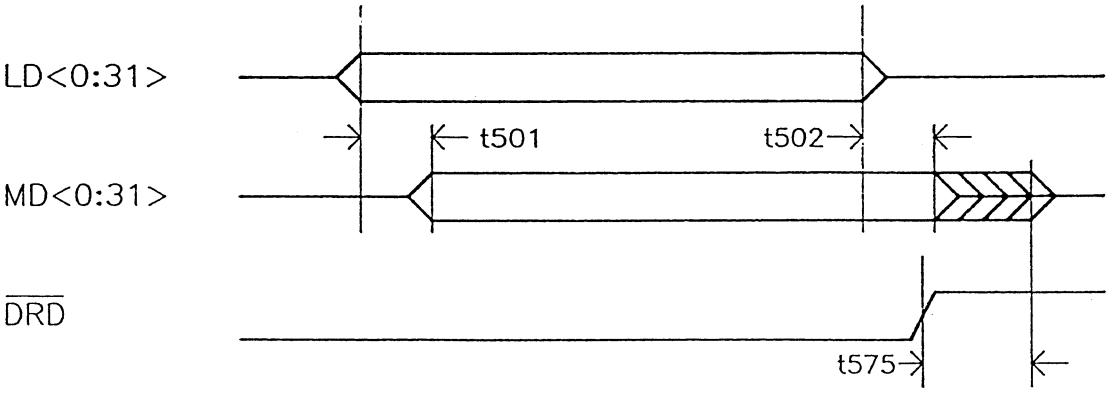
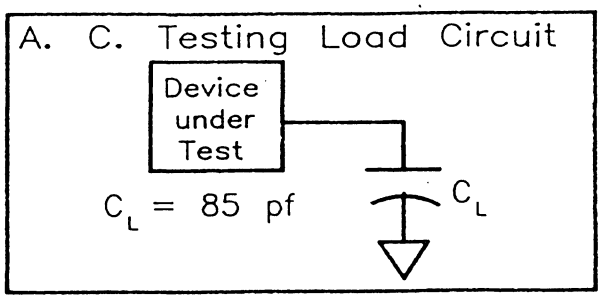


Figure 6.12 32 Bit Master Read from DRAM on LD Bus


A. C. Testing Load Circuit
Device under Test
C_L = 85 pf
C_L

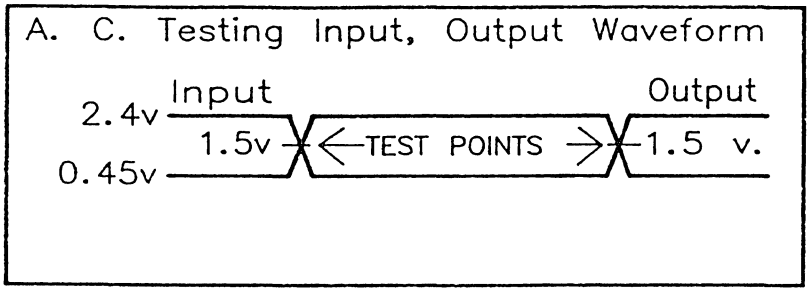
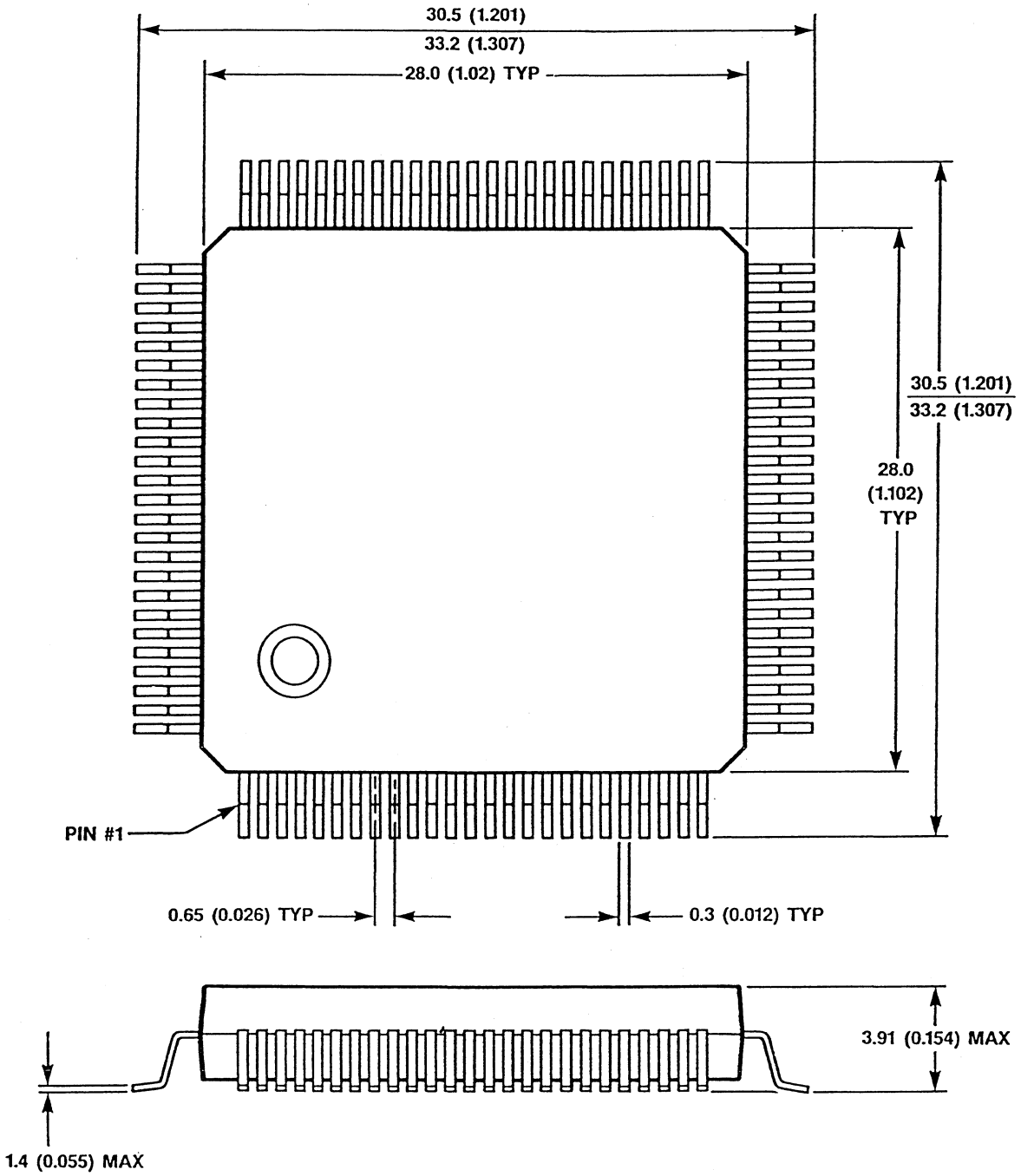

A. C. Testing Input, Output Waveform
Input
Output
2.4v
1.5v
TEST POINTS
1.5 v.
0.45v

Figure 6.13

DIMENSIONS: mm (in)



144 PIN PLASTIC FLAT PACKAGE (SQUARE)

FEATURES

- Eight Independent DMA channels
- Extended Mode Operation
- 64K I/O addressing capability. I/O address generation optional.
- Register/Program Compatibility with 8237 in the compatible mode.
- 16 MByte memory addressing capability
- Data transfer between memory and I/O
- Status signals compatibility to 80286
- Serial DMA operation
- Read Verification mode
- Virtual DMA support for channels 0 and 4
- Each channel individually programmable to support either byte or word transfer
- DRAM refresh Logic support for 256KB, 1MB and 4MB DRAMS

FUNCTIONS

The 82C223 DMA Controller performs the following functions in a CHIPS/250 or CHIPS/280 implementation. Figure 7-1 Shows the block diagram of 82C223.

- NMI Bus time out capability
- Error recovery mechanism
- Refresh clock generation
- Central Arbitration Control Point (CACP) intergrated on chip:
  - * 16 Arbitration Levels
  - * Central Arbitration
  - * Local Arbitration
  - * Burst Mode Operation
- Fabricated in 1.5 micron CMOS technology
- 100% compatibility with IBM PS/2 family
- Available in 84 pin PLCC or 100 pin PFP packages.

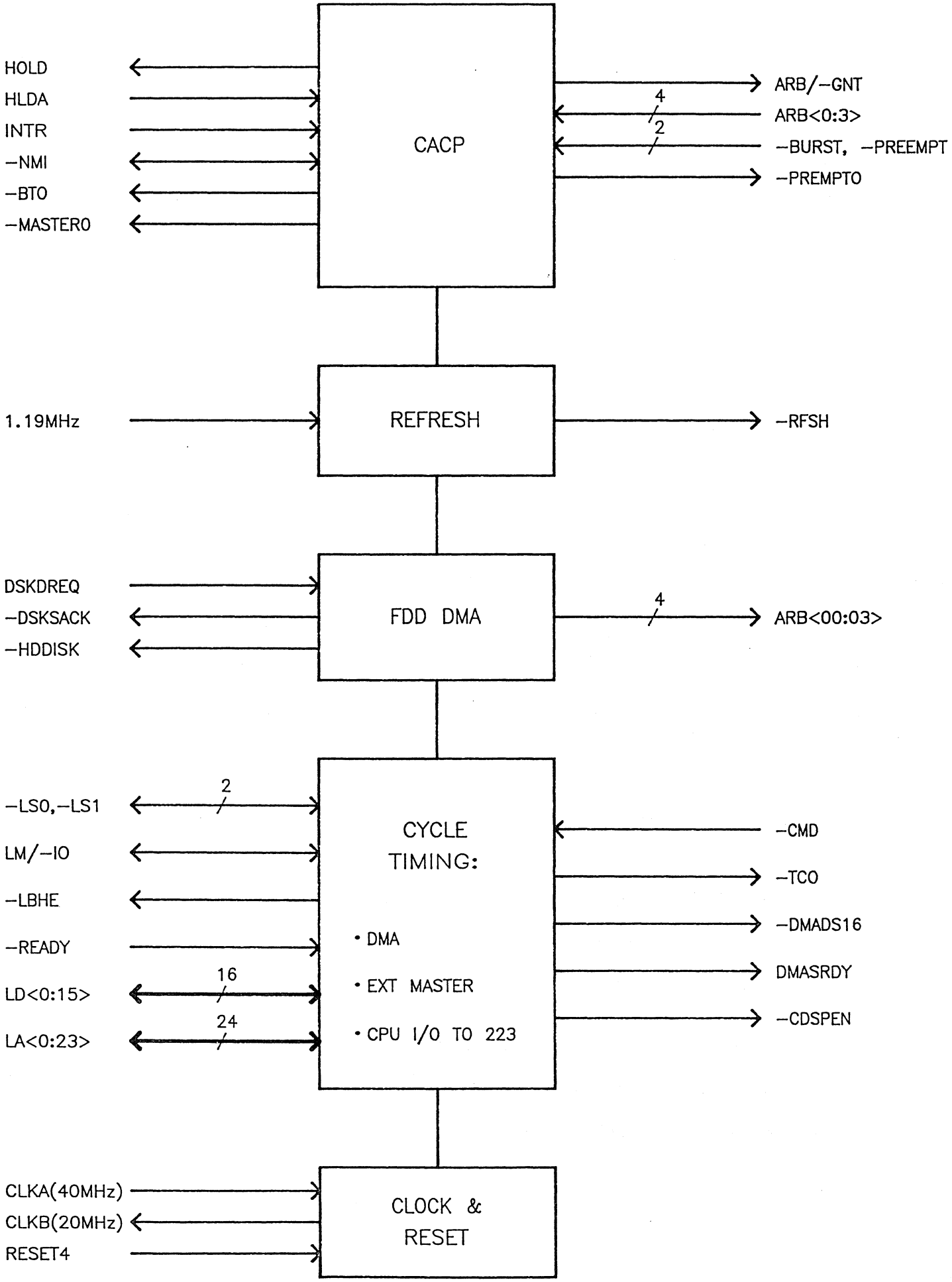


Figure 7.1 82C223 Block Diagram

1.0 OVERVIEW

The 82C223 DMA Controller incorporates the micro channel Central Arbitration Control Point (CACP), eight programmable DMA channels, 11-bit wide memory refresh, and other miscellaneous logic.

While maintaining complete compatibility with the DMA implementation on IBM PS/2 Models, the chip integrates additional features like error recovery and refresh clock generation logic. The 82C223 along with the CHIPS/250 or the CHIPS/280 CHIPSet, provides a highly integrated high performance solution for IBM PS/2 compatible implementation.

The 82C223 DMA controller is implemented using advanced CMOS technology and is available in either 84 pin PLCC or 100 pin PFP packages.

2.0 CACP

The Central Arbitration Control Point allows slave DMA devices or external Bus Masters to share control of the system bus. It supports bursting devices and implements a "Fairness" scheme that ensures all requesting device get access to the system bus. It supports up to sixteen arbitrating devices such as slave DMA peripherals or intelligent Bus Masters.

The micro channel has two states, one called the arbitration state and the other called the grant state distinguished by the level of the ARB/-GNT signal. If ARB/-GNT is high, then it is in the arbitration state and when low, it is in the grant state.

Each local arbiter (MASTER or a DMA slave) on the channel is assigned a unique 4 bit arbitration level. Level 0 has the highest priority and level 15 the lowest. The level 15 is reserved for the system CPU.

A DMA slave requests the use of the MCA by activating the -PREEMPT line. The Central Arbitration Control Point (CACP) raises the ARB/-GNT line signifying the start of an arbitration cycle. During this interval, the DMA slave drives its arbitration levels onto the 4 ARB pins.

If any other device also requests the bus, it or they also assert their priority levels on the 4 ARB pins. Each competing device compares the levels it is driving on the pins with the levels already on the pins. If the device sees a higher priority level on the bus than it is trying to assert, then it is declared a loser. The highest priority device is declared the winner.

At the end of the arbitration cycle (signified by the CACP dropping the ARB/-GRNT line) each device that participated in the arbitration cycle will know if it won or lost the bus. If the device won the bus, it raises the -PREEMPT line.

During arbitration, HOLD is asserted, if not already active. When the 82C223 samples HLDA active, it enters the grant state. The winning arbiter (one with the highest priority) must drive its arbitration levels throughout the grant state. If no local arbiter is requesting the bus, the HOLD is not asserted and the system CPU receives the channel control.

Devices that want to perform multi-byte transfers must assert -BURST until the last byte is transferred. A burst cycle is terminated by the requesting device, after the programmed number of transfers or if another device asserts its -PREEMPT line. If burst transfer is interrupted by another device requesting channel access, the remaining bytes or words will be transferred when the bursting device gains control of the bus after participating in another arbitration cycle.

If the DMA transfer is completed, as indicated by the activation of terminal count, the channel is awarded to the next higher priority device or to the system processor.

The 82C223 supports a "Fairness" feature, which if enabled in an adapter, preempts the current bus master within a specified time. When the bursting device samples -PREEMPT active during its transfer, it should complete the current cycle and de-assert the -BURST output. It should not participate in any further arbitration cycles until it samples -PREMPT inactive.

If the bursting device continues to hold -BURST active after detecting the activation of the -PREEMPT signal, an error condition is assumed after 7.8 micro seconds, and an NMI is generated. When an NMI is generated, the arbitration register bit <6> and bit <5> (Bus Time Out indication) is set to a one and the ARB/-GNT is driven to the high state, forcing the bursting device to terminate the cycle. The NMI interrupt handler should clear this condition by writing a zero to bit <6> or by activating reset.

The arbitration mechanism can be disabled by writing a one at the arbitration register bit <6> at the I/O address 90 (hex). The arbitration period is 300 ns if the arbitration register bit <5> is set to zero; otherwise it is 600 nsec (Note: During read operation bit <5> gives the status of the Bus Time Out condition. During write cycles, this bit determines the duration of the arbitration cycle). The period may be longer if a refresh cycle occurs during the arbitration state or the HLDA signal, if required, does not become asserted in time. The arbitration register bit <7> controls the HOLD signal during the arbitration state.

3.0 DMA CONTROLLER

The 82C223 supports 8 DMA channels which generate the memory address and control signals to transfer information between peripheral and memory directly without requiring CPU intervention. Each DMA channel can be independently programmed for byte or word transfers.

The DMA channels have a 24 bit address register and a 16 bit transfer count register, allowing it to access up to 16 MBytes of memory and transfer blocks as large as 65536 words.

The DMA controller offers:

- Register/program level compatibility with the 8237 DMA controller in the "compatible mode."
- Direct interface to the processor status lines in the "program mode". In the Master mode, it generates address, status and control signals that emulate the timing of the 286 CPU.
- Eight independently programmable DMA channels that can perform either byte or word transfers.
- Unlike the PC/AT implementation which supports single cycle transfer, the 82C223 supports two cycle transfers, i.e. a read from a peripheral device followed by a write to a memory device and vice versa.
- Supports extended mode

3.1 DMA Operation

The 82C223 performs a two cycle transfer with a minimum cycle time of 200 ns for both I/O and memory accesses. This cycle can be extended by asserting -CHRDYRTN inactive. When transferring data between I/O peripherals and memory, data is first obtained from the source device and held in a temporary holding register. During the second cycle, data is transferred from the holding register to the target device. The 82C223 can be programmed not to generate I/O addresses during DMA transfers. When programmed to operate in this mode, the I/O addresses are forced to be all zeroes.

A local arbiter may be assigned a level that is in turn assigned to a particular DMA channel. If the arbiter requires the services of the DMA controller, it has to participate in the arbitration cycle and win the channel. If the channel is unmasked, the DMA channel is the bus controller carrying out the requested data transfer. On the other hand, if it is masked off, the bus master logic of the local arbiter must perform data transfers.

The 82C223 supports single transfers, burst transfers or perform read verification. In the single byte transfer mode, data is transferred on a byte-by-byte basis. In the burst transfer mode, data is transferred as long as the -BURST output is active and no terminal count is received. In the Read Verification mode, one byte is read from memory.

Upon reset, DMA channels 0 through 7 are assigned to the arbitration levels 0 through 7, respectively. The DMA channels 0 and 4 may be programmed to different arbitration levels through their 'Arbus' register.

3.2 DMA Cycles

The 82C223 DMA controller emulates the timing of a 10 MHz 80286 processor and connects directly to the processor status lines. In the program state, it receives programming information from the CPU controller. In the Master mode, it has three states (similar to the 286 CPU):

1. The idle state
2. The status state
3. The command state

3.3 Idle State

It is in the idle state, when after initialization, no DMA requests are received or following reset when it is in the program mode.

3.4 Status State

When the 82C223 receives a DMA request from an unmasked channel, it asserts HOLD to the CPU. Upon getting HLDA from the CPU, it asserts the appropriate status lines to perform the requested data transfer. This could be either a transfer from memory to a peripheral device, or a transfer of data from the peripheral to memory. In either case, data is first read from the source device and latched into a temporary register. A second cycle is performed to transfer data from the register to the target device.

3.5 Command State

It is during the command state, which is the cycle following the status state, that the 82C223 receives data from the selected device if it is a read operation, or transfers data from the temporary register to the target device during a write operation. This cycle can be extended by -CHRDYRTN to accommodate slower memory devices or peripherals.

A DMA bus cycle consists of one or two memory cycles and one I/O cycle, which are inseparable. A transfer may be 8 bit or 16 bit, but it must always be from memory to I/O or I/O to memory. No memory to memory transfers are supported. However, during a verify operation, only a memory read cycle is executed. 16 bit memory transfers at odd address boundaries are split into two consecutive 8 bit memory cycles by the 82C223. If a 16 bit I/O transfer occurs at an odd address boundary, the 82C223 will force the I/O address to be even (LA0 is forced to zero) and then performs one 16 bit transfer cycle. Each data transfer cycle is terminated by the synchronous -READY pulse asserted.

Either -LS1 for a read or -LS0 for a write becomes asserted at the beginning of a bus cycle. The LM/-IO is HIGH if it is a memory cycle, and it is low if an I/O cycle. When a multiple data transfer is required, the -BURST signal must be asserted by the winning arbiter using the DMA channel until the last transfer cycle, or until the -TC (Terminal Count) is pulsed.

Once the terminal count is reached, the channel is masked off. The -LBHE signal becomes asserted whenever the upper half of the data path is used. The DMA channel of interest must be programmed with its starting address, I/O address (if the I/O address generation option is selected), transfer count, transfer direction, and transfer size (either byte or word transfer) through the PC/AT compatible mode or the extended mode.

3.6 REFRESH

The 1.19 MHz clock input is divided by 18 internally to cause a refresh request every 15.1 usec. During the refresh cycle, the 82C223 drives the -PREMPTO signal for an arbitration cycle. Once the ARB/-GNT signal goes HIGH and the system CPU is in a hold state, the refresh cycle is completed with the ARB/-GNT signal in the ARB state (HIGH). Memory refresh can never be disabled after a reset. The refresh address is 11-bits wide and the refresh cycle is the same as a memory read cycle with the -RFSH signal asserted. The upper 13 address lines are unknown and the -LBHE is always HIGH.

3.7 LOCAL ARBITER

The 82C223 has a local arbiter with a level 2 priority for the system diskette controller, which asserts the DSKDREQ for a DMA service. It then drives the -PREMPTO signal for an arbitration cycle. Once the arbitration state is entered, the local arbiter participates in arbitration using the ARBO<3:0> lines. When the local arbiter wins, it asserts disk acknowledge -DSKDACK, at which point the DSKDREQ may be deactivated. If channel 2 is masked off, the DSKDREQ is simply ignored, and level 2 is available for another arbiter.

Symbol	Type	PLCC	PFP	Description
ARB/-GNT	O	23	14	When LOW, i.e in the "grant "state, this signal indicates that the winning arbiter is in control of the micro channel. When HIGH or in the "arbitration" state, an arbitration cycle is in progress and/or the arbitration has been masked off.
-PREEMPT	I	32	24	This input signal, if active, causes an arbitration cycle to occur. A requesting arbiter should stop driving this signal when it is granted control of the micro channel.
-PREMPTO	O	26	18	This signal is a "prempt" request, and is driven in the grant state, when an NMI is generated, or if the local arbiter for channel 2 (Diskette interface) requests channel access. This signal should be fed back to the -PREEMPT input pin through an open collector driver.
ARB0-ARB3	I	28 29 30 31	20 21 22 23	ARB <3:0> are driven by the arbiters requesting bus cotrol at the beginning of an arbitration cycle. After the arbitration has been settled and ARB/-GNT goes LOW, only the winning arbiter drives these lines until the next arbitration cycle occurs.

Symbol	Type	PLCC	PFP	Description
ARBO0-ARBO3	O	17 18 19 20	8 9 10 11	These signals are driven by the local arbiter inside the 82C233. These lines should be fed back to the ARB <3:0> inputs through open collector drivers.
-TCO	O	24	15	This signal generates a short pulse during an I/O Read or and I/O Write cycle to indicate that the terminal count of the current DMA channel has been reached.
-BURST	I	27	19	This signal must be asserted (LOW) if the bus owner (the winning Arbiter) wants to carry out more than one bus cycle.
DSKDREQ	I	8	96	This is a special channel 2 request input and is normally used by the system diskette controller.
-DSKDACK	O	7	95	Acknowledges that the diskette request on channel 2 has been granted, and the DMA channel is now in control of the micro channel. This is valid throughout the entire grant state.
-HDDISK	O	11	99	This output is driven low for high density diskette drives. It is high for all other accesses.
HOLD	O	6	94	This is the hold request for the system CPU. The signal becomes active during the arbitration state when a refresh, a DMA channel or a MASTER requests for the micro channel.

Symbol	Type	PLCC	PFP	Description
HLDA	I	9	97	This is the acknowledgement from the system CPU to the HOLD request.
LM/-IO	B	5	93	When one of the status signals (-LS1 or -LS0) becomes active, an I/O cycle is starting if LM/-IO is LOW, or a memory cycle if it is high.
-LS1 -LS0	B B	81 80	83 82	The status signals (-LS0 and -LS1), indicate the beginning of a valid bus cycle. In both the DMA slave and master modes, only one status signal should be active to be a valid cycle for the 82C223. When -LS0 is LOW, it is a Write cycle and when -LS1 is LOW, it is a Read cycle.
-LBHE	O	51	47	This signal, normally HIGH, becomes actively driven when the 82C223 enters master mode. When LOW, the upper half of the 16 bit data bus is used. When HIGH the upper half is not used for data transfers.
-NMI	B	10	98	This is an open drain bi-directional signal which allows the wire OR'ing of NMI sources. When a bus time-out is detected by the 82C223, this signal is driven LOW. When the signal is detected LOW at the pin, the channel arbitration is disabled, i.e., the ARB/-G signal is driven HIGH and remains HIGH until unmasked by software.

Symbol	Type	PLCC	PFP	Description
-BTO	O	13	3	This signal is asserted when a bus time-out is detected by the 82C223.
INTR	I	12	1	Interrupt request input. Allows 82C223 to Pre-empt a burst DMA when a CPU interrupt is pending.
-READY	I	79	81	This is an input synchronous to the 20MHz clock used to terminate the current DMA bus cycle.
-CMD	I	14	4	This signal is used in both master and slave modes. In master mode, the signal should be synchronized with the 20 MHz clock, and during a DMA Read cycle its rising edge is used to latch the data in the 82C223. In slave mode, the rising edge is used to terminate the 82C223's internal operation.
DMASRDY	O	16	7	This signal is normally HIGH and goes LOW when the 82C223 is accessed until it is ready to finish the cycle.
-DMADS16	O	15	5	This is asserted whenever the address on the bus falls within the 82C223 I/O address range.
1.19MHz	I	21	12	This is the clock source for the internal refresh request generation which occurs at 15usec intervals.
-RFSH	O	25	17	This is asserted LOW, whenever a refresh cycle is in progress.

Symbol	Type	PLCC	PFP	Description
LD0	B	33	26	LD<15:0> is the 16 bit data bus used during master and slave modes. Even address byte data must use the lower half of the bus and odd address byte data must use the upper half of the bus.
LD1	B	35	28	
LD2	B	37	30	
LD3	B	39	32	
LD4	B	41	36	
LD5	B	45	40	
LD6	B	47	42	
LD7	B	49	45	
LD8	B	34	27	
LD9	B	36	29	
LD10	B	38	31	
LD11	B	40	34	
LD12	B	44	39	
LD13	B	46	41	
LD14	B	48	44	
LD15	B	50	46	
LA0	B	52	48	LA <15:0> are bi-directional signals. If a valid address is within the 82C223s I/O space, it responds to the cycle In the master mode, these are driven by the 82C223.
LA1	B	53	49	
LA2	B	54	51	
LA3	B	55	52	
LA4	B	56	54	
LA5	B	57	55	
LA6	B	58	56	
LA7	B	59	58	
LA8	B	60	59	
LA9	B	61	60	
LA10	B	62	61	
LA11	B	65	64	
LA12	B	66	65	
LA13	B	67	66	
LA14	B	68	67	
LA15	B	69	68	
LA16	O	70	70	LA<23:16> are tri-stated outputs, driven only during a DMA master cycle by the 82C223.
LA17	O	71	71	
LA18	O	72	72	
LA19	O	73	73	
LA20	O	74	74	
LA21	O	76	77	
LA22	O	77	79	
LA23	O	78	80	

Symbol	Type	PLCC	PFP	Description
-MASTERO	O	82	85	This signal is asserted whenever both HOLD and HLDA are active, and it is not a refresh or DMA cycle.
RESET4	I	4	92	This is the reset input.
-CDSPEN	O	3	90	This signal becomes asserted whenever the address on the bus falls in the I/O address range 100 hex through 107 hex.
CLKA	I	2	89	40 MHz input clock with 50% duty cycle.
CLKB	O	83	86	20 MHz output clock with 50% duty cycle.

POWER SUPPLIES

Symbol	PLCC	PFP	Description
VDD	42 84 63	25 50 75 100	Power Supply (+5V)
VSS	1 22 43 64	13 38 63 76 88	Ground
NC		2,6,16 33,35, 37,43 53,57 62,69 78,84, 87,91	Not Connected

82C233 REGISTER DESCRIPTIONS

Arbitration Register

I/O Address: 90H

Bit	Access	Description
7	Read/Write	When set to "1", no HOLD is asserted to the CPU during an arbitration cycle. When the CPU is not the bus owner, and this bit is set to "0", then HOLD is maintained until the end of the arbitration cycle. Default = 0
6	Read/Write	Setting this bit to a 1, masks off the arbitration mechanism and drives the ARB/-GNT signal HIGH. This bit is also set to a 1 if an NMI occurs. ARB/-GNT can be cleared by writing a 0 to this bit. Default = 1
5	Read/Write	During write accesses, setting this bit to a 1, extends the ARB/-GNT signal from a 300 ns minimum cycle time to a 600 ns minimum cycle time. During read operations, if this bit is set, a bus time out has occurred (This bit is set internally by the bus time out logic). It can be cleared by writing a 0 to bit <6> above, or by a reset. Default = 0
4	Write	Should be set to zero
3-0	Read	These are read only bits which are used following a bus time-out condition during diagnostics, and represent the arbitration level of the winning arbiter at the last grant state. Always write these bits as 0.

4.0 COMPATIBLE MODE

In the compatible mode, channels 0 through 3 are configured as 8 bit DMA channels, and the remaining channels are configured as 16 bit channels. The I/O address is fixed to the value of 0000 (hex).

Registers shared by the DMA channels are described below:

Status Register(Read Only)

The status of the DMA channels can be determined by reading the Status Register. Information is available to determine if a channel has reached the terminal count and whether an external service request is pending. Bits <3:0> are cleared by RESET or each time the status register is read. Bits <7:4> are set every time the corresponding channel has controlled the bus and cleared by RESET. These bits are not affected by the state of the Mask Register bits. All bits are cleared following a reset condition or if the status register is read.

Bits	Function
7	Channel 3 or 7 Request
6	Channel 2 or 6 Request
5	Channel 1 or 5 Request
4	Channel 0 or 4 Request
3	TC on Channel 3 or 7
2	TC on Channel 2 or 6
1	TC on Channel 1 or 5
0	TC on Channel 0 or 4

Mask Register (Write Only)

Each channel has an associated mask bit, which is used to inhibit external DMA requests from generating transfer cycles. Each mask bit can be programmed to be set or cleared. Following reset, all mask bits are set. A RESET or Clear Mask Register command clears all the mask bits.

Bits	Value	Function
7-3		Must be zero
2	0	To clear mask bit
	1	To set mask bit
1,0		These two bits select the specific mask bit which is to be set or reset.
	00	Selects channel 0 or 4
	01	Selects channel 1 or 5
	10	Selects channel 2 or 6
	11	Selects channel 3 or 7

Write Mask (Write Only)

This command sets or resets all the mask bits.

Bits	Value	Function
7-4		Must be 0.
3	0	To unmask channel 3 or channel 7
	1	To mask channel 3 or channel 7
2	0	To unmask channel 2 or channel 6
	1	To mask channel 2 or channel 6
1	0	To unmask channel 1 or channel 5
	1	To mask channel 1 or channel 5
0	0	To unmask channel 0 or channel 4
	1	To mask channel 0 or channel 4

Master Clear (Write Only)

This command has the same effect as a hardware RESET. A write into this register clears the status register and masks off the channel.

Clear Mask (Write Only)

A write into this register unmasks all the channels in the group.

Clear Byte Pointer (Write Only)

This command is normally executed prior to reading from or writing to the address or word count registers. This initializes the flip flop to point to the low byte of the register and allows the CPU to read or write to the register bytes in the correct sequence.

Memory Address (Read/Write)

This register is logically 2 bytes long. After the byte pointer has been cleared, each byte can be written in or read out in succession from the lower byte to the upper byte at the same byte register location.

Upon reset the contents of this register are unknown.

Transfer Count (Read/Write)

The transfer count is 2 bytes long. After the byte pointer has been cleared, each byte can be written in or read out in succession from the lower byte to the upper byte at the same byte register location.

Upon reset the contents of this register are unknown.

Page Table (Read/Write)

This is the most significant byte of the 24 bit memory address.

Upon reset the contents of this register are unknown.

Mode (Write Only)

Each channel has a mode register associated with it. All the Mode Registers reside at the same I/O location. Bit 0 and 1 of the Mode Register determine which channels' Mode Register gets written to. The remaining six bits control the mode of the selected channel.

Bits	Value	Function
7,6		Reserved. Must be 0
5		Reserved. Must be 0
4		Reserved. Must be 0
3,2	00 01 10 11	For Verify Operation For Write Operation For Read Operation Reserved
1,0	00 01 10 11	Selects channel 0 or 4 Selects channel 1 or 5 Selects channel 2 or 6 Selects channel 3 or 7

Upon reset the contents of this register are unknown.

5.0 EXTENDED MODE

The extended mode uses two byte locations, called the Extended Address register (18 hex) and the Extended Data register (1A hex), to program all the DMA and CACP registers. Only the features that are different from the compatible mode are described in detail in the following section.

When programming in extended mode, operations that require data transfer must set up the Extended Address register appropriately and then access the Extended Data register for actual data transfer. Other operations need to access only the Extended Address register for what is called direct execution.

The extended address register uses the lower nibble to specify which channel is used. The upper nibble specifies the operation to be performed. Whenever the register is accessed, the byte pointer is cleared.

Bits <7:4> hex	**Register/Bits Accessed**
0	I/O Address ,Register
1	Reserved
2	Memory Address Register(Write Only)
3	Current Memory Address (Read Only)
4	Transfer Count Register(Write Only)
5	Current Transfer Count (Read Only)
6	Status Register (Read Only)
7	Extended Mode
8	Arbus Register
9	Set Single Mask Bit (direct execution)
A	Reset Single Mask Bit (direct execution)
B	Reserved
C	Reserved
D	Master Clear (direct execution)
E	Reserved
F	Reserved

Upon reset the contents of this register is unknown.

Extended Mode (Read/Write)

Through the extended mode register (one per DMA channel), in addition to the features offered through the compatible mode, any channel can be programmed to perform 8 bit or 16 bit transfers with or without programmed I/O address.

Bits	Value	Function
7	0	Reserved
6	0 1	For 8 bit transfer For 16 bit transfer
5	0	Reserved
4	0	Reserved
3	0 1	For Read Memory For Write Memory
2	0 1	For Verify For Data Transfer
1	0	Reserved
0	0 1	For I/O address = 0000 For Programmed I/O Address

I/O Address (Read/Write)

The I/O address must be programmed when the Extended Mode register bit <0> is set to one.

Upon reset the contents of this register are unknown.

Status (Read Only)

Once the Extend Address register is set to point to the Status Register, the two status registers for channel 0/channel 3 and channel 4/channel 7 can be read successively.

Arbus (Read/(Write)

This is a 4 bit wide register and uses the lower nibble. The upper nibble reflects the contents of the Arbus register for Channel 4. The channel portion of the Extended Address register must be set within the range 0 through 7. This register can be written to only if the channel is either 0 or 4. If read, the register returns the channel number for the channels 1, 2, 3, 5, 6, & 7. For channels 0 & 4, the register returns whatever value the register was programmed with previously.

Master Clear (Write Only)

This masks off all the DMA channels.

REGISTER SUMMARY

ADDRESS	REGISTER
0000	Channel 0 Memory Address (LOW, MIDDLE)
0001	Channel 0 Transfer Count
0002	Channel 1 Memory Address (LOW, MIDDLE)
0003	Channel 1 Transfer Count
0004	Channel 2 Memory Address (LOW, MIDDLE)
0005	Channel 2 Transfer Count
0006	Channel 3 Memory Address (LOW, MIDDLE)
0007	Channel 3 Transfer Count
0008	Channel<0:3> Status Register
000A	Channel<0:3> Mask Register
000B	Channel<0:3> Mode Register
000C	Clear Byte Pointer
000D	Channel<0:3> Master Clear
000E	Channel<0:3> Clear Mask
000F	Channel<0:3> Write Mask
0018	Extended Address
001A	Extended Data
0081	Channel 2 Memory Address (HIGH)
0082	Channel 3 Memory Address (HIGH)
0083	Channel 1 Memory Address (HIGH)
0087	Channel 0 Memory Address (HIGH)
0089	Channel 6 Memory Address (HIGH)
008A	Channel 7 Memory Address (HIGH)
008B	Channel 5 Memory Address (HIGH)

ADDRESS	REGISTER
008F	Channel 4 Memory Address (HIGH)
0090	Arbitration
00C0	Channel 4 Memory Address (LOW, MIDDLE)
00C2	Channel 4 Transfer Count
00C4	Channel 5 Memory Address (LOW, MIDDLE)
00C6	Channel 5 Transfer Count
00C8	Channel 6 Memory Address (LOW, MIDDLE)
00CA	Channel 6 Transfer Count
00CC	Channel 7 Memory Address (LOW, MIDDLE)
00CE	Channel 7 Transfer Count
00D0	Channel <4:7> Status Register
00D4	Channel <4:7> Mask Register
00D6	Channel <4:7> Mode Register
00D8	Clear Byte Pointer
00DA	Channel <4:7> Master Clear
00DC	Channel <4:7> Clear Mask
00DE	Channel <4:7> Write Mask

82C233 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Voltage	VCC		7.0	V
Input Voltage	VIN	-0.5	VCC + 0.5	V
Storage Temperature	TSTG	-40	125°	C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions described under operating conditions.

82C223 DC Characteristics

Parameter	Symbol	Min	Max	Units
Input Low Voltage	V_{IL}	-0.5	0.8	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V
Output Low Voltage	V_{OL}		0.45	V (Note 1)
Output High Voltage	V_{OH}	2.4		V (Note 2)
Input Leakage Current	I_{IL}	-10	10	uA(Note 2)
Output Float leakage Current	I_{OZ1}	-10	10	uA(Note 3)
Power Supply Current				mA

Note 1: IOL = 4mA and IOH = -4mA for all output and I/O pins.

Note 2: 0 < Vin < VCC

Note 3: 0.45 < Vout < VCC

(T_A = 0°C to 70°C, VCC = 4.75V to 5.25V, A.C. load = 80pf)

SLAVE MODE TIMING (I/O Read/Write to the 82C223)	**Min**	**Max**	**Units**	**Notes**
t300 Address setup to status active	5		ns	
t301 -DMADS16 active from Address Valid	5	30	ns	
t303 Status width	50	300	ns	
t304 Status to DMASRDY inactive		30	ns	
t305 Read data set up to DMASRDY	0		ns	
t306 Read data hold from -CMD inactive	0	25	ns	
t307 Write data setup time to -CMD active	0		ns	
t308 Write data hold from -CMD inactive	0		ns	

ARBITRATION TIMING	**Min**	**Max**	**Units**	**Notes**
t320 Arbitration pulse width (300ns nominal)	290		ns	
t321 Arbitration pulse width (600ns nominal)	590		ns	
t322 ARB (0:3) turn-on from ARB/GNT- high		50	ns	
t323 ARB (0:3) stable before ARB/GNT- low	10		ns	
t324 Last -CMD or -BURST to ARB/GNT- high	50		ns	

MASTER MODE TIMING (I/O or Memory Read/ Write controlled by the 82C223)	**Min**	**Max**	**Units**	**Notes**
t330 Address, M/-IO valid delay	5	30	ns	
t331 Status active delay	2	15	ns	
t332 Status inactive delay	2	15	ns	
t333 -LBHE active from clock	2	12	ns	

MASTER MODE TIMING (continued)	Min	Max	Units	Notes
t334 -LBHE turn off from clock	2	12	ns	
t335 -READY set up to clock	20		ns	
t336 -READY hold from clock	8		ns	
t337 Read data set up to clock	20		ns	
t338 Read data hold from clock	15		ns	
t339 Write data delay from clock	0	25	ns	
t340 Write data hold from clock	50		ns	
t341 -TC active delay from clock	0	12	ns	
t342 -TC active hold from clock	30		ns	

REFRESH TIMING	Min	Max	Units	Notes
t350 Address, M/-IO, active delay	5	30	ns	
t351 -RFSH active delay	5	30	ns	
t352 -RFSH inactive delay	5	30	ns	
t353 Status active delay	2	15	ns	
t354 Status inactive delay	2	15	ns	
t355 -LBHE active from clock	5	20	ns	
t356 -LBHE turn off from clock	5	20	ns	
t357 -READY set up to clock	20		ns	
t358 -READY hold from clock	30		ns	
t359 ARB/-G to grant from clock	100		ns	

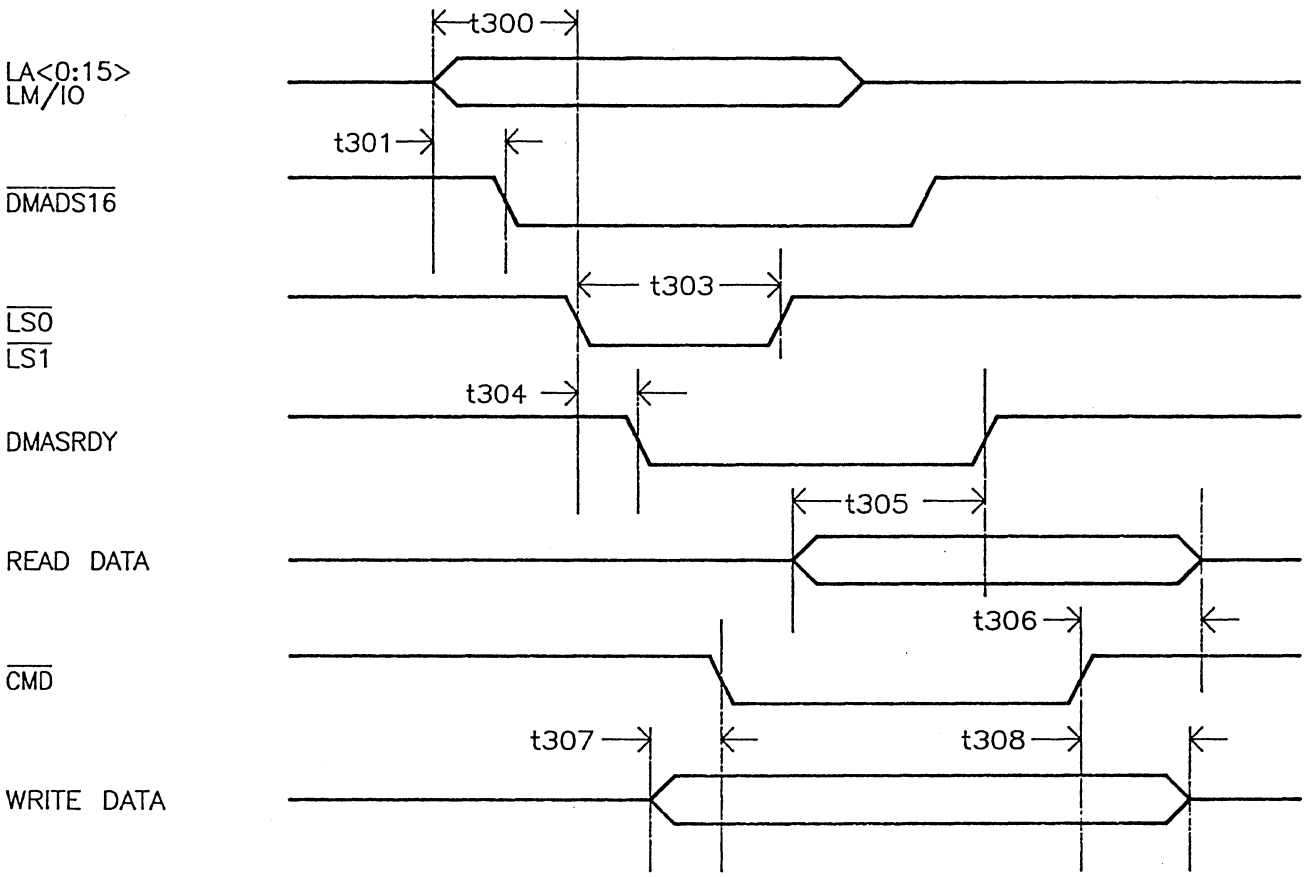


Figure 8.1 SLAVE MODE TIMING

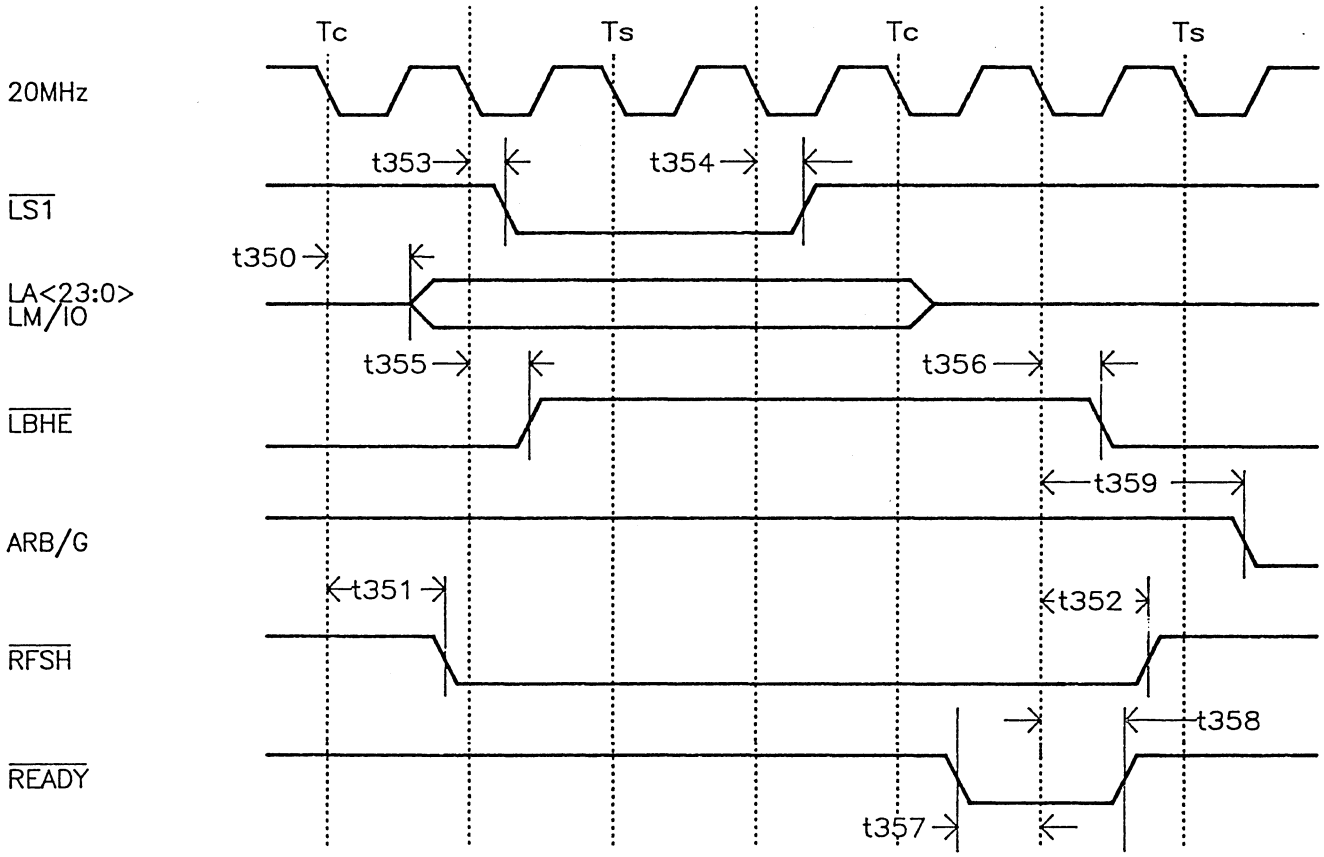


Figure 8.2 REFRESH TIMING

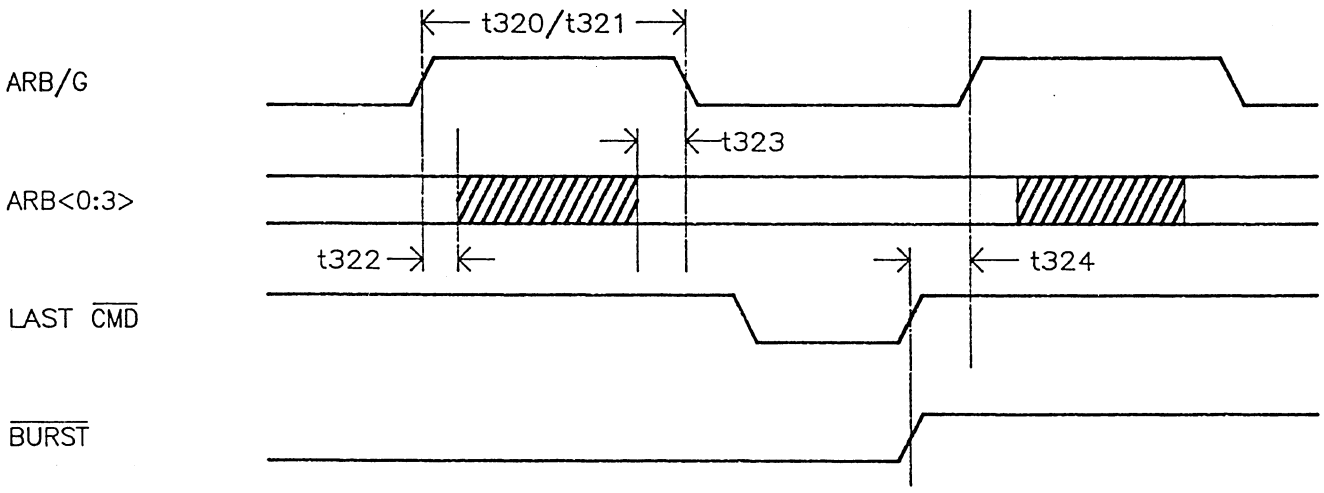


Figure 8.3 ARBITRATION TIMING

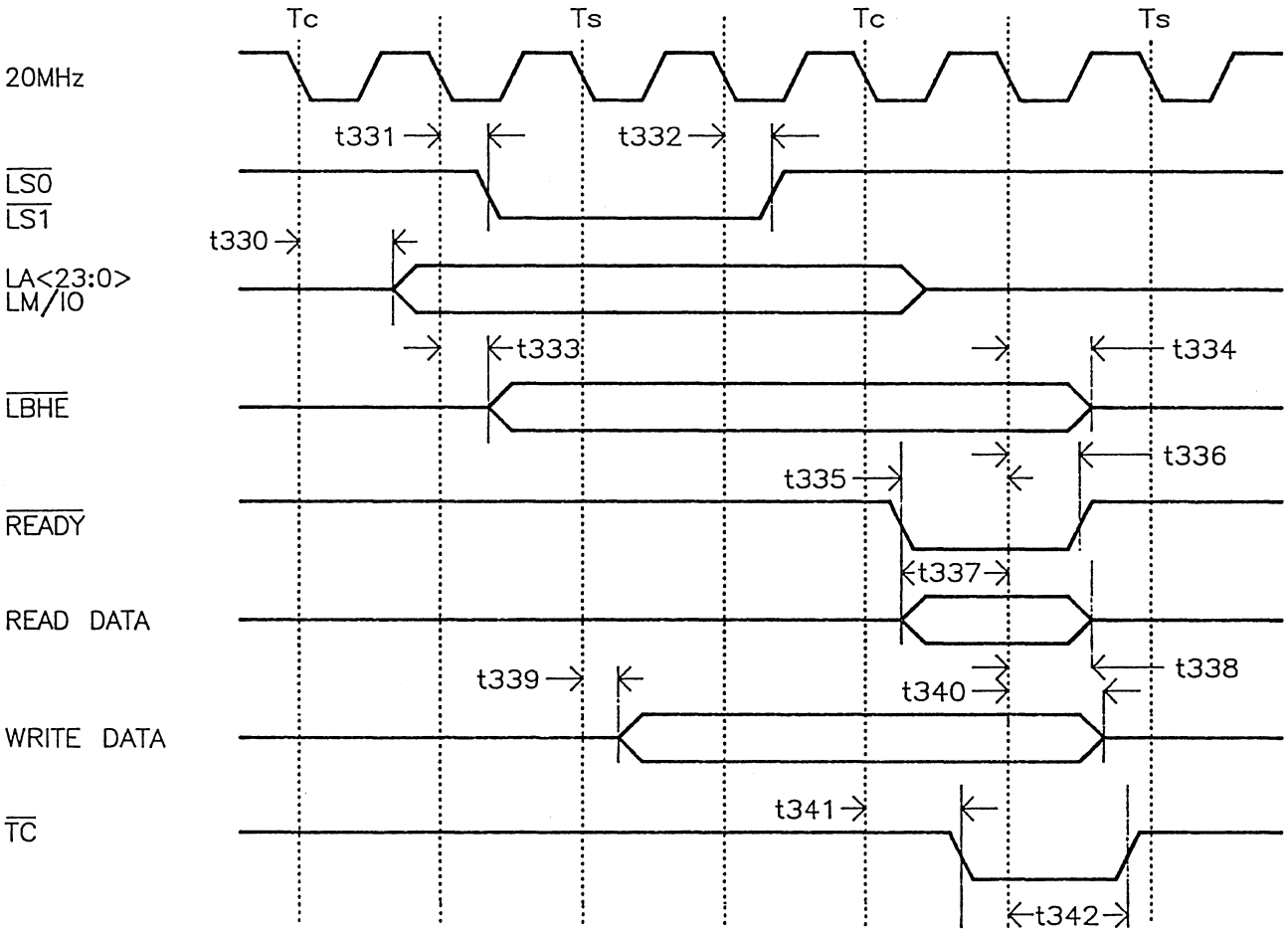


Figure 8.4 MASTER MODE

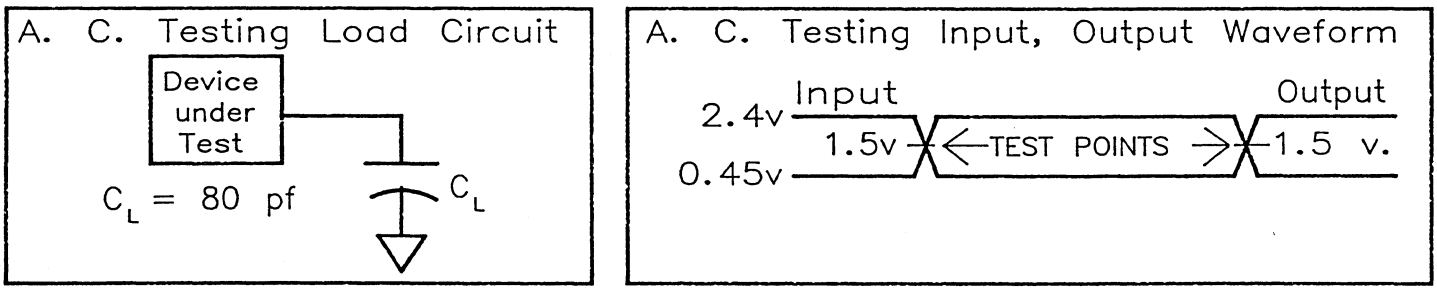
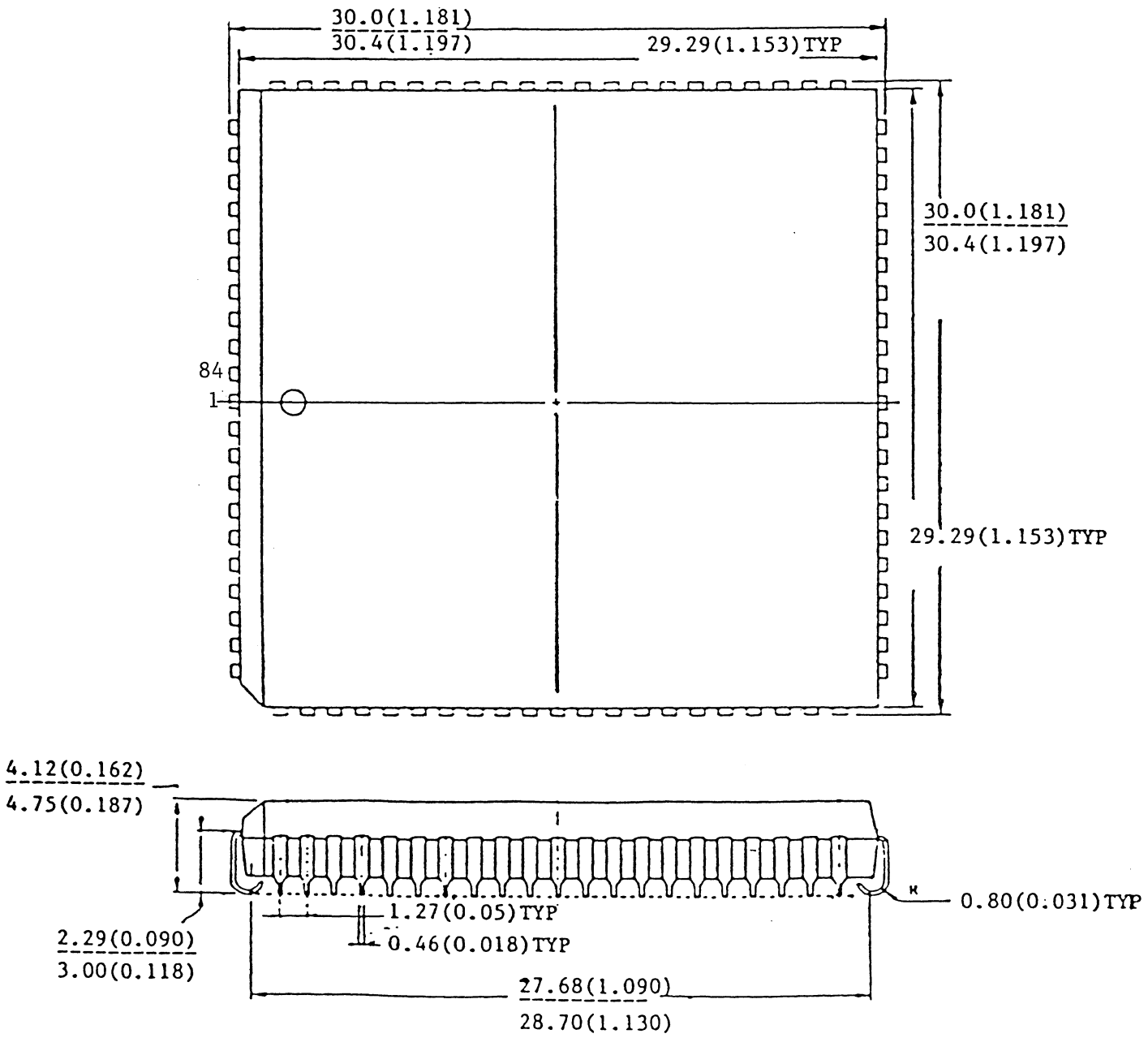

A. C. Testing Load Circuit
Device under Test
C_L = 80 pf
C_L
A. C. Testing Input, Output Waveform
Input
Output
2.4v
1.5v
TEST POINTS
1.5 v.
0.45v

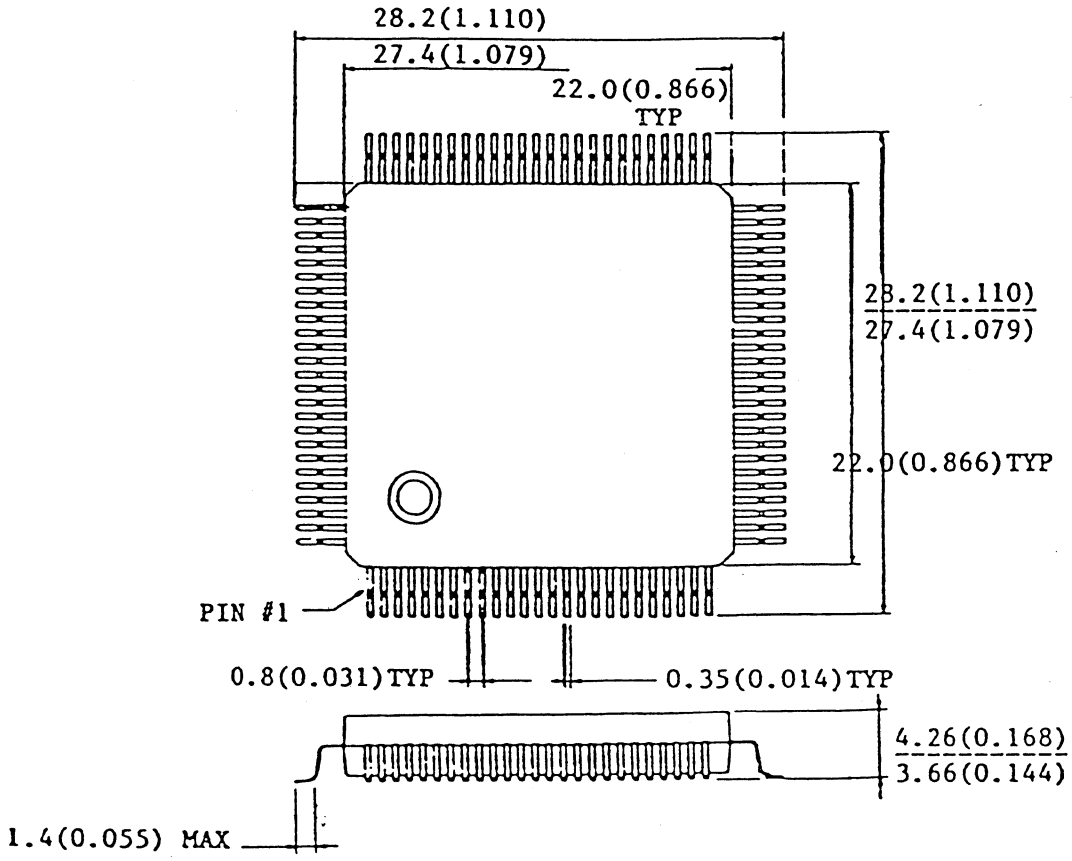
Figure 8.5

84-Pin Plastic Leaded Chip Carrier (PLCC)
Socket = AMP 821573-1 or Equivalent



Dimensions: mm (in)

100-Pin Plastic Flat Pack (Square) (PFP)



FEATURES

- Two Intel 8259 compatible interrupt controllers
- Intel 8254 Compatible Timer
- Watchdog Timer
- Motorola 146818 Compatible real time clock
- 114 bytes of CMOS battery Backed RAM
- 8 bit Bi-directional Parallel Port
- System Control Registers
- Card Setup Signals
- Fabricated in 1.5 micron CMOS Technology
- Available in 84 pin PLCC or 100 pin PFP packages

The 82C226 along with the CHIPS/250 or the CHIPS/280 CHIPSet, provides a highly integrated, high performance solution for PS/2 family compatible implementation.

The 82C226 is fabricated using CMOS technology and is available in 84 pin PLCC or 100 pin PFP packages.

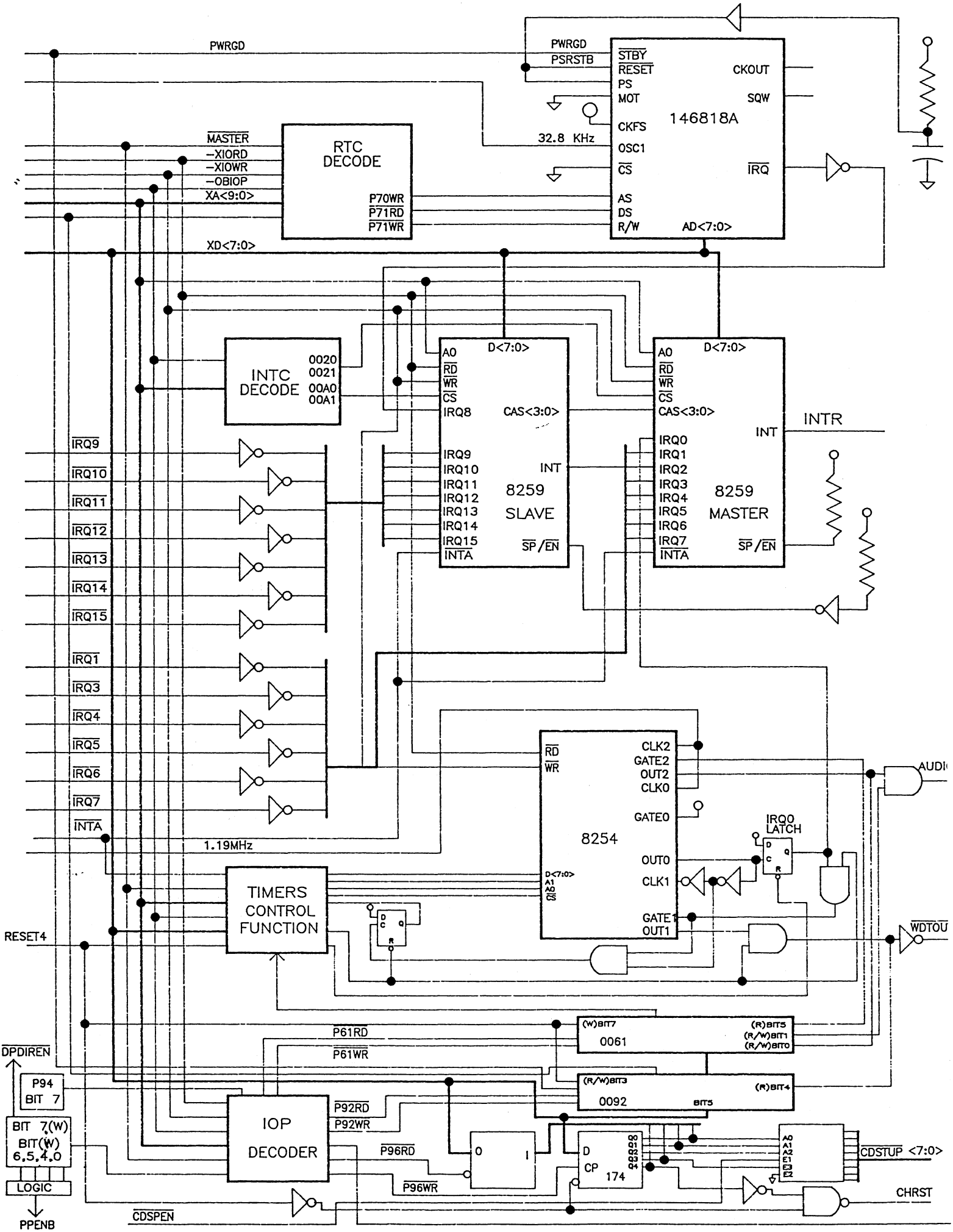
1.0 OVERVIEW

The 82C226 is an LSI implememtation of the standard peripherals required to implement a PS/2 compatible system board. This device contains the following:

- One MC 146818 compatible Real Time Clock
- Two 8259 compatible Interrupt Controllers
- One 8254 compatible Timer/Counter
- Three system control registers
- One parallel port
- Programmable I/O decode signals to be used in a CHIPS250 integrated system.

Figure 9-1 shows the configuration of the System Peripheral Chip 280 (SPC). The SPC's Function Control Unit provides control signals to meet all the related features found in PS/2 systems:

- Security lock function
- Level sensitive interrupt
- Watch dog timer function


PWRGD
PWRGD
PSRSTB
STBY
RESET
PS
MOT
CKFS
OSC1
CS
AS
DS
R/W
AD<7:0>
CKOUT
SQW
IRQ
146818A
32.8 KHz
MASTER
-XIORD
-XIOWR
-OBIOP
XA<9:0>
RTC
DECODE
P70WR
P71RD
P71WR
XD<7:0>
INTC
DECODE
0020
0021
00A0
00A1
D<7:0>
A0
RD
WR
CS
IRQ8
CAS<3:0>
IRQ9
IRQ10
IRQ11
IRQ12
IRQ13
IRQ14
IRQ15
INTA
INT
8259
SLAVE
SP/EN
IRQ0
IRQ1
IRQ2
IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
8259
MASTER
INTR
IRQ9
IRQ10
IRQ11
IRQ12
IRQ13
IRQ14
IRQ15
IRQ1
IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
INTA
1.19MHz
8254
CLK2
GATE2
OUT2
CLK0
GATE0
OUT0
CLK1
GATE1
OUT1
IRQ0
LATCH
AUDI
TIMERS
CONTROL
FUNCTION
RESET4
WDTOU
P61RD
P61WR
(W)BIT7
0061
(R)BIT5
(R/W)BIT1
(R/W)BIT0
DPDIREN
P94
BIT 7
(R/W)BIT3
0092
BIT5
(R)BIT4
BIT 7(W)
BIT(W)
6,5,4,0
LOGIC
PPENB
IOP
DECODER
P92RD
P92WR
P96RD
P96WR
0
1
D
CP
174
CDSTUP <7:0>
CHRST
CDSPEN

The 82C226 supports sixteen sources of interrupts. These channels are partitioned into two cascaded controllers (INTC1,INTC2) with each supporting eight interrupt requests.

The 82C226 provides three timer/counters: channel 0, channel 1 and channel 2. Channel 0 and channel 2 are driven from the 1.19 MHz clock input. Counter 0 is connected to IRQ0 of Interrupt Controller 1. Counter 1 may be programmed to generate pulses or square waves for use by external devices. In a CHIPS/250 and CHIPS/280 implementation, this is used for tone generation for the speaker. The third channel, Channel 2 is used to monitor correct system operation. It monitors IRQ0 to determine if it is being serviced.

A Real Time Clock is included in the 82C226 for maintaining the time and date. This subsystem also contains 128 bytes of non volatile memory. The clock calender and the RAM are kept active when the system is powered down, by connecting this sub-system to an external battery.

The 82C226 additionally includes a bi-directional parallel port that allows attachment of various devices that transfer 8 bits of parallel data at standard TTL levels. The parallel port is designed to be compatible with the parallel port implementation of the PC/AT. Additionally, it can be programmed to support bi-directional input output functions.

2.0 REAL TIME CLOCK

2.1 Functional Description

This section of the SPC combines a complete time-of-day clock with alarm and one hundred year calendar, a programmable periodic interrupt and 128 bytes of nonvolatile RAM. The internal clock circuitry uses 14 bytes of this memory. Provisions are made to enable the device to operate in a low power (battery back-up) mode to protect the contents of the RAM and clock during system power down. The RESET1- input, when active (low), puts the SPC in low-power mode.

2.2 Register Access

Reading or writing to the 128 locations in the Real Time Clock is accomplished by performing an output to port 070H with the output data (XD0-6) equal to the Index Address of the location you wish to access. The address will be latched into the Index Address Register on the rising edge of -IOWR. The Index Address Register is then used as a pointer to the specific byte in the Real Time Clock, which may be read or written by asserting -XIORD or -XIOWR with an address on the XA<9:0> inputs of 071H.

When performing I/O operations to the Real Time Clock addresses, interrupts should be inhibited to avoid having interrupt routines change the address register before data is read or written.

The following steps are required to access the Real Time Clock:

1. Out to port hex 070 with the RTC address that will be accessed. Bits <6:0> determine which of the 128 bytes is to be accessed.

2. An In or Out operation from/to port 0071 should be performed to access data from the RTC.

Note: The NMI mask bit resides at port hex 070, Bit 7.

The -MASTER signal is a status from DMA controller indicating that the current bus owner is an external intelligent controller. When -MASTER is active, the decode unit inhibits accesses to the RTC internal registers. Additionally, the RTC decode unit monitors the SECLOCK (Security Lock) signal (System Control Register A, bit 3). When SECLOCK is sampled active, it disables accesses to the secured area, 38-3F hex, inside the RTC. The secured area is used to store the user's password in the PS/2 system. Note that only locations 38-3F hex are prevented from being accessed if SECLOCK is active.

2.3 Address Map

Table 9-1 illustrates the internal register/RAM organization of the Real Time Clock. The 128 addressable locations are divided into 10 bytes which normally contain the time, calendar and alarm data, four control and status bytes and 114 general purpose RAM bytes. All 128 bytes are readable by the CPU. The CPU may also write to all locations except Registers C, D, Bit 7 of Register A and Bit 7 of the Seconds (00 hex) Byte which is always 0.

Table 9-1 Address Map for Real Time Clock

Index	Function
00	Seconds
01	Seconds Alarm
02	Minutes
03	Minutes Alarm
04	Hours
05	Hours Alarm
06	Day of Week
07	Date of Month
08	Month
09	Year
0A	Register A
0B	Register B
0C	Register C
0D	Register D
0E-7F	User RAM

2.4 Time Calendar and Alarm Bytes

The CPU can obtain the time and calendar information by reading the appropriate locations in the Real Time Clock. Initialization of the time, calendar and alarm information is accomplished by writing to these locations. Information is stored in these locations in binary-coded decimal (BCD) format.

Before initialization of the internal registers can be performed, the SET bit in Register B should be set to a "1" to prevent Real Time Clock updates from occurring. The CPU then initializes the first 10 locations in BCD format.

Table 9-2

Index Register Address	Function	BCD Range
0	Seconds	00-59
1	Seconds Alarm	00-59
2	Minutes	00-59
3	Minutes Alarm Hours (12 hour mode)	00-59 01-12 (AM) 81-92 (PM)
4	Hours (24 hour mode) Hours Alarm (12 hour mode)	00-23 01-12 (AM) 81-92 (PM)
5	Hours Alarm (24 hour mode)	00-23
6	Day of Week	01-07
7	Day of Month	01-31
8	Month	01-12
9	Year	00-99

Table 9-2 above shows the format for the ten clock, calendar and alarm locations. The 24/12 bit in Register B determines whether the hour locations will be updated using a 1-12 or 0-23 format. After initialization the 24/12 bit cannot be changed without re-initializing the hour locations. In 12 hour format the high order bit of the hours byte in both the time and alarm bytes will indicate PM when it is a "1".

During updates, which occur once per second, the 10 bytes of time, calendar and alarm information are unavailable to be read or written by the CPU for a period of 2ms. These 10 locations cannot be written during this time. Information read while the Real Time Clock is performing an update will be undefined. The Update Cycle section shows how to avoid Update Cycle/CPU contention problems.

The alarm bytes can be programmed to generate an interrupt at a specific time or they can be programmed to generate a periodic interrupt. To generate an interrupt at a specific time, the user need only program the time that the interrupt is to occur into the 3 alarm bytes. Alternately, a periodic interrupt can be generated by setting the high order two bits in an alarm register to a "1", which turns that byte into a "don't care". For instance, an interrupt can be generated every hour by programming a C0H into Register 5, or an interrupt can be generated once a second by programming the same value into all three alarm registers.

2.5 Static RAM

The 114 bytes of RAM from Index Address 0EH to 7FH are not affected by the Real Time Clock. These bytes are accessible during the update cycle and may be used for whatever the designer wishes. Typical applications will use this as nonvolatile storage for configuration and calibration parameters since this device is normally battery powered when the system in turned off.

2.6 Control and Status Registers

The 82C226 contains four registers (A,B,C and D) used to control the operation and monitor the status of the Real Time Clock. These registers are located at Index Address 0AH-0DH and are accessible by the CPU at all times.

Register A (0AH)

(Read/Write register except UIP)

msb lsb

b7	b6	b5	b4	b3	b2	b1	b0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP Update in progress flag is a status bit used to indicate when an update cycle is about to take place. A "1" indicates that an update cycle is taking place or is imminent. UIP will go active (High) 244us prior to the start of an update cycle and will remain active for an additional 2ms while the update is taking place. The UIP bit is read only and is not affected by Reset. Writing a "1" to the SET bit in Register B will clear the UIP status bit.

DV2-DV0 These three bits are used to control the Divider/Prescaler on the Real Time Clock. While the 82C226 can operate at frequencies higher than 32.768 Khz, this is not recommended for battery powered operation due to the increased power consumption at these higher frequencies. These bits are not affected by reset.

Register A (0AH) (continued)

DV2	DV1	DV0	OSCI Freq.	Mode
0	0	0	4.194304 MHz	Operate
0	0	1	1.048576 MHz	Operate
0	1	0	32.768 Khz	Operate
1	1	X	Reset Divider	Options

Divider Options

RS3-RS0 These four bits control the Periodic Interrupt rate. The Periodic interrupt is derived from the Divider/Prescaler in the Real Time Clock and is separate from the Alarm Interrupt. Both the alarm and periodic interrupts do however, use the same interrupt channel in the Interrupt Controller. Use of the Periodic Interrupt allows the generation of interrupts at rates higher than once per second. Below are the interrupt rates for which the Real Time Clock can be programmed.

Rate Selection				Time Base (OSCI Input)	
RS3	RS2	RS1	RS0	4.194304 MHz 1.048576 MHz	32.768 Khz
0	0	0	0	None	None
0	0	0	1	30.517 us	3.90526 ms
0	0	1	0	61.035 us	7.8125 ms
0	0	1	1	122.070 us	122.070 us
0	1	0	0	244.141 us	244.141 us
0	1	0	1	488.281 us	488.281 us
0	1	1	0	976.562 us	976.562 us
0	1	1	1	1.953125 ms	1.953125 ms
1	0	0	0	3.90625 ms	3.90625 ms
1	0	0	1	7.8125 ms	7.8125 ms
1	0	1	0	15.625 ms	15.625 ms
1	0	1	1	31.25 ms	31.25 ms
1	1	0	0	62.5 ms	62.5 ms
1	1	0	1	125 ms	125 ms
1	1	1	0	250 ms	250 ms
1	1	1	1	500 ms	500 ms

Note: As shown above, the periodic interrupt rate is independent of time base when RS3-0 = 0011 or higher (assuming DV2-0 are correctly set to match the actual OSCI input frequency.)

Register B (0BH)

(Read/Write Register)

msb lsb

b7	b6	b5	b4	b3	b2	b1	b0
SET	PIE	AIE	UIE	0	0	24/12	DSE

SET Writing a "0" to this bit enables the Update Cycle and allows the Real Time Clock to function normally. When set to a "1" the Update Cycle is inhibited and any cycle in progress is aborted. The SET bit is not affected by reset.

PIE The Periodic Interrupt Enable Bit controls the generation of interrupts based on the value programmed into the RS3-RS0 bits of Register A. This allows the user to disable this function without affecting the programmed rate. Writing a "1" to this bit enables the generation of periodic interrupts. This bit is cleared to a "0" by reset.

AIE The generation of alarm interrupts is enabled by setting this bit to a "1". Once this bit is enabled the Real Time Clock will generate an alarm whenever a match occurs between the programmed alarm and clock information. If the don't care condition is programmed into one or more of the Alarm Registers, this will enable the generation of periodic interrupts at rates of one second or greater. This bit is cleared by PSRSTB.

UIE (Update-ended Interrupt Enable). When set to 1, this bit enables the Update Ended Flag Bit (UF) in Regiater C to assert INTR. The PSRSTB- pin going low or the SET bit going high clears UIE.

24/12 The 24/12 control bit is used to establish the format of both the Hours and Hours Alarm bytes. If this bit is a "1", the Real Time Clock will interpret and update the information in these two bytes using the 24 hour mode. This bit can be read or written by the CPU and is not affected by reset.

DSE The Real Time Clock can be instructed to handle daylight savings time changes by setting this bit to a "1". This enables two exceptions to the normal time keeping sequence to occur. On the last Sunday in April an exception is processed which increments the time from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October a similar exception is executed which will cause the time to change from 1:59:59 AM to 1:00:00 AM. Setting this bit to a "0" disables the execution of these two exceptions. PSRSTB/and RESET4 have no effect on this bit.

Register C (0CH)

(Read only register)

msb lsb

b7	b6	b5	b4	b3	b2	b1	b0
IRQF	PF	AF	UF	0	0	0	0

IRQF The Interrupt Request Flag bit is set to a "1" when any of the conditions which can cause an interrupt is true and the interrupt enable for that condition is true. The condition which causes this bit to be set, also generates an interrupt. The logic expression for this flag is:

IRQF = PF & PIE
+ AF & AIE
+ UF & UIE

This bit and all other active bits in this register are cleared by reading the register or by activating the PSRSTB/ input pin. Writing to this register has no effect on the contents.

PF The Periodic Interrupt Flag is set to a "1" when a transition, which is selected by RS3-RS0, occurs in the divider chain. This bit will become active, independent of the condition of the PIE control bit. The PF bit will then generate an interrupt and set IRQF if PIE is a "1".

AF A "1" appears in the AF bit whenever a match has occurred between the time registers and alarm registers during an update cycle. This flag is also independent of its enable (AIE) and will generate an interrupt if AIE is true.

UF Update-ended interrupt flag. This bit is set after each update cycle. If UIE in Register B is set, then IRQF will be set when UF becomes set, and INTR will be generated. The UF bit is cleared by PSRSTB- or by reading Register C.

Register D (0DH)

(Read only register)

msb lsb

b7	b6	b5	b4	b3	b2	b1	b0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

VRT The Valid RAM and Time Bit indicates the condition of the contents of the Real Time Clock. This bit is cleared to a "0" whenever the PSRSTB- input pin is LOW. This pin is normally derived from the power supply which supplies Vcc to the device and will allow the user to determine whether the registers have been initialized since power was applied to the device. RESET4 has no effect on this bit and it can only be set by reading Register D. All unused register bits will be "0" when read and cannot be written to.

Note: The power sense and reset functions normally available separately in a 146818 are tied together in the 82C226. The combined signal is PSRSTB- (Power Sense/Reset Strobe) and never goes inactive except during battery disconnect or manual "CMOS discharge."

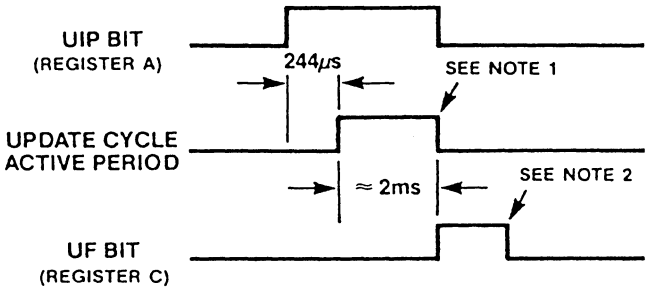
2.7 UPDATE CYCLE

During normal operation the Real Time Clock will perform an update cycle once every second. The performance of an update cycle is contingent upon the divider bits DV2-DV0 not being cleared, and the SET bit in Register B cleared. The function of the update cycle is to increment the clock/calendar registers and compare them to the Alarm Registers. If a match occurs between the two sets of registers, an alarm is issued and an interrupt will be issued if the alarm and interrupt control bits are enabled.

During the time that an update is taking place, the lower 10 registers are unavailable to the CPU. This is done to prevent the possible corruption of data in the registers or the reading of incorrect data. To avoid contention problems between the Real Time Clock and the CPU, a flag is provided in Register A to alert the user of an impending update cycle. This Update In Process Bit (UIP) is asserted 244us before the actual start of the cycle and is maintained until the cycle is complete. Once the cycle is complete the UIP bit will be cleared and the Update Flag (UF) in Register C will be set. Figure 9-2 illustrates the update cycle. CPU access is always allowed to Registers A through D during update cycles.

Two methods for reading and writing to the Real Time Clock are recommended. Both of these methods will allow the user to avoid contention between the CPU and the Real Time Clock for access to the time and date information.

The first method is to read Register A, determine the state of the UIP bit and if it is "0", perform the read or write operation. For this method to work successfully the entire read or write operation (including any interrupt service routines which might occur) must not require longer than 244us to complete from the beginning of the read of Register A to the completion of the last read or write operation to the Clock Calendar Registers.



NOTE:

1. REGISTERS 0-9 ARE UNAVAILABLE TO BE READ OR WRITTEN DURING THIS TIME.
2. UF BIT CLEARED BY CPU READ OF REGISTER C.

FIGURE 9-2 UPDATE CYCLE

The second method of accessing the lower 10 registers is to read Register C once and disregard the contents. Then subsequently continue reading this register until the UF bit is a "1". This bit will become true immediately after an update has been completed. The user then has until the start of the next update cycle to complete a read or write operation.

2.8 POWER-UP/DOWN

Most applications will require the Real Time Clock to remain active whenever the system power is turned off. To accomplish this the user must provide an alternate source of power to the 82C226. This alternate source of power is normally provided by connecting a battery to the Vcc supply pin of the device. A means should be provided to switch from the system power supply to the battery. A circuit such as the one shown in Figure 9-3 may be used to eliminate power drain on the battery when the entire 82C226 is active. The circuit shown here will allow for reliable transitions between system and battery power without undue battery power drain.

Note: The Vin maximum specification should never be exceeded when powering the system up or down. Failure to observe this specificaiton may result in damage to the device. Also, the battery voltage should not be high enough to cause a net increase in VCMOS when +5V power is turned off. Otherwise, VCMOS will continue to be powered by the battery even when +5V is on, and in addition, Q1 will conduct in the reverse direction, resulting in even more drain on the battery when +5V is on.

A pin is provided on the device to protect the contents of the Real Time Clock and reduce power consumption whenever the system is powered down. This pin (PWRGD) should be low whenever the system power supply is not within specifications for proper operation of the system. This signal may be generated by circuitry in either the power supply or on the system board. The PWRGD input will disable all unnecessary inputs during the time the system is powered down to prevent noise on the inactive pins from causing increased Icc. This pin must therefore be inactive for the remainder of the device to operate properly when system power is applied.

One pin is provided to initialize the device whenever power is applied to the 82C226. This pin (PSRSTB) will not alter the RAM or Clock/Calendar contents but it will initialize the necessary control register bits. (See previous sections for discussion of the control register bits affected by PSRSTB) Assertion of PSRSTB disables the generation of interrupts and sets a flag indicating that the contents of the device may not be valid. A recommended circuit for controlling the PSRSTB input is also shown in Figure 9-3.

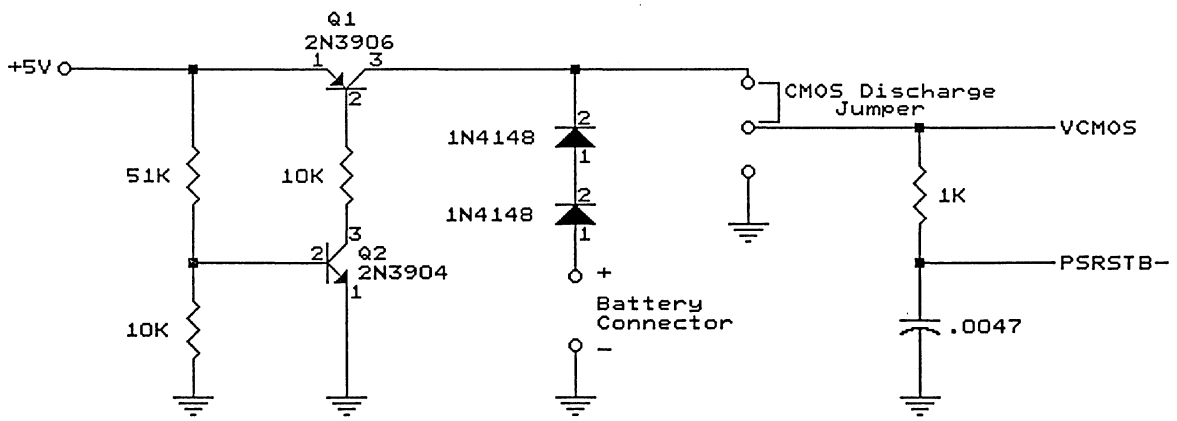


FIGURE 9-3 POWER CONVERSION CIRCUITRY

3.0 SYSTEM CONTROL REGISTERS

Several bits in I/O port 0061 hex (System Control Port B) and I/O port 92 (System Control Port A) are allocated to this chip to perform the control or status functions. Note that the other bits of those I/O ports reside in the CPU controller or BUFFER chip. Care is required in designing with these three chips to avoid bus contention.

4.0 INTERRUPT CONTROLLER

The system provides 16 levels of interrupts. The interrupt requests can be masked individually.

Note: The main difference between the interrupt controller implementation on the PC/AT and the PS/2 family is that in the PS/2, the controller is programmed to operate in the level sensitive mode as opposed to the edge triggered mode.

Figure 9-1 shows the system connections used in a PS/2 system.

The programmable interrupt controllers in the 82C226 function as a system wide interrupt manager in a CHIPS/250 and CHIPS/280 system. They accept requests from peripherals, resolve priority on pending interrupts and interrupts in service, issue an interrupt request to the CPU, and provide a vector which is used as an index by the CPU to determine which interrupt service routine to execute.

A variety of priority assignment modes are provided,which can be re-configured at any time during system operation, allowing the complete interrupt subsystem to be restructured, based on the system environment.

4.1 Overview

Two interrupt controllers, INTC1 and INTC2, are included in the 82C226. Each of the interrupt controllers is equivalent to an 8259A device operating in iAPX86 Mode. The two devices are interconnected and must be programmed to operate in Cascade Mode (see Figure 9-4) for proper operation of all 16 interrupt channels. INTC1 is located at addresses 020H-021H and is configured for Master operation (defined below) in Cascade Mode. INTC2 is a Slave device (defined below) and is located at 0A0H-0A1H. The Interrupt Request output signal from INTC2 (INT) is internally connected to the interrupt request input Channel 2 (IR2) of INTC1. The address decoding and Cascade interconnection matches that of the PS/2 .

Two additional interconnections are made to the interrupt request inputs of the interrupt controllers. The output of Timer 0 in the Counter/Timer subsystem is connected to Channel 0 (IR0) of INTC1. Interrupt request from the Real Time Clock is connected to Channel 0 (IRQ8) of INTC2. Table 9-3 lists the interrupt assignments as used in a PS/2 compatible implementation:

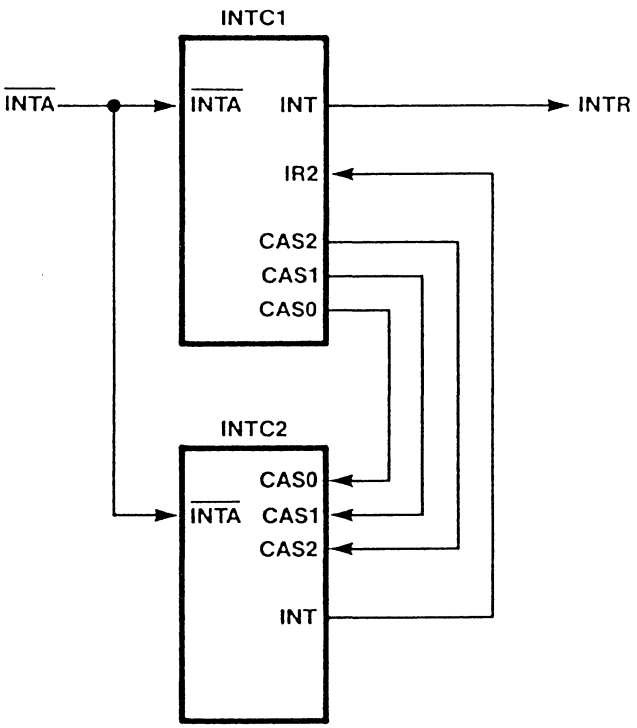


FIGURE 9-4 INTERNAL CASCADE INTERCONNECT

Table 9-3 Interrupt Assignments

Interrupt Level	Function
IRQ0	Timer
IRQ1	KeyBoard
IRQ2	Cascade to slave interrupt controller (INTC2)
IRQ3	Primary Serial Port
IRQ4	Alternate Parallel Port
IRQ5	Not used
IRQ6	Diskette Controller
IRQ7	Parallel Port
IRQ8	Real Time Clock
IRQ9	Redirect Cascade
IRQ10	Not used
IRQ11	Not used
IRQ12	Mouse Interrupt
IRQ13	80387/80287 exception interrupt
IRQ14	Hard Disk
IRQ15	Not used

Description of the Interrupt Subsystem will pertain to both INTC1 and INTC2 unless otherwise noted. Wherever register addresses are used, the address for the INTC1 register will be listed first and the address for the INTC2 register will follow in parenthesis. Example 020H (0A0H)

4.2 Controller Operation

Figure 9-5 is a block diagram of the major elements in the interrupt controller. The Interrupt Request Register (IRR) is used to store requests from all of the channels which are requesting service. Interrupt Request its are labeled using the Channel Name IR7-IR0. The In-Service Register (ISR) contains all the channels which are currently being serviced (more than one channel can be in service at a time). In-Service Register bits are labeled IS7-IS0 and correspond to IR7-IR0. The Interrupt Mask Register (IMR) allows the CPU to disable any or all of the interrupt channels. The Priority Resolver evaluates inputs from the above three registers, issues an interrupt request, and latches the corresponding bit into the In-Service Register. During interrupt acknowledge cycles, a master controller outputs a code to the slave device which is compared in the Cascade Buffer/Comparator with a three bit ID code previously written. If a match occurs in the slave controller, it will generate an interrupt vector. The contents of the Vector Register are used to provide the CPU with an interrupt vector during Interrupt Acknowledge (INTA) cycles.

4.3 Interrupt Sequence

The 82C226 allows the CPU to perform an indirect jump to a service routine in response to a request for service from a peripheral device. The indirect jump is based on a vector which is provided by the 82C226 on the second of two CPU generated INTA cycles (the first INTA cycle is used for resolving priority and the second cycle is for transferring the vector to the CPU). The events which occur during an interrupt sequence are as follows:

1. One or more of the interrupt requests (IR7-IR0) becomes active, setting the corresponding IRR bit(s).

2. The interrupt controller resolves priority based on the state of the IRR, IMR and ISR and asserts the INTR output if appropriate.

3. The CPU accepts the interrupt and responds with an INTA cycle.

4. During the first INTA cycle, the highest priority ISR bit is set and the corresponding IRR bit is reset. The internal Cascade address is generated and the XD7-XD0 outputs remain tri-stated.

5. The CPU will execute a second INTA cycle, during which the 82C226 will drive an 8-bit vector onto the data pins XD7-XD0, which is in turn latched by the CPU. The format of this vector is shown in Table 9-4. Note that V7-V3 in Table 9-4 are programmable by writing to Initialization Control Word 2 (see Initialization Command Words section below).

6. At the end of the second INTA cycle, the ISR bit will be cleared if the Automatic End Of Interrupt mode is selected (see End Of Interrupt section below). Otherwise, the ISR bit must be cleared by an End Of Interrupt (EOI) command from the CPU at the end of the interrupt service routine.

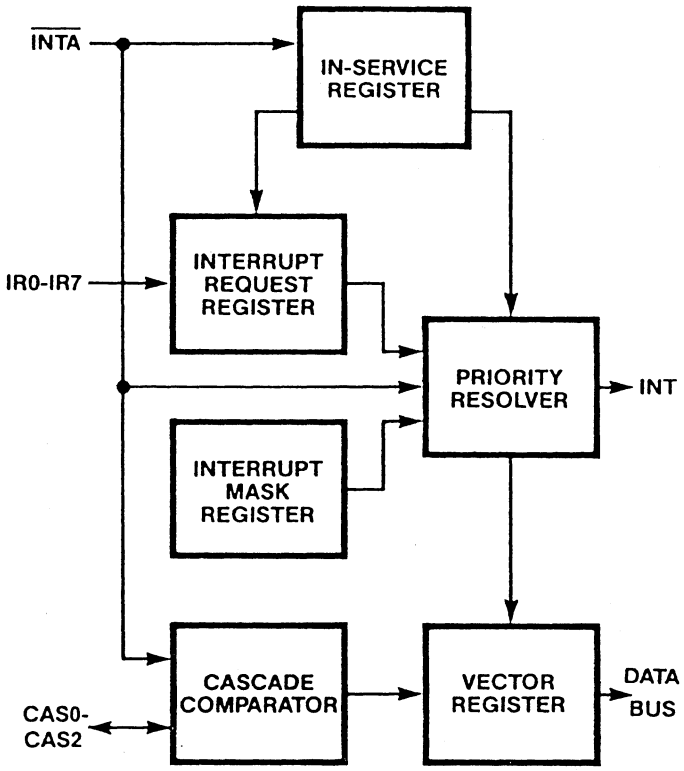


FIGURE 9-5 INTERRUPT CONTROLLER BLOCK DIAGRAM

Table 9-4

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	V7	V6	V5	V4	V3	1	1	1
IR6	V7	V6	V5	V4	V3	1	1	0
IR5	V7	V6	V5	V4	V3	1	0	1
IR4	V7	V6	V5	V4	V3	1	0	0
IR3	V7	V6	V5	V4	V3	0	1	1
IR2	V7	V6	V5	V4	V3	0	1	0
IR1	V7	V6	V5	V4	V3	0	0	1
IR0	V7	V6	V5	V4	V3	0	0	0

If no interrupt request is present at the beginning of the first INTA cycle (i.e., a spurious interrupt) INTC1 will issue an interrupt level 7 vector during the second INTA cycle.

End Of Interrupt

EOI is defined as the condition which causes an ISR bit to be reset. Determination of which ISR bit is to be reset can be done by a CPU command (specific EOI) or, the Priority Resolver can be instructed to clear the highest priority ISR bit (non-specific EOI).

The 82C226 can determine the correct ISR bit to reset when operated in modes which do not alter the fully nested structure, since the current highest priority ISR bit is necessarily the last level acknowledged and serviced. In conditions where the fully nested structure is not preserved, a specific EOI must be generated at the end of the interrupt service routine. An ISR bit that is masked, in Special Mask Mode by a IMR bit, will not be cleared by a non-specific EOI command. The interrupt controller can optionally generate an Automatic End Of Interrupt (AEOI) on the trailing edge of the second INTA cycle.

Priority Assignment

Assignment of priority is based on an interrupt channel's position relative to the other channels in the interrupt controller. After the initialization sequence, IR0 has the highest priority, IR7 has the lowest, and priority assignment is fixed (Fixed Priority Mode). Priority assignment can be rotated either manually (Specific Rotation Mode) or automatically (Automatic Rotation Mode) by programming Operational Command Word 2 (OCW2).

Fixed Priority Mode - This is the default condition which exists unless rotation (either manual or automatic) is enabled, or the controller is programmed for Polled Mode. In Fixed Priority Mode, interrupts are fully nested with priority assigned as shown:

	Lowest							Highest
Priority Status	7	6	5	4	3	2	1	0

Nesting allows interrupts of a higher priority to generate interrupt requests prior to the completion of the interrupt in service. When an interrupt is acknowledged, priority is resolved, the highest priority request's vector is placed on the bus and the ISR bit for that channel is set. This bit remains set until an EOI (automatic or CPU generated) is issued to that channel. While the ISR bit is set, all interrupts of equal or lower priority are inhibited. Note that a higher priority interrupt which occurs during an interrupt service routine will only be acknowledged if the CPU has internally re-enabled interrupts.

Specific Rotation Mode - Specific Rotation allows the system software to re-assign priority levels by issuing a command which redefines the highest priority channel.

Before Rotation

	Lowest							Highest
Priority Status	7	6	5	4	3	2	1	0

(Specific Rotation command issued with Channel 5 specified)

After Rotation

	Lowest							Highest
Priority Status	5	4	3	2	1	0	7	6

Automatic Rotation Mode - In applications where a number of equal priority peripherals are requesting interrupts, Automatic Rotation may be used to equalize the priority assignment. In this mode a peripheral, after being serviced, is assigned the lowest priority. All peripherals connected to the controller will be serviced at least once in 8 interrupt requests to the CPU from the controller. Automatic rotation will occur,if enabled, due to the occurrence of EOI (automatic or CPU generated).

Before Rotation (IR4 is highest priority request being serviced)

ISR Status Bit	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
	0	1	0	1	0	0	0	0

	Lowest							Highest
Priority Status	7	6	5	4	3	2	1	0

After Rotation (IR4 service completed)

ISR Status Bit	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
	0	1	0	0	0	0	0	0

	Lowest							Highest
Priority Status	4	3	2	1	0	7	6	5

4.4 PROGRAMMING THE INTERRUPT CONTROLLER

Two types of commands are used to control the 82C226 interrupt controllers, Initialization Command Words (ICW) and Operational Command Words (OCW).

Initialization Command Words

The initialization process consists of writing a sequence of 4 bytes to each interrupt controller. The initialization sequence is started by writing the first Initialization Command Word (ICW1) to address 020H (0A0H) with a 1 on bit 4 of the data byte. The interrupt controller interprets this as the start of an initialization sequence and does the following:

1 The Initialization Command Word Counter is reset to zero.
2 ICW1 is latched into the device
3 Fixed Priority Mode is selected
4 IR7 is assigned the highest priority
5 The Interrupt Mask Register is cleared
6 The Slave Mode Address is set to 7
7 Special Mask Mode is disabled
8 The IRR is selected for Status Read operations

The next three I/O writes to address 021H (0A1H) will load ICW2-ICW4. See Figure 9-6 for a flow chart of the initialization sequence. The initialization sequence can be terminated at any point (all 4 bytes must be written for the controller to be properly initialized) by writing to address 020H (0A0H) with a 0 in data bit 4. Note, this will cause OCW2 or OCW3 to be written.

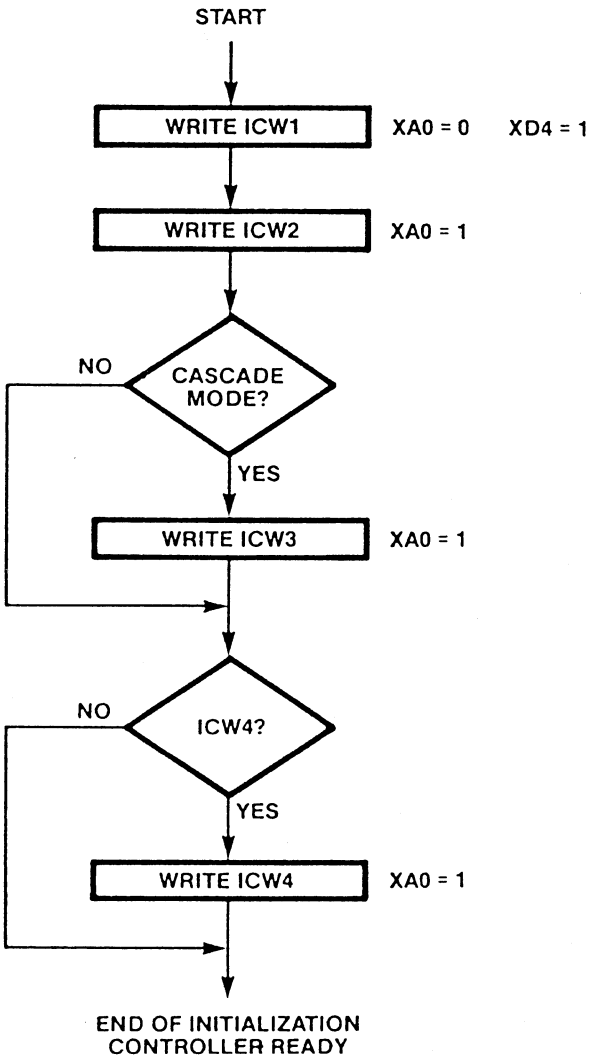


FIGURE 9-6 INITILIZATION SEQUENCE

ICW1 - Address 020H (0A0H)

(Write Only Register)

msb lsb

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	SI	LTM	X	SM	X

SI Bit-4 indicates to the interrupt controller that an Initialization sequence is starting and must be a 1 to write ICW1.

LTM Bit-3 selects level or edge triggered inputs to the IRR. If a 1 is written to LTM, a "high" level on the IRR input will generate an interrupt request. The IR must be active until the first INTA cycle is started to generate the proper interrupt vector (an IR7 vector will be generated if the IRR input is de-asserted early) and the IR must be removed prior to EOI to prevent a second interrupt from occcuring.

SM Bit-1 selects between Single Mode and Cascade Mode. Single Mode is used whenever only one interrupt controller (INTC1) is used and is not recommended for this device. Cascade Mode allows the two interrupt controllers to be connected through IR2 of INTC1. INTC1 will allow INTC2 to generate its own nterrupt vectors if Cascade Mode is selected and the highest priority IR pending is from an INTC2 input. INTC1 and INTC2 must be programmed for Cascade Mode for both devices to operate.

ICW2 - Address 021H (0A1H)

(Write Only Register)

msb lsb

b7	b6	b5	b4	b3	b2	b1	b0
V7	V6	V5	V4	V3	X	X	X

V7-V3 These bits are the upper 5 bits of the interrupt vector and are programmable by the CPU. The lower three bits of the vector are generated by the Priority Resolver during INTA (see Table 9-4). INTC1 and INTC2 need not be programmed with the same value in ICW2.

ICW3 Format for INTC1 - Address 021H

(Write Only Register)

msb lsb

b7	b6	b5	b4	b3	b2	b1	b0
S7	S6	S5	S4	S3	S2	S1	S0

S7-S0 Select which IR inputs have Slave Mode controllers connected. ICW3 in INTC1 must be written with a 04H for INTC2 to function.

ICW3 Format for INTC2 - Address 0A1H

msb lsb

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	ID2	ID1	ID0

ID2-ID0 Determine the Slave Mode address the controller will respond to during the cascaded INTA sequence. ICW3 in INTC2 should be written with a 02H for Cascade Mode operation. Note, b7-b3 should be zero.

ICW4 - Address 021H (0A1H)

(Write Only Register)

msb lsb

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	EMI	X	X	AEOI	X

EMI Bit 4 will Enable Multiple Interrupts from the same channel in Fixed Priority Mode. This allows INTC2 to fully nest interrupts, when Cascade Mode with Fixed Priority Mode are both selected, without being blocked by INTC1. Correct handling of this mode requires the CPU to issue a non-specific EOI command to INTC2 and check its In-Service Register for zero, when exiting an interrupt service routine. If zero, a non-specific EOI command should be sent to INTC1. If non-zero, no command is issued.

AEOI Auto End Of Interrupt is enabled when ICW4 is written with a zero in bit 1. The interrupt controller will perform a non-specific EOI on the trailing edge of the second INTA cycle. Note, this function should not be used in a device with fully nested interrupts unless the device is a cascade Master.

Operational Command Words

Operational Command Words (OCW's) allow the 82C226 interrupt controllers to be controlled or re-configured at any time while operating. Each interrupt has 3 Ocw's which can be programmed to affect the proper operating configuration and a Status Register to monitor controller operation.

Operational Command Word 1 (OCW1) is located at address 021h (0A1h) and may be written any time the controller is not in Initialization Mode. Operational Command Words 2 and 3 (OCW2,OCW3) are located at address 020H (0A0H). Writing to address 020H (0A0H) with a 0 in bit 4 will place the controller in operational mode and load OCW2 (if data bit 3 = 0) or OCW3 (if data bit 3 = 1).

OCW1 - Address 021H (0A1H)

(Write Register)

msb lsb

b7	b6	b5	b4	b3	b2	b1	b0
M7	M6	M5	M4	M3	M2	M1	M0

M7-M0 These bits control the state of the Interrupt Mask Register. Each Interrupt Request can be masked by writing a 1 in the appropriate bit position (M0 controls IR0 etc.). Setting an IMR bit has no effect on lower priority requests. All IMR bits are cleared by writing ICW1.

OCW2 - Address 020h (0A0h)

(Write Only Register)

msb lsb

b7	b6	b5	b4	b3	b2	b1	b0
R	SL	EOI	SI	2/3	L2	L1	L0

R This bit in conjunction with SL and EOI selects operational function. Writing a 1 in bit 7 causes one of the rotate functions to be selected.

R	SL	EOI	Function
1	0	0	Rotate on auto EOI enable *
1	0	1	Rotate on non-specific EOI

* This function is disabled by writing a zero to all three bit positions.

SL This bit in conjunction with R and EOI selects operational function. Writing a 1 in this bit position causes a specific or immediate function to occur. All specific commands require L2-L0 to be valid except no operation.

R	SL	EOI	Function
0	1	0	No operation
0	1	1	Specific EOI Command
1	1	0	Specific Rotate Command
1	1	1	Rotate on specific EOI

EOI This bit in conjunction with R and SL selects operational function. Writing a 1 in this bit position causes a function related to EOI to occur.

R	SL	EOI	Function
0	0	1	Non-specific EOI Command
0	1	1	Specific EOI Command
1	0	1	Rotate on non-specific EOI
1	1	1	Rotate on specific EOI

SI Writing a 0 in this bit position takes the interrupt controller out of initialize mode and writes OCW2 or OCW3.

2/3 If the I/O write places a 0 in bit 4 (SI), then writing a 0 in bit 3 (2/3) selects OCW2 and writing a 1 will select OCW3.

L2-L0 These three bits are internally decoded to select which interrupt channel is to be affected by the Specific command. L2-L0 must be valid during three of the four specific cycles (see SL above).

OCW3 - Address 020H (0A0H)

(Write Only Register)

msb lsb

b7	b6	b5	b4	b3	b2	b1	b0
0	ESMM	SMM	SI	2/3	PM	RR	RIS

ESMM Writing a 1 in this bit position enables the Set/Reset Special Mask Mode function controlled by bit 5 (SMM). ESMM allows the other functions in OCW3 to be accessed and manipulated without affecting the Special Mask Mode state.

SMM If ESMM and SMM both are written with a 1 the Special Mask Mode is enabled. Writing a 1 to ESMM and a 0 to SMM disables Special Mask Mode. During Special Mask Mode, writing a 1 to any bit position inhibits interrupts and a 0 enables interrupts on the associated channel by causing the Priority Resolver to ignore the condition of the ISR.

SI See SI above.

2/3 See 2/3 above.

PM Polled Mode is enabled by writing a 1 to bit 2 of OCW3, causing the 82C226 to perform the equivalent of an INTA cycle during the next I/O read operation to the controller. The byte read during this cycle will have bit 7 set if an interrupt is pending. If bit 7 of the byte is set, the level of the highest pending request will be encoded on bits 2-0. The IRR will remain frozen until the read cycle is completed at which time the PM bit is reset.

RR When the RR bit (bit 1) is 1, reading the Status Port at address 020h (0A0h) will cause the contents of IRR or ISR (determined by RIS) to be placed on XD7-XD0. Asserting PM forces RR reset.

RIS This bit selects between the IRR and the ISR during Status Read operations if RR = 1.

5.0 Timer/Counters

The IPC integrates an 8254 compatible timer/counter. The timer subsection provides three programmable timer/counters; Channel 0, Channel 2 and Channel 3. Channel 0 and Channel 2 are similar to Channel 0 and Channel 2 of the IBM personal computer systems and corresponds to Channel 0 and Channel 2 in the 8254. Channel 3, called watch dog timer, is implemented with Channel 1 in the 8254. The control function unit has to monitor various situations while writing the command words to 8254 to guarantee that each channel is programmed correctly.

Channel 0 : System Timer

GATE0 is always enabled, which will make timer mode 1 and mode 5 invalid for Channel 0.

CLK0 is driven by 1.19MHZ.

OUT0's rising edge will set IRQ0 latch which is connected to INTC. The latch may be cleared by a system reset, an interrupt acknowledge cycle with a vector 08, or an I/O write to port hex 061 with bit 7 equal to 1. Signals derived from OUT0 are used to gate and clock Channel 3. For proper operation of Channel 3 (Watch Dog Timer) timeout function, Channel 0 must be programmed to either timer mode 2 or timer mode 3. Channel 0's Counter can either be programmed to operate in 16-bit binary or BCD count down

Channel 2 : Speaker Tone Generation

GATE2 is controlled by bit 0 of I/O port 0061 hex. Setting this bit causes GATE2 to go high. CLK2 is driven by 1.19MHZ. OUT2 goes to two places:

1. Input port 0061 hex bit 5

2. OUT2 is also Logically And'ed with I/O port 0061 hex bit 1. The AND gate's output drives the "Audio Sum Node" signal.

This channel supports all program modes (mode 0 - 5). Channel 2's counter may be programmed to operate in 16-bit binary or BCD count down mode.

Channel 3: Watch Dog Timer

The 8254's Channel 1 is used to emulate the Watch Dog Timer function.

GATE1 is tied to IRQ0, which is set by the rising edge of Timer 0 output.

CLK1 is driven by inverted Channel 0's OUT0. In the PS/2 system the Watch Dog Timer uses the rising edge of Channel 0's OUT0 to decrement the counter, while in 8254, the falling edge of the clock input is used to decrement the counter.

OUT1 is And'ed with -WDTDIS and generates the -WDTOUT signal which is normally floating and goes low when the Watch Dog Timer is enabled and time out situation had occurred. This condition is usually caused by the IRQ0 not being serviced within a specified period of time. The time depends on the count value set for Channel 3. The activation of WDTOUT triggers the NMI and sets port 092h, bit 4.

Channel 3 only operates in mode 0 and 8-bit binary count. Channel 3 operation is defined only when Channel 0 is programmed to operate in mode 2 or mode 3. Channel 3 is enabled (-WDTDIS = 1) by writing 10h to I/O port 0047h, followed by writing a count value to I/O port 0044h. Channel 3 is disabled (-WDTDIS = 0) by writing 10h to port 0047h and NOT writing a count value to port 0044h, or by systems reset. When Channel 3 is enabled and IRQ0 is active for more than one period of Channel 0's OUT0, an INHIBIT signal is generated which prevents writing data to Channel 0 (port 0040h) or Channel 3 (port 0044h). INHIBIT is never active when Channel 3 is disabled

Control Function

Following are I/O registers allocated to system timer/counters:

0040h Read/Write Counter 0
0042h Read/Write Counter 2
0043h Write only Control Byte for Channel 0 or 2

Channel 0 Count Register

Before accessing Port 040H, port 043 must be programmed with the appropriate control word followed by an initial count value to port 040H.

Channel 2 Count Register

Before accessing Port 042H, port 43H must be programmed with the appropriate control word, followed by an initial count value to port 42H

Control Word (Port 43H)

The Control Word register is a write only register. The bit definitions are as follows:

F3 - F0 - Bits 7 through 4 determine the command to be performed.

M2 - M0 - Bits 3 through 1 determine the counter's mode during Read/Write Counter Commands or select the counter during a read back command.

BCD - Bit 0 selects binary coded decimal counting format during Read/Write Counter Commands.

Bit 7	Bit 6	Function
F3	F2	
0	0	Select counter 0
0	1	Reserved
1	0	Select counter 1
1	1	Reserved

Bit 5	Bit 4	Function
F1	F0	
0	0	Counter latch command
0	1	Read/write counter bits 7-0 only
1	0	Read/write counter bits 15-8 only
1	1	Read/write counter bits 7-0 first then bits 15-8

Bit 3 M2	Bit 2 M1	Bit 1 M0	Function
0	0	0	mode 0
0	0	1	mode 1
x	1	0	mode 2
x	1	1	mode 3
1	0	0	mode 4
1	0	1	mode 5

Bit 0	
BCD	
0	16-bit binary count
1	BCD count(4 decades)

0044h Read/Write Counter 3
0047h Write only Control Byte for Channel 3

Count Register for Channel 3 (IO Port 44H)

Before accessing Port 044H, port 47H must be programmed with the appropriate control word, followed by an initial count value to port 44H

Control Byte (Port 47H)

This is a write only register. The bit definitions are as follows:

Bit 7	Bit6	
SC1	SC0	
0	0	select counter 3
0	1	reserved
1	0	reserved
1	1	reserved

Bit 5	Bit 4	
RW1	RW0	
0	0	counter latch command select counter 3
0	1	read/write counter bits 7-0 only
1	0	reserved
1	1	reserved

Bit 3-0 = 0 mode 0 and binary count only

6.0 Parallel Port Controller

The 82C226 integrates a parallel port to provide support for devices that require 8 bit parallel data transfer. Unlike the PC-AT implementation where the parallel port was used to transfer data in one direction only, namely output, the parallel port implementation on 82C226 supports an extended mode which supports bi-directional data transfers. Additionally, the port supports a level sensitive interrupt and adds a register that reflects the status of the interrupt.

Parallel Port Programmable Option Select

The parallel port can be programmed to reside at three different I/O locations, and the desired location can be selected by setting bits <5,6> in system POS register 102.

Bit 6	Bit 5	Function
0	0	Parallel1
0	1	Parallel 2
1	0	Parallel 3

Parallel Port Configuration

The corresponding address assignments are shown below:

	Data Address Hex	Status Address Hex	Parallel Control Address in Hex
Parallel 1	03BC	03BD	03BE
Parallel 2	0378	0379	037A
Parallel 3	0278	0279	027A

Parallel Port Extended Mode

The extended mode option of the parallel port can be selected b y setting port 102 bit 7 to a zero. In the extended mode, the parallel port is configured to support bi-directional data transfers.

Mode	Access	Bit 7 Reg 102	Direction	System Reset
Extended	Write	0	0	1
Extended	Write	0	0	0
Extended	Read	0	1	0
Compatible	Write	1	not allowed	0

Data Address Port

The normal PC/AT mode and the extended mode access the data address port. In the PC/AT mode, the data presented at this port is transferred directly to the outputs. During a Read operation, the data that was written during the last access is read back.

In the extended mode, the data presented to the Data Address port is transferred to the output only if the direction bit is set to the write mode. During a read operation, if the direction bit is set to the write mode, then the data last written to the data address register is read back. If the direction bit is set to read, then the data presented at the parallel port is read back.

Status Port (PSP)

The Status Port is a read only register. The bit definitions are as shown below:

Bit	Function	Description
7	-BUSY	When low, it indicates that the port is currently busy and cannot accept new data.
6	-ACK	This bit provides a handshake mechanism for data transfer. When active, it signals that the 8 bit parallel device, normally a printer, is able to accept another byte of data.
5	PE	This bit, when set, indicates an error condition, that requires users attention. When interfacing to a printer, this bit indicates an error condition such as paper end.
4	SLCT	This bit when set, indicates that the device has been selected.
3	-ERROR	This bit when set, reports an error condition.
2	-IRQ Status	When this bit is set to 0, the printer has acknowledged he previous transfer using the '-acknowledge' signal.
1,0		Not used

Parallel Port Control (PCP)

The Parallel Control port is a read or write port. A write operation to this port latches the six least-significant data bits of the bus. The sixth bit corresponds to the direction control bit and is only applicable in the extended mode. The remaining five bits are compatible with previous implementations as shown in the following figure. A read operation to the Parallel Control Port presents the system microprocessor the data that was last written to it, with the exception of the write-only direction bit.

Bit	Function	Description
7,6		Reserved
5	Direction	This bit controls the direction of the data port. This is a write-only bit.
4	IRQEN	This bit enables the parallel port interrupt. When this bit is set to 1, an interrupt occurs when the '-acknowledge' sign changes from active to inactive.
3	SLCT IN	This bit controls the 'select in' (SLCT IN) signal. When this bit is set to 1, the printer is selected.
2	-INIT	This bit controls the 'initialize printer' (-INIT) signal. When this bit is set to 0, the printer starts.
1	AUTO FDXT	This bit controls the 'automatic feed XT' (AUTO FD XT) signal. Then this bit is set to 1, the printer will automatically line feed after each line is printed.
0	STROBE	This bit controls the 'strobe' signal to the printer. When this bit is set to 1, data is pulse-clocked into the printer.

System Control Registers

The last section of the SPC contains three system control registers and a decoder.

Port 0061h: System Control Register B

System Control Register B is accessed by I/O read or write operations to I/O address 0061h. The bit definitions are shown below:

The external master cannot access this port.

Bit	Function	Description
7 write read	PARITY CHECK	 A write operation with this bit set to 1, resets IRQ0 latch Default = 0 This bit indicates the state of the parity check latch. A high means that a priority error has occurred. Default = 0
6 write read	CHANNEL CHECK	 Reserved This bit returns the state of the Channel Check latch. A high shows that a channel check has occurred. Default = 0
5 write read	TIMER 2 OUT	 Reserved This bit returns the condition of timer/counters Channel 2's OUT signal
4 write read	REFRESH TOGGLE	 Reserved This bit is toggled for each refresh request.
3 write read	CHAN. CHK. ENABLE	 A write operation with this bit set to 0 enables Channel Check. This bit is st to high during a power on reset. A read operation reflects the last write result.

Port 0061h: System Control Register B (continued)

2 write read	PARITY CHK. ENABLE	Set this bit to 0, enable parity check. During power on reset, set this bit to 0. Return result of the last write to this bit.
1 write read	SPEAKER ENABLE	A write operation with bit set to 1, enables speaker data. This bit is set to 0 during a power on reset. Return result of the last write to this bit.
0 write read	TIMER 2 ENABLE	A write operation with this bit is set to 1, enables the gate input of timer/counter Channel 2. Default = 0. Return result of the last write to this bit.

Port 0092: System Control Register A

The external master cannot access this port.

The following shows the definition of each bit in I/O port 0092h.

Bit	Type	Function
5 write read	Reserved	 Reserved = 0 Reserved, always return 1
4 write read	WATCHDOG TIMEOUT	 Reserved This read only bit reflects watch dog timer output state, a high indicated that the watch dog timer timed out.
3 write read	PASSWORD LOCK	 Setting this bit to 1 locks the 8-byte (38-3F) secured area reserved for password. This bit can be cleared only by the power on reset signal once being written to 1. Return result of the last write.
2 write read	(RESERVED)	 Reserved Reserved, always return 1
1 write read	A20 ENABLE	 Setting this bit 0 disables the A20 set to 0 during system reset. Return result of the last write.

Port 0092: System Control Register A (continued)

Bit	Type	Function
0 write	ALT RESET	This bit is set to 0 by a system reset or a write operation. When set to 1, the alternate reset signal will be pulsed for 100 to 125 ns. The reset occurs after a minimum delay of 6.72 micro seconds. This bit remains high after the reset pulse. If this bit is a 0, Power-On-Self-Test (POST) assumes the system was just powered on. If this bit is a 1, POST assumes a switch from the Protected mode to the Real mode has taken place.
read		See description of the write section.

Port 0096: Channel Position Select Register

Each channel position has a unique "setup" line (-CDSTUP) associated with it. Prior to a setup cycle, an I/O operation to port 0096h sets the bit pattern to select the channel position to which the subsequent setup operation will occur. The following table shows the valid bit-patterns

Channel Selected	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
none	0	0	0	0	0	x	x	x
1	0	0	0	0	1	0	0	0
2	0	0	0	0	1	0	0	1
3	0	0	0	0	1	0	1	0
4	0	0	0	0	1	0	1	1
5	0	0	0	0	1	1	0	0
6	0	0	0	0	1	1	0	1
7	0	0	0	0	1	1	1	0
8	0	0	0	0	1	1	1	1
Channel reset	1	0	0	0	x	x	x	x

Note: Bits 6, 5 and 4 return highs when port 0096 is read since they do not exist.

Port 0096h is cleared by a system reset. The Channel reset signal is also enabled during a system reset.

The external master can not access this port.

Other Registers

System Board Setup/Enable Register (Port 94_H)

When this bit 7 of Port 94H is set to 1, it enables the various functions of the system board and system board resident I/O functions. When set to zero, these functions are placed in set up.

The default state of this bit is '1' (enable state).

Model 60 Support

SPC also provides a signal to control I/O port 0076H's access. The -P76EN signal will becomes active when the I/O port 0076H is accessed. The IPC has to force this signal high in the system power off situation. The P76ENB is qualified by the MASTERB signal

Symbol	Type	PLCC	PFP	Description
XD7-XD0	I/O	24-31	18-25	DATA BUS: The data lines are tri-state bi-directional lines connected to peripheral data bus. The outputs are actively driven by the SPC during I/O read to the Interrupt Controller registers (Interrupt Request Register, In-Service Register and the Interrupt Mask Register), the Timer/Counter registers (namely the contents of these counters and the status of the System Timer (Channel 0), Tone Generator (Channel 2), and Watch Dog Timer (Channel 3), the Real Time Clock internal registers and on-chip configuration registers and I/O ports 61H, 92H, 96H and 102H. The XD bus drivers are disabled and inputs are read from the CPU during I/O write cycles when CPU is programming the Interrupt Controller registers, the Timer/Counter registers and the Real Time Clock registers and RAM and on-chip configuration registers and I/O ports. During the interrupt acknowledge sequence, the interrupt controller puts the interrupt vector byte on the XD- bus. Data bus XD7-XD0 also acts as multiplexed address/data bus for the Real Time Clock.
XA9-XA0	I	34-43	30-39	ADDRESS BUS: This is the latched peripheral address bus used to address various registers in the interrupt controllers, Timer/Counters, registers and I/O ports.
RESET4	I	16	10	RESET4: Reset is active high input. It does not affect clock functions.
-ADL	I	18	12	ADDRESS LATCH: SPC uses -ADL to latch XA(9:0) and -OBIOP. -ADL also resets parallel port interrupt.

Symbol	Type	PLCC	PFP	Description
-XIORD	I	65	66	I/O READ: I//O Read is active low command from the CPU to read the SPC internal registers. The data from the SPC internal registers is driven on SPC XD-bus. The external bus master cannot access any of SPC registers except the interrupt controller registers.
-XIOWR	I	52	49	I/O WRITE: I/O Write is an active low command from the CPU to write into the internal SPC registers. The data on the XD bus is written into the register selected by the XA bus. The external bus master cannot access any SPC registers except interrupt controller internal registers.
-MASTER	I	33	29	EXTERNAL BUS MASTER: (Active Low) When active low it indicates external bus master has control of the lens. -MASTER is used to qualify all on chip register decodes (except Interrupt Controller registers) to ensure that external bus master cannot access on chip registers except those to interrupt controllers.
-OBIOP	I	17	11	ON BOARD I/O PERIPHERAL: (Active Low) -OBIOPB decodes XA15 - XA10. When XA15 - XA10 are all zero, this signal goes low. This signal is used to qualify all on chip register decodes.

INTERRUPT CONTROLLER

Symbol	Type	PLCC	PFP	Description
-IR15:9 -IR7:6 -IR5:3 -IR1	I	76-82 83,84 1-3 4	81-87 88,89 91-93 94	INTERRUPTREQUESTS: Asynchronous inputs. An interrupt is generated by applying proper level interrupt is generated by applying proper level to any Interrupt Request pin.
-INTA	I	14	8	INTERRUPT ACKNOWLEDGE: (Active low) This pin is driven by the CPU controller to instruct the interrupt controller to put the interrupt vector data on the XD bus by a series of two -INTA pulses
INTR	O	70	71	INTERRUPT: (Active High). This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU controller and is connected to CPU INTR input pin.

TIMER

Symbol	Type	PLCC	PFP	Description
TMRCLK	I	23	17	TIMER CLOCK: Clock input for Timer/Counter Channel 0 and 2. (1.19 MHz)
AUDIO	O	19	13	AUDIO SUM NODE: Output of Timer 2.Timer 2 is used for tone generation for speaker and is clocked by 1.19 MHz clock (TMRCLK pin).
WDT	O	20	14	WATCH DOG TIMER TIMEOUT: Output of timer 3 (Watch Dog Timer). The clock input of this timer is internally connected to OUT0 and gate input is internally connected to IRQ0. Open drain output.

REAL TIME CLOCK

Symbol	Type	PLCC	PFP	Description
OSCI	I	72	73	OSCILLATOR INPUT: The time base(32.768 Khz) for time functions is connected to this pin.
PSRSTB	I	13	7	POWER SENSE, RESET: This pin does not affect clock calendar or RAM functions. When PSRSTB and TEST pin are both low, the following occurs: a) Periodic Interrupt Enable (PIE) bit is cleared to zero. b) Alarm Interrupt Enable (AIE) bit is cleared to zero. c) Update ended Interrupt Enable (UIE) bit is cleared to zero. d) Update ended Interrupt Flag (UF) bit is cleared to zero. e) Interrupt Request Status Flag (IRQF) is cleared to zero. f) Periodic Interrupt Flag (PF) bit is cleared to zero. g) The part is not accessible by CPU h) Alarm Interrupt Flag (AF) bit is cleared to zero. i) Square Wave output enable bit is cleared to zero.

REAL TIME CLOCK (continued)

Symbol	Type	PLCC	PFP	Description
PWRGD	I	12	6	POWER GOOD: Power Good pin must be high for bus cycles in which the CPU accesses the RTC. When PWRGD is low, all address, data, data strobe and R/W pins are disconnected from the processor.
TEST	I	15	9	TEST: Test is an active high input.It initializes various internal registers so that the test program starts in a known state. It should be tied low in normal operation.

PARALLEL PORT

Symbol	Type	PLCC	PFP	Description
BUSY	I	68	69	PRINTER BUSY: Active High. When active it indicates the printer is busy and cannot accept data.
-ACKB	I	67	68	PRINTER ACKNOWLEDGE: Active Low.When low, it indicates that printer has received a character and is ready to accept another.
PE	I	69	70	PRINTER PAPER END: Active High. This pin indicates that printer has detected end of paper.
SLCT	I	71	72	SELECT PRINTER: Active High. When this pin is '1', it indicates that the printer has been selected.
-ERROR	I	73	74	PRINTER ERROR: Active low. When this input is low, it indicates that printer has encountered an error condition.

PARALLEL PORT (continued)

Symbol	Type	PLCC	PFP	Description
PP(7:4) PP(3:0)	I/O	54-57 59-62	55-58 60-63	PARALLEL PORT: Printer data port.
-SLCTINO	O	8	98	SELECT IN SIGNAL FOR PRINTER: Active low, open drain. When active, this signal indicates the printer is selected.
-INITO	O	7	97	INITIALIZE PRINTER: Active low, open drain. When active, it initializes the printer.
-ATFDXTO	O	6	96	AUTOFEED XT: Active low, open drain.When low, the printer will automatically line feed one line after each line is printed.
-STROBEO	O	5	95	STROBE SIGNAL TO THE PRINTER: Active low. When low, the data is pulse clocked into the printer.
-PDPRD	O	10	100	PARALLEL DATA PORT READ: Active low.This signal is the parallel data port's transceiver direction control signal. When low, it indicates read.
-PCPRD	O	9	99	PARALLEL PORT CONTROL REGISTER READ:Active low. When low it enables the Parallel Port Control Register signals (-SLCTIN, INIT, -ATFDXT, -STROBE) onto the system data bus.

CHANNEL SET UP

Symbol	Type	PLCC	PFP	Description
-CDSPEN	I	66	67	CHANNEL SETUP ENABLE: Active low. This signal goes low when I/O operation in the address range 100_H - 107_H is performed.
-CDSTUP8:1	O	51-44	48-41	CHANNEL SETUP: Active low. Each channel position has a unique set up signal (CDSTUP). When low, it indicates that channel has been selected for subsequent set up.
CHRST	O	64	65	CHANNEL RESET: Active high. When high it resets the channel.
-P76ENB	O	22	16	PORT 76 ENABLE: Active low. Any I/O operation to port 76 drives this signal active. This signal is forced high during system power down (PWRDN=0).

POWER SUPPLIES

PLCC	PFP	Description
53,11 21,24 58,74	1, 5 15, 50 51, 59 75, 76 26, 27	Ground
32,63 75	64, 79 80	VCC

82C226 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max	Units
Supply Voltage	Vcc		7.0	V
Input Voltage	Vin	-0.5	Vcc+0.5V	
Storage Temperature	Tstg	-40	125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions described under operating conditions.

82C226 DC Characteristics

Operating Conditions: T_A = 0°C to 70°C, VCC = 4.75 to 5.25V

Parameter	Symbol	Min.	Max	Units
Input Low Voltage	Vil	-0.5	0.8	V
Input High Voltage	Vih	2.0	Vcc+0.5V	
Output Low Voltage	Vol		0.45	V(Note 1)
Output High Voltage	Voh	2.4		V(Note 1)
Input Leakage Current	Iil	-10	10	uA(Note 2)
Output Float Leakage Current	Ioz1	-10	10	uA(Note 3)
Power Supply Current				mA

Note 1:
Iol = 4mA and Ioh = -4mA for INTR, AUDIO, -WDT, -PDPRD, -CDSTUPi, -P76ENB.
Iol = 8mA and Ioh = -8mA for XDi.
Iol = 24mA and Ioh = -15 mA for PPi, CHRST.
Iol = 20mA for -STROBEO, -ATFDXTO, -INITO, -SLCTINO.

Note 2:
0 < Vin < Vcc

Note 3:
0.45 < Vout < Vcc

CPU INTERFACE		Min	Max	Units
t600	Address setup to command active	30		ns
t601	Command active period	100		ns
t602	Address hold time from command inactive	0		ns
t603	Data valid delay		100	ns
t604	Data hold time from XIOR inactive	0		ns
t605	Tristate to driving D8-D0 from XIOR active	5	40	ns
t606	Data setup time XIOW inactive	80		ns
t607	Data hold time from XIOW inactive	0		ns
t608	XIOR, XIOW Command recovery time	90		ns

INTERRUPT CONTROLLER TIMING		Min	Max	Units
t620	Interrupt output delay		300	ns
t621	End of INTA to next INTA within an INTA sequence only	80		ns

REAL TIME CLOCK		Min	Max	Units
t630	Real time clock cycle time		500	ns
t631	PSRSTB High Delay from Vcc	5		us
t632	PSRSTB Low Pulse Width	5		us
t633	VRT Bit Valid Delay		2	us

TIMERS		Min	Max	Units
t640	TMRCLK Period	100		ns
t641	TMRCLK low time	50		ns
t642	TMRCLK high time	50		ns
t643	TMRCLK low to NMI active	200		ns

PARALLEL PORT		Min	Max	Units
t650	Data output delay from XIOW high	20		ns
t651	Data setup time to XIORD	15		ns
t652	Data hold time from XIORD	10		ns
t653	CTRL/STATUS setup to XIORD high	20		ns
t654	CTRL/STATUS hold from XIORD high	10		ns

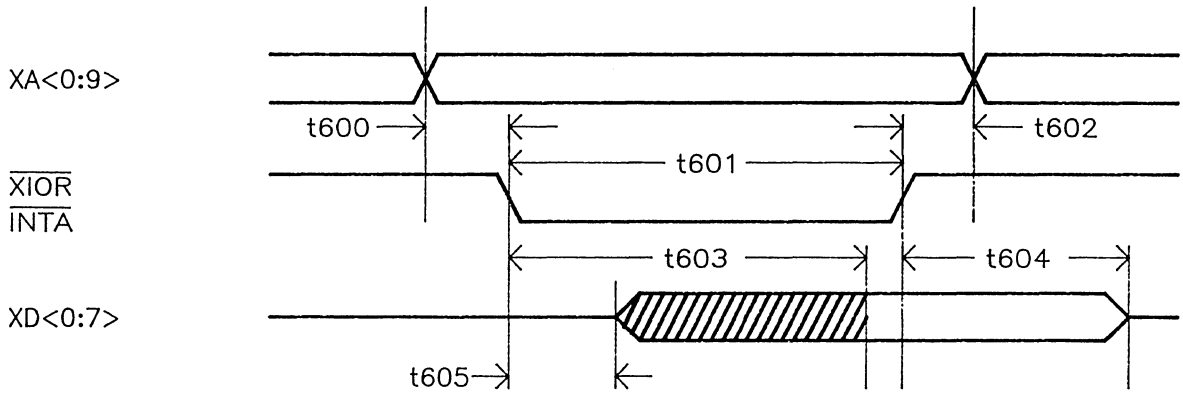


Figure 10.1 226 PERIPHERAL READ/INTA CYCLE

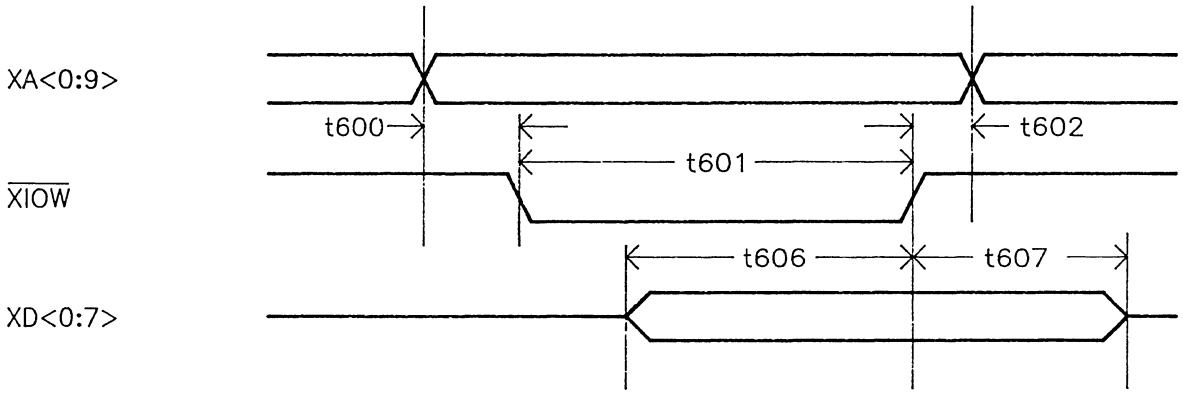


Figure 10.2 226 PERIPHERAL WRITE CYCLE

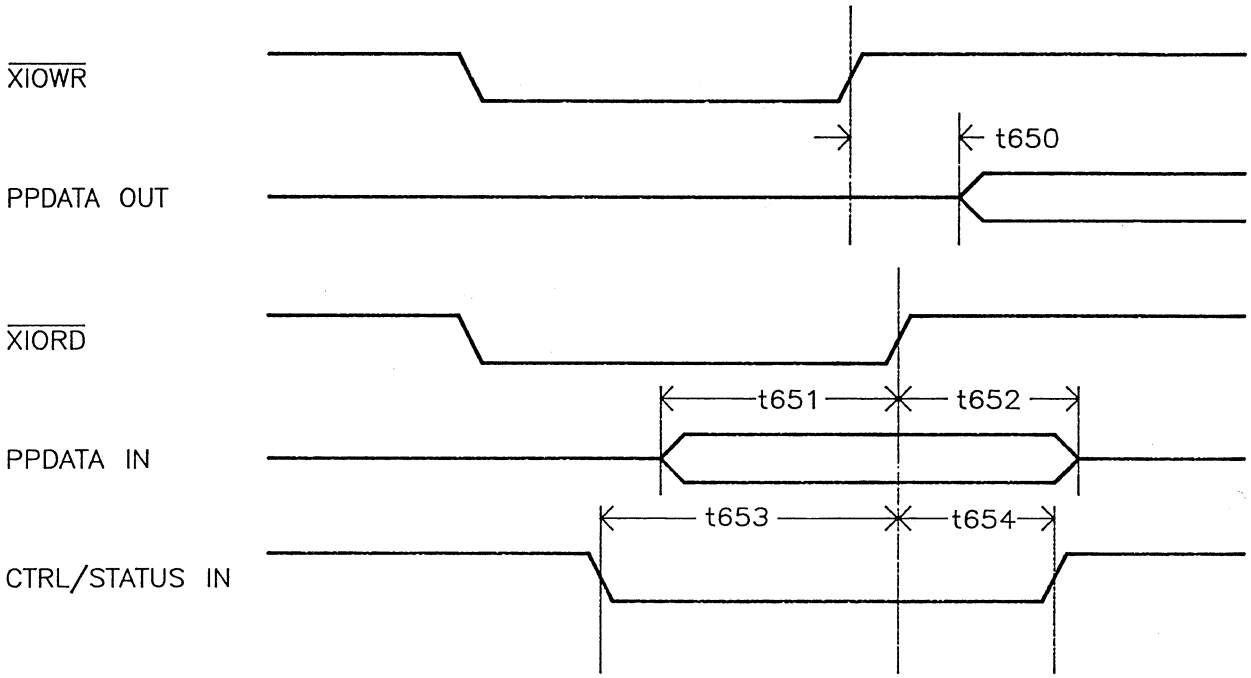


Figure 10.3 PARALLEL PORT

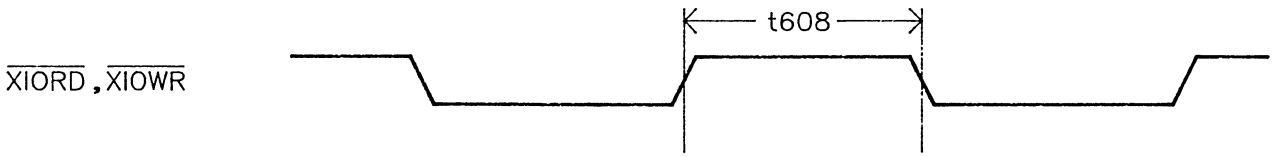


Figure 10.4 226 COMMAND RECOVERY

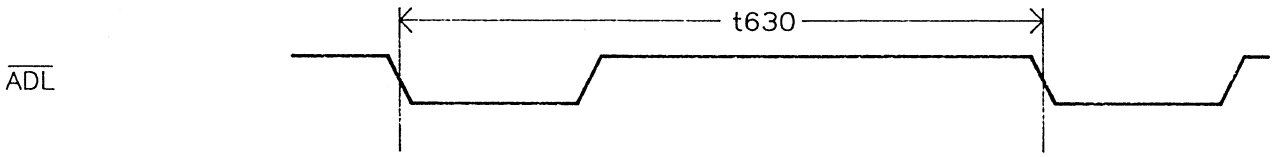


Figure 10.5 226 RTC ACCESS

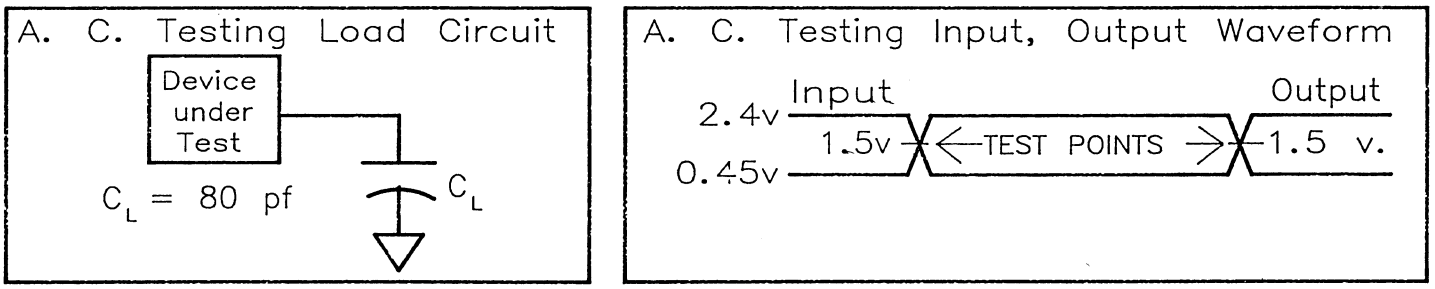

A. C. Testing Load Circuit
Device under Test
C_L = 80 pf
C_L
A. C. Testing Input, Output Waveform
Input
Output
2.4v
1.5v
0.45v
TEST POINTS
1.5 v.

Figure 10.9

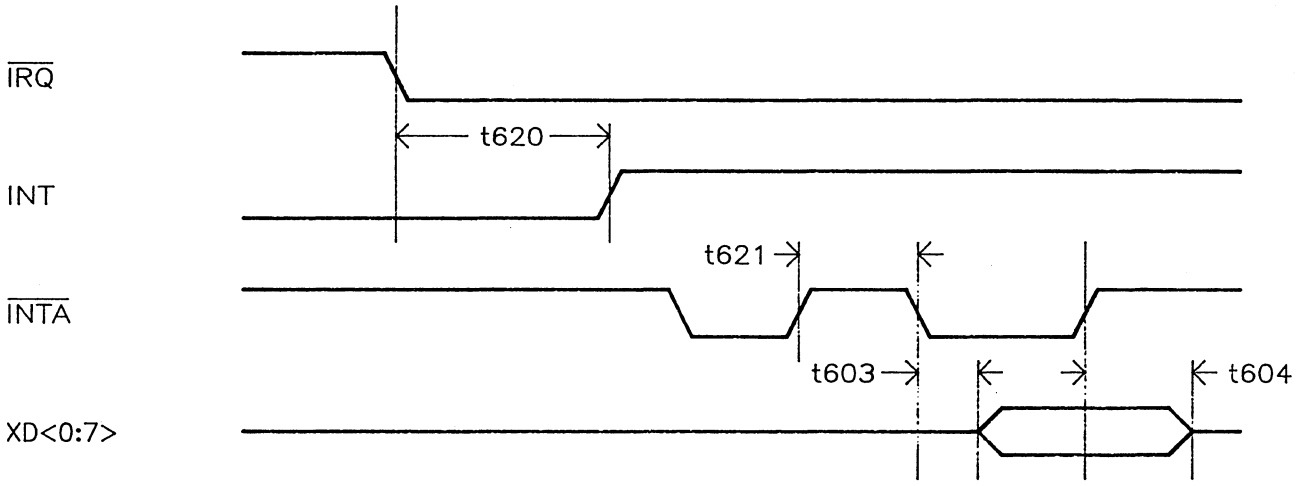


Figure 10.6 INTA SEQUENCE

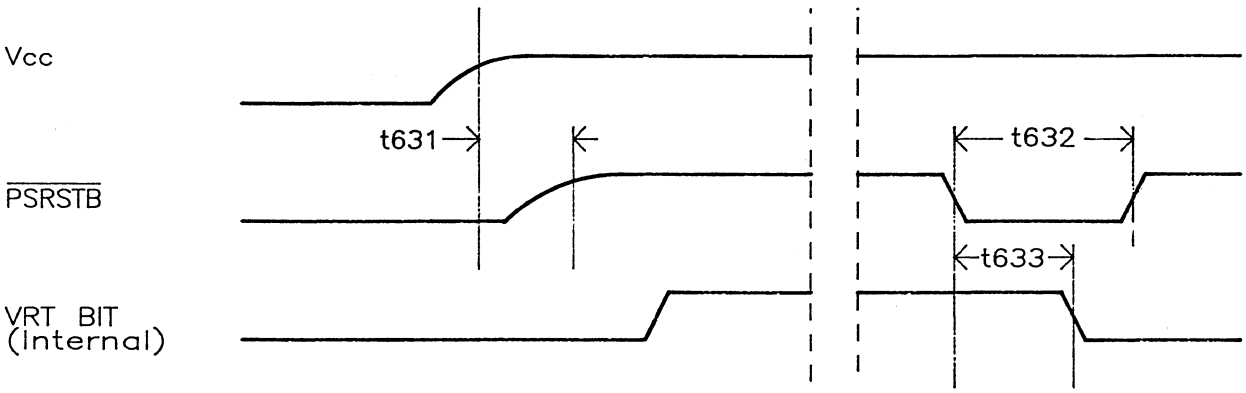


Figure 10.7 226 REAL TIME CLOCK POWER-UP SEQUENCE

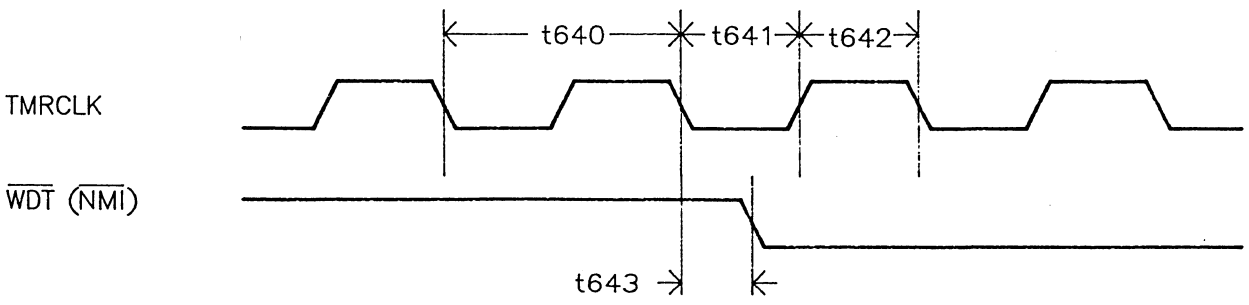
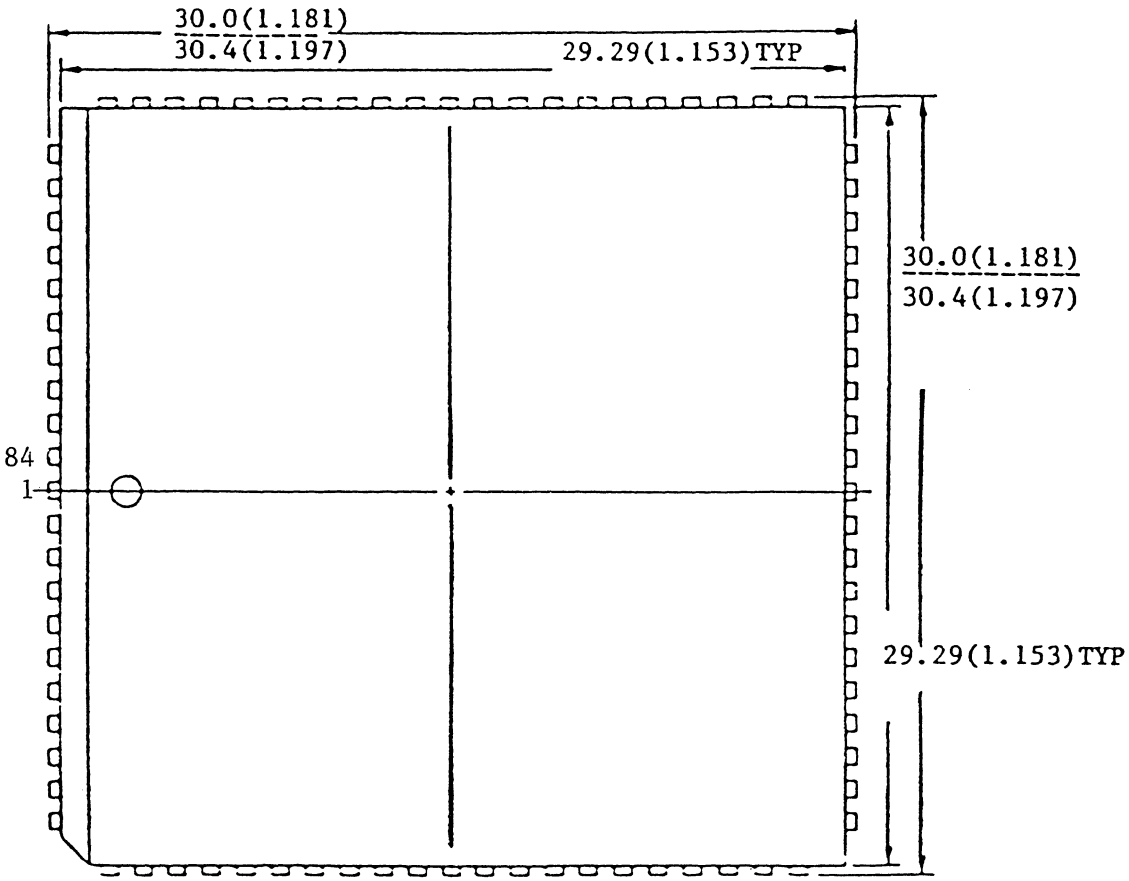
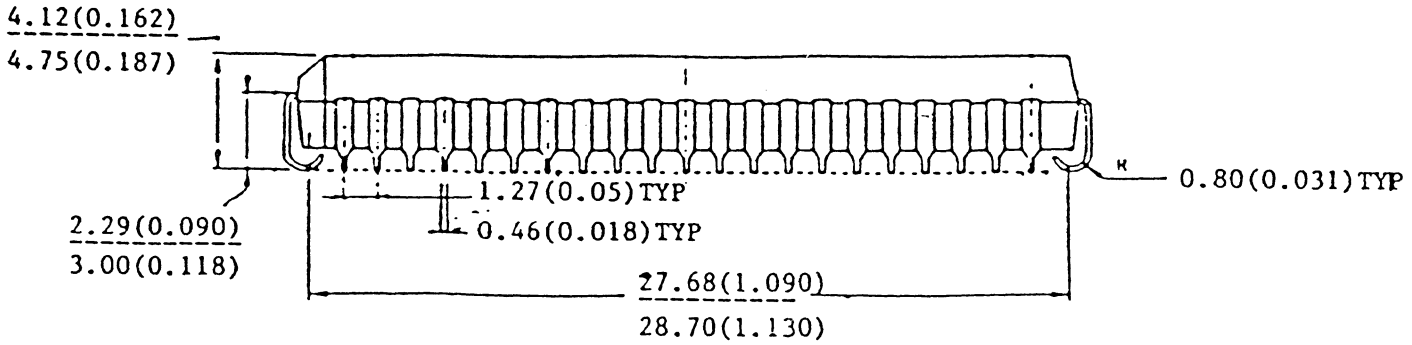


Figure 10.8 WATCHDOG TIMER

84-Pin Plastic Leaded Chip Carrier (PLCC)
Socket = AMP 821573-1 or Equivalent





Dimensions: mm (in)

100-Pin Plastic Flat Pack (Rectangular) (PFP)