82C100
IBM™ PS/2 Model 30 and Super XT™ Compatible Chip

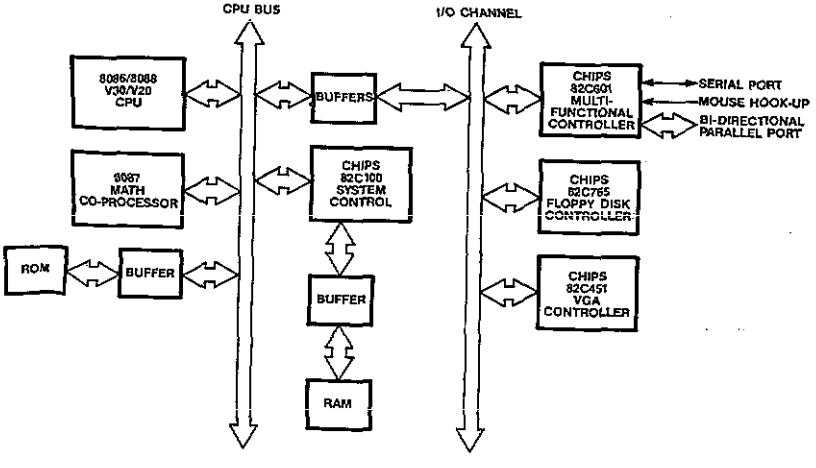
- **100% PC/XT compatible**
- **Build IBM PS/2™ Model 30 with XT software compatibility**
- **Bus Interface compatible with 8086, 80C86, V30, 8088, 80C88, V20**
- **Includes all PC/XT functional units compatible with:**

  8284, 8288, 8237, 8259, 8254, 8255, DRAM control, SRAM control, Keyboard control, Parity Generation and Configuration registers

- **Key superset features: EMS control, dual clock, and power management**
- **Complete system requires 12 ICs plus memory**
- **10 MHz Zero wait state operation**
- **Applicable for high performance Desktop PCs, Laptop PCs and CMOS Industrial Control Applications**
- **Single chip implementation available in 100-pin flat pack**

The 82C100 is a single chip implementation of most of the system logic necessary to implement a super XT compatible system with PS/2 Model 30 functionality using either an 8086 or 8088 microprocessor. The 82C100 can be used with either 8 or 16-bit microprocessors. The 82C100 includes features which will enable the PC manufacturer to design a super PS/2 Model 30/XT compatible system with the *highest performance* at 10 MHz zero wait state system with an 8086, the *highest functionality* with dual clock and 2.5 MB DRAM (with integrated Extended Memory System control logic), the *lowest power* implementation by utilizing the on-chip power management features and the *highest integration* with the lowest component count SMT design.

The 82C100 can be combined with CHIPS' 82C601 Multifunction Controller and 82C451 VGA Graphics Controller to provide a high performance, high integration PS/2 Model 30 type system.



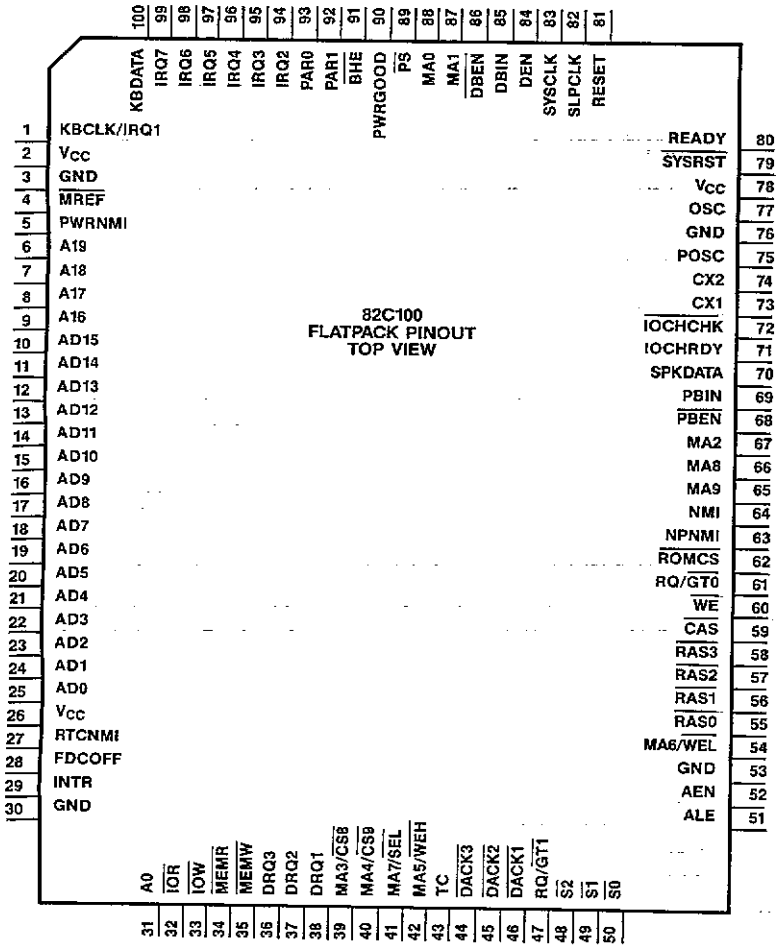
Super XT Model 30 Compatible System

The 82C100 supports most of the peripheral functions on the PS/2 Model 30 planar board: 8284 compatible clock generator with the option of 2 independent oscillators, 8288 compatible bus controller, 8237 compatible DMA controller, 8259 compatible interrupt controller, 8254 compatible timer/counter, 8255 compatible peripheral I/O port, XT Keyboard interface, Parity Generation and Checking for DRAM memory and memory controller for DRAM and SRAM memory sub-systems.

The 82C100 enables the user to add PS/2 Model 30 superset functionality on the planar board: dual clock with synchronized switching between the two clocks, built-in Lotus-Intel-Microsoft™ (LIM) EMS support for up to 2.5 Megabytes of DRAM and power management features for SLEEP mode as well as SUSPEND/RESUME operations. The SLEEP and SUSPEND/RESUME features help in preserving the battery life in laptop portable applications.

The 82C100 supports a very flexible memory architecture. For systems with DRAMs, the DRAM controller supports 64K, 256K and 1M DRAMs. These DRAMs can be organized in four banks of up to a maximum of 2.5 MB on the planar board. The 2.5 MB memory can be implemented with 2 banks of 1M × 1 DRAMs, partitioned locally as 640KB of real memory and 1.875MB of EMS memory. For systems which require low operating power and minimum standby power dissipation, the chips provide the decode logic which in conjunction with external decoders allows selection of up to 640KB of static RAM. This option is useful in laptop portable applications.

The 82C100 is packaged in a 100-pin plastic flatpack.


82C100
FLATPACK PINOUT
TOP VIEW
1 KBCLK/IRQ1
2 VCC
3 GND
4 MREF
5 PWRNMI
6 A19
7 A18
8 A17
9 A16
10 AD15
11 AD14
12 AD13
13 AD12
14 AD11
15 AD10
16 AD9
17 AD8
18 AD7
19 AD6
20 AD5
21 AD4
22 AD3
23 AD2
24 AD1
25 AD0
26 VCC
27 RTCNMI
28 FDCOFF
29 INTR
30 GND
31 A0
32 IOR
33 IOW
34 MEMR
35 MEMW
36 DRQ3
37 DRQ2
38 DRQ1
39 MA3/CS8
40 MA4/CS9
41 MA7/SEL
42 MA5/WEH
43 TC
44 DACK3
45 DACK2
46 DACK1
47 RQ/GT1
48 S2
49 S1
50 S0
51 ALE
52 AEN
53 GND
54 MA6/WEL
55 RAS0
56 RAS1
57 RAS2
58 RAS3
59 CAS
60 WE
61 RQ/GT0
62 ROMCS
63 NPNMI
64 NMI
65 MA9
66 MA8
67 MA2
68 PBEN
69 PBIN
70 SPKDATA
71 IOCHRDY
72 IOCHCHK
73 CX1
74 CX2
75 POSC
76 GND
77 OSC
78 VCC
79 SYSRST
80 READY
81 RESET
82 SLPCLK
83 SYSCLK
84 DEN
85 DBIN
86 DBEN
87 MA1
88 MA0
89 PS
90 PWRGOOD
91 BHE
92 PAR1
93 PAR0
94 IRQ2
95 IRQ3
96 IRQ4
97 IRQ5
98 IRQ6
99 IRQ7
100 KBDATA

82C100 Pin Description

Pin No.	Pin Type	Symbol	Pin Description
Clocks and Reset Logic			
73	I	CX1	**Crystal/oscillator input.** CX1 is an input for a passive crystal circuit or packaged oscillator to generate the initial system timings. This frequency is divided by three to generate the default system clock when the system is powered up. The type of crystal is 14.31818 MHz, parallel resonance, fundamental frequency.
74	O	CX2	**Crystal/oscillator output.** CX2 is the inverted output of CX1. If a crystal is used, then CX2 should be connected to the crystal circuit. If an oscillator is used, then CX2 should be left unconnected.
75	I	POSC	**Optional Oscillator input.** The POSC input is divided by three to generate alternate system timing (other than 4.77 MHz). Typically POSC is a 24 MHz or 30 MHz oscillator with a 50% duty cycle, for 8 MHz or 10 MHz sytems, respectively. The maximum POSC frequency is 30 MHz. System timing is software selectable from the configuration register.
83	O	SYSCLK	**System Clock.** SYSCLK is a continuous running clock with selectable frequency and duty cycle. The duty cycle is either 33% for INTEL 808X CPUs, or 50% for NEC V20/30 CPUs. The SYSCLK frequency is selected from either 1/3 of the POSC or 1/3 of the CX1 frequencies. The default is 4.77 MHz, 33% duty cycle.
82	O	SLPCLK	**Sleep Clock Output.** SLPCLK is similar to SYSCLK, except that SLPCLK can be disabled through software. SLPCLK provides the clock for the CPU and other static devices. In the OFF state it is LOW and the default is enabled.
77	O	OSC	**Oscillator output.** OSC is a continuous running square wave with a 50% duty cycle, derived from the frequency generated by CX1. Normally this is used for the 14.3818 MHz.
90	I	PWRGOOD	**Power Good.** An active high indicator that the power supply is stable, it also starts the clocks and the internal system functions. PWRGOOD is generated by the power supply, by monitoring V_{CC}.
89	I	$\overline{PS}$	**Power Sense.** An active low input which indicates the system configuration is invalid, due to a power loss. An active low level on $\overline{PS}$ and $\overline{SYSRST}$ resets the 82C100 internal ports and configuration registers to their default values. If power has been lost, $\overline{PS}$ must be held low until PWRGOOD is high and $\overline{SYSRST}$ has returned high.

82C100 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Pin Description
79	I	$\overline{\text{SYSRST}}$	**System Reset.** $\overline{\text{SYSRST}}$ is an active low Schmitt trigger input for power-up reset. $\overline{\text{SYSRST}}$ initializes the 82C100 circuitry (but not the registers which are initialized by $\overline{\text{PS}}$). This signal also generates the RESET output used to reset the CPU, 8087 and other peripherals. It should be held active until PWRGOOD becomes active.
28	O	FDCOFF	**Floppy Disk Controller OFF.** FDCOFF is a programmable output, normally LOW. If FDCOFF is enabled (by a bit in a configuration register), and sleep mode is entered, the FDCOFF output pin will go high. This condition causes the FDC and other peripherals to be disabled, thus reducing power consumption. FDCOFF should be connected to FDC and other chip enable pins.
CPU Interface			
81	O	RESET	**RESET.** RESET is an active high output derived from the $\overline{\text{SYSRST}}$ input. RESET should be used to reset the CPU, the 8087, and the external peripherals.
48	I	$\overline{\text{S2}}$	**Processor Status Signals.** These signals are status inputs from the CPU. $\overline{\text{S0}}$-$\overline{\text{S2}}$ should be pulled up with 4.7K-10K resistors.
49	I	$\overline{\text{S1}}$	
50	I	$\overline{\text{S0}}$	
91	I	$\overline{\text{BHE}}$	**Byte High Enable.** $\overline{\text{BHE}}$ is an input signal. $\overline{\text{BHE}}$ and A0 from the CPU indicate the type of bus transfer.

$\overline{\text{BHE}}$	A0	Type
0	0	16 bit transfer
0	1	odd byte transfer
1	0	even byte transfer
1	1	invalid (for 16 bit CPU)

If the 82C100 is used with an 8 bit processor, $\overline{\text{BHE}}$ should be tied high through a 4.7K to 10K resistor. The 82C100 uses the "invalid" state to perform the correct bus conversion for an 8 bit processor. $\overline{\text{BHE}}$ is floated to the high impedance state during "hold" cycles, so it should be pulled up with 4.7K-10K resistor.

80	O	READY	**READY.** READY is an active high, asynchronous output indicates that a memory or I/O transfer can complete. READY is internally synchronized to meet the setup/hold times of the processor.

82C100 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Pin Description
29	O	INTR	**Interrupt Request.** INTR is an active high output from the internal Interrupt Controller. It should be connected to the INTR pin of the CPU.
64	O	NMI	**Non-Maskable Interrupt.** A LOW to HIGH transition on NMI causes an interrupt at the end of the current instruction. It should be connected to the NMI input of the CPU.
61	B	RQ/$\overline{GT0}$	**Request/Grant.** These signals are used by bus masters other than the CPU to gain control of the CPU local bus. In the Model 25/30 or XT application,the other bus masters are the 8087 numeric co-processor, and the 82C100 itself. RQ/$\overline{GT0}$ has higher priority than RQ/$\overline{GT1}$. 808X RQ/$\overline{GT}$ signals are internally pulled up, so external pullups are not necessary. See the Request/Grant section of this data sheet for more information.
47	B	RQ/$\overline{GT1}$	
Local Bus Interface			
6	B	A19	**Address Bits A19-16.** During processor cycles, these are inputs for the high order address bits. During DMA cycles, the 82C100 sources the high order address on these lines. These should be connected directly to the processor address lines and to the system address latches.
7	B	A18	
8	B	A17	
9	B	A16	
10	B	AD15	**Local Address/Data Bus Bits 15:0.** During the T1 phase of a CPU cycle the processor sources the address on these lines. The 82C100 sources the address during hold acknowledge and interrupt acknowledge cycles. AD0-AD7 should be isolated from the 82C100 using bidirectional buffers to prevent bus contention during bus conversion cycles. $\overline{PBEN}$ enables the buffers and PBIN controls the direction.
11	B	AD14	
12	B	AD13	
13	B	AD12	
14	B	AD11	
15	B	AD10	
16	B	AD9	
17	B	AD8	
18	B	AD7	
19	B	AD6	
20	B	AD5	
21	B	AD4	
22	B	AD3	
23	B	AD2	
24	B	AD1	
25	B	AD0	
31	O	A0	**Address Bit 0.** This signal represents the state of address bit 0. It is latched and should be used throughout the system instead of AD0 that would normally be latched externally from the AD bus. The 82C100 toggles this bit *during bus conversion cycles. It should be buffered (in a* normal system) but not routed through transparent latches like the other address bits.

82C100 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Pin Description
32	O	$\overline{IOR}$	**I/O Read.** An active low strobe that informs the I/O devices to put their data on the bus. All the commands ($\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$, and $\overline{IOW}$) can be delayed one cycle through software. The delay is necessary when running the CPU at high speed. Delaying the commands allow more data and address setup time. Default is no delay.
33	O	$\overline{IOW}$	**I/O Write.** An active low strobe that informs the I/O devices that data is available on the bus.
34	O	$\overline{MEMR}$	**Memory Read.** An active low strobe that informs the memory devices to put their data on the bus.
35	O	$\overline{MEMW}$	**Memory Write.** An active low strobe that informs the memory devices that data is available on the bus.
51	O	ALE	**Address Latch Enable.** ALE is used by the address buffer/ latch to latch the address. During the second half of a bus conversion cycle, a second ALE will not be generated by the 82C100.
52	O	AEN	**Address Enable.** When high, this signal is an indication to the devices on the I/O channel that DMA is active, meaning the DMA channel has control of the address bus, data bus, and the appropriate command lines.
84	O	DEN	**Data Enable.** Provided to control the output enable of 245 type transceiver. DEN is active during memory and I/O accesses and for INTA cycles. It floats to the high impedance state in "hold acknowledge" cycles. This signal is equivalent to the DEN signal generated by an 8288 bus controller. It is normally not used in XT/Model 30 type applications.
93	B	PAR0	**Parity Bit 0.** The parity bit from the low order byte of the DRAMs. A HIGH means there are an odd number of 1's in memory, including the parity bit itself, thus odd parity.
92	B	PAR1	**Parity Bit 1.** The parity bit from the high order byte of the DRAMs. A HIGH means there are an odd number of 1's in memory, including the parity bit itself, thus odd parity. This signal is not used in 8 bit only systems.
71	I	IOCHRDY	**I/O Channel Ready.** An active high signal from the I/O channel. It is normally HIGH indicating that the addressed device on the channel is ready to complete the data transfer. Slow I/O or memory devices pull this signal LOW to lengthen bus cycles. IOCHRDY should be pulled up with a 4.7K resistor, because if there are no add-in boards present, this signal would float to an undefined state.

82C100 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Pin Description
72	I	IOCHCHK	**I/O Channel Check.** This signal goes low when there is parity or other error on memory or devices on the I/O channel. IOCHCHK should be pulled up with a 4.7K resistor, because if there are no add-in boards present, this signal would float to an undefined state.
Buffer Controls			
86	O	DBEN	**Data Buffer Enable.** DBEN enables the data transceiver between the I/O channel data bus and 82C100.
85	O	DBIN	**Data Buffer Direction.** A HIGH allows data to flow from the I/O channel to the internal bus. Normally low, this means the data direction is to the I/O channel. DBIN is used to control the direction of the buffer for the system data bus.
68	O	PBEN	**Processor Buffer Enable.** An active low signal, PBEN enables the data buffer between the processor and the 82C100. It is high during DMA cycles so that the data bus is tri-stated. PBEN is qualified with DEN to avoid bus contention during T2 cycles.
69	O	PBIN	**Processor Buffer Direction.** A HIGH on PBIN allows data to flow from the processor to the 82C100. PBIN controls the direction of the data buffer on the local data bus.
Memory Controls			
62	O	ROMCS	**ROM Chip Select.** This signal goes low for memory accesses in the address range F0000H-FFFFFH. It would normally be tied to the chip select inputs of the BIOS ROM(s).
Note: All DRAM signals (MA9-0, RAS3-0, CAS and WE should be buffered if connected to more than 9 memory devices)			
65	O	MA9	**Multiplex Address Bits 9 and 8.** Should be connected to DRAM address bits 9 and 8.
66	O	MA8	
Note: The following 5 pins have different functions depending on whether static RAMs or Dynamic RAMs are used with the 82C100. The functions change based on a bit in the configuration registers.			
41	O	MA7/SEL	DRAM: **Multiplex Address Bit 7.** Should be connected to DRAM address bit 7. SRAM: **Select.** An active low decode address range 0-640K (00000-9FFFFH).

82C100 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Pin Description
54	O	MA6/$\overline{WEL}$	DRAM: **Multiplex Address Bit 6.** Should be connected to DRAM address bit 6. SRAM: **Write Enable Low Bank.** An active low strobe that writes data to the low byte. Should be connected to the write enable of the low byte static RAMs.
42	O	MA5/$\overline{WEH}$	DRAM: **Multiplex Address Bit 5.** Should be connected to DRAM address bit 5. SRAM: **Write Enable High Bank.** An active low strobe that writes data to the high byte. Should be connected to the write enable of the high byte static RAMs.
40	O	MA4/$\overline{CS9}$	DRAM: **Multiplex Address Bit 4.** Should be connected to DRAM address bit 4. SRAM: **Chip Select 9.** An active low chip select for the address range 90000-9FFFFH. Should be connected to the chip selects of the SRAM located at address 90000-9FFFFH.
39	O	MA3/$\overline{CS8}$	DRAM: **Multiplex Address Bit 3.** Should be connected to DRAM address bit 3. SRAM: **Chip Select 8.** An active low chip select for the address range 80000-8FFFFH. Should be connected to the chip selects of the SRAM located at address 80000-8FFFFH.
67	O	MA2	**Multiplexed Address Bits 2-0.** These should be connected to DRAM address bits 2-0.
87	O	MA1	
86	O	MA0	
55	O	$\overline{RAS0}$	**$\overline{RAS3}$-0.** Active low row address strobes for DRAM banks 0-3. Each bank is 9 bits wide (1 bit for parity). Byte referencing is done using the $\overline{RAS}$ signal. For more information, see the DRAM Interface section of this data sheet.
56	O	$\overline{RAS1}$	
57	O	$\overline{RAS2}$	
58	O	$\overline{RAS3}$	
59	O	$\overline{CAS}$	**$\overline{CAS}$.** Active low column address strobe for all DRAMs.
60	O	$\overline{WE}$	**$\overline{WE}$.** Active low write enable for all DRAMs.
4	O	$\overline{MREF}$	**Memory Refresh.** $\overline{MREF}$ is the output of the independent refresh timer signifying that a refresh cycle is occurring. The refresh rate is programmable from 838 ns to 214 μs.
DMA and Interrupt Controller Interface			
36	I	DRQ3	**DMA Request 3-1.** These signals are asynchronous requests used by peripherals to request DMA services. They have a fixed priority: channel 1 is the highest and channel 3 is the lowest. DRQ must be held active HIGH until it is acknowledged by the corresponding DACK.
37	I	DRQ2	
38	I	DRQ1	

82C100 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Pin Description
44 45 46	O O O	$\overline{\text{DACK3}}$ $\overline{\text{DACK2}}$ $\overline{\text{DACK1}}$	**DMA Acknowledge 3-1.** An active low acknowledgement signal generated by the 82C100 as a result of a request for DMA service (via a DRQ line) and a successful arbitration. These lines must be pulled up with 10Kohm resistors.
43	O	TC	**Terminal Count.** An active high output pulse from the DMA Controller, indicating the end of a DMA transfer (transfer count register = 0).
94 95 96 97 98 99	I I I I I I	IRQ2 IRQ3 IRQ4 IRQ5 IRQ6 IRQ7	**Interrupt Request 2-7.** Active high asynchronous inputs to the interrupt controller generated by I/O devices. They are edge-triggered, but should be held active HIGH until acknowledged.
63	I	NPNMI	**Numeric Co-Processor NMI.** An active high signal indicating that an error has occurred during numeric instruction execution. This is an active high, edge-sensitive input. If enabled, will cause an NMI to the CPU. The NMI service routine has to determine which NMI occurred by reading the NMI Status Register.
27	I	RTCNMI	**Real Time Clock NMI.** When the Real Time Clock needs immediate attention, it can generate RTCNMI. This is an active high, edge-sensitive input. If enabled, will cause an NMI to the CPU. The NMI service routine has to determine which NMI occurred by reading the NMI Status Register.
5	I	PWRNMI	**Power Fail NMI.** A monitoring circuit generates PWRNMI when it detects imminent loss of power. This is an active high, edge-sensitive input. If enabled, will cause an NMI to the CPU. The NMI service routine has to determine which NMI occurred by reading the NMI Status Register.
Keyboard and Speaker Interface			
1	B	KBCLK/IRQ1	**Keyboard Clock/Interrupt Request 1.** KBCLK is a bidirectional open drain signal. Defaults to KBCLK when using an XT style keyboard. The 82C100 synchronizes the internal keyboard logic with this signal. It sources the clock for the keyboard when sending serial data to the keyboard and receives the clock when the keyboard is sending data. If an external Model 25/30 style keyboard interface is used (and selected through the Internal Configuration Register), IRQ1 is the shared, active high Interrupt Request 1 input from the keyboard controller, pointing device, and real time clock.
100	B	KBDATA	**Keyboard Data.** KBDATA is an open drain bidirectional serial data to or from the keyboard. This line is unused if a Model 25/30 external keyboard interface is used.

82C100 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Pin Description
70	O	SPKDATA	**Speaker Data.** SPKDATA should be buffered, and the output of the buffer should go through a low pass filter. The output of the filter connects to the speaker.
Power and Grounds			
2,26,78	—	V_{CC}	**Power Supply.**
3,30, 53,76	—	GND	**Ground.**

Notes:
1. The 82C100 provides four RAS signals to select which byte will be written. A single CAS and WE is provided for all banks.
2. PAR1 is provided for 16 bit 8086 systems with DRAM. Usage of this is determined by setting of the internal configuration registers.
3. BHE is provided for 8086 systems.
4. A packaged oscillator is assumed for the processor clock if the CPU clock is above 4.77MHz (14.318MHz/3).
5. The following explains the abbreviations used in the pin type/direction column.

Pin	Meaning
I	Input B
B	Input and Output (3-state)
O	Output

Functional Description

The 82C100 is a single chip VLSI implementation of most of the system logic for Enhanced or Super XT designs. It can also be used to build systems that are functional equivalents of the IBM Model 25/30, but with 100% XT compatibility. The device contains the equivalent of the 8288 Bus Controller, 8284 Clock Generator, 10 MHz 8237 DMA Controller, 8259 Interrupt Controller, 8255 Programmable Peripheral Interface, 8254 Programmable Interval Timer, Memory Controller, EMS Controller, and offers enhanced features such as Power Management Logic, Data Conversion Logic, Programmable Internal Configuration Registers, Programmable Wait States for Memory, I/O, and DMA, and Decoding Logic.

SYSTEM CLOCK

The system clock circuit is functionally equivalent to the 8284 clock generator with the addition of logic to support 2 different clock frequencies. One is generated from the standard 14.318MHz crystal or oscillator. The other is optional and allows the processor and IO channel to operate at frequencies up to 10 MHz. This is generated by an external oscillator and must be 3 times the desired processor clock frequency (for example a 10 MHz CPU clock requires a 30 MHz oscillator). Additional logic is also included to generate two system clocks, a continuously running clock (SYSCLK) and a software controlled clock (SLPCLK). SYSCLK provides uninterrupted timing pulses at the maximum clock frequency. In a lap-top or other application where current consumption must be minimized, SLPCLK is used to clock the processor and other system logic that does not require constant operation. SLPCLK can be stopped using a BIOS function call that causes the processor to enter standby mode to conserve battery power.

All the system clock outputs are started when PWRGOOD is true (high). When PWRGOOD is false, all clock outputs are low.

BUS CONTROLLER

The bus controller is functionally equivalent to the 8288 bus controller. It provides command generation and controls the timing of the internal bus and I/O channel, including logic for command delays (commands will be active at T3 instead of T2). The I/O channel timing is the same as the system timing—that is 10 MHz bus timing for 10 MHz systems. The wait states for memory, I/O and DMA cycles are programmable for flexibility. The bus controller module is enabled by $\overline{\text{SYSRST}}$ going high. As long as $\overline{\text{SYSRST}}$ is low, the bus controller is inactive. For proper operation $\overline{\text{SYSRST}}$ should stay low for a minimum of 200 milliseconds after PWRGOOD is high.

Local Bus Arbitration

The local processor bus is a multi-master bus and is shared between the CPU, numeric coprocessor, and the 82C100. Normally the CPU is the active bus master, but the other masters can force the CPU to release the local bus using the RQ/$\overline{\text{GT}}$ line. If the coprocessor is present (ICR 43H bit 1 is 1) the 82C100 uses RQ/$\overline{\text{GT1}}$ for the bus exchange, otherwise it uses the RQ/$\overline{\text{GT0}}$ line. Because of this, a co-processor can be installed or removed without the need for changing jumpers.

RQ/$\overline{\text{GT0}}$ from the 82C100 should be connected to RQ/$\overline{\text{GT0}}$ of the CPU. RQ/$\overline{\text{GT1}}$ from the 82C100 should be connected to RQ/$\overline{\text{GT1}}$ of the co-processor, and RQ/$\overline{\text{GT1}}$ of the CPU to RQ/$\overline{\text{GT0}}$ of the coprocessor.

The sequence of events on the RQ/$\overline{\text{GT}}$ lines is as follows:

1. Another bus master makes a bus request to the CPU by asserting a one clock wide pulse in any bus cycle on a RQ/$\overline{\text{GT}}$ line.
2. The CPU responds by asserting a pulse during T4 or Ti, also one clock wide. This indicates to the requestor that the CPU will float the local bus and enter the "hold acknowledge" state in the next clock cycle, disconnecting the CPU from the local bus. The requestor now can take control of the bus.
3. When finished, the requesting master asserts another pulse to the CPU, and relinquishes control of the local bus at the next clock.

Each master to master bus exchange requires three pulses. After each bus exchange there must be one dead cycle for synchronizing purposes. Requests can occur when CPU is idle or during a memory cycle.

If a request is made during a memory cycle, the CPU releases control at T4 when the following conditions are met:

a. Request occurs in or before T2
b. Not executing a LOCKed instruction
c. Not in the first INTA sequence
d. Not in the first byte of a bus conversion cycle.

If request is made when CPU is idle, the CPU will:

a. Release the bus on the next clock
b. The DMA cycle will start within the next three clock cycles.

DMA CONTROLLER

The 82C100's DMA controller is functionally equivalent to the 8237 DMA controller. It has 4 DMA channels, address increment/decrement and masking of individual DMA requests. The DMA controller supports single, block, demand and memory to memory transfer modes. All DMA data transfers require 5 clock cycles per byte. The DMA controller does not support cascading.

DMA controller generates the memory address and control signals necessary to transfer information between a peripheral device and memory directly. Each DMA channel has a pair of 16-bit counters and a reload register for each counter. The 16-bit counters allow the DMA to transfer blocks as large as 65,536 bytes.

During normal operation, the DMA subsystem will be in either the Idle condition, the Program condition or the Active condition. In the Idle condition the DMA controller will be executing cycles consisting of only one state. The idle state SI is the default condition and the DMA will remain in this condition unless the device has been initalized and one of the DMA requests is active or the CPU attempts to access one of the internal registers.

When a DMA request becomes active the device enters the Active condition and issues a hold request to the system. Once in the Active condition the 82C100 will generate the necessary memory addresses and command signals to accomplish a memory-to I/O, I/O-to-memory, or a memory-to-memory transfer. Memory-to-I/O and I/O-to-memory transfers take place in one cycle while memory-to-memory transfers require two cycles. During transfers between memory and I/O, data is presented on the system bus by either memory or the requesting device and the transfer is completed in one cycle. Memory-to-memory transfers however, require the DMA to store data from the read operation in an internal register. The contents of this register is then written to memory on the subsequent cycle.

Due to the large number of internal registers in the DMA subsystem, an internal flip-flop is used to supplement the addressing of the count and address registers. This bit is used to select between the high and low bytes of these registers. The flip-flop will toggle each time a read or write occurs to any of the word count or address registers in the DMA. This internal flip-flop will be cleared by hardware RESET or a Master Clear command and may be set or cleared by the CPU issuing the appropriate command.

Figure 1 shows all the register information necessary to program DMA controller. Special commands are supported by the DMA subsystem to control the device. These commands do not make use of the data bus, but are derived from a set of addresses, the internal select, read and write. These commands are Master Clear Register, Clear Mask Register, Clear Mode Register Counter, Set and Clear Byte Pointer Flip-Flop. These are discussed later.

ADDRESS	OPERATION			
ADDRESS	READ	WRITE	Flip-Flop	Register Function
000h	0	1	0	Read Channel 0 Current Address Low Byte
	0	1	1	Read Channel 0 Current Address High Byte
	1	0	0	Write Channel 0 Base and Current Address Low Byte
	1	0	1	Write Channel 0 Base and Current Address High Byte
001h	0	1	0	Read Channel 0 Current Word Count Low Byte
	0	1	1	Read Channel 0 Current Word Count High Byte
	1	0	0	Write Channel 0 Base and Current Word Count Low Byte
	1	0	1	Write Channel 0 Base and Current Word Count High Byte
002h	0	1	0	Read Channel 1 Current Address Low Byte
	0	1	1	Read Channel 1 Current Address High Byte
	1	0	0	Write Channel 1 Base and Current Address Low Byte
	1	0	1	Write Channel 1 Base and Current Address High Byte
003h	0	1	0	Read Channel 1 Current Word Count Low Byte
	0	1	1	Read Channel 1 Current Word Count High Byte
	1	0	0	Write Channel 1 Base and Current Word Count Low Byte
	1	0	1	Write Channel 1 Base and Current Word Count High Byte
004h	0	1	0	Read Channel 2 Current Address Low Byte
	0	1	1	Read Channel 2 Current Address High Byte
	1	0	0	Write Channel 2 Base and Current Address Low Byte
	1	0	1	Write Channel 2 Base and Current Address High Byte
005h	0	1	0	Read Channel 2 Current Word Count Low Byte
	0	1	1	Read Channel 2 Current Word Count High Byte
	1	0	0	Write Channel 2 Base and Current Word Count Low Byte
	1	0	1	Write Channel 2 Base and Current Word Count High Byte
006h	0	1	0	Read Channel 3 Current Address Low Byte
	0	1	1	Read Channel 3 Current Address High Byte
	1	0	0	Write Channel 3 Base and Current Address Low Byte
	1	0	1	Write Channel 3 Base and Current Address High Byte
007h	0	1	0	Read Channel 3 Current Word Count Low Byte
	0	1	1	Read Channel 3 Current Word Count High Byte
	1	0	0	Write Channel 3 Base and Current Word Count Low Byte
	1	0	1	Write Channel 3 Base and Current Word Count High Byte
008h	0	1	X	Read Status Register
	1	0	X	Write Command Register
009h	0	1	X	Read DMA Request Register
	1	0	X	Write DMA Request Register
00Ah	0	1	X	Read Command Register
	1	0	X	Write Single Bit DMA Request Mask Register
00Bh	0	1	X	Read Mode Register
	1	0	X	Write Mode Register

Figure 1. DMA Registers

ADDRESS	OPERATION			
ADDRESS	READ	WRITE	Flip-Flop	Register Function
00Ch	0	1	X	Set Byte Pointer Flip-Flop
	1	0	X	Clear Byte Pointer Flip-Flop
00Dh	0	1	X	Read Temporary Register
	1	0	X	Master Clear
00Eh	0	1	X	Clear Mode Register Counter
	1	0	X	Clear All DMA Request Mask Register Bits
00Fh	0	1	X	Read All DMA Request Mask Register Bits
	1	0	X	Write All DMA Request Mask Register Bits

Figure 1. DMA Registers (continued)

Register Description

Current Address Register

Each DMA channel has a 16-bit Current Address Register which holds the address used during transfers. Each channel can be programmed to increment or decrement this register whenever a transfer is completed. This register can be read or written by the CPU in consecutive 8-bit bytes.

Current Word Count Register

Each channel has a Current Word Count Register which determines the number of transfers to perform. The actual number of transfers performed will be one greater than the value programmed into the register. The register is decremented after each transfer until it goes from zero to FFFFh. When this roll-over occurs the 82C100 will generate T/C.

Base Address Register

Associated with each Current Address Register is a Base Address Register. This is a write only register which is loaded by the CPU when writing to the Current Address Register. The purpose of this register is to store the initial value of the Current Address Register.

Base Word Count Register

This register preserves the initial value of the Current Word Count Register. It is also a write only register which is loaded by writing to the Current Word Count Register.

Command Register

This register controls the overall operation of a DMA subsystem. The register can be read or written by the CPU and is cleared by either RESET or a Master Clear command.

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
DAK	DRQ	EW	RP	CT	CD	AH	M-M

DAK—DACK active level is determined by bit 7. Programming a 1 in this bit position makes DACK an active high signal.

DRQ—DREQ active level is determined by bit 6. Writing a 1 in this bit position causes DREQ to become active low.

EW—Extended Write is enabled by writing a 1 to bit 5, causing the write commands to be asserted one DMA cycle earlier during a transfer.

RP—Writing a 1 to bit 4 causes the 82C100 to utilize a rotating priority scheme for honoring DMA requests. The default condition is fixed priority.

CT—Compressed timing is enabled by writing a 1 to bit 3 of this register. The default 0 condition causes the DMA to operate with normal timing.

CD—Bit 2 is the master disable for the DMA controller. Writing a 1 to this location disables the DMA subsystem. This function is normally used whenever the CPU needs to reprogram one of the channels to prevent DMA cycles from occuring.

AH—Writing a 1 to bit 1 enables the address hold feature in Channel 0 when performing memory-to-memory transfers.

M-M—A 1 in the bit 0 position enables Channel 0 and Channel 1 to be used for memory-to-memory transfers.

Mode Register

Each DMA channel has a Mode Register associated with it. All four Mode Registers reside at the same I/O address. Bits 0 and 1 of the Write Mode Register command determine which channel's Mode Register gets written. The remaining six bits control the mode of the selected channel. Each channel's Mode Register can be read by sequentially reading the Mode Register location. A Clear Mode Register Counter command is provided to allow the CPU to restart the mode read process at a known point. During mode read operations, bits 0 and 1 will both be 1.

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
M1	M0	DEC	AI	TT1	TT0	CS1	CS0

(Read/Write Register)

M1-M0—Mode selection for each channel is accomplished by bits 6 and 7.

M1	M0	MODE
0	0	Demand Mode
0	1	Single Cycle Mode
1	0	Block Mode
1	1	Cascade Mode

DEC—Determines direction of the address counter. A one in bit 5 decrements the address after each transfer.

AI—The Autoinitialization function is enabled by writing a 1 in bit 4 of the Mode Register.

TT1-TT0—Bits 2 and 3 control the type of transfer which is to be performed.

TT1	TT0	TYPE
0	0	Verify Transfer
0	1	Write Transfer
1	0	Read Transfer
1	1	Illegal

CS1-CS0—Channel Select bits 1 and 0 determine which channel's Mode Register will be written. Read back of a mode register will result in bits 1 and 0 both being ones.

CS1	CS0	CHANNEL
0	0	Channel 0 select
0	1	Channel 1 select
1	0	Channel 2 select
1	1	Channel 3 select

Request Register

This is a four bit register used to generate software requests (DMA service can be requested either externally or under software control). Request Register bits can be set or reset independently by the CPU. The Request Mask has no effect on software generated requests. All four bits are read in one operation and appear in the lower four bits of the byte. Bits 4 through 7 are read as ones. All four request bits are cleared to zero by RESET.

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	RB	RS1	RS0

(Write Operation)

RB—The request bit is set by writing a 1 to bit 2. RS1-RS0 select which bit (channel) is to be manipulated.

RS1-RS0—Channel Select 0 and 1 determine which channel's Mode Register will be written. Read back of the mode register will result in bits 0 and 1 both being ones.

RS1	RS0	CHANNEL
0	0	Channel 0 select
0	1	Channel 1 select
1	0	Channel 2 select
1	1	Channel 3 select

Format for the Request Register read operation is shown below.

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
1	1	1	1	RC3	RC2	RC1	RC0

(Read Operation)

RC3-RC0—During a Request Register read, the state of the request bit associated with each channel is returned in bits 0 through 3 of the byte. The bit position corresponds to the channel number.

Request Mask Register

The Request mask register is a set of four bits which are used to inhibit external DMA requests from generating transfer cycles. This register can be programmed in two ways. Each channel can be independently masked by writing to the Write Single Mask Bit location. The data format for this operation is shown below.

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	MB	MS1	MS0

(Set/Reset Operation)

MB—Bit 2 sets or resets the request mask bit for the channel selected by MS1 and MS0. Writing a 1 in this bit position sets the mask, inhibiting external requests.

MS1-MS0—These two bits select the specific mask bit which is to be set or reset.

MS1	MS0	CHANNEL
0	0	Channel 0 select
0	1	Channel 1 select
1	0	Channel 2 select
1	1	Channel 3 select

Alternatively all four mask bits can be programmed in one operation by writing to the Write All Mask Bits address. Data format for this and the Read All Mask Bits function is shown below.

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	MB3	MB2	MB1	MB0

(Read/Write Operation)

MB3-MB0—Each bit position in the field represents the mask bit of a channel. The mask bit number corresponds to the channel number associated with the mask bit.

All four mask bits are set following a RESET or a Master Clear command. Individual channel mask bits will be set as a result of terminal count being reached, if Autoinitialize is disabled. The entire register can be cleared, enabling all four channels, by performing a Clear Mask Register operation.

Status Register

The status of all four channels can be determined by reading the Status Register. Information is available to determine if a channel has reached terminal count and whether an external service request is pending. Bits 0-3 of this register are cleared by RESET, Master

Clear or each time a Status Read takes place. Bits 4-7 are cleared by RESET, Master Clear or the pending request being deasserted. Bits 4-7 are not affected by the state of the Mask Register Bits. The channel number corresponds to the bit position.

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
DRQ3	DRQ2	DRQ1	DRQ0	TC3	TC2	TC1	TC0

(Read Only Register)

Temporary Register

The Temporary Register is used as a temporary holding register for data during memory-to-memory transfers. The register is loaded during the first cycle of a memory-to-memory transfer from D0-D7. During the second cycle of the transfer, the data in the Temporary Register is output on the D0-D7 pins. Data from the last memory-to-memory transfer will remain in the register unless a RESET or Master Clear occurs.

Special Commands

Five Special Commands are provided to make the task of programming the device easier. These commands are activated as a result of a specific address and assertion of either a read or write. Information on the data lines is ignored by the 82C100 whenever an write activated command is issued, thus data returned on read activated commands is invalid.

Clear Byte Pointer Flip-Flop—This command is normally executed prior to reading or writing to the address or word count registers. This initializes the flip-flop to point to the low byte of the register and allows the CPU to read or write the register bytes in correct sequence.

Set Byte Pointer Flip-Flop—Setting the Byte Pointer Flip-Flop allows the CPU to adjust the pointer to the high byte of an address or word count register.

Master Clear—This command has the same effect as a hardware RESET. The Command Register, Status Register, Request Register, Temporary Register, Mode Register Counter and Byte Pointer Flip-Flop are cleared and the Request Mask Register is set. Immediately following Master Clear or RESET, the DMA will be in the Idle Condition.

Clear Request Mask Register—This command enables all four DMA channels to accept requests by clearing the mask bits in the register.

Clear Mode Register Counter—In order to allow access to four Mode Registers while only using one address, an additional counter is used. After clearing the counter all four Mode Registers may be read by doing successive reads to the Read Mode Register address. The order in which the registers will be read is Channel 0 first, Channel 3 last.

INTERRUPT CONTROLLER

The interrupt controller is the functional equivalent of the 8259A plus additional logic. It supports one non-maskable (NMI) and eight maskable interrupt levels. Interrupt levels 2-7 are available at the system IO channel. When used with an XT-type keyboard, Interrupt levels 0 and 1 are generated internal to the 82C100. Level 0 is the highest priority and it is connected to Counter/Timer channel 0 to provide a periodical interrupt for the timer tick. In an XT system, Level 1 is used for the keyboard and is connected internally to the keyboard interface. In a Model 25/30-type system, Level 1 is brought out to a pin and the interrupt must be generated by the external keyboard interface. It is shared by the keyboard, pointing device such as a mouse, and the real time clock; the sharing mechanism is handled by external hardware and the BIOS service routine through interrupt vector 71H.

The Interrupt Controller also handles Non Maskable Interrupts coming from the Real Time Clock, Numeric CoProcessor, Power Failure Indicator, Parity Checker, and the IO Channel Check (IOCHCHK) signal. Since only one NMI pin exists on the processor, the NMI service routine reads a register to determine the source of the NMI.

Interrupt Assignments:

Level	System Board	I/O Channel
NMI	Parity Check CoProcessor Real Time Clock Power Failure	I/O Channel Check
IRQ0	Timer Channel 0	Not Available
IRQ1	Keyboard Pointing Device (opt) Real Time Clock (opt)	Not Available
IRQ2	Video	Available
IRQ3	Not Used	Available
IRQ4	Serial Port	Available
IRQ5	Hard Disk	Available
IRQ6	Floppy Disk	Available
IRQ7	Parallel Port	Available

Figure 2 is a block diagram of the major elements in the interrupt controller. The Interrupt Request Register (IRR) is used to store requests from all of the channels which are requesting service. Interrupt Request Register bits are labeled using the Channel Name IR7-IR0. The In-Service Register (ISR) contains all the channels which are currently being serviced (more than one channel can be in service at a time). In-Service Register bits are labeled IS7-IS0 and correspond to IR7-IR0. The Interrupt Mask Register (IMR) allows the CPU to disable any or all of the interrupt channels. The Priority Resolver evaluates inputs from the above three registers, issues an interrupt request, and latches the corresponding bit into the In-Service Register. During interrupt acknowledge cycles, a master controller outputs a code to the slave device which is compared in the Cascade Buffer/Comparator with a three bit ID code previously written. If a match occurs in the slave controller, it will generate an interrupt vector. The contents of the Vector Register are used to provide the CPU with an interrupt vector during Interrupt Acknowledge (INTA) cycles.

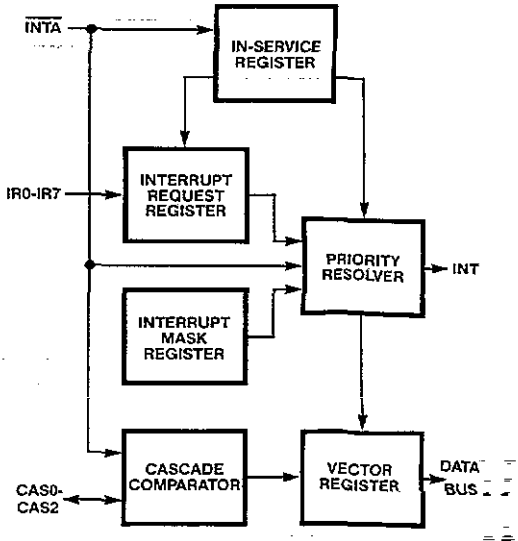


Figure 2. Interrupt Controller Block Diagram

Two types of commands are used to control the 82C100 interrupt controllers. Initialization Command Words (ICWs) and Operational Command Words (OCWs).

Initialization Command Words

The initialization process consists of writing a sequence of 3 bytes to the interrupt controller. The initialization sequence is started by writing the first Initialization Command Word (ICW1) to address 020H with a 1 on bit 4 of the data byte. The interrupt controller interprets this as the start of an initialization sequence and does the following:

1—The Initialization Command Word Counter is reset to zero.
2—ICW1 is latched into the device
3—Fixed Priority Mode is selected
4—IR7 is assigned the highest priority
5—The Interrupt Mask Register is cleared
6—The Slave Mode Address is set to 7
7—Special Mask Mode is disabled
8—The IRR is selected for Status Read operations

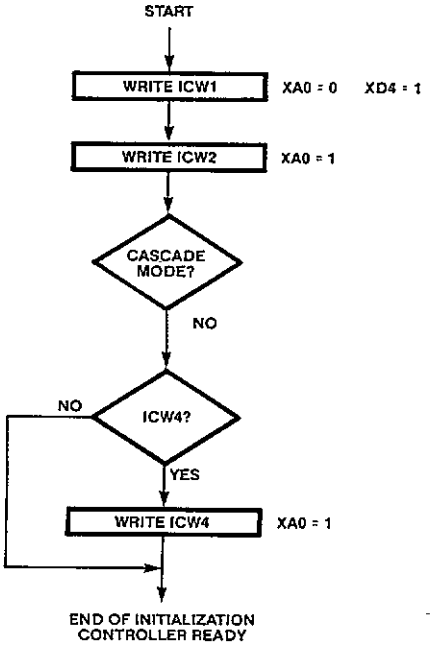


Figure 3. Initialization Sequence

The next two I/O writes to address 021H will load ICW2 and ICW4. See Figure 3 for a flow chart of the initialization sequence. The initialization sequence can be terminated at any point (all 3 bytes must be written for the controller to be properly initialized) by writing to address 020H with a 0 in data bit 4. Note, this will cause OCW2 to be written.

ICW1—Address 020H

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	SI	LTM	X	SM	IC4

(Write Only Register)

SI—Bit 4 indicates to the interrupt controller that an Initialization Sequence is starting and must be a 1 to write ICW1.

LTM—Bit 3 selects level or edge triggered inputs to the IRR.

SM—Bit 1 selects between Single Mode and Cascade Mode.

IC4—Bit 0 selects ICW4 needed or not needed.

ICW2—Address 021H

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
V7	V6	V5	V4	V3	X	X	X

(Write Only Register)

V7-V3—These bits are the upper 5 bits of the interrupt vector and are programmable by the CPU. The lower three bits of the vector are generated by the Priority Resolver during INTA.

ICW4—Address 021H

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	EMI	X	X	AEOI	X

(Write Only Register)

EMI—Bit 4 will Enable Multiple Interrupts from the same channel in Fixed Priority Mode.

AEOI—Auto End Of Interrupt is enabled when ICW4 is written with a zero in bit 1. The interrupt controller will perform a non-specific EOI on the trailing edge of the second INTA cycle.

Operational Command Words

Operational Command Words (OCWs) allow the 82C100 interrupt controller to be controlled or reconfigured at any time while operating. Each interrupt has 3 OCWs which can be programmed to affect the proper operating configuration and a Status Register to monitor controller operation.

Operational Command Word 1 (OCW1) is located at address 021h and may be written any time the controller is not in Initialization Mode. Operational Command Words 2 and 3 (OCW2,OCW3) are located at address 020H. Writing to address 020H with a 0 in bit 4 will place the controller in operational mode and load OCW2 (if data bit 3 = 0) or OCW3 (if data bit 3 = 1).

OCW1—Address 021H

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
M7	M6	M5	M4	M3	M2	M1	M0

(Read/Write Register)

M7-M0—These bits control the state of the Interrupt Mask Register. Each Interrupt Request can be masked by writing a 1 in the appropriate bit position (M0 controls IR0 etc.). Setting an IMR bit has no affect on lower priority requests. All IMR bits are cleared by writing ICW1.

OCW2—Address 020h

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
R	SL	EOI	SI	2/3	L2	L1	L0

(Write Only Register)

R—This bit in conjunction with SL and EOI selects operational function. Writing a 1 in bit 7 causes one of the rotate functions to be selected.

R	SL	EOI	Function
1	0	0	Rotate on auto EOI enable*
1	0	1	Rotate on non-specific EOI
1	1	0	Specific Rotate Command
1	1	1	Rotate on specific EOI

***This function is disabled by writing a zero to all three bit positions.**

SL—This bit in conjunction with R and EOI selects operational function. Writing a 1 in this bit position causes a specific or immediate function to occur. All specific commands require L2-L0 to be valid except no operation.

R	SL	EOI	Function
0	1	0	No operation
0	1	1	Specific EOI Command
1	1	0	Specific Rotate Command
1	1	1	Rotate on specific EOI

EOI—This bit in conjunction with R and SL selects operational function. Writing a 1 in this bit position causes a function related to EOI to occur.

R	SL	EOI	Function
0	0	1	Non-specific EOI Command
0	1	1	Specific EOI Command
1	0	1	Rotate on non-specific EOI
1	1	1	Rotate on specific EOI

SI—Writing a 0 in this bit position takes the interrupt controller out of initialize mode and writes OCW2 or OCW3.

2/3—If the I/O write places a 0 in bit 4 (SI), then writing a 0 in bit 3 (2/3) selects OCW2 and writing a 1 will select OCW3.

L2-L0—These three bits are internally decoded to select which interrupt channel is to be affected by the Specific command. L2-L0 must be valid during three of the four specific cycles (see SL above).

OCW3—Address 020H

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
0	ESMM	SMM	SI	2/3	PM	RR	RIS

(Write Only Register)

ESMM—Writing a 1 in this bit position enables the Set/Reset Special Mask Mode function controlled by bit 5 (SMM). ESMM allows the other functions in OCW3 to be accessed and manipulated without affecting the Special Mask Mode state.

SMM—If ESMM and SMM both are written with a 1 the Special Mask Mode is enabled. Writing a 1 to ESMM and a 0 to SMM disables Special Mask Mode. During Special Mask Mode, writing a 1 to any bit position inhibits interrupts and a 0 enables interrupts on the associated channel by causing the Priority Resolver to ignore the condition of the ISR.

SI—See SI above.

2/3—See 2/3 above.

PM—Polled Mode is enabled by writing a 1 to bit 2 of OCW3, causing the 82C100 to perform the equivalent of an INTA cycle during the next I/O read operation to the controller. The byte read during this cycle will have bit 7 set if an interrupt is pending. If bit 7 of the byte is set, the level of the highest pending request will be encoded on bits 2-0. The IRR will remain frozen until the read cycle is completed at which time the PM bit is reset.

RR—When the RR bit (bit 1) is 1, reading the Status Port at address 020h will cause the contents of IRR or ISR (determined by RIS) to be placed on D7-D0. Asserting PM forces RR reset.

RIS—This bit selects between the IRR and the ISR during Status Read operations if RR = 1.

Interrupt Sharing

Interrupt Sharing allows more than one device to use a single interrupt level. In a Model 25/30, the keyboard, pointing device and real-time-clock all share the same interrupt level. In a Model 25/30 look-alike design, a keyboard/mouse interface that emulates IBM's implementation must be done with external hardware. In the 82C100's "PS/2" keyboard mode, the IRQ1 line is an input driven by the external keyboard/mouse interface. The external circuit must insure that if multiple interrupt requests are pending, the interrupt line must return to the inactive (low) state after each interrupt is serviced. This will insure that the interrupt controller in the 82C100 sees a rising edge for each interrupt, otherwise the request will be lost.

TIMER

The timer circuit is functionally equivalent to the 8254 timer. Channel 0 is used as a general-purpose and software interrupt timer. Channel 1 is unused, and channel 2 is used to support tone generation for the audio speaker. The timer channel clock rate, referred to as TMRCLK in rest of the explanation, is derived by dividing a 4.77 MHz clock by 4. Each channel has a minimum timing resolution of 840ns.

The Counter/Timer (CTC) in the 82C100 is general purpose, and can be used to generate accurate time delays under software control. The CTC contains 3 16-bit counters (Counter 0-2) which can be programmed to count in binary or binary coded decimal (BCD). Each counter operates independently of the other two and can be programmed for operation as a timer or a counter.

All three of the counters shown in Figure 4 are controlled from a common set of control logic. The Control Logic decodes control information written to the CTC and provides the controls necessary to load, read, configure and control each counter. Counter 0 and Counter 1 can be programmed for all six modes, but Mode 1 and Mode 5 have limited usefulness due to the lack of an external hardware trigger signal. Counter 2 can be operated in any of six modes listed below.

Mode 0	Interrupt on terminal count
Mode 1	Hardware retriggerable one-shot
Mode 2	Rate generator
Mode 3	Square wave generator
Mode 4	Software triggered strobe
Mode 5	Hardware retriggerable strobe

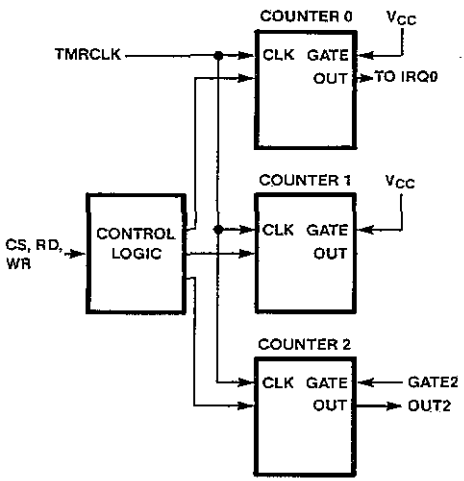


Figure 4. Counter/Timer Block Diagram

Counter Description

Each counter in the CTC contains a Control Register, a Status Register, a 16-bit Counting Element (CE), a pair of 8-bit Counter Input Latches (CIL,CIH),and a pair of 8-bit Counter Output Latches (COL,COH).

The Control Register stores the mode and command information used to control the counter. The Control Register may be loaded by writing a byte, containing a pointer to the desired counter, to the Write Control Word address (043h). The remaining bits in the byte contain the mode, the type of command, and count format information.

The Status register allows the software to monitor counter condition and read back the contents of the Control Register.

The Counting Element is a loadable 16-bit synchronous down counter. The CE is loaded or decremented on the falling edge of TMRCLK. The CE contains the maximum count when a 0 is loaded; which is equivalent to 65536 in binary operation or 10000 in BCD. The CE does not stop when it reaches 0. In Modes 2 and 3 the CE will be reloaded and in all other modes it will wrap around to FFFF in binary operation or 9999 in BCD.

The CE is indirectly loaded by writing one or two bytes (optional) to the Counter Input Latches, which are in turn loaded into the CE. This allows the CE to be loaded or reloaded in one TMRCLK cycle.

The CE is also read indirectly by reading the contents of the Counter Output Latches. COL and COH are transparent latches which can be read while transparent or latched (see Latch Counter Command).

Programming The CTC

After power-up the condition of CTC Control Registers, counter registers, CE, and the output of all counters is undefined. Each counter must be programmed before it can be used.

Counters are programmed by writing a Control Word and then an initial count. The Control Register of a counter is written by writing to the Control Word address (see Figure 5). The Control Word is a write only location.

Address	Function
040h	Counter 0 Read/Write
041h	Counter 1 Read/Write
042h	Counter 2 Read/Write
043h	Control Register Write Only

Figure 5. Counter/Timer Address Map

M2-M0—Bits 3-1 determine the counter's mode during Read/Write Counter Commands (see Read/Write Counter Command) or select the counter during a Read-Back Command (see Read-Back Command). Bits 3-1 become "don't care" during Latch Counter Commands.

Control Word—(043H)

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
F3	F2	F1	F0	M2	M1	M0	BCD

(Write Only Register)

F3-F0—Bits 7-4 determine the command to be performed.

BCD—Bit 0 selects binary coded decimal counting format during Read/Write Counter Commands. Note, during Read-Back Command this bit must be 0.

Read/Write Counter Command

When writing to a counter, two conventions must be observed:

1—Each counters Control Word must be written before the initial count is written.

2—Writing the initial count must follow the format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

A new initial count can be written into the counter at any time after programming without rewriting the Control Word providing the programmed format is observed.

During Read/Write Counter Commands M3-M0 are defined as follows:

F3	F2	F1	F0	Command
0	0	0	0	Latch Counter 0 (see Counter Latch Command)
0	0	0	1	Read/Write Counter 0 LSB Only
0	0	1	0	Read/Write Counter 0 MSB Only
0	0	1	1	Read/Write Counter 0 LSB then MSB
0	1	0	0	Latch Counter 1 (see Counter Latch Command)
0	1	0	1	Read/Write Counter 1 LSB Only
0	1	1	0	Read/Write Counter 1 MSB Only
0	1	1	1	Read/Write Counter 1 LSB then MSB
1	0	0	0	Latch Counter 2 (see Counter Latch Command)2
1	0	0	1	Read/Write Counter 2 LSB Only
1	0	1	0	Read/Write Counter 2 MSB Only
1	0	1	1	Read/Write Counter 2 LSB then MSB
1	1	X	X	Read-Back Command (see Counter Read-Back Command)

MSB = most significant byte
LSB = least significant byte

M2	M1	M0	Function
0	0	0	Select Mode 0
0	0	1	Select Mode 1
X	1	0	Select Mode 2
X	1	1	Select Mode 3
1	1	0	Select Mode 4
1	1	1	Select Mode 5

Latch Counter Command

When a Latch Counter Command is issued, the counter's output latches (COL,COH) latch the current state of the CE. COL and COH remain latched until read by the CPU, or the counter is reprogrammed. The output latches then return to a "transparent" condition. In this condition the latches are enabled and the contents of the CE may be read directly.

Latch Counter Commands may be issued to more than one counter before reading the first counter to which the command was issued. Also, multiple Latch Counter Commands issued to the same counter without reading the counter will cause all but the first command to be ignored.

Read-Back Command

The Read-Back Command allows the user to check the count value, Mode, and state of the OUT signal and Null Count Flag of the selected counter(s).

The format of the Read-Back Command is:

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
1	1	LC	LS	C2	C1	C0	0

LC—Writing a 0 in bit 5 causes the selected counter(s) to latch the state of the CE in COL and COH.

LS—Writing a 0 in bit 4 causes the selected counter(s) to latch the current condition of it's Control Register, Null Count and Output into the Status Register. The next read of the Counter will result in the contents of the Status Register being read (see Status Read).

C2-C0—Writing a 1 in bit 3 causes Counter 3 to latch one or both of the registers specified by LC and LS. The same is true for bits 2 and 1 except that they enable Counters 1 and 0 respectively.

Each counter's latches remain latched until either the latch is read or the counter is reprogrammed.

If LS = LC = 0, status will be returned on the next read from the counter. The next one or two reads (depending on whether the counter is programmed to transfer one or two bytes) from the counter result in the count being returned.

Status Byte

msb							lsb
b7	b6	b5	b4	b3	b2	b1	b0
OUT	NC	F1	F0	M2	M1	M0	BCD

OUT—Bit 7 contains the state of the OUT signal of the counter

NC—Bit 6 contains the condition of the Null Count Flag. This flag is used to indicate that the contents of the CE are valid. NC will be set to a 1 during a write to the Control Register or the counter. NC is cleared to a 0 whenever the counter is loaded from the counter input registers.

F1-F0—Bits 5-4 contain the F1 and F0 Command bits which were written to the Command Register of the counter during initialization. This information is useful in determining whether the high byte, the low byte or both must be transferred during counter read/write operations.

M2-M0—These bits reflect the mode of the counter and are interpreted in the same manner as in Write Command operations.

BCD—*Bit 0 indicates* the CE is operating in BCD format.

Counter Operation

Due to the previously stated restrictions in Counter 0 and Counter 1, Counter 2 will be *used as the example* in describing counter operation, but the description of Mode 0, 2, 3 and 4 is relevant to all counters.

The following terms are defined for describing CTC operation.

TMRCLK pulse—A rising edge followed by a falling edge of the TMRCLK.

trigger—The rising edge of the GATE2 input.

counter load—The transfer of the 16-bit value in CIL and CIH to the CE.

initialized—A Control Word written and the Counter Input Latches loaded.

Counter 2 operates in one of the following modes.

Mode 0—*Interrupt on terminal count*

Writing the Control Word causes OUT2 to go low and remain low until the CE reaches 0, at which time it goes back high and remains high until a new count or Control Word is written. Counting is enabled when GATE2 = 1. Disabling the count has no effect on OUT2.

The CE is loaded with the first TMRCLK pulse after the Control Word and initial count are loaded. When both CIL and CIH are written, the CE is loaded after CIH is written (see Write Operations). This TMRCLK pulse does not decrement the count, so for an initial count of N, OUT2 does not go high until N+1 TMRCLK pulses after initialization. Writing a new initial count to the counter reloads the CE on the next TMRCLK pulse and counting continues from the new count.

If an initial count is written with GATE2 = 0, it will still be loaded on the next TMRCLK pulse but counting does not begin until GATE2 = 1. OUT2 therefore, goes high N TMRCLK pulses after GATE2 = 1.

Mode 1—Hardware retriggerable one-shot

Writing the Control Word causes OUT2 to go high initially. Once initialized the counter is armed and a trigger causes OUT2 to go *low on the next* TMRCLK pulse. OUT2 then remains low until the counter reaches 0. An initial count of N results in a one-shot pulse N TMRCLK cycles long.

Any subsequent triggers while OUT2 is low cause the CE to be reloaded, extending the length of the pulse. Writing a new count to CIL and CIH will not affect the current one-shot unless the counter is retriggered.

Mode 2—Rate generator

Mode 2 functions as a divide-by-N counter, with OUT2 as the carry. Writing the Control Word during initialization sets OUT2 high.

When the initial count is decremented to 1, OUT2 goes low on the next TMRCLK pulse. The following TMRCLK pulse returns OUT2 high, reloads the CE and the process is repeated. In Mode 2 the counter continues counting (if GATE2 = 1) and will generate an OUT2 pulse every N *TMRCLK cycles.* Note that a count of 1 is illegal in Mode 2.

GATE2 = 0 disables counting and forces OUT2 high immediately. A trigger reloads the the CE on the next TMRCLK pulse. Thus GATE2 can be used to synchronize the counter to external events.

Writing a new count while counting does not affect current operation unless a trigger is received. Otherwise, the new count will be loaded at the end of the current counting cycle.

Mode 3—Square wave generator

Mode 3 is similar to Mode 2 in every respect except for the duty cycle of OUT2. OUT2 is set high initially and remains high for the first half of the count. When the first half of the initial count expires, OUT2 goes low for the remainder of the count.

If the counter is loaded with an even count, the duty cycle of OUT2 will be 50% (high = low = N/2). For odd count values, OUT2 is high one TMRCLK cycle longer than it is low. Therefore, high = (N+1)/2 and low = (N-1)/2.

Mode 4—Software triggered strobe

Writing the Control Word causes OUT2 to go high initially. Expiration of the initial count causes OUT2 to go low for one TMRCLK cycle. GATE2 = 0 disables counting but has no effect on OUT2. Also, a trigger will not reload the CE.

The counting sequence is started by writing the initial count. The CE is loaded on the TMRCLK pulse after initialization. The CE begins decrementing one TMRCLK pulse later. OUT2 will go low for one TMRCLK cycle, (N+1) cycles after the initial count is written.

If a new initial count is written during a counting sequence, it is loaded into the CE on the next TMRCLK pulse and the sequence continues from the new count. This allows the sequence to be "retriggerable" by software.

Mode 5—Hardware triggered strobe

Writing the Control Word causes OUT2 to go high initially. Counting is started by trigger. The expiration of the initial count causes OUT2 to go low for one TMRCLK cycle. GATE2 = 0 disables counting.

The CE is loaded on the TMRCLK pulse after a trigger. Since loading the CE inhibits decrementing, OUT2 will go low for one TMRCLK cycle, (N+1) TMRCLK cycles after the trigger.

If a new count is loaded during counting, the current counting sequence will not be affected unless a trigger occurs. A trigger causes the counter to be reloaded from CIL and CIH, making the counter "retriggerable".

GATE2

In Modes 0, 2, 3 and 4 GATE2 is level sensitive and is sampled on the rising edge of TMRCLK. In Modes 1, 2, 3 and 5 the GATE2

Mode	Condition		
	Low	Rising	High
0	Disables Counting	—	Enables Counting
1	—	a) Initiates Counting b) Resets Out Pin	—
2	a) Disables Counting b) Forces Out Pin High	Initates Counting	Enables Counting
3	a) Disables Counting b) Forces Out Pin High	Initiates Counting	Enables Counting
4	Disables Counting	—	Enables Counting
5	—	Initiates Counting	—

Figure 6. Gate Pin Function

input is rising-edge sensitive. This rising edge sets an internal flip-flop whose output is sampled on the next rising edge of TMRCLK. The flop-flop resets immediately after being sampled. Note that in Modes 2 and 3 the GATE2 input is both edge and level sensitive.

PROGRAMMABLE PERIPHERAL INTERFACE (PPI)

The 82C100 PPI is a subset of the 8255. It has all the four registers, but it is limited to mode 0 (basic input/output). No handshake is required when data is read from or written to a specific port. I/O address 60H is referred as port A, 61H is port B and 62H is port C.

The programming is similar to that of the 8255 PPI, but the external interface is different. Some of the bits are internal and hardwired so they cannot be changed.

The input portion of port A (60H) is for the keyboard scan code (if an XT-type keyboard is being used). If a PS/2 type keyboard is being used (selected by a bit in the configuration registers) Port A (60H) is disabled so that it may be implemented externally. Port B (61H) is the control port and port C (62H) is the status port for various system functions described below. Port 63H is the command/mode register for these three I/O ports. In the normal operation of the PC/XT, the control word is programmed to 99H: Port A (60H), and port C (62H) are inputs, and port B (61H) is output.

To Program the PPI:

1. Select the desired operational modes for both group A and group B, by selecting the appropriate combination of bits 6:5, and bit 2.
2. Bit 7 should be 1 to select the Mode Set function.
3. Select the grouping of inputs and outputs (bits 0, 1, 3, and 4)
4. Write the Mode Control word to port 63H.

Single Bit Set/Reset Mode

Any of the bits in port C can be Set/Reset using a single OUT instruction. To Set/Reset any Port C bits:

1. Select the bit to be set/reset (bits 3:1).
2. Select bit 0 for set (1) or reset (0).
3. Set bit 7 to 0 to select the Single Bit mode.
4. Write the control word to port 63H.

Parallel Port Bit Definition

Port A (60H) - R (XT Keyboard Mode Only)

R-Keyboard Scan Code

Port B (61H) - W

bit 0	TMR2GTSPK - Timer 2 Gate Speaker Controls the Gate 2 input of the timer. 0 - Stop count of timer 2. If SPKDATA bit (bit 1) is set to HIGH then SPKDATA output (pin 70) will be HIGH, else it will be LOW. 1 - Enable counting of timer 2.
bit 1	SPKDATA - Speaker Data 0 - Disable Speaker Data, SPKDATA output (pin 70) will remain LOW. 1 - Enable Speaker Data.
bit 2	Reserved
bit 3	Read High/Low Switches 0 - Low Nibble Switches 1 - High Nibble Switches
bit 4	$\overline{\text{PCKEN}}$, Parity Check Enable. 0 - Enable Parity Check. Default. 1 - Disable Parity Check.
bit 5	$\overline{\text{IOCHCKEN}}$, I/O Channel Check Enable. 0 - Enable I/O Channel Check. Default. 1 - Disable I/O Channel Check.

bit 6	KBCLKLO, Keyboard Clock Low. For XT keyboards only. 0 - Hold Keyboard Clock Low. 1 - Normal Keyboard Clock.
bit 7	KBEN, Keyboard enable/clear. Clear port 60 and generate keyboard clear NMI if port 72, bit 6 is set. 0 - Enable Keyboard. 1 - Clear Keyboard.

Port C (62H) - R

Note: The lower nibble of Port C is used to read the configuration DIP switches present in an XT system. The switches are read as two groups of four. The high group is read when bit 3 of Port B is high and the low group is read when bit 3 of Port B is low. In a system with the 82C100, these switches do not physically exist. They are emulated by a configuration register. They are provided for *soft*ware compatibility only. The values listed here are those used by IBM in the latest XT, however they don't actually control anything. Note that bits 0, 2, 3 and 4 have been redefined in the Model 25/30. Since these bits are just values and do not actually control any hardware, a Model 25/30 compatible BIOS could use these bits as they are defined by the Model 25/30 instead of the XT definitions.

Low Switches

bit 0	Loop on POST 0 - Do not loop on POST 1 - Loop on POST, if any of the POST routine fails - used for diagnostic purposes.
bit 1	Co-Processor Installed 0 - No coprocessor. 1 - Coprocessor is installed.
bit 2:3	Planar Ram Size. 00 - 256K 01 - 512K 10 - 576K 11 - 640K

High Switches

bits 0:1	Display Type at Power-up 00 - EGA 01 - CGA 40×25 10 - CGA 80×25 11 - Monochrome 80×25
bits 2:3	Number of Diskette Drives 00 - 1 Drive 01 - 2 Drives 10 - 3 Drives 11 - 4 Drives
bit 4	Reserved
bit 5	Timer Channel 2 Out Status of Timer Channel 2 output. When this bit does not change status, timer channel 2 is not working, because: a. TMR2GTSPK is disabled and/or b. channel 2 has not correctly been programmed.
bit 6	I/O Channel Check 0 - I/O CH CK line is inactive. 1 - I/O CH CK line is active - error occurred.
bit 7	RAM Parity Check 0 - No parity error has occurred. 1 - Parity error on the mother board RAM has occurred

Port 63H (R/W) - Mode Set Definition

bit 7	Mode Select (0 - Single Bit Set/Reset mode—see below) 1 - Mode Set Function
bits 6:5	Mode Selection for Group A 00 - Mode 0 01 - Mode 1 1X - Mode 2
bit 4	Port A mode (Group A) 0 - Output 1 - Input

bit 3	Port C Upper Nibble (Group A) 0 - Output 1 - Input
bit 2	Group B Mode Select 0 - Mode 0 1 - Mode 1
bit 1	Port B (Group B) 0 - Output 1 - Input
bit 0	Port A Lower Nibble (Group B) 0 - Output 1 - Input

Port 63H (R/W) - Single Bit Set/Reset Mode

bit 7	Mode Select 0 - Single Bit Set/Reset Mode (1 - Mode Set Function—see above)
bit 6:4	Don't Care
bit 3:1	Bit Select 000 - Bit 0 001 - Bit 1 010 - Bit 2 011 - Bit 3 100 - Bit 4 101 - Bit 5 110 - Bit 6 111 - Bit 7
bit 0	Set/Reset 0 - Reset 1 - Set

KEYBOARD INTERFACE

The keyboard interface makes provisions to bypass the internal logic so a PS/2 style keyboard may be used. Selection is done through the Internal Configuration Registers. When this option is selected, Port 60H is essentially turned off so that it may be implemented externally.

KBDATA and KBCLK are open collector and are both input and output when using an XT keyboard. KBDATA is unused and KBCLK becomes the IRQ1 input when the 82C100 is used in PS/2 keyboard mode.

In XT Keyboard mode, the interface logic assembles the serial data from the keyboard into bytes. Timing and synchronization is provided by the KBCLK signal. Internally there are shift registers clocked by KBCLK.

To Receive Characters:

When a key is depressed or released, the keyboard controller sends a scan code. The keyboard logic assembles the incoming serial data to a byte. Whenever a byte of information is ready, an IRQ1 is sent to the interrupt controller. The IRQ1 interrupt service routine reads port 60H to get the keyboard scan code and acknowledges by sending a positive pulse on port 61H, this clears the shift register for the next character.

MEMORY INTERFACE

The 82C100 has a powerful memory controller. It generates the control signals for static and dynamic RAMs, and the BIOS ROM.

The DRAM control function has an independent DRAM refresh timer that can be programmed to generate a refresh rate from 838ns to 214μS. It also generates all the necessary timings and controls for 4 banks of DRAM arrays. The signals are $\overline{RAS3\text{-}0}$, $\overline{CAS}$, $\overline{WE}$, and the multiplexed addresses MA0-MA9 during refresh and memory accesses. Refresh and power to the DRAM portion of memory can be maintained during SUSPEND mode at the user's discretion.

Control signals for SRAM are multiplexed with MA addresses. They include chip selects and write enables. SRAM/DRAM operation is selected by a bit in the configuration registers.

$\overline{ROMCS}$ is used to select the ROM BIOS. It is decoded for address range F0000H:FFFFFH.

ROM Interface

ROMCS is active low for the 64K address range F0000 to FFFFF, qualified with MEMR. If power consumption is not a concern, ROMCS should be connected to the Output Enable (OE) of the ROM, and the Chip Enable (CE) should be tied to ground. If power consumption is of concern, the ROMCS should be tied to both the Output and Chip Enables, at the expense of slower access time. Two ROMs would be used in a 16 bit system, and one ROM would be used in an 8 bit system.

SRAM Interface

The control signals for a typical static RAM are OE, CE, and WE. The 82C100 provides some of these signals and others must be generated by an external decoder. WEL should be connected to the WE inputs of the low/even bank, and WEH to the high/odd bank. WEH and WEL should be buffered if more than ten devices are connected. CS8 and CS9 are decoded 64K segment for address 80000H and 90000H. Assuming 32K×8 RAMs are used, CS8 and CS9 can be connected directly to the CE pins, and the OEs are tied to MEMR. The other CSs are generated by a 74×138 decoder. Consult the following Static RAM Subsystem figures for reference.

Dynamic RAM Interface

The memory configuration on the system board is defined in the configuration registers. Four bits are used to select one of the sixteen predefined configurations from 128KB to 2.5MB, 8 bit or 16 bit. Connections to the DRAMs are simplified, because all the control and timing signals are generated by the 82C100. The 82C100 generates RAS, CAS, WE and all addresses. CPU commands are active at the beginning of T2. Memory cycles are divided into 3 segments for timing generation. At 1/3 of T2 RAS is active, at 2/3 of T2 the DRAM address is multiplexed and WE is active (if a write cycle), and CAS is active at the end of T2 (at beginning of T3). Commands are inactive at T4, whereas DRAM controls are inactive at 1/3 of T4 to account for data hold time.

Address translations for LIM EMS are internal. The value in the EMS register is combined with the lower address bits to make the complete DRAM address.

The following table shows the actual address bits present on the multiplexed address (MA) lines for RAS and CAS cycles for 8 and 16 bit memory modes depending on the type of memory device used.

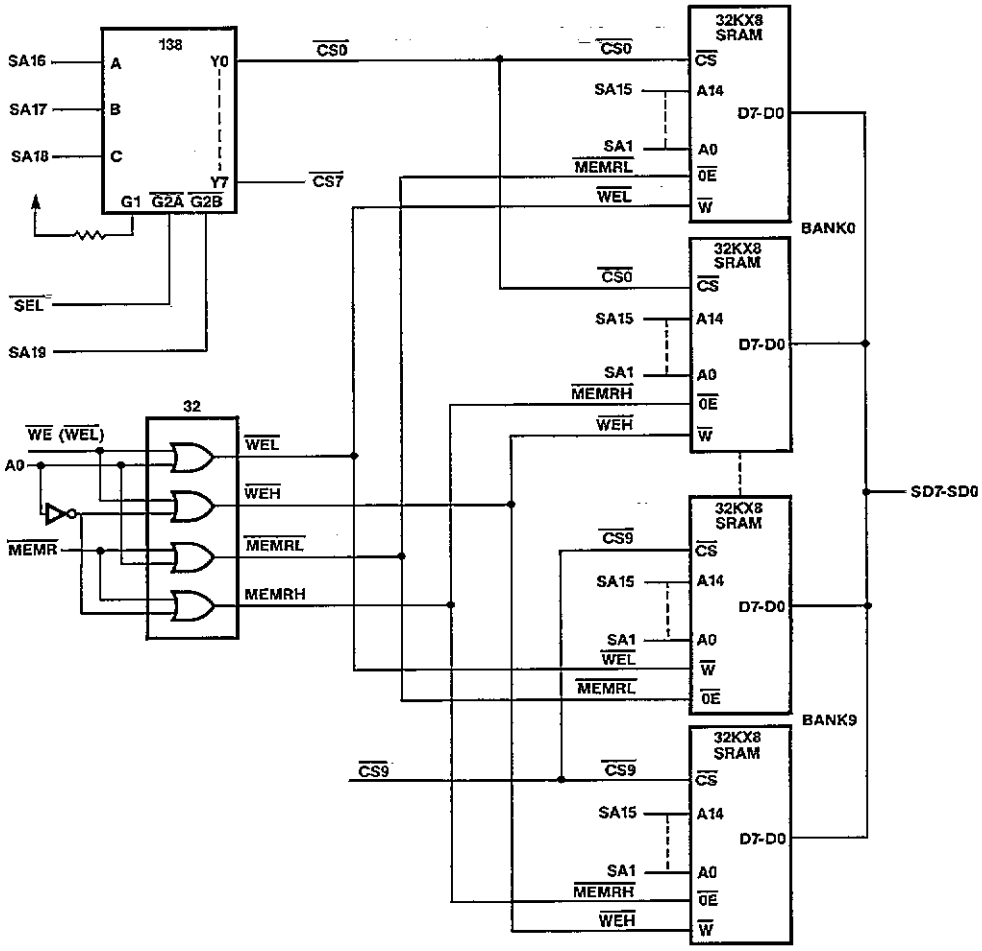
8 Bit Memory Configuration

MA Outputs	09	08	07	06	05	04	03	02	01	00
RAS (All devices)	09	08	07	06	05	04	03	02	01	00
CAS (64K devices)	—	—	09	10	15	14	13	12	11	08
CAS (256K devices)	—	16	17	10	15	14	13	12	11	09
CAS (1M devices)	18	16	17	10	15	14	13	12	11	19

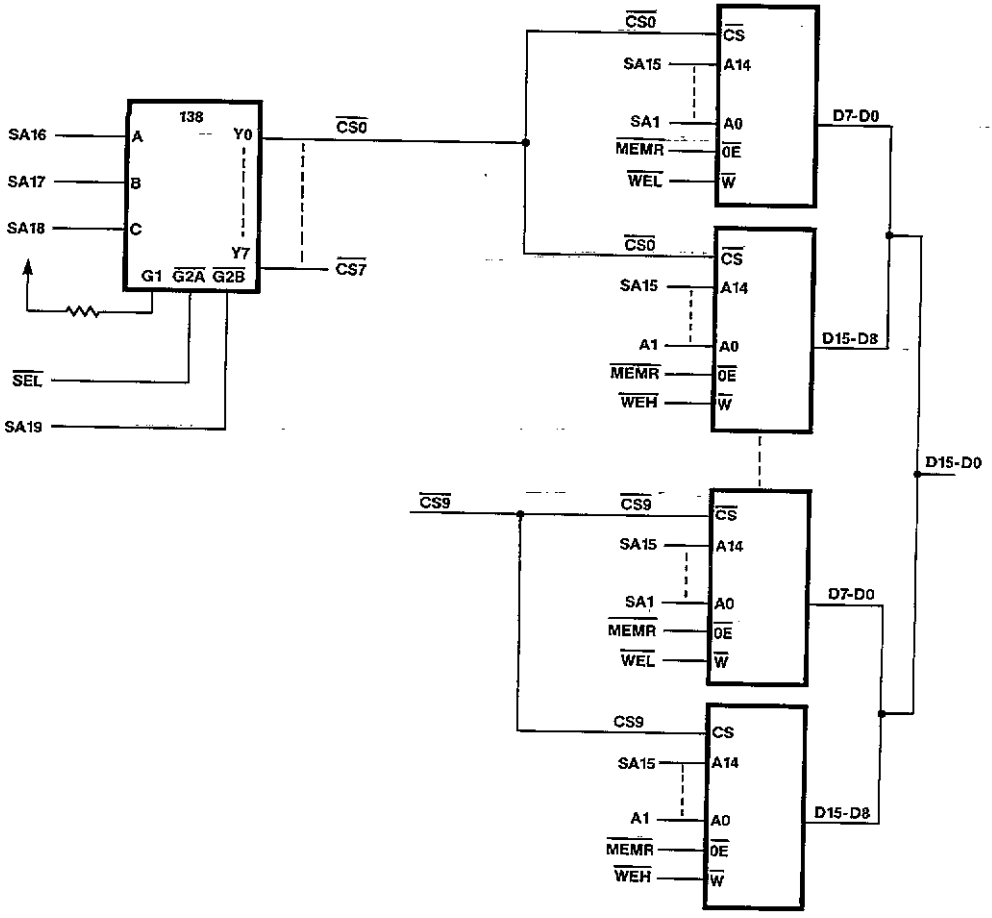
16 Bit Memory Configuration

MA Outputs	09	08	07	06	05	04	03	02	01	00
RAS (All devices)	09	08	07	06	05	04	03	02	01	10
CAS (64K devices)	18	16	09	10	15	14	13	12	11	—
CAS (256K devices)	18	16	17	10	15	14	13	12	11	—
CAS (1M devices)	18	16	17	20	15	14	13	12	11	19

8-BIT SRAM INTERFACE



16-BIT SRAM INTERFACE



Also note that in the following table the device size refers to the address width, not necessarily the number of bits per device. For example, two 256K×4 DRAMs could be used instead of eight 256K×1 devices to give the same amount of memory. Although the 256K×4 devices contain 1 megabit, they are connected and treated in the memory configuration register as a 256K device.

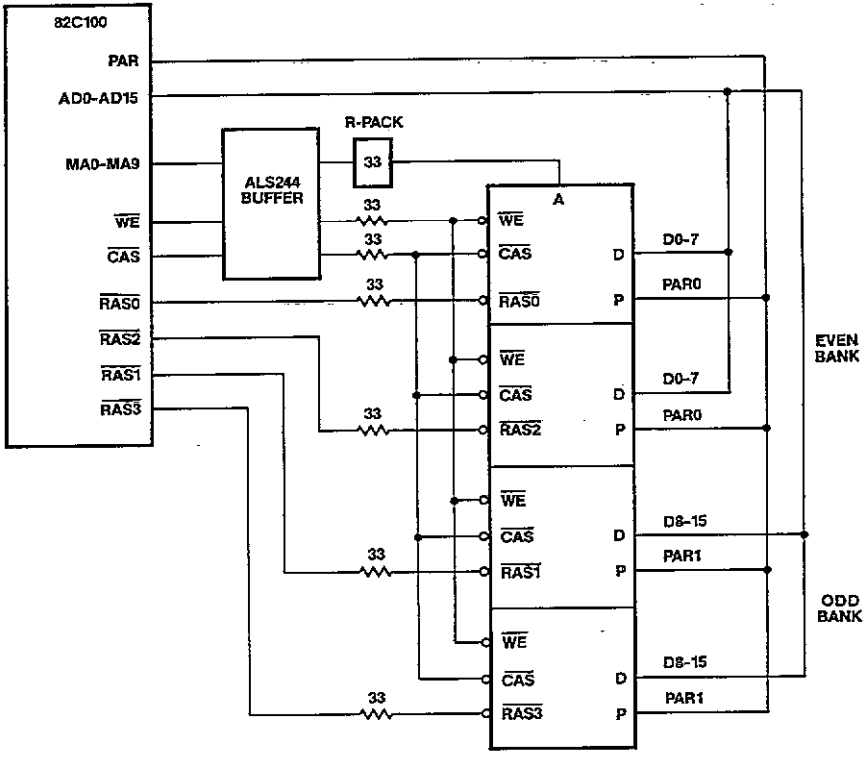
The following describes which MA lines to connect to the DRAMs for both 8 and 16 devices:

For 8 bit configurations:

64K devices	Use MA0-7
256K devices	Use MA0-8
1M devices	Use MA0-9

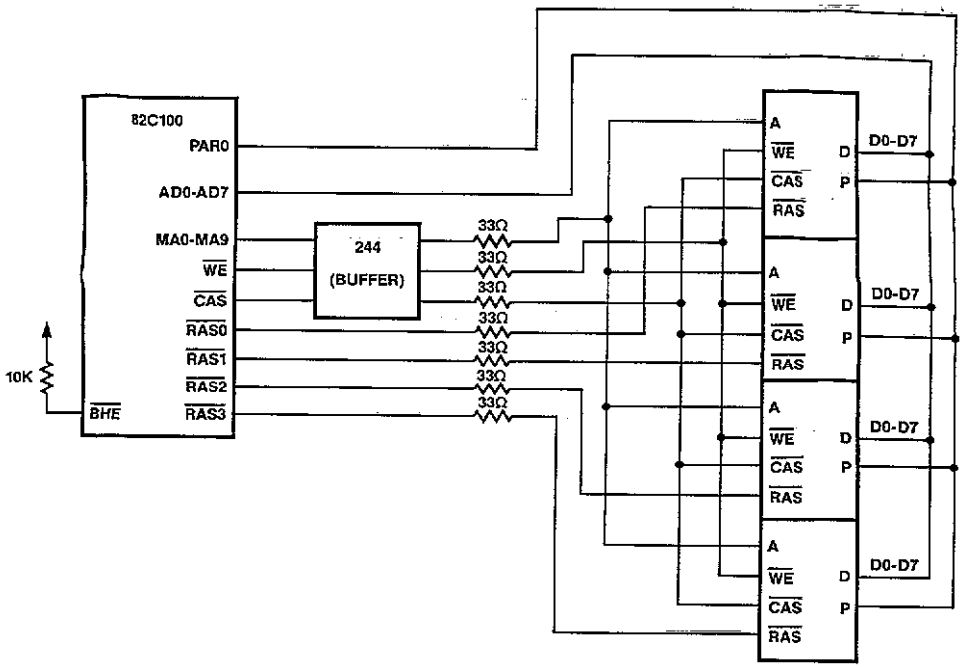
For 16 bit configurations:

64K Devices	Use MA1-8
256K Devices	Use MA1-9
1M Devices	Use MA0-9



NOTE: MA0-MA9, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS0}$-$\overline{RAS3}$ ARE CAPABLE OF DRIVING UP TO 9 DRAM LOADS WITHOUT EXTERNAL BUFFER. ASSUMING DRAM I_{IL} IS 10μA PER LOAD, AND C_t = 7pF/LOAD

8-BIT DRAM INTERFACE



I/O Channel Interface

The I/O Channel interface has been enhanced by adding variable I/O wait state and command delays to account for slow peripherals and add-on cards. AD0 to AD19 are decoded to provide various internal device chip selects while AD10 to AD15 will be used for EMS page register address. For all internal I/O accesses $\overline{DBEN}$ and DBIN are low, thus the system bus data buffer is enabled, and the direction is outward to the I/O channel. For external accesses DBIN is low for I/O writes, and high for I/O reads. The addresses (A1-A19) are latched by the transparent latches (74XX373 or equivalent), controlled by the ALE signal. An internally latched A0 signal is used in conjunction with the above. It should be buffered, but not latched in the transparent latches. The 82C100 toggles this bit for bus conversion cycles.

During bus conversion cycles a second set of commands are generated by the 82C100. First, the 82C100 toggles A0 incrementing the address. A second ALE is not generated. $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$, $\overline{MEMW}$, AEN, DEN, $\overline{DBEN}$, and DBIN will be generated accordingly creating the second cycle.

Configuration Registers

INTERNAL CONFIGURATION/CONTROL REGISTERS

Selection of the various options in the 82C100 is done through the configuration registers. There are six internal registers used to define the 82C100 configuration. These are accessed through a pair of IO ports (22H, and 23H). The definitions and index addresses of these are given below.

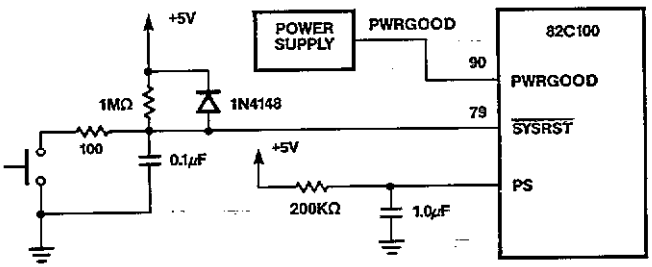
Accessing the Configuration Registers is a two step process:

Step 1: Write the index of the configuration register to IO port 22H.

Step 2: Followed by a read/write to IO port 23H.

To minimize accidental writes to these configuration registers, any access to location 23H must be preceeded by a write to location 22H.

The configuration setup should be the first task performed after power is turned on, because it defines how the 82C100 interfaces to the rest of the system. For example, it selects the memory size, bus size and timing options of the commands. The configuration values can be stored in external battery-backed-up SRAM such as in the 82C606 CHIPSpak.



Internal Configuration Registers Definition

Index 40H: R/W - Clock/Mode Size.

bit 7: CLKSEL - Clock Select

0 = Slow Clock (4.77MHZ). Default.
1 = Fast Clock (Max=10MHZ)

bit 6: DC - Processor Clock duty cycle

0 = 33% duty cycle (8088/86). Default.
1 = 50% duty cycle (V20/V30)

bits 5-3: Reserved.

bit 2: 2C - Two Clocks. Two clocks are present.

0 - One clock. 4.77MHz only. Default.
1 - Two clocks. A second clock is at the POSC input.

This bit must be set before the clock source can be switched to run at a higher speed.

bit 1: DS - DMA Clock Select

0 - Use system clock for DMA.
1 - Use system clock divided by 2 for DMA.

bit 0: 16 - 16 bit memory/IO

Enables the bus conversion logic. It implies that an 8086 (or V30) processor with 16 bit bus is installed.

0 - 8 bit mode.
1 - 16 bit mode. Default.

If the 82C100 is used with an 88/V20 then the BIOS must reset this bit immediately.

Index 41H:R/W - System Configuration

bit 7: MT - Memory Type.

0 - DRAM. Default.
1 - SRAM.

bit 6: SR - Software Reset.

0 - Disable Software Reset Function. Default.
1 - Enable Software Reset Function.

bit 5: SH - SRAM Control HIGH

0 - SRAM control outputs forced low at power down.
1 - SRAM control outputs forced high at power down.

bit 4: Reserved.

bit 3: CD - Command Delay

0 - Normal command timing. Default. Commands are asserted during T2.
1-Delay command by 1 cycle. Commands are asserted during T3 instead of T2 to allow additional time for adapters to decode their address. The command is actually shortened by 1 cycle. An additional wait state should be specified to maintain the normal command width.

bit 2: SM - System Memory Timing

0 - Normal wait states. System memory timing as controlled by other configuration register bits. Default setting.

1 - Reduced wait states. The number of wait states is forced to 0 for system memory cycles. System memory is defined as memory in the 0-640K range and EMS address space that is controlled by the 82C100. When the command delay bit is set and an additional wait state has been specified to maintain command width, this bit should also be set to keep system memory timing the same.

bit 1: Reserved.

bit 0: EP - Enable Parity

0 - Enable parity check logic. Default.
1 - Disable parity check logic.

Index 42H:R/W - Configuration Valid

bits 7-1:	Reserved
bit 0:	VC - Valid Configuration 0 - Invalid configuration. When the 82C100 is powered up for the first time, this bit is 0, indicating that the configuration data in the configuration registers is invalid and should be set accordingly. It is also reset *to 0 whenever PS goes low for a* minimum of 20 ns, regardless of Vdd status. 1 - Valid Configuration. This bit is set to a 1 by the configuration routine after it has successfully set the configuration registers. This bit will remain a 1 as long as power remains connected to the 82C100, or unless PS goes low for longer than 20 ns.

Index 43H:R/W - DIP Switch Emulation

Used to emulate the configuration DIP switches in an XT system. Default is 30H (1 floppy, monochrome display, 256KB, no 8087). This register is provided for software compatibility only and does not actually control any devices. The exception is bit 1, that tells the 82C100 whether or not a co-processor is present. The state of this bit tells the 82C100 which RQ/GT line to use. The BIOS should scan the devices present at power-up (if the battery-backed-up SRAM that holds the configurations is determined to be invalid or not present) and set this register accordingly.

bits 7:6:	Number of diskette drives installed 00 - 1 Floppy disk installed 01 - 2 Floppy disks installed 10 - 3 Floppy disks installed 11 - 4 Floppy Disks installed
bits 5:4:	Display type 00 - EGA 01 - CGA 40 × 25 10 - CGA 80 × 25 11 - Monochrome 80 × 25
bits 3:2:	RAM size on system board 00 - 256KB 01 - 512KB 10 - 576KB 11 - 640KB
bit 1:	8087 Numeric coprocessor installed 0 - Not installed 1 - Installed
bit 0:	Loop on POST (for manufacturing test) 0 - Do not loop on POST 1 - Loop on POST

Index 44H: R/W - Substitute NMI Vector Register, Byte 0
Index 45H: R/W - Substitute NMI Vector Register, Byte 1
Index 46H: R/W - Substitute NMI Vector Register, Byte 2
Index 47H: R/W - Substitute NMI Vector Register, Byte 3

These four registers store the NMI vector that is substituted whenever an NMI is performed. This prevents modification of the NMI vector except under control of the BIOS.

Index 48H: R/W - Refresh Timer Counter

The 82C100 provides a programmable refresh counter which allows usage of slow refresh DRAMs. Each value is a multiple of 838 ns (14.31818 Mhz divided by 12). A value of 00H is invalid, because the counter will never start. Therefore the minimum allowable value is 01H for 838 ns, and the maximum value is FFH for 214 μs.

Index 49H: R/W - Wait State Select, Refresh Enable, and Keyboard Type

There are separate wait settings for I/O, memory, and DMA. The minimum number of wait states for I/O and DMA cycles is one, and the minimum for memory accesses is zero. The maximum for I/O and DMA is four, and three for memory. The refresh counter can be disabled by clearing bit 1. Bit 0 selects the type of keyboard to be used. When a PS/2 Model 25/30 keyboard is selected the

KBDATA output will be disabled, the KBCLK pin will become the IRQ1 input and port 60H will not be enabled allowing it to exist externally.

bit 7-6: MWS - Memory Wait State

00 - 0 Wait States. Default.
01 - 1 Wait State.
10 - 2 Wait States.
11 - 3 Wait States.

bit 5-4: IOWS - I/O Wait State

00 - 1 Wait State. Default.
01 - 2 Wait States.
10 - 3 Wait States.
11 - 4 Wait States.

bit 3-2: DMAWS - DMA Wait State

00 - 1 Wait State. Default.
01 - 2 Wait States.
10 - 3 Wait States.
11 - 4 Wait States.

bit 1: $\overline{\text{REFEN}}$ - Refresh Enable

0 - Disable Refresh Counter. Default
1 - Enable Refresh Counter.

bit 0: PS2KB - PS/2 Type Keyboard.

0 - XT compatible keyboard type. Default.
1 - PS/2 type keyboard.

Index 4AH: Reserved

Index 4BH: R/W - Sleep/Memory Configuration

bit 7: SL - Sleep mode enable.

0 - Sleep Function Disabled. Default.
1 - Sleep Function Enabled

bit 6: SN - Substitute NMI Vector.

The CPU attempts to read from locations 00008:0000BH when an NMI interrupt acknowledge sequence is performed. If this bit enabled, then the 82C100 substitutes the NMI vector stored in CREG<44:47H> for the vector stored in memory.

0 - Disabled. Default.
1 - Enabled.

bit 5: SP - Suspend.

0 - Disabled. Default.
1 - Enabled.

bits 4: DS - DMA Sleep Enable.

When high, this bit will stop the clock from being applied to the DMA circuit while the system is "sleeping", thus reducing power consumption. This bit does not affect operation if the sleep function is not enabled.

0 - Disabled. Default.
1 - Enabled. No DMA clock during sleep.

bits 3:0: Memory Configuration.

Four bits are used to specify one of 16 predefined 8 or 16 bit configurations from 128KB to 2.5MB.

8 bit wide Configurations

Value	B0	B1	B2	B3	Sys	EM	Total
0	—	—	—	—	—	—	0K
1	64K	64K	—	—	128K	—	128K
2	64K	—	256K	—	320K	—	320K
3	64K	64K	256K	—	384K	—	384K
4	64K	64K	256K	256K	640K	—	640K
5	256K	—	—	—	256K	—	256K
6	256K	256K	—	—	512K	—	512K
7	256K	256K	256K	—	640K	128K	768K
8	256K	256K	256K	256K	640K	384K	1024K
9	256K	256K	256K	256K	512K	512K	1024K
A	—	—	1M	—	640K	384K	1024K
B			I N V A L I D				
C	256K	256K	1M	—	640K	896K	1536K
D	—	—	1M	1M	640K	1408K	2048K
E			I N V A L I D				
F	256K	256K	1M	1M	640K	1920K	2560K

16 bit wide Configurations

Value	B0	B1	B2	B3	Sys	EM	Total
0	—	—	—	—	—	—	0K
1	64K	64K	—	—	128K	—	128K
2			I N V A L I D				
3			I N V A L I D				
4	64K	64K	256K	256K	640K	—	640K
5			I N V A L I D				
6	256K	256K	—	—	512K	—	512K
7			I N V A L I D				
8	256K	256K	256K	256K	640K	384K	1024K
9	256K	256K	256K	256K	512K	512K	1024K
A			I N V A L I D				
B			I N V A L I D				
C			I N V A L I D				
D	—	—	1M	1M	640K	1408K	2048K
E			I N V A L I D				
F	256K	256K	1M	1M	640K	1920K	2560K

Memory Configuration Options

The first column is the value that should be set in the memory configuration field. The next four columns specify the type of device used for the respective bank. The next two columns summarize the amount of memory available for system or EMS. The last column indicates the total amount of planar memory. Note: Only configurations with pairs of banks with identical devices are valid for 16 bit systems. This is because in 16 bit mode, B0 and B1 become a single 16 bit bank with the low order byte in B0 and the high order byte in B1. The same thing happens with B2 and B3.

Index 4CH: R/W - EMS Configuration Register

bit 7:4: Expanded Memory IO port address.

These bits define the single IO address port through which the EMS page registers are accessed. Bits 15:14 of the IO address are used to select which of the four page registers is being accessed.

Caution: Values that are (R)eserved should not be used, they may cause conflicts with other devices.

Value	IO Address	Value	IO Address
0H	208H	8H	288H (R)
1H	218H	9H	298H (R)
2H	228H (R)	AH	2A8H
3H	238H (R)	BH	2B8H
4H	248H (R)	CH	2C8H (R)
5H	258H	DH	2D8H (R)
6H	268H	EH	2E8H
7H	278H (R)	FH	2F8H (R)

bits 3:0: Expanded Memory Base Address

This Base Address specifies the starting address of the first 16K byte page that expanded memory is accessible at. Up to 3 more pages can be made accessible starting at successive 16K blocks.

Value	Base Address	Value	Base Address
0H	C0000H	5H	D4000H
1H	C4000H	6H	D8000H
2H	C8000H	7H	DC000H
3H	CC000H	8H	E0000H
4H	D0000H	9-FH	Reserved

4DH: Reserved
4EH: Reserved
4FH: Reserved

ADDITIONAL I/O REGISTERS

There are several extra registers needed for the enhanced features of the 82C100 such as power management. These are I/O registers located in Planar I/O Map (below 100H), and are extensions of the standard PC architecture.

72H - R/W - NMI Control

bit 7	Reserved.
bit 6	Enable Keyboard Clear NMI This bit is used when the system has been put to sleep, waiting for a keyboard entry. It will generate NMI when port 61, bit 7 is enabled. 0 - Disable Keyboard Clear NMI. Default. 1 - Enable Keyboard Clear NMI
bit 5	Enable Suspend NMI Setting this bit to 0 inhibits NMIs generated by a system POWER OFF. If the power is turned off with this bit reset to 0, and the state of the system is not saved, the application cannot resume after the next power on sequence. 0 - Disable Suspend NMI. Default. 1 - Enable Suspend NMI
bit 4	Enable Keyboard Data NMI If the bit is set to 1, an NMI will be generated when there is a pulse on KBDATA pin. This feature is used with sleep mode, to wake the system on each keystroke. (Only on XT keyboards) 0 - Disable Keyboard Data NMI. Default. 1 - Enable Keyboard Data NMI
bit 3	Enable RTC NMI 0 - Disable RTC NMI. Default. 1 - Enable RTC NMI 82C100 will generate an NMI, if this bit is set to 1, and the RTCNMI input is high, to wake the system through an RTC function such as alarm mode.

bit 2	Sleep Clock ON/OFF 0 - Sleep Clock ON. Default. 1 - Sleep Clock OFF. When this bit is set to 1, SLPCLK output of the 82C100 (pin 82) will be inactive (stays LOW) after a HALT instruction is executed.
bit 1	FDC Power Control 0 - Disable FDC Power. Default. 1 - Enable FDC Power Setting this bit to 1 will set the FDCOFF output to high. Its usage is to turn off peripherals such as the FDC to lower power consumption.
bit 0	Reserved

7EH - R/W - NMI Status, indicates the source of NMI.

When an NMI is generated, software needs to know what the source is in order to process the correct NMI service routine. The source of the NMI is latched into this register. The NMI generated to the processor is an ORed condition of any of the NMI Status register bits.

bit 7	Reserved
bit 6	IOCHCK, I/O Channel Check (pin 72) status. When this bit is set to 1, the IOCHCHK input (pin 72) is LOW indicating a parity or other error indication on memory or devices on the I/O channel.
bit 5	PERR, System memory parity error. This bit is set to 1 when there is a parity error in the planar system memory. During a memory read cycle, PAR1 (pin 92), and PAR0 (pin 93) bits are compared with the calculated parity. If they do not agree, an NMI will be generated (if NMI's are enabled), and this bit will be set.
bit 4	Keyboard Clear
bit 3	Suspend NMI Suspend NMI bit is set to 1 when all of the following conditions are met: 1. NMI Enable is set (port AxH bit 7 is 1), 2. PWRNMI input (pin 5) is high, 3. Index 4BH, bit 5 is high. This bit remains set until PWRNMI is LOW or NMI Enabled is reset.
bit 2	RTCNMI The RTCNMI bit is set to 1 when NMI is Enabled (port AxH bit 7 is 1), and the RTCNMI input (pin 27) is high. It remains set until either is reset.
bit 1	Reserved
bit 0	Keyboard Data

7FH - R/W - Power Control and Reset.

bit 7	Low Battery (suggested usage) 0 - Battery is fine 1 - Battery is low
bit 6	External Power (suggested usage) 0 - No External Power 1 - Other external power than Power Supply
bit 5:4	Reserved
bit 3	Software Controlled Reset 0 - Inactive 1 - Asserts System Reset When this bit is set, the RESET output (pin 81) will be active for a minimum of four clock pulses. Bit 6 of configuration register 41H must be set high for this function to work.
bit 2	Reserved

bit 1	Request POWER OFF. Generates Suspend NMI. Setting this bit to 1 causes a Suspend NMI to be generated that will cause a power off sequence (handled by software and external hardware). This bit should be Set/Reset through BIOS function call (INT 15H).
bit 0	Reserved

AxH - W - NMI Control (x = 0 through FH)

bit 7	NMI Enable 0 - Disable all NMIs. 1 - Enable all NMIs. Default. Resetting this bit to 0 masks off the NMI signal to the CPU. But an NMI can be recognized through software, because the source of the NMI is stored in the above NMI status register.
bit 6:0	Reserved

Enhanced Operating Modes

EXPANDED MEMORY SYSTEM

The Lotus/Intel/Microsoft Expanded Memory Specification is a functional definition of bank *switched* memory expansion modules and driver programs. EMS allows up to 8MB of expansion memory viewed as 16KB logical pages. One to four pages are available to the application software, and they can be contiguous to 64KB.

Expanded memory should not be confused with **Extended** memory. Extended memory is memory at physical addresses above 1MB while expanded memory is bank-switched and addressed below 1MB. Extended memory applies to systems with CPUs that can address physical memory larger than 1 MB, such as the 80286 or 80386.

The LIM EMS allows application software to access to memory greater than the normal 640K limit in PC and XT architecture machines. A page mapping scheme is managed by an EMS software driver. At any time up to 4 pages of successive 16KB are made accessible through various windows located from C0000H to EFFFFH. There are two registers in the Internal Configuration Register, EMIO (Expanded Memory IO port address) and EMBA (Expanded Memory Base Address). EMBA specifies the starting memory address for the first 16KB page, and EMIO defines the I/O port address for the page register. Bits 15:14 of this address are used to select which of the four page registers are being accessed. The I/O address of the page register is set in ICR 4CH.

Currently there are several varieties of Expanded Memory Specifications. The 82C100 supports the LIM EMS version 4.0.

SOFTWARE CONSIDERATIONS

The EMS installable driver, the EMM (Expanded Memory Manager), provides the hardware independent interface to the application software. The application communicates directly with the EMM through INT 67H without MSDOS intervention.

For more information please refer to:

The Lotus/Intel/Microsoft Expanded Memory Specification, Version 4.0. It is available by calling Intel at 800-538-3373.

EMS Configuration definition:

bit 7:4	EMIO	
	0H	x208H
	1H	x218H
	2H	x228H (R)
	3H	x238H (R)
	4H	x248H (R)
	5H	x258H
	6H	x268H
	7H	x278H (R)
	8H	x288H (R)
	9H	x298H (R)
	AH	x2A8H
	BH	x2B8H
	CH	x2C8H (R)
	DH	x2D8H (R)
	EH	x2E8H
	FH	x2F8H (R)

	Where x = 0, 4, 8 or CH to select one of the four EMS page registers. This upper nibble must be sent correctly by the I/O instruction, but is not used in the actual decode of the I/O port. Note that those ports marked with an (R) should not be used because of potential address conflicts.	
3:0	EMBA	
	0H	C0000H
	1H	C4000H
	2H	C8000H
	3H	CC000H
	4H	D0000H
	5H	D4000H
	6H	D8000H
	7H	DC000H
	8H	E0000H
	9H:FH	Reserved

To access EMS memory:

1. Select starting memory address through the ICR, i.e.:
   a. Write Index 4CH to port 22H
   b. Select EMBA to be used (low nibble)
   c. Select EMIO to be used (high nibble)
   d. Write EMBA and EMIO (as a byte) to port 23H.
2. Write the four EMS page registers. The address is determined by EMIO plus the highest 2 bits (bit 15:14) of the I/O port address to select which of the four registers being accessed. Each byte in the page register selects a 16KB block of EMS memory.
3. The EMS memory is then accessed through the window selected above (EMBA). The size of the window is 64KB. The four 16KB pages are located within the window according to the following table:

Page Register	Address
0	Window base
1	Window base + 8000H*
2	Window base + 4000H*
3	Window base + C000H

*** Note that these are not in order.**

The bit assignment of the page registers is as per the LIM specification. The MSB (Most Significant Bit) is the enable bit for accessing the expanded memory. Setting that bit allows software to access expanded memory. The rest of the bits are used for selecting any of the available 16KB pages. The maximum value of the page register would depend on how much memory is available for EMS.

For example in 1 MB system, upper 384KB can be addressed as expanded memory. In this case the valid page register values in order to access the expanded memory would be 80H through 97H, as there are 18H pages available for expanded memory.

POWER MANAGEMENT

The 82C100 implements power management features that reduce power consumption and prolong battery life for lap-top type systems. The BIOS needs to be extended to support the additional hardware. The power management features are:

A. Sleep Mode

When sleep mode is entered, the system clock is stopped when waiting for an external event to occur, such as a keyboard/floppy busy condition.

B. Suspend/Resume Mode

Suspend/Resume mode is a system option that enables a user to turn off (Suspend) the system and save the current application. When power is turned on, the application is resumed.

Extra circuitry is needed to allow power to be turned off under program control and to prevent power from being turned OFF directly from the ON/OFF switch.

Sleep Mode

The sleep function is used to stop the system clocks when an application is waiting for an external event such as an input from the keyboard or an IO operation. This mode is used to reduce power consumption and extend battery life. When the system is in sleep

mode, interrupts are processed as normal. After each interrupt is serviced, control is returned to the sleep function to find out if the specified event has occurred. If it has, control is returned to the application; otherwise sleep mode is reentered.

There are two System Clocks available from the 82C100. SYSCLK is a free running clock, SLPCLK is SYSCLK that can be turned OFF through software. SLPCLK should be used by the processor, coprocessor, and any other static peripherals that consume less power when the clock is not present and can be recovered by reissuing the clock.

The FDCOFF, (Floppy Disk Controller OFF) output (pin 28), will be forced HIGH when SLEEP is invoked. The purpose is to turn off the FDC and other peripherals, so power consumption will be minimized. FDCOFF should be connected to the chip enable of the peripherals. Most chip enables are active low, so FDCOFF can be connected directly.

The internal DMACLK is normally off when in SLEEP, but it can be selected to be on by setting a bit in the ICR. In SLEEP mode, the rest of the circuitry inside the 82C100 is still active. The 82C100 is still functional but DMA requests (including refresh) will be lost because the processor is not being clocked. The current version of the part does not wake up the CPU in response to a DMA (refresh) request. This implies that a system using sleep mode would use static RAMs. If DRAMs need to be refreshed during sleep mode, an external circuit to perform this function must be added.

The application can invoke sleep mode through the system services function call (interrupt 15). The BIOS automatically invokes sleep mode for device busy conditions or when waiting for input from the keyboard.

The mechanism of SLEEP mode is as follows:

1. SLEEP mode must be enabled by setting bit 7 of ICR 4BH to 1.
2. Enable the NMI Control (default I/O Address 72H)
3. Application software requests SLEEP by passing a SLEEP parameter, and issues INT15 to BIOS.
4. The BIOS then does its housekeeping, saving all the necessary parameters and registers for it to return properly. Then it activates the sleep command by setting bit 2 of port 72H (NMI Control Register). As soon as this bit is written, FDCOFF (pin 28) becomes active to disable the FDC. The 82C100 then waits for a HALT instruction before turning off SLPCLK, to allow software to finish executing any further code.

To recover from sleep mode:

1. An external device issues an NMI or IRQ. The 82C100 turns SLPCLK on whenever it sees an interrupt request, whether it is an IRQ or a NMI.
2. The BIOS retrieves the machine states and resumes the previous application.

System Suspend (Power Off)

When PWRGOOD is inactive (LOW), the system is in power down mode. All of the clocks are at DC, input lines are at tristate and output lines are at either tristate or LOW. Power can be turned off by throwing a real power ON/OFF switch, or done through software. The system suspend feature allows a controlled power-off sequence. Power is not shut off immediately—the system goes through a power-down sequence beforehand. The purpose is to save the machine states, so that it can resume operation as normal when power is turned on.

When the user presses the power switch to OFF or when an application requests a system POWER-OFF through a BIOS call (INT 15), the BIOS suspend function saves the necessary system information in a non-volatile RAM area.

System Resume (Power On)

When the power-on sequence is started in RESUME mode, the self-test procedures are activated. POST checks to see if the Suspend mode is enabled. If so, it does a modified reset. If it passed the diagnostics successfully,

then the information saved during the SUSPEND sequence is restored and a return from the NMI is executed. This causes the program that was executing when SUSPEND mode was invoked to resume execution.

CLOCK GENERATION AND SWITCHING

The 82C100 supports two clock speeds for the CPU and system bus: 4.77 MHz, and 1/3 of the POSC frequency. It also supports two duty cycles: 33% and 50% to support 808X and NEC's V20/V30 CPUs. Clock switching is synchronized, based on an edge detector that holds the clock low while switching from one clock to the other eliminating any short clock pulses.

On power up the defaults are:

4.77 MHz system clock (210 ns clock cycle)
33% duty cycle for CPU clock

To switch clock speed or duty cycle the following sequence should be followed:

1. Set the desired number of wait states for memory, I/O and DMA, and command delay to guarantee setup and hold time for the new bus speed. Write these values to the appropriate ICR (please refer to Internal Configuration Register section).
2. Switch the clock by writing to ICR 40H.

I/O CHANNEL TIMING CONTROL

I/O channel timing can be manipulated by setting the appropriate number of wait states, and setting command delay ON/OFF. Adding wait states makes the cycles longer and provides more data setup time. The wait state logic adds Tw's between T3 and the last cycle (T4). On the other hand, delaying the command gives more time for address setup. If command delay is enabled, the commands ($\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$, and $\overline{MEMW}$) are delayed by one clock cycle and become active at T3 instead of T2. Therefore the time between address valid to command active is 1 cycle longer than normal cycles, allowing more time for external devices to decode the address. Command delay is applicable for both I/O and memory cycles. By setting ICR 41H bit 3 to 1, commands are delayed by 1 cycle. Default is normal, no delays.

DATA CONVERSION

Since the 82C100 can operate with 16 bit processors (8086 or V30), a 16 bit multiplexed data bus must be supported. The 82C100 will control and perform data conversion between the 16 bit processor data and the 8 bit IO channel.

The effect of bus conversions are:

1. A 16 bit processor read is converted to two 8 bit IO channel reads.
2. A 16 bit processor write is converted to two 8 bit IO channel writes.

The 82C100 recognizes the need for bus conversion cycles when the following three conditions are met:

1. $\overline{BHE}$ is LOW.
2. A0 is LOW.
3. External cycles. 82C100 determines internal or external cycles by decoding the address and status information. The cycles requiring bus conversion are: Any memory access to a location not in the planar RAM or ROM and I/O cycles to locations not internal to the 82C100.

The cross over is done internally. The 82C100 provides the signals to control the enables and directions of the external buffers. Refer to the conversion cycle timing on the next pages.

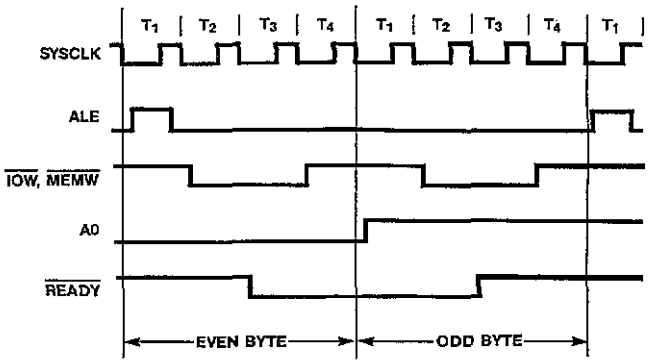
16 bit CPU write to 8 bit device sequence:

1. The 82C100 issues NOT-READY (READY is low) to the CPU when it recognizes any bus conversion cycles.
2. CPU transfers 16 bit data to the 82C100.
3. 82C100 allows the low byte to go through by setting $\overline{PBEN}$ LOW and PBIN HIGH.
4. The low byte is transfered directly to the I/O channel. $\overline{DBEN}$ is set LOW to enable the I/O channel data buffer.
5. After low byte transfer, 82C100 toggles A0 to HIGH, sending the odd address to the I/O channel.

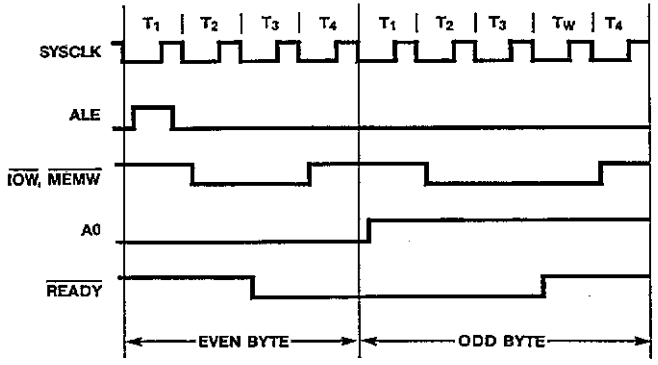
6. The high byte is transfered to the low byte internal to the 82C100. The write command is generated and a wait state is added if programmed to do so. The second (high) byte is transfered.
7. READY is set to HIGH, indicating the end of transfer.

16 bit CPU read from 8 bit device sequence:

1. 82C100 issues NOT-READY to CPU.
2. A0 is set LOW.
3. The 82C100 generates a read command and reads the low byte external data into the on board low byte.
4. A0 is toggled HIGH.
5. A second read command is generated.
6. The 82C100 transfers the low byte into high byte internally.
7. The 82C100 changes READY to HIGH indicating the end of transfer.



Write Conversion Cycle
(0 Memory Wait States)



Read Conversion Cycle
(0 Memory Wait States)

Address Mapping

IO MAP

Address	R/W	Description
DMA Controller		
000H	R/W	DMA Channel 0 current address
001H	R/W	DMA Channel 0 current word count
002H	R/W	DMA Channel 1 current address
003H	R/W	DMA Channel 1 current word count
004H	R/W	DMA Channel 2 current address
005H	R/W	DMA Channel 2 current word count
006H	R/W	DMA Channel 3 current address
007H	R/W	DMA Channel 3 current word count
008H	W	DMA Command Register
	R	DMA Status Register
009H	W	DMA Request Register
00AH	W	DMA Single Bit Mask Register
00BH	W	DMA Mode Register
00CH	W	DMA Clear Byte Pointer
00DH	W	DMA Master Clear
00EH	W	Clear Mask Register
00FH	W	DMA Write All Mask Register Bit

Interrupt Controller		
020H	W	INTC ICW1
	W	INTC OCW2
	W	INTC OCW3
	R	INTC Interrupt Request Register (I_{RR})
	R	INTC In-Service Register (ISR)
	R	INTC Polling Data Byte
021H	W	INTC ICW2
	W	INTC ICW4
	W	INTC OCW5
	R	INTC Interrupt Mask Register (IMR)

Internal *Configuration* Registers		
022H	R/W	Internal Configuration Index Register
023H	R/W	Internal Configuration Data Register

Index		Description
40H	R/W	Clock/Mode
41H	R/W	System Configuration
42H	R/W	Configuration Valid
43H	R/W	PC/XT DIP Switch Emulation
44H	R/W	NMI Vector Byte 0 (LSB)
45H	R/W	NMI Vector Byte 1
46H	R/W	NMI Vector Byte 2
47H	R/W	NMI Vector Byte 3 (MSB)
48H	R/W	Refresh Counter
49H	R/W	Wait, Refresh, Keyboard
4AH	—	Reserved
4BH	R/W	Memory Configuration
4CH	R/W	EMS Control
4D:4FH	—	Reserved

Timer/Counter Registers		
040H	R/W	Timer 0 Count Load/Read
041H	R/W	Timer 1 Count Load/Read
042H	R/W	Timer 2 Count Load/Read
043H	R/W	Timer Control Word

PPI Registers		
060H	R/W	Parallel Port A
061H	R/W	Parallel Port B
062H	R/W	Parallel Port C

Additional I/O Registers		
072H	R/W	NMI Control
07EH	R/W	NMI Status
07FH	R/W	Power Control
0AxH	R/W	NMI Mask
0CxH	R/W	Reserved
0ExH	R/W	Reserved

Note: x = 0-FH

DMA Page Registers		
080H	W	DMA Channel 0 Page Register
081H	W	DMA Channel 1 Page Register
082H	W	DMA Channel 2 Page Register
083H	W	DMA Channel 3 Page Register

EMS Page Registers		
x208H	R/W	EMS Page Register
x218H	R/W	EMS Page Register
x228H (R)	R/W	EMS Page Register
x238H (R)	R/W	EMS Page Register
x248H (R)	R/W	EMS Page Register
x258H	R/W	EMS Page Register
x268H	R/W	EMS Page Register
x278H (R)	R/W	EMS Page Register
x288H (R)	R/W	EMS Page Register
x298H (R)	R/W	EMS Page Register
x2A8H	R/W	EMS Page Register
x2B8H	R/W	EMS Page Register
x2C8H (R)	R/W	EMS Page Register
x2D8H (R)	R/W	EMS Page Register
x2E8H	R/W	EMS Page Register
x2F8H (R)	R/W	EMS Page Register

Notes:
1. x = 0H, 4H, 8H, or CH
2. (R) are reserved and should not be used to avoid conflicts with other devices.
3. *Only one of these registers will exist at one time.* The actual address used is programmable.

Memory Map		
00000-9FFFFH	R/W	RAM
C0000-EFFFFH	R/W	EMS
F0000-FFFFFH	R	ROM

82C100 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	3.0	5.5	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{OP}	-25	85	°C
Storage Temperature	T_{STG}	-40	125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C100 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	°C

Capacitance (T_A = 25°C, V_{CC} = GND = 0V)

Sym	Parameter	Min.	Max.	Units	Test Conditions
C_{IN}	Input Capacitance	—	10	pF	SYSCLK = 0.5MHz
C_{OUT}	Output Capacitance	—	20	pF	Returned to V_{SS}
$C_{I/O}$	I/O Capacitance	—	20	pF	Unmeasured pins

DC Characteristics (T_A = 25°C, V_{CC} = 5V ± 5%)

Sym	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage	—	0.4	V	I_{OL} = 4.0mA (1)
V_{OH}	Output High Voltage	2.4	—	V	I_{OH} = -4.0mA (2)
V_{CL}	Clock Output Low		0.4	V	I_{OL} = 4.0mA
V_{CH}	Clock Output High	3.9		V	I_{OH} = -4.0mA
I_{IL}	Input Leakage Current	-10	20	µA	V_I = V_{CC} to 0V
I_{OL}	Output Leakage Current	-10	20	µA	V_O = V_{CC} to 0.45V
I_{CC}	V_{CC} Supply Current	—	30	mA	POSC = 30MHz
I_{STBY}	Standby Current	—	100	µA	POSC = DC

Notes:
1. I_{OL} = 12mA for $\overline{RASn}$, AD0-AD7, I_{OL} = 24mA for KBCLK, KBDATA.
2. I_{OH} = -24mA for $\overline{RASn}$, AD0-AD7.

82C100 AC Characteristics (T_A = 0-70°C, V_{CC} = 5V ±5%)

Symbol	Parameter	Min	Max	Units
Reset Signals				
t1	V_{CC} Valid to PWRGOOD Active	1		ms
t2	PWRGOOD to $\overline{SYSRST}$ Inactive	200		ms
t3	RESET Active from PWRGOOD	0		ns
t4	RESET Inactive from CLK	10	Tc/3	ns
t5	PWRGOOD to $\overline{PS}$ Inactive	10		µs

82C100 AC Characteristics (Continued)

Symbol	Parameter	Min	Max	Units
Clock Signals				
t10	CX1, POSC Cycle Time	34		ns
t11	CX1, POSC Rise Time		10	ns
t12	CX1, POSC Fall Time		10	ns
t13	CX1, POSC High Time	10		ns
t14	CX1, POSC Low Time	10		ns
t15	CX1, POSC to OSC Delay	8	14	ns
t17	OSC Cycle Time	34		ns
t18	OSC Rise Time		8	ns
t19	OSC Fall Time		8	ns
t21	OSC High Time			ns
t22	OSC Low Time			ns
t23	CLK Rise Time		8	ns
t24	CLK Fall Time		8	ns
t25	CLK High Time (33% Duty Cycle)			ns
t26	CLK Low Time (33% Duty Cycle)			ns
t27	CLK High Time (50% Duty Cycle)			ns
t28	CLK High Time (50% Duty Cycle)			ns
t29	CLK Cycle Period (T_C)	100		ns
POSC	POSC Frequency	DC	30	MHz
OSCI	OSCI Frequency	DC	30	MHz
Arbitration and Ready Signals				
t30	$\overline{RQ}$ Active from CLK	5	45	ns
t31	$\overline{RQ}$ Inactive from CLK	5	35	ns
t32	$\overline{GT}$ Setup from CLK	5	35	ns
t33	$\overline{GT}$ Setup from CLK	5	45	ns
t34	$\overline{REL}$ Active from CLK	5	45	ns
t35	$\overline{REL}$ Inactive from CLK	5	30	ns
t36	$\overline{IOCHRDY}$ Setup to CLK	5	30	ns
t37	$\overline{IOCHRDY}$ Hold to CLK	5	30	ns
t38	READY Inactive from CLK	0	15	ns
t39	READY Active from CLK	0	15	ns
CPU Interface Signals				
t40	ALE Active from CLK	5	40	ns

82C100 AC Characteristics (Continued)

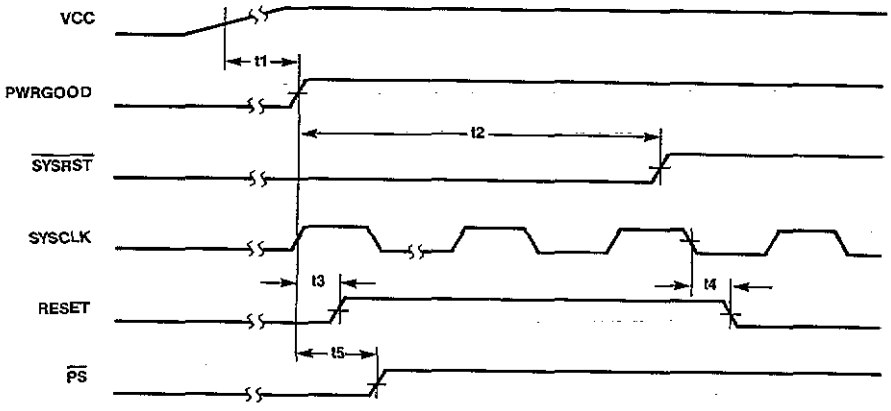
Symbol	Parameter	Min	Max	Units
t41	ALE Inactive from CLK (rising edge T1)	8	24	ns
t42	$\overline{PBEN}$ Active from CLK	10	30	ns
t44	$\overline{PBEN}$ Inactive from CLK	$T_C/3$	$T_C/3+35$	ns
t45	PBIN Delay from CLK	5	30	ns
t46	PBIN Active from CLK	$T_C/3$	$T_C/3+20$	ns
t47	PBIN Inactive from CLK	$2T_C/3$	$2T_C/3+30$	ns
t48	$\overline{DBEN}$ Active from CLK (read)	$2T_C/3$	$2T_C/3+30$	ns
t49	$\overline{DBEN}$ Active from CLK (write)	0	30	ns
t50	$\overline{DBEN}$ Inactive from CLK (read/write)	$T_C/3$	$2T_C/3$	ns
t51	DBIN Active from CLK	0	60	ns
t52	DBIN Inactive from CLK	$T_C/3$	$T_C/3+30$	ns
t53	Command Active from CLK	0	45	ns
t54	Command Inactive from CLK	0	45	ns
t55	DEN Active from CLK (read)	$2T_C/3$	$2T_C/3+30$	ns
t56	DEN Active from CLK (write)	0	30	ns
t57	DEN Inactive from CLK (read)	10	30	ns
t58	DEN Active from CLK (write)	$2T_C/3$	$2T_C/3+30$	ns
t59	$\overline{BHE}$ Active from CLK	10	45	ns
t60	$\overline{BHE}$ Inactive from CLK	10	45	ns
t61	A0 Delay from CLK	20	55	ns
DRAM Control Signals				
t63	$\overline{RAS}$ Active from CLK	$T_C/3$	$T_C/3+25$	ns
t64	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ Inactive from CLK	$T_C/3$	$T_C/3+25$	ns
t65	$\overline{CAS}$ Active from CLK	0	20	ns
t66	$\overline{WE}$ Active from CLK	$2T_C/3$	$2T_C/3+25$	ns
t67	Row Address Delay From CLK	30	85	ns
t68	Column Address Delay From CLK	$2T_C/3$	$2T_C/3+25$	ns
t69	Address Float Delay From CLK	$T_C/3$	$T_C/3+30$	ns
ROM and SRAM Signals				
t70	$\overline{ROMCS}$ Active from CLK	0	30	ns
t71	$\overline{ROMCS}$ $\overline{CSn}$, $\overline{SEL}$ Inactive from CLK	0	30	ns
t72	$\overline{CSn}$, $\overline{SEL}$ Active from CLK	0	55	ns
t73	SRAM $\overline{WE}$ Active from CLK	0	60	ns
t74	SRAM $\overline{WE}$ Inactive from CLK	0	40	ns

82C100 AC Characteristics (Continued)

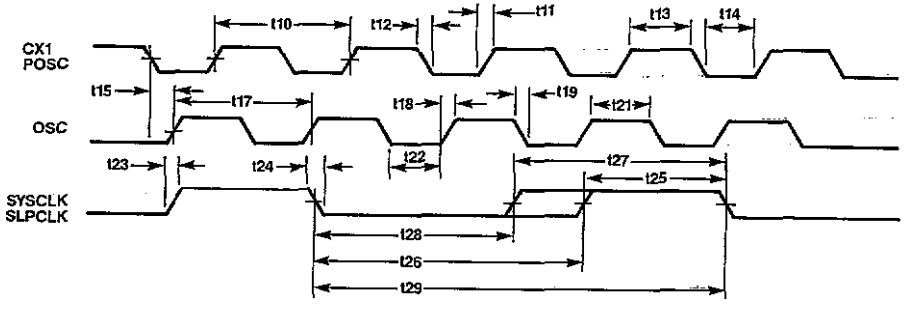
Symbol	Parameter	Min	Max	Units
DMA Controller Signals				
t80	DREQ Setup to CLK	0		ns
t81	DREQ Hold to CLK	0		ns
t82	AEN Active from CLK	$2T_C/3$	$2T_C/3+30$	ns
t83	AEN Inactive from CLK	$2T_C/3$	$2T_C/3+30$	ns
t84	DACK Active from CLK	0	100	ns
t85	DACK Inactive from CLK	0	100	ns
t86	Command Active from CLK	0	45	ns
t87	Command Inactive from CLK	0	45	ns
t89	AD0-AD15, A16-A19 Valid from CLK	0	60	ns
Interrupt Controller Signals				
t112	INTR Active from IRQ		300	ns
t113	INTR Inactive from CLK	0	45	ns
t116	INTR Vector Setup from CLK	30		ns
t117	INTR Vector Hold from CLK	10		ns
t118	IRQ, NMI Low Width	100		ns
t119	Command Recover Time	150		ns

Notes:
1. Measured between 1.0V to 3.5V for 8088/8086 CPU
2. Measured between 1.5V adn 3.0V for V20/V30 CPU

82C100 Timing Diagrams

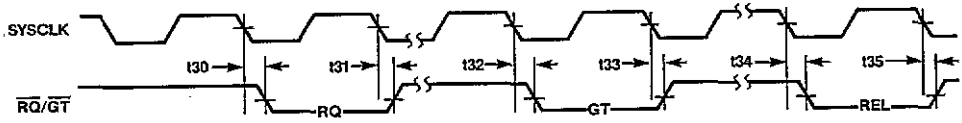


Reset Signals

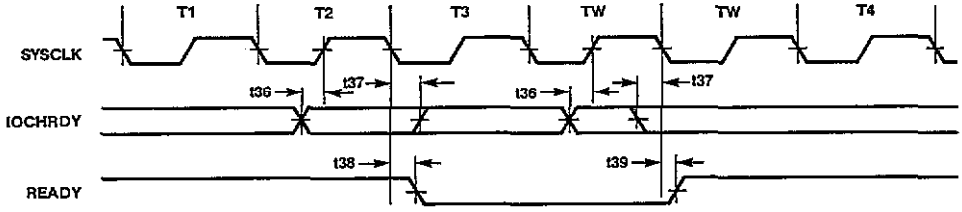


Clocks

82C100 Timing Diagrams *(Continued)*

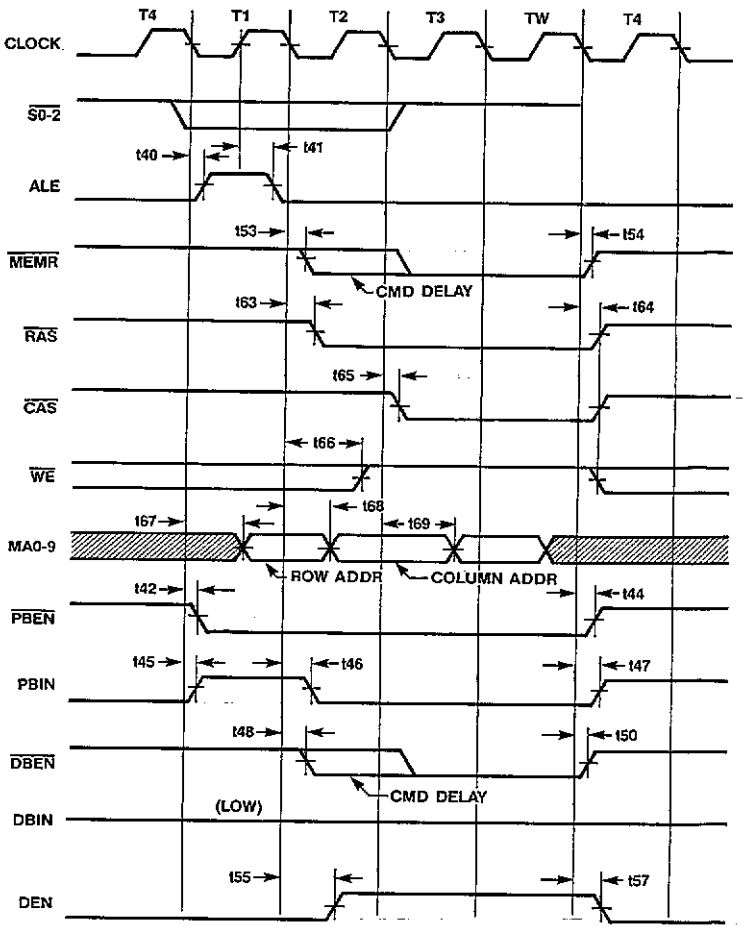


Request/Grant/Release



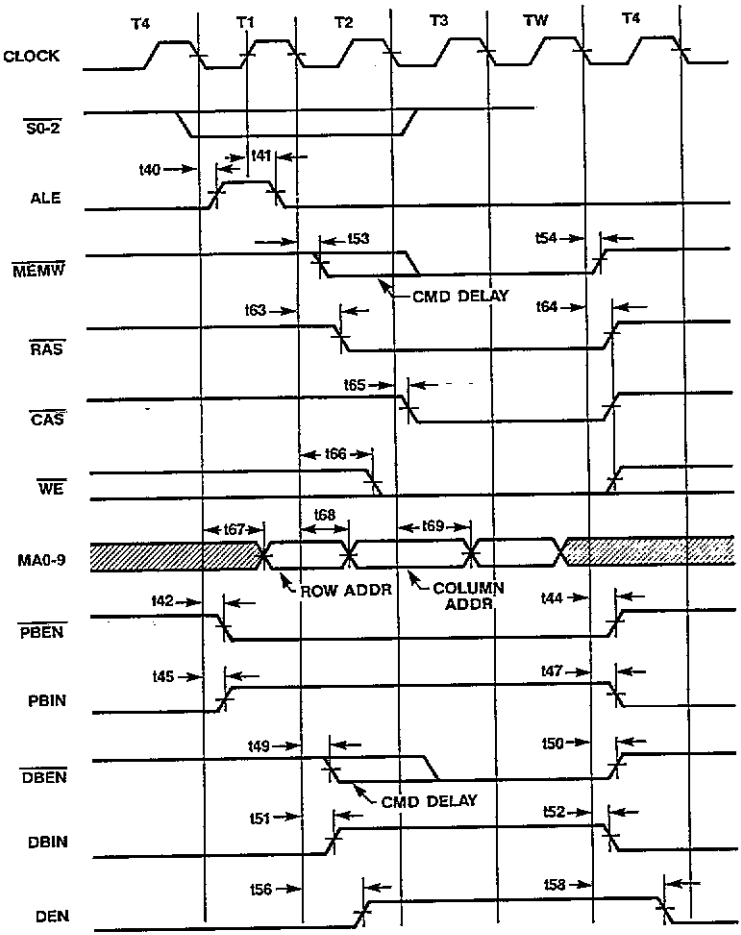
Ready Timing

82C100 Timing Diagrams (Continued)



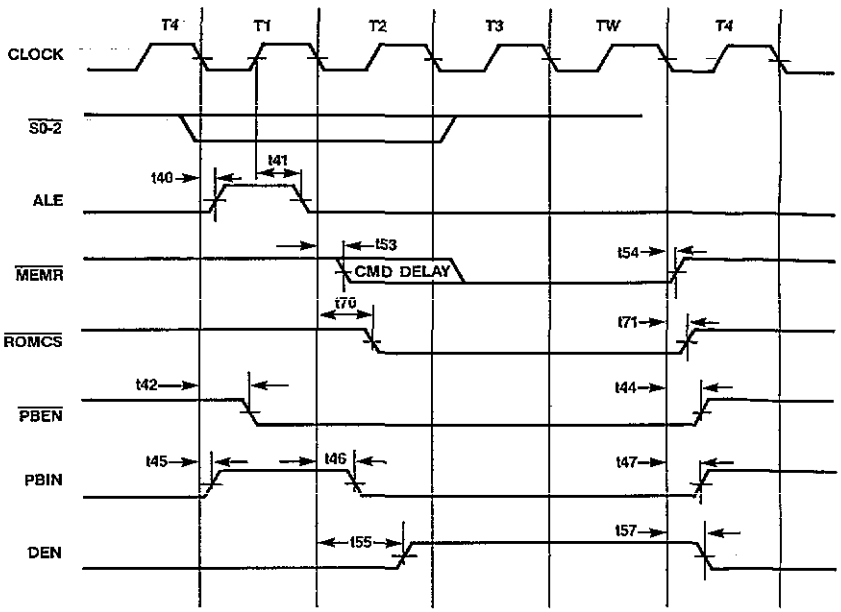
Memory Read

82C100 Timing Diagrams (Continued)



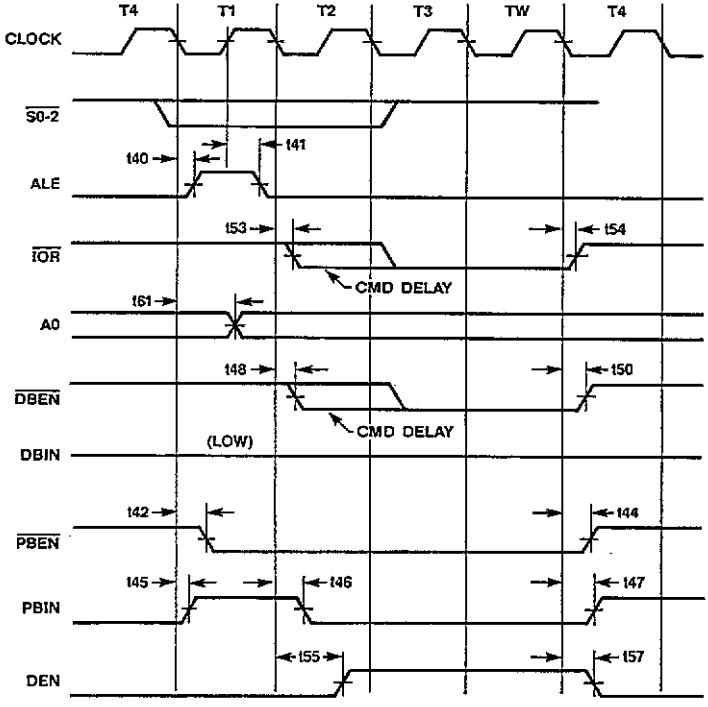
Memory Write

82C100 Timing Diagrams (Continued)



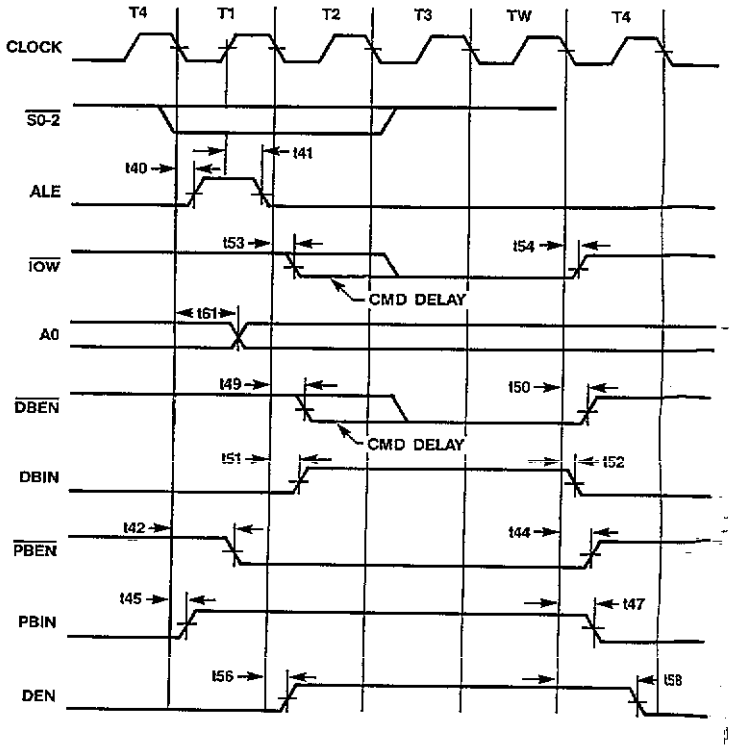
ROM BIOS Read

82C100 Timing Diagrams (Continued)



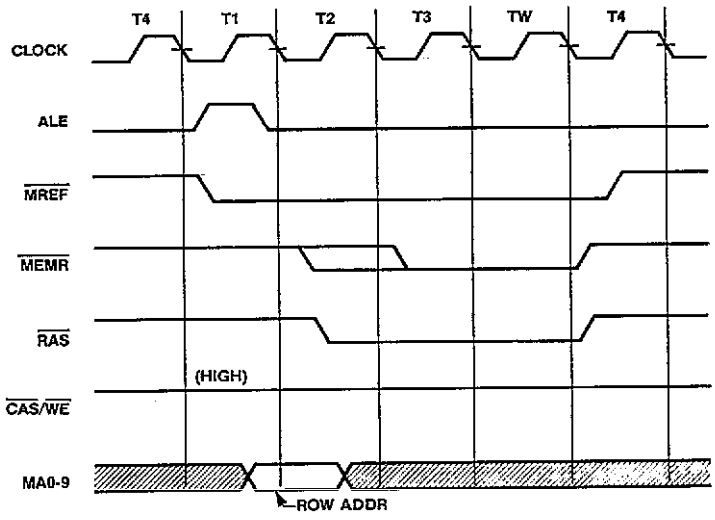
I/O Read

82C100 Timing Diagrams (Continued)

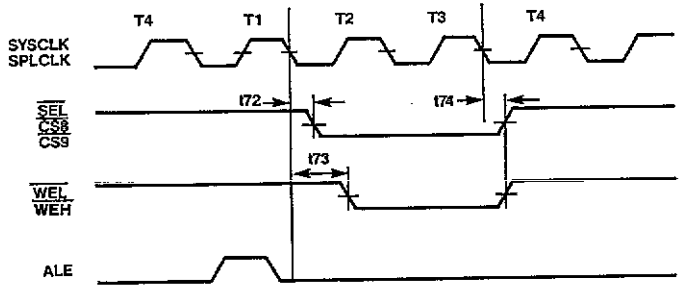


I/O Write

82C100 Timing Diagrams (Continued)

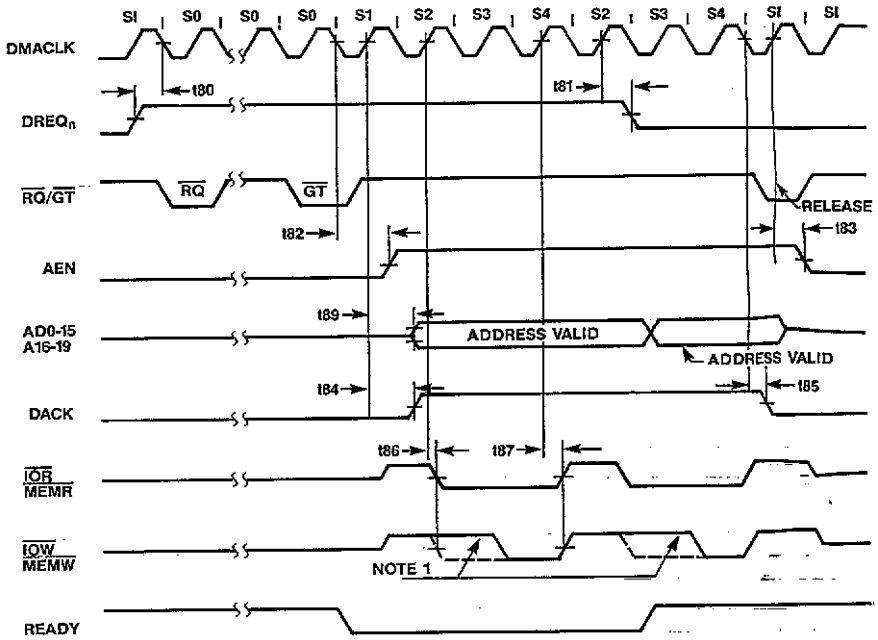


Memory Refresh Cycle



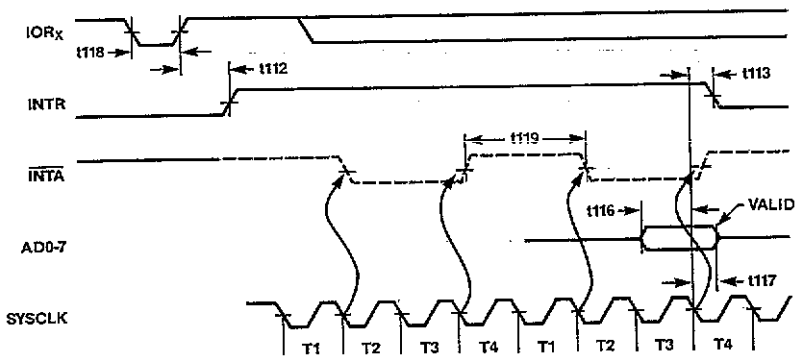
Static RAM Timing

82C100 Timing Diagrams (Continued)



Note 1: Extended Write Mode

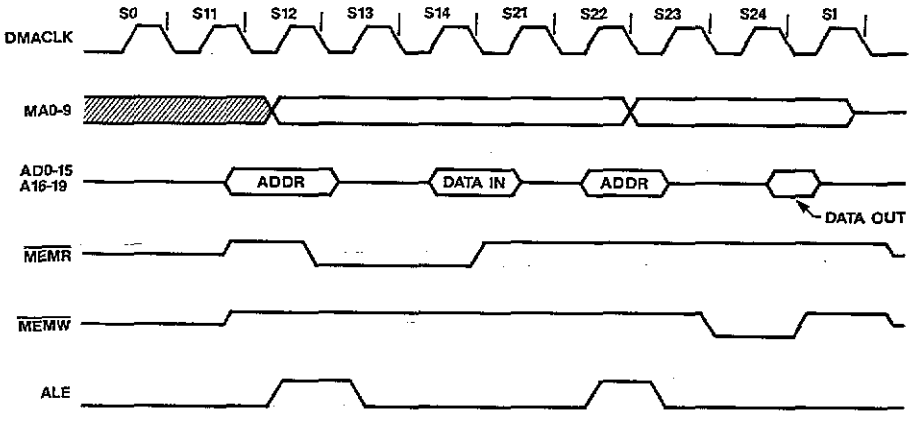
DMA Basic Timing



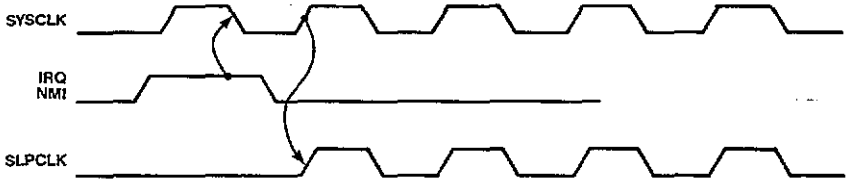
Note 1: INTA is internal to the 82C100

INTA Sequence/NMI Vector Substitution

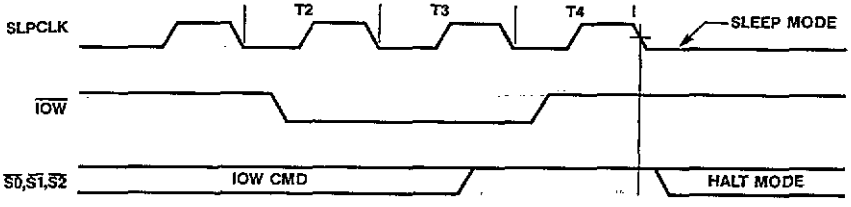
82C100 Timing Diagrams (Continued)



Memory to Memory DMA Transfer

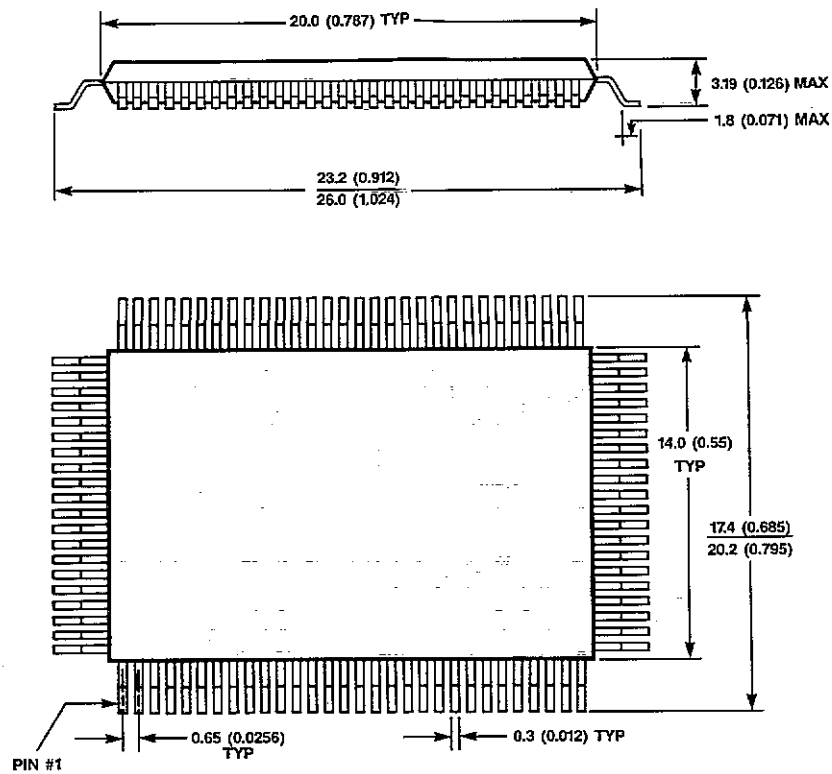


Wake Up Sequence



Sleep Sequence

100-PIN PLASTIC FLAT PACKAGE (RECTANGULAR) DIMENSIONS: mm (in)



Ordering Information

Order Number	Package Type
F82C100	PFP-100

Notes:
1. PFP = Plastic Flat Package

CHIPS Regional Sales Offices

California, Irvine
Chips & Technologies, Inc.
(714) 852-8721

California, San Jose
Chips & Technologies, Inc.
(408) 437-8877

Georgia, Norcross
Chips & Technologies, Inc.
(404) 662-5098

Germany, Munich
Chips & Technologies, Inc.
49.89.4610.0530

Illinois, Itasca
Chips & Technologies, Inc.
(312) 250-0075

Korea, Seoul
Chips & Technologies, Inc.
82 2 551 2723

Massachusetts, Burlington
Chips & Technologies, Inc.
(617) 273-3500

Pennsylvania, Blue Bell
Chips & Technologies, Inc.
(215) 540-2214

Texas, Dallas
Chips & Technologies, Inc.
(214) 702-9855

Taiwan, R.O.C.
Taipei
Chips & Technologies, Inc.
886 2 717-5595

CHIPS International Distributors

CENTRAL AMERICA

Central America
Mexico, Guadalajara
Sonika
5236-474-250

FAR EAST

Australia
Victoria, Burwood
R&D Electronics
61-808-8911

Hong Kong
Kwun Tong, Hong Kong,
Wong's Kong King Ltd.
852-345-0121

India
Santa Clara, CA (USA)
Silicon Electronics
(408) 988-4408

Israel
Tel-Aviv
CVS
9723-544-7475

Japan
Tokyo
ASCII Corporation
813-479-0486

Korea
Seoul
Kortronics Enterprises
82 2 562 90557

Singapore
Singapore
Chartered Telmos Design
PTE Ltd.
65 778 9331

Taiwan, R.O.C.
Taipei
Union Technology Corp.
886-2-501-8170

Taipei
World Peace
Industrial Co., Ltd.
886-2-505-6345

EUROPE

Belgium, Bruxelles
Auriema Belgium S.A./N.V.
32 (02) 523-62-95

Finland, Helsinki
OY Fintronic AB
358 06926022

France, Le Chesnay
A2M
331 39.54.91.13

Germany, Nettatal
Rein Elektronik GmbH
49 (02153) 733-0

Italy, Balsamo
Moxel S.r.l.
39 (02) 61.29.0521

Netherlands, Eindhoven
Auriema Nederland B.V.
31 (0) 40-816565

Spain, Madrid
Compania Electronica
de Tecnicas
Aplicadas, S.A.
34-1-754-3001

Spain, Barcelona
Compania Electronica
de Tecnicas
Aplicadas, S.A.
34-3-300-7712

Switzerland, Dietikon
DataComp AG
41 01 740 51 40

United Kingdom, Berkshire,
Maidenhead
Katakana Limited
Maidenhead 44 628 75641

NORDIC COUNTRIES

Denmark, Herlev
Nordisk Elektronik A/S
45-284-20-00

Norway, Hvalstad
Nordisk Elektronik A/S
47 02 84 62 10

Sweden, Kista
Nordisk Elektronik A.B.
468 703 4630

CHIPS Sales Representatives

UNITED STATES

Alabama, Huntsville
The Novus Group, Inc.
(205) 534-0044

Arizona, Scottsdale
AzTECH Component Sales
(602) 991-6300

California, Santa Clara
Magna Sales
(408) 727-8753

California, San Diego
S.C. Cubed
(619) 481-0757

California, Thousand Oaks
S.C. Cubed
(805) 496-7307

California, Tustin
S.C. Cubed
(714) 731-9206

Colorado, Wheat Ridge
Wescom Marketing, Inc.
(303) 422-8957

Florida, Casselberry
Dyne-A-Mark Corporation
(407) 831-2822

Florida, Clearwater
Dyne-A-Mark Corporation
(813) 441-4702

Florida, Ft. Lauderdale
Dyne-A-Mark Corporation
(305) 771-6501

Georgia, Lilburn
The Novus Group, Inc.
(404) 263-0320

Idaho, Boise
Wescom Marketing, Inc.
(208) 335-6654

Illinois, Hoffman Estates
Micro-Tex, Inc.
(312) 382-3001

Indiana, Carmel
Giesting & Associates
(317) 844-5222

Maryland, Annapolis
ESS
(301) 269-4234

Massachusetts, Woburn
Mill-Bern Associates, Inc.
(617) 932-3311

Michigan, Comstock Park
Giesting & Associates
(616) 784-9437

Michigan, Livonia
Giesting & Associates
(313) 478-8106

Minnesota, Eden Prairie
High Technology Sales Assoc.
(612) 944-7274

New Jersey, Bellmawr
T.A.I.
(609) 933-2600

New York, Commack
ERA, Incorporated
(516) 543-0510

North Carolina, Raleigh
The Novus Group
(919) 833-7771

Ohio, Cincinnati
Giesting & Associates
(513) 385-1105

Ohio, Cleveland
Giesting & Associates
(216) 261-9705

Oregon, Beaverton
L-Squared Limited
(503) 629-8555

Pennsylvania, Pittsburgh
Giesting & Associates
(412) 963-5832

Texas, Austin
OM Sales
(512) 388-1151

Texas, Houston
OM Sales
(713) 789-4426

Texas, Richardson
OM Sales
(214) 690-6746

Utah, Salt Lake City
Wescom Marketing, Inc.
(801) 269-0419

Washington, Kirkland
L-Squared Limited
(206) 827-8555

Wisconsin, Waukesha
Micro-Tex, Inc.
(414) 542-5352

CANADA

Ontario, Kanata
Electro Source, Inc.
(613) 592-3214

Ontario, Rexdale
Electro Source, Inc.
(416) 675-4490

Quebec, Pointe Claire
Electro Source, Inc.
(514) 630-7846

Chips and Technologies, Inc.
3050 Zanker Road, San Jose, CA 95134 408-434-0600 telex 272929 CHIPS UR