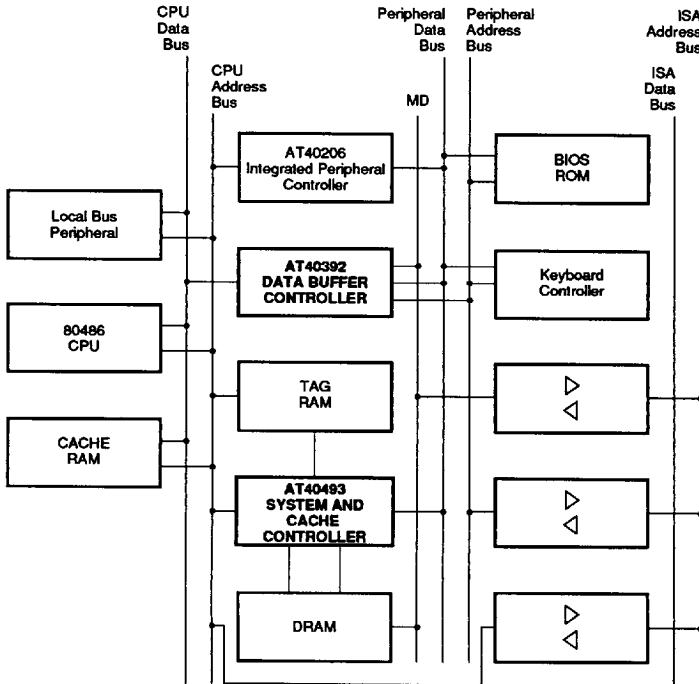


**Features**

- Two-Chip PC/AT Compatible Chip Set for 80486 Based Systems  
 Operating up to 50 MHz  
     AT40493 System and Cache Controller  
     AT40392 Data Buffer Controller
- Two 160-Pin Quad Flatpacks
- On-Chip Support for Direct-Mapped Write-Back Cache
- 0 Wait State Cache Read Hit and Programmable 0/1 Wait State Cache Write Hit
- Two Programmable Non-Cacheable Regions
- On-Chip Tag Comparator
- Burst Line Fill During Cache Read Misses
- Page Mode Main Memory Operation with Programmable Wait States Supporting Platform Memory Sizes up to 64 Mbytes
- Support for 256K, 1-Mbit and 4-Mbit DRAMs
- Low Power CAS# Before RAS#, Transparent DRAM Refresh
- Low Power, Slow Refresh for Laptop PC Operation
- Parity Generation and Detection
- Support for Shadow RAM
- Cacheable Video BIOS Option
- 8042 Emulation for Fast CPU Reset and Gated A20 Generation
- ISA Bus Control with Programmable Clock
- 0 or 1 Wait State for 16-Bit ISA Bus Cycles
- Support for Local Bus Peripherals
- Supports 2-1-1-1 and 3-2-2-2 Cache and DRAM Burst Cycles

**80486  
PC/AT  
Chip Set**

**Block Diagram**



9



1074177 0005723 0??

## Description

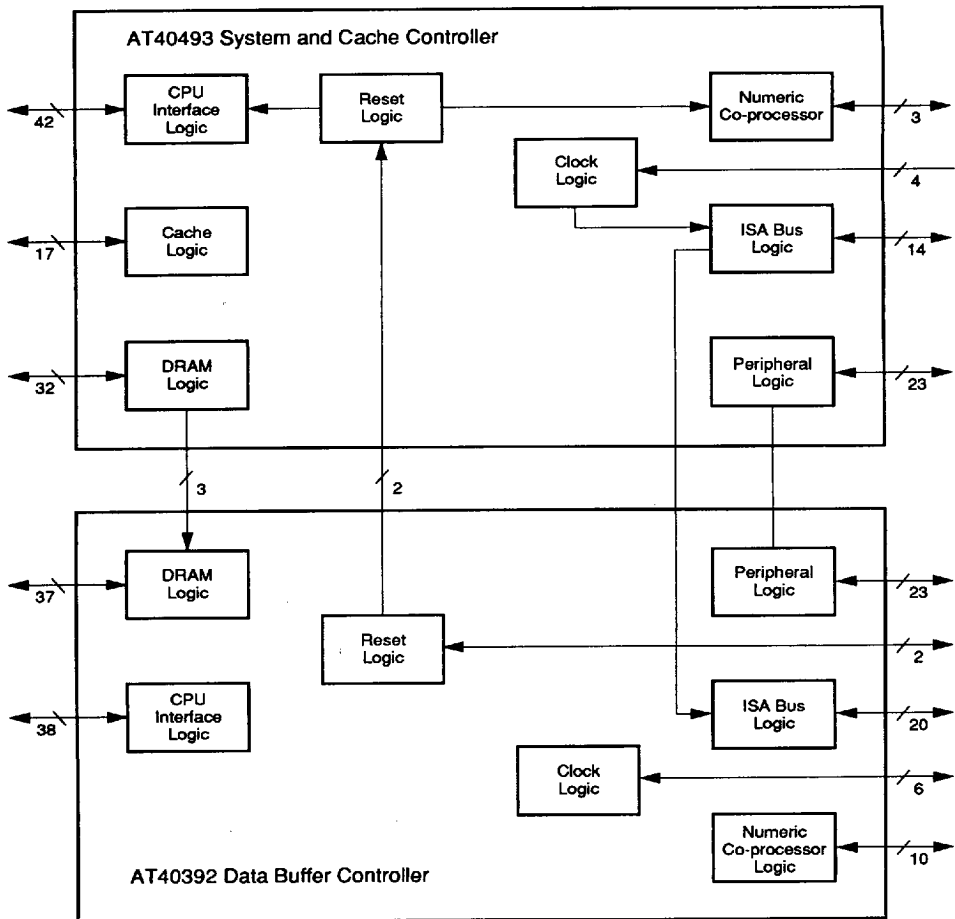
The Atmel AT40493/AT40392 chip set is an IBM PC/AT compatible chip set for 80486 based systems operating up to 50 MHz. The high integration and an on-chip write-back, direct-mapped cache controller design allows maximum system performance. Together with a peripheral controller, such as the AT40206 integrated peripheral controller, a very high performance, yet low cost, 80486 motherboard can be built with a minimum number of components.

The AT40493 system controller performs the system control, memory and cache control functions. The system control logic consists of the following logic blocks: CPU control, AT bus cycle control, numeric co-processor control, synchronous clock circuitry and peripheral bus control. The memory and cache controller functions consist of a write-back, direct-mapped cache controller and a paged mode DRAM controller. The AT40493 supports cache sizes up to 512 Kbytes (16-byte line

size), platform memory sizes up to 64 Mbytes and burst mode for all system configurations.

The AT40392 data buffer controller performs the data buffer and co-processor interface functions. The data buffer logic performs bus conversion logic for various 8-, 16- and 32-bit data movements as required among the system buses. The other functions of the AT40392 are co-processor interface, keyboard controller decoding, reset and generation of various peripheral clocks.

Low cost systems are made possible through the support of single ROM/EPROM BIOS configurations. The BIOS ROM/EPROM can be either 8-bit or 16-bit. DRAM is located on the system platform bus, thus reducing DRAM speed requirements by at least 15 ns.







**Ordering Information**

CPU Clock (MHz)	Power Supply	Ordering Code	Package	Operation Range
25	5 V ± 5%	AT40493-25 AT40392-25	160Q 160Q	Commercial (0°C to 70°C)
33	5 V ± 5%	AT40493-33 AT40392-33	160Q 160Q	Commercial (0°C to 70°C)
50	5 V ± 5%	AT40493-50 AT40392-50	160Q 160Q	Commercial (0°C to 70°C)

Package Type	
160Q	160 Lead, Plastic Gull Wing Quad Flat Package (PQFP)



■ 1074177 0005727 712 ■