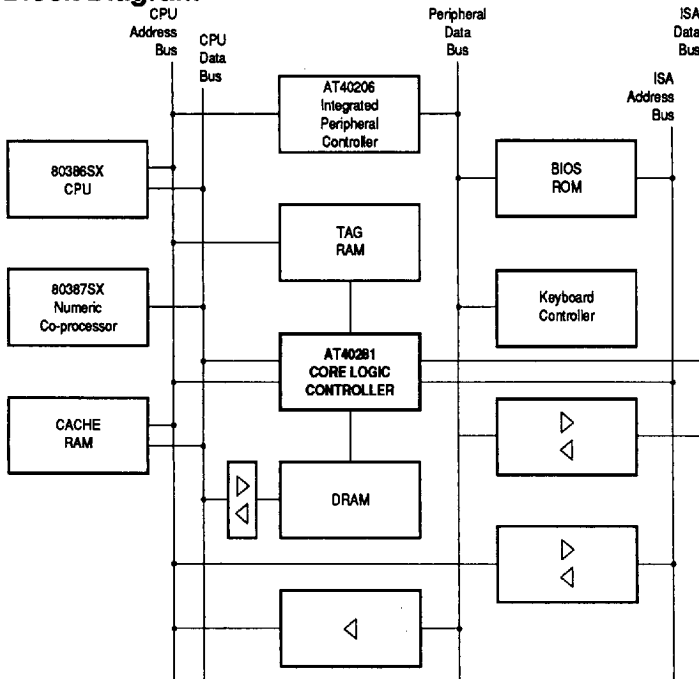


Features

- One-Chip PC/AT Compatible Core Logic Controller for 80386SX Systems operating up to 33 MHz
- One 160-Pin Quad Flatpack, 1-Micron CMOS Technology
- CPU Interface and ISA Bus Control
- Direct Mapped Posted Write Cache Controller with Burst Cache Fill
- Numeric Co-processor Support
- OS/2 Alternate Hot Reset Support
- Programmable Clock Generator for the ISA Bus
- Port B Register and NMI Logic
- 256K, 1-Mbit and 4-Mbit DRAM Support
- Up to 16 Mbytes Platform Memory
- Shadow RAM Support
- Multiple Interleave Paging (MIP™) of Platform Memory

**386SX
Core Logic
Controller**

Block Diagram



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Description

The Atmel AT40281 is a highly integrated single-chip core logic controller for 80386SX PC/AT systems operating up to 33 MHz. The chip integrates system control functions including reset logic and generation of the system clocks (CPU clock, ISA bus clock and the 1.19 MHz clock for the timer input), the local bus and ISA bus controllers, the memory controller and a direct mapped posted write cache controller.

The AT40281 decodes the CPU and ISA bus states to arbitrate among the various bus masters in the system. Data bus conversion, bus steering functions and data buffers and latches are all integrated on chip.

A variety of memory configurations and types of DRAMs can be used with the AT40281. Platform memory parity checking and generation are supported along with shadow RAM for

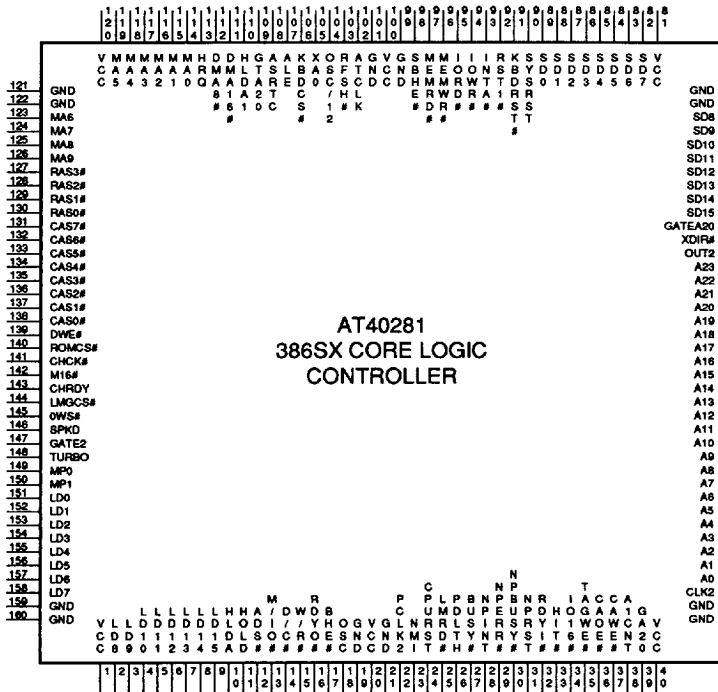
BIOS, single ROM/EPROM for BIOS and address remapping of the unused memory between 640K and 1 Mbit to the top of memory.

The AT40281 also incorporates Multiple Interleaved Paging (MIP) of the platform memory which improves performance in both cache and cacheless configurations by minimizing the number of wait states required during DRAM accesses.

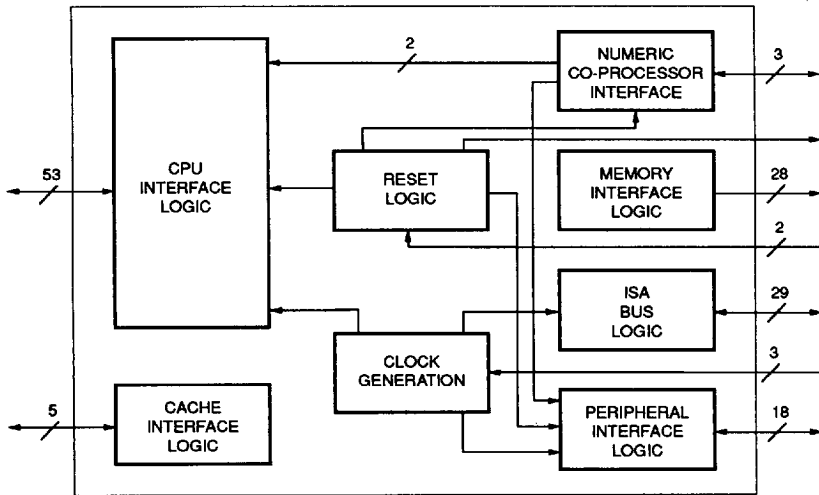
The programmable functions of the AT40281 are programmed through seven Configuration Registers.

Together with a standard peripheral controller such as the AT40206 IPC and a minimum number of other components, the AT40281 allows the use of a single board design for both cache and cacheless high performance, yet low cost, 80386SX PC/AT systems.

Pin Configuration



Core Logic Controller Block Diagram



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Ordering Information

CPU Clock (MHz)	Power Supply	Ordering Code	Package	Operation Range
16	5V±5%	AT40281-16	160Q	Commercial (0° to 70°C)
20	5V±5%	AT40281-20	160Q	Commercial (0° to 70°C)
25	5V±5%	AT40281-25	160Q	Commercial (0° to 70°C)
33	5V±5%	AT40281-33	160Q	Commercial (0° to 70°C)

Package Type	
160Q	160 Lead, Plastic Gull Wing Quad Flat Package (Flatpack)

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AT40281

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