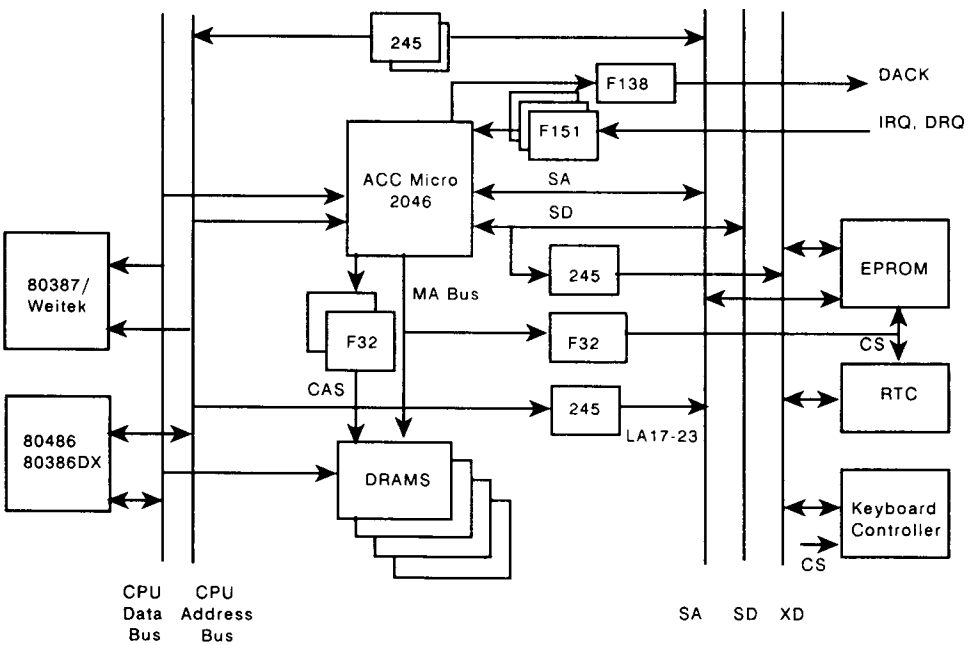
2046
486DX/486SX/386DX Single Chip AT

The ACC Micro 2046 single chip AT is designed for system designers to build a high performance 486DX/486SX/386DX AT systems. The 2046 single chip AT supports a local CPU bus, a system memory bus, and compatible AT buses. The AT bus clock can be synchronous or asynchronous to the CPU clock to support compatible AT bus timing. The built-in peripheral controller and on chip direct mapped cache controller add flexibility for designers to design high performance systems for different requirements.

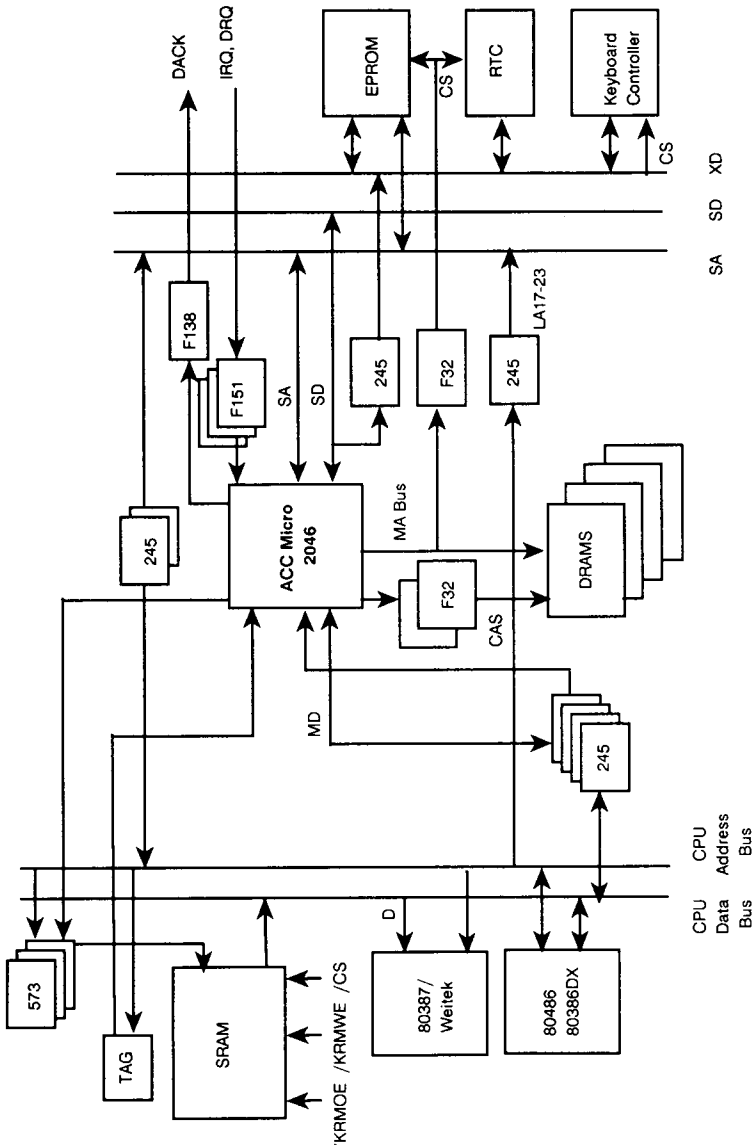
Features

* 100% IBM PC/AT compatible
* Supports 486DX up to 50 Mhz
* Supports 486SX and 487SX
* Supports Intel Low Power 486DX/SX
* Supports 386DX up to 40 MHz
* Supports 387 and Weitek 4167/3167 numerical coprocessors
* Supports 1x or 2x system clock
* Integrated flexible direct mapped cache controller for up to 2048KB
* Supports posted write or write-through cache operation
* Supports 3 programmable non-cacheable ranges
* Supports 64 MB DMA address space
* Supports one to four memory banks of 32 bit DRAM using 256K,1M or 4M DRAMs allowing 64 Mbytes on system board.
* Operates with page mode or two/four way page interleaved mode
* Programmable DRAM timing parameters
* Programmable slow refresh
* Supports hidden refresh
* Support Dynamic Memory remapping
* Unused RAS and CAS lines can be disabled
* Supports shadow RAM for video and system BIOS
* Supports 8 or 16 bit wide BIOS ROMs in 128K or 64K EPROM space
* Supports single ROM
* Supports 512K ROM size
* Middle BIOS can be disabled
* Bus "quiet" mode assures that slot bus signal lines are driven only during slot accesses
* Port B and NMI logic
* Internal switching and programmable CLK2 for sleep mode operation (can be divided by 2/4/8/16)
* Fast reset/Fast gate A20 (Port 92)
* Support for PC/AT compatible and turbo modes
* Independent ISA Bus control
* Parity generation and detection logic
* Integrated Peripheral Functions: 2x8237, 2 x 8259, 1 x 8254.
* Bus conversion between D,SD and XD
* Data latches and buffers included
* 208-pin PQFP device

2046 System Block Diagram
486/386DX Without Cache Application



2046 System Block Diagram
486/386DX with Cache Application



Functional Description

Interrupt Controllers

There are two programmable interrupt controllers for the 2046. They are fully compatible with Intel's 8259 controller, providing up to 15 interrupt sources (14 external and 1 internal). The internal line connects to the 8254 Counter 0 output.

These interrupt controllers prioritize interrupt requests to the CPU.

DMA

The 2046 has two DMA controllers, compatible with the Intel 8237, which provide a total of seven external DMA channels.

Combined with the Memory Mapper, each DMA channel has a 24-bit address output to access data throughout the 64 megabyte system address space. Channel 0 through channel 3 support 8-bit peripherals, transferring data to or from an 8 or 16-bit memory. Each channel can transfer data in 64 Kbyte pages. Channel 4 is used for cascading and is not available externally. Channel 5 through channel 7 support 16-bit I/O adapters, transferring data a word at a time. These channels can transfer in 128 Kbyte pages.

All address latching functions for DMA operation are done inside the 2046. Configuration register 0Ah, bit 1, and bit 0, provide address bits 24 and 25 for 64M Byte DMA address.

Features include

* Address increment or decrement.
* Seven independent DMA channels with independent auto initialization for each channel.
* Each DMA request can be controlled individually to enable or disable.

Memory Mapper

The 2046 has a built-in equivalent logic to the 74LS612, generating the upper address bits during a DMA cycle.

Source Memory Mapper	8237
(for DMA Channels 0 - 3)	
Address	A23.... A16 A15.... A0
(for DMA Channels 5 - 7)	
Address	A23 .... A17 A16.... A1

Timer/Counter

The 2046 provides three internal counters which are compatible with the 8254. The clock input for each counter is tied to a clock of 1.19 MHz, which is derived by dividing the 14.318 MHz

crystal input by 12. The output of Counter 0 is connected to the IRQ0 input of interrupt controller 1. Counter 1 initiates a refresh cycle and Counter 2 generates sound waveforms for the speaker.

Features:

* Three independent 16-bit counters
* Count binary or BCD

2046 I/O Address Map

The 2046 I/O address decode is fully compatible to the IBM PC/AT requirements. The 2046 has decoded the I/O address range from 000 to 0FF to allow users to use the I/O areas not used by the IBM PC/AT.

Hex Range	Device
000-00F	DMA controller 1, 8237A-5
020-021	Interrupt controller 1, 8259A,Master
040-043	Timer, 8254
060-064	8042 (Keyboard)
070-071	Real-time clock, NMI (non-maskable interrupt) mask
080-08F	DMA page register, 74LS612
092	Alternative Gate A20 and FAST RESET Register.
0A0-0A1	Interrupt controller 2, 8259A
0C0-0DF	DMA controller 2, 8237A-5
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F2	2046 Configuration Register Index
0F3	2046 Configuration Register Data
0F8-0FF	Math Coprocessor

PIO

The PIO is the system configuration to control the speaker port. It also has circuitry to detect refresh. This condition can be read back as Bit 4 of I/O Port 61h.

Refresh Generation Logic

Refresh circuitry contains an 8-bit counter for address SA0-7 during a refresh. In addition, three more address counter bits are presented inside the 2046 to support refresh for DRAMs up to 4M bits.

Refresh/DMA Arbitration Logic

The 2046 contains circuitry to control a refresh cycle.

There are two possible sources for a hold request to the CPU. Either the DMA controller issues a hold request or the output of Counter 1 in the 8254 makes a low to high transition. The HOLD line is active when either source is requesting a hold. The hold request from the DMA controller is sampled on the rising edge of the DMA clock and the request from the timer is sampled on the falling edge of the DMA clock.

If the DMA controller's hold wins the arbitration, the HOLD is asserted, and it waits for a signal back from the CPU. When the DMA controller is finished, it negates its hold request signal to the arbiter. The arbitration then switches to a REFRESH cycle if there is a pending hold from the Counter/Timer, otherwise the arbiter inactivates the HOLD line and returns control to the CPU.

If a refresh cycle wins the arbitration, the HOLD is asserted and the 2046 pulls the /REFRESH pin low. /REFRESH remains low

for four SYSCLK rising edges. On the fourth rising edge of SYSCLK, the HOLD line is inactivated. However, if there is a pending hold request from the DMA controller on the fourth rising edge of SYSCLK, the REFRESH cycle is extended for one more SYSCLK cycle. The hold request arbiter then acknowledges the hold request from the DMA controller.

NMI and Port B Logic

The 2046 contains non-maskable interrupt (NMI) signal generation logic. An NMI can be caused by an I/O error or by a parity error. Port B indentifies the source of the error. At power up, the NMI signal is masked off. NMI is enabled by writing to I/O address 070 hex with Bit 7 low; NMI is disabled by writing to I/O addresss 070 hex with Bit 7 high.

Bus Controller and Converter

The D/-C, W/-R and M/-IO signals carry data from the CPU, announcing a bus cycle and defining its type. Tables 1.1a and 1.1b list and define the different types of bus cycles.

Table 1.1a ACC Micro 2046 386DX Bus Cycle Definitions

M/-IO	D/-C	W/-R	Bus Cycle Type	
0	0	0	Interrupt acknowledge	
0	0	1	Does not occur.	
0	1	0	I/O data read.	
0	1	1	I/O data write.	
1	0	0	Memory code read.	
1	0	1	Halt if Address = 2;	Shutdown if Address = 0
			(/BE0 High	(/BE0 Low
			/BE1 High	/BE1 High
			/BE2 Low	/BE2 High
			/BE3 High	/BE3 High
			A2-A31 Low)	A2-A31 Low)
1	1	0	Memory data read.	
1	1	1	Memory data write.	

Table 1.1b ACC Micro 2046 486 Bus Cycle Definitions

M/-IO	D/-C	W/-R	Bus Cycle Type	
0	0	0	Interrupt acknowledge	
0	0	1	Halt if Address=2; (/BE0 High /BE1 High /BE2 Low /BE3 High A2-A31 Low)	Shutdown if Address=0 (/BE0 Low /BE1 High /BE2 High /BE3 High A2-A31 Low)
0	1	0	I/O data read.	
0	1	1	I/O data write.	
1	0	0	Memory code read.	
1	0	1	Does not occur.	
1	1	0	Memory data read.	
1	1	1	Memory data write.	

The bus controller has four operation modes.

AT CPU Mode

This mode is active when HLDA is low. The CPU bus controller generates /IOR, /IOW, /INTA, /MEMR, and /MEMW signals.

DMA Mode

DMA mode is active if HLDA and AEN are active. The DMA controller drives the /IOR, /IOW, /MEMR, and /MEMW signals.

Refresh Mode

Refresh mode is active when HLDA and /REFRESH are active. /MEMR becomes active at this time to perform a refresh on both AT bus and local DRAM.

Master Mode

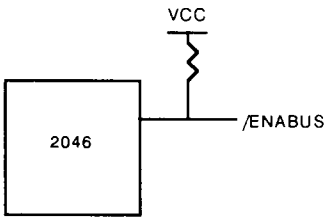
Master mode is active when HLDA is active and a card in the AT slot pulls /MASTER low. The card controls system address, data line and control line.

Bus Conversion

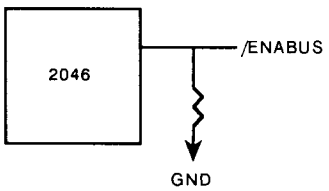
The 2046 contains logic to convert between 16-bit and 8-bit data accessing. During a bus conversion cycle, the AT bus command strobe (/MEMR, /MEMW, /IOR, or /IOW) is activated two times.

CPU Interface

The 2046 supports the 486DX/SX and 386DX CPUs. The CPU interface selection is determined by detecting a pull up or pull down resister on pin 29 (/ENABUS) during the reset period. A pull down resister on pin 29 will trigger the 2046 operating in the 486 mode. A pull up resister on pin 29 will trigger the 2046 operating in the 386DX mode.



386DX mode configuration



486 mode configuration

80387 Interface Control

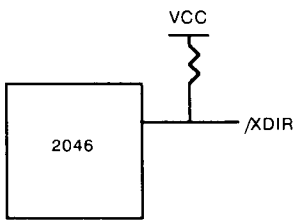
The 80387 interfaces directly to the 386DX with the error-reporting logic built in the 2046. A coprocessor error is sent to the 2046, generating an interrupt request to the CPU, followed by a service request. A write operation to I/O port 0F0 will clear the interrupt request.

Clock Generator

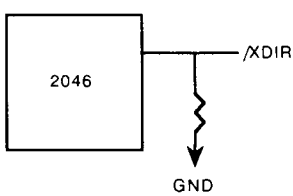
The 2046 Clock Generator provides clock signals to support internal and external timing requirements. It provides clock outputs for the CPU, the NPU, and the Keyboard Controller. Clock signals are generated from three clock sources. A 14.318 MHz crystal is connected to X14M1 and X14M2 to generate a 14.318 MHz frequency. An alternative external oscillator (16 MHz) is connected to pin EXT16M to provide an optional 16 MHz input clock for the AT Bus. CLKSRC input is one or two times of the CPU operation clock providing turbo mode operation in single phase or double phase clock mode respectively. CLKSRC is driven by an external oscillator. The AT Bus clock can be derived from three places. It can be generated by dividing down the CLKSRC to an approximated 16M frequency, or it can be generated by dividing the 14.318M frequency down to half (to 7.15M), or it can be generated from the external 16M directly.

Clock Mode Selection

The 2046 supports both single phase clock and double phase clocks. The clock phase is determined by detecting a pull up or pull down resister on pin 28 (/XDIR) during reset period. A pull-up resister on pin 28 will trigger the 2046 to operate in double phase clock. A pull down resister on pin 28 will trigger the 2046 to operate in single phase clock.

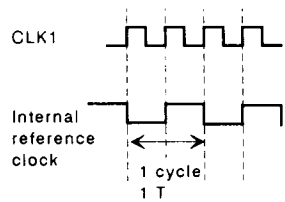


Double phase clock



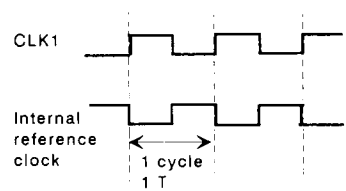
Single phase clock

The double phase clock has a clock source which is two times of the CPU operation clock. In double phase clock, every cycle consists of two CLKI periods. Double phase clock can be used for both the 486DX/SX systems or 386DX systems. In the 486 mode, the 2046 provides a dedicated 486CLK which is a half of the CLKSRC for 486 CPU. The 2046 double phase clock operation supports both page interleaved mode and page mode memory controller.



Double phase clock

The single phase clock has a clock source which is one times of the CPU operation clock. In single phase clock, every CLKI input period becomes one completed cycle. Single phase clock is used primarily for the 486 systems. Either CLKOUT or 486CLK can be used as 486 CPU clock input. The 2046 in single phase clock mode only supports a page mode memory controller.



Single phase clock

Turbo Speed Control Logic

The CPU clock frequency can be switched between CLKSRC and the AT clock. The frequency switch can be generated through either hardware or software. A TURBO pin is provided to support a front panel turbo speed switch. TURBO high selects CLKSRC as the CPU clock. TURBO low selects AT Bus clock as the CPU clock.

For power conservation, a standby mode clock control is provided. A system needs to pre-select the standby frequency first, then an intelligent BIOS will monitor the activity of the system. If all pre-defined conditions of the standby mode are satisfied, the system will go into the standby mode by programming bit 3 of register 8h to 1 or if Turbo/Sleep bit has been set to 1, the Turbo pin low will force the system into sleep mode.

The standby mode CPU operating frequency can be pre-set by programming bit 2-0 of configuration register 8h. If AT Bus clock source is at 16 MHz, the standby frequencies output of CLKOUT are set as follows:

Bit 2	Bit 1	Bit 0	Frequency
0	0	0	16 MHz
1	0	0	8 MHz
1	0	1	4 MHz
1	1	0	2 MHz
1	1	1	1 MHz

Memory Controller

The Memory Controller is a key feature of the 2046. This versatile circuit provides complete control of up to 64 megabytes of system DRAM. In any control mode, it generates up to four Row Address Strobes (/RAS0-3) and one Memory Write Enable signal (/WEN). The Memory Controller also provides the interface to transfer control to a DMA controller or an AT Bus master.

Memory Control Modes

The 2046 features two memory control modes: Page Interleaved Mode and Page Mode. These options provide flexibility and optimize system performance. Both will be running at 0 wait state when a page hit occurs in pipeline mode. With Page Interleaved mode, a minimum of three wait states are asserted when a memory miss occurs. Mode select is done by programming the power up select register, Register 5h, bit 4.

Page Interleaved Mode

The 2046 implements a 4-way and 2-way page interleaved memory controller, providing optimum system performance for high speed CPUs. The Page Interleaved Memory Controller operates on two principles: Page Mode Memory access, which is much faster than random access, and the sequential and localized patterns it follows. The Page Interleaved Memory Controller organizes the memory array into interleaved pages by banks, operating up to four banks simultaneously in Page mode. Each bank of memory consists of 36 bits of DRAM (four 8-bit bytes plus four parity bits).

The size of a memory page is determined by the type of DRAM installed. The page sizes are a result of the physical architecture of the DRAM. Once page interleaved mode is selected, a row can be kept active (/RAS low) almost indefinitely (up to 10uS), allowing any number of column accesses along that same row. Each row, and any intersecting column access along that same row, is defined as a "Page Hit." This results in a zero wait state access. If any subsequent memory access selects a new row, it is defined as a "Page Miss" and results in a minimum of three wait state access.

The organization and operation of the memory array is dependent on the type and quantity of memory installed (See "Configuration Registers" section). Memory performance is improved when a greater number of open pages, up to four, are used. This provides a larger and more flexible "zero wait state" work space. The open page on each bank retains the last row address selected on that particular bank.

The RAS precharge time can be programmed to 2 or 3 cycles by programming bits 1 and 3 of Register 1h. One or two more wait states can also be inserted in read or write cycles to utilize slower DRAM in the cache system.

Page Mode

Page mode provides even more flexibility for high speed cache system. In page mode operation, four RAS are generated, but only one will be activated at any time. Logically four banks behave as one large bank of memory. All the DRAM parameters can be programmed including RAS precharge time, RAS to CAS delay, CAS precharge time, CAS width for read and write cycles. All these parameters can be programmed on a cycle by cycle basis. Please refer to Register 0Bh page mode setup.

Memory Control Mode and CPU Clock Mode

In double phase clock mode, the 2046 can operate in either Page Interleaved mode or Page mode. Four CAS are generated from the 2046, one for each bank which should be logically anded with the four byte enable signals MBE_x to generate individual CAS for every byte in that bank. Refer to the double phase clock memory controller application diagram (Fig. 1.1a).

In single phase clock mode, the 2046 operates in Page mode. One CAS is provided for each byte. Totally four CAS are generated and are shared by all banks. Refer to the single phase clock mode memory controller application diagram (Fig. 1.1b).

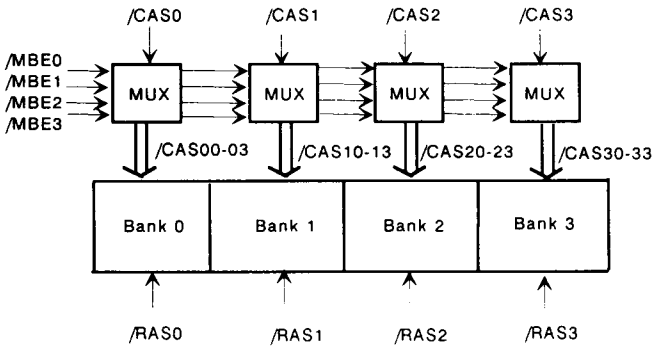


Figure 1.1a Memory Controller Application Diagram in Double Phase Clock

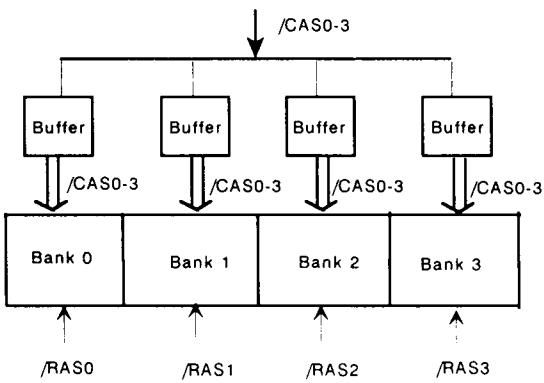


Figure 1.1b Memory Controller Application Diagram in Single Phase Clock

Memory Mapping

Memory Mapping translates system RAM within the 640 KB to 1MB range, which is reserved for the system ROM and BIOS application, to an accessible address range above the physical RAM space. For example, if 4 MB of memory are installed, and the memory mapping feature is on, the DRAMs in the 640 KB to 1MB range are mapped to an address immediately above 4 MB.

Memory Mapping is enabled by bit 7 of register 0 in the configuration registers. When Shadow RAM is enabled simultaneously with Memory Mapping, the quantity of RAM available for Memory Mapping is reduced.

If Shadow RAM segment F is enabled, 320KB of RAM can be mapped. If Shadow segment E is enabled, 256KB of RAM can be mapped. If any of the segments C0, C1, or D are enabled, 128 KB of RAM can be mappped. The mapping function can only be used in memory configurations 0, 1, 2, 3, and 4 in page interleaved mode and all memory options, except option 24, in page mode.

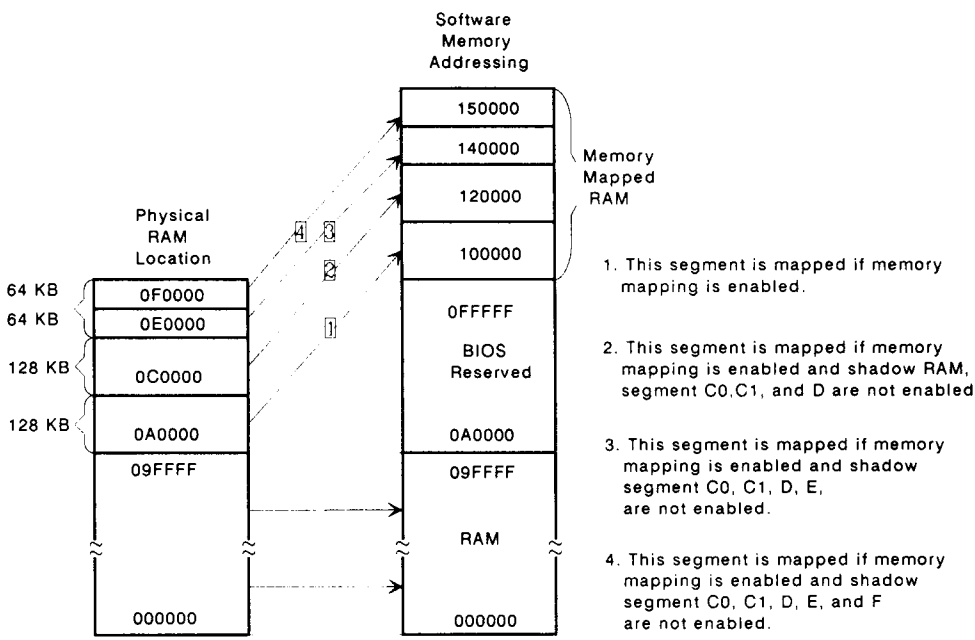


Figure 1.2 Memory Mapping for a 1 MB System

Shadow RAM

Shadow RAM provides an option to transfer BIOS or video-extension BIOS program codes into system RAM. This option provides significant performance improvement for applicatons requiring intensive BIOS calls.

Shadow RAM implements an alternate BIOS source by copying the complete EPROM program code into system RAM. This is referred to a "shadowing" because the DRAM and EPROM are both located at the same physical address space. This change is transparent to the rest of the system. ROM can be disabled, allowing the RAM to respond in its place. The advantage of this procedure is that DRAM access time is typically much faster than EPROM access time.

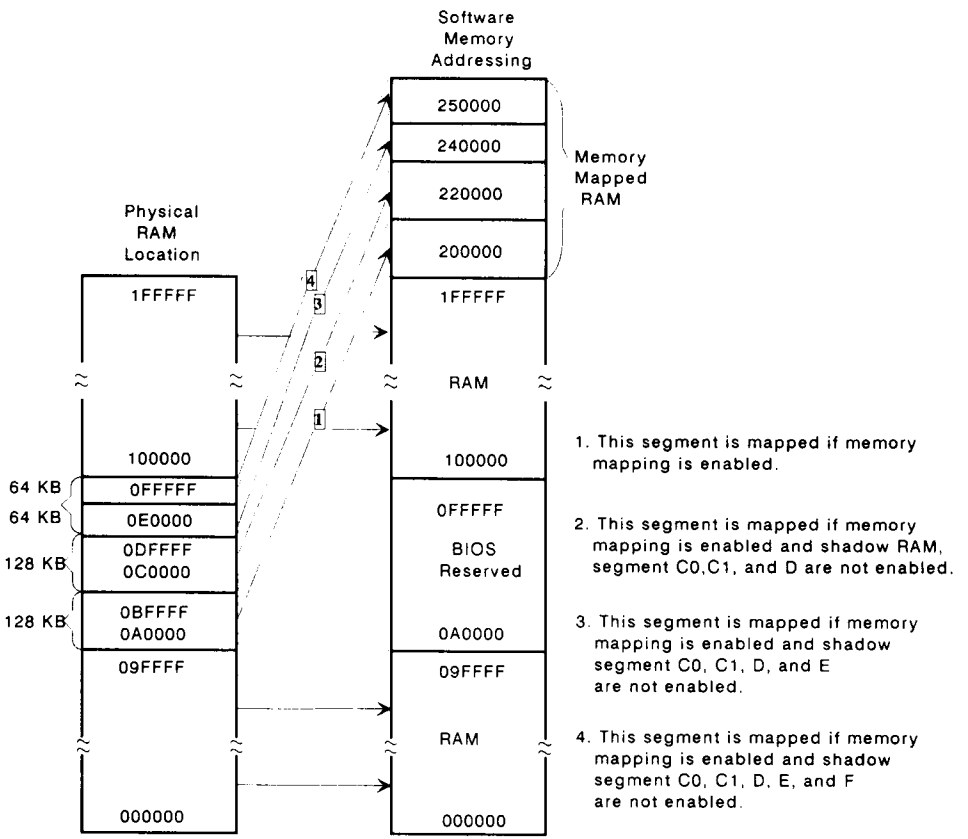


Figure 1.3 Memory Mapping for a 2 MB System

The 2046 Shadow RAM is configured in five independent segments: 00C0000 to 00C7FFF (Shadow C0), 00C8000 to 00CFFFF (Shadow C1, 00D0000 to 00DFFFF (Shadow D), 00E0000 to 00EFFFF (Shadow E), and 00F0000 to 00FFFFF (Shadow F), as shown in Fig. 1.4. Each segment can be enabled for shadow operation individually or simultaneously.

Enabling a Shadow RAM segment requires two steps. The "shadow enable" configuration bit for the segment to be shadowed must be set to allow the transfer of code from EPROM to DRAM. The second step sets the "Shadow Read Only" configuration bit of the corresponding segment to protect the Shadow RAM.

OS/2 Optimization

The 2046 implements OS/2 optimization, which is a more efficient way to switch back and forth between real and protected modes in an OS/2 environment when frequent DOS calls are made. Conventional methods require the processor to communicate with the keyboard controller in switching to protected mode and activating gate A20.

With OS/2 optimization, the 2046 allows control of software CPU reset and A20 gating through Port 92h.

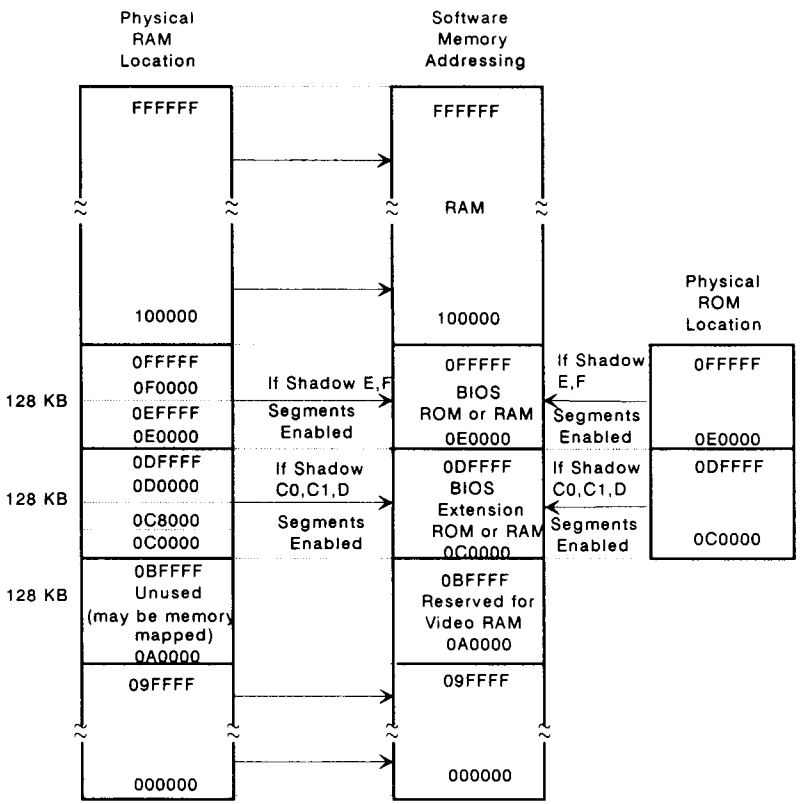


Figure 1.4 ACC Micro 2046 Shadow RAM Address Map

Configuration Register Port 92h, Fast A20 Gate, and Alternative RESET Control

Bit	Function
7-2	Reserved
1	A20 Gate
0	Alternate CPU reset

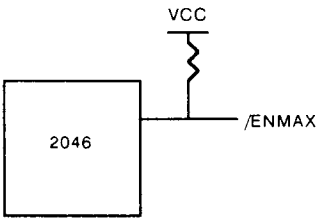
Bit 1 This bit controls CPU address bit A20. When set to 1, it enables A20. When set to 0, this bit makes the A20 Signal inactive, thus preventing the Address bus from going beyond the 0FFFFFh boundary in Real Mode. Although it has the same function as the keyboard controller's GATE-A20 signal, it is much faster because it is just a simple I/O write operation. Default is 0.

Bit 0 By setting this bit to 1, application softwares can reinitialize the microprocessor and switch the operation from Protected Mode to Real Mode. Setting this bit does not reset the whole system, it only affects the CPU. This reset function is the same as that of the keyboard controller's "KBRST" signal. However, it provides a faster reset sequence. This bit can be read by application software to determine if it is a hot rest or cold boot. It can only be set to 0 by writing a 0 to bit 0 of the register or by power up. Default is 0.

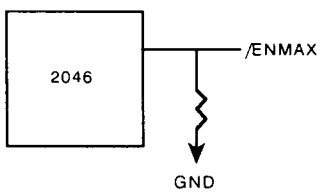
8-bit/16-bit ROM Options

The 2046 supports both 8-bit and 16-bit ROM Data buses. It is configured by a pull-up or a pull-down resistor on pin 139 ENMAX# as demonstrated below:

8-bit ROM configuration



16-bit ROM configuration



The 16-bit ROM is treated as a 16-bit Bus memory. It can be accessed more efficiently and it takes less time to finish a cycle.

The 8-bit ROM is located in the local I/O Bus and treated as an AT Bus device. Due to its narrow data path and long cycle, the performance of ROM cycles will not be as efficient as that of the 16-bit option. However, as the 2046 provides BIOS shadow capability, this inefficiency can be avoided by moving the BIOS code from the 8-bit ROM to a 32-bit local RAM.

128K/64K ROM BIOS Range

The ROM BIOS range can be set to two different sizes--64K or 128K--to accommodate various application requirements. Refer to configuration 0h definition to configure the size of the ROM BIOS Range.

Staggered Refresh Logic

The 2046 refresh logic works to perform a periodic refresh for both system DRAM and extended RAM on the AT Bus. The 2046 initiates a refresh cycle by driving its /REFRESH output low, and driving the refresh address onto the MA Bus, simultaneously generating staggered refresh pulses on the four RAS outputs. The RAS outputs are staggered to reduce the current drain caused by the refresh operation.

During each refresh cycle, the 2046 drives the current refresh address onto the AT address bus. This provides the refresh address for extended memory.

Direct Mapped Cache Controller

The 2046 supports a high performance cache system by using the built-in direct mapped cache controller or a dedicated cache controller, such as Intel's 82385 or 82395. A cache system contains a copy of frequently used code and address from main memory in a zero wait state SRAM. The program locality is such that, in most cases, the system can fetch the needed data and codes from the cache. The cache system reduces the average memory access to nearly zero wait state and increases the whole system's performance dramatically.

The built-in 2046 direct mapped cache controller arranges the tags in such a way that each address in the main memory corresponds to a single cache directly. This keeps the design simple and reduces the cost of a high performance cache system.

In a 486 AT system, if the internal cache of 486 is enabled, the 2046 direct mapped cache can be used as secondary cache to further improve the system performance especially in a multi-user, multi-task environment.

Posted Write and Write Through

The 2046 cache controller supports write-through and post write cache update options to prevent old data from being used.

The write-through option is the simplest way to keep cache coherent. In a cache write hit cycle, the memory controller will update the DRAM at the same time that it is written to the cache. The 2046 cache controller default mode is write-through mode.

The 2046 also supports posted write cache system by programming configuration register 4h, bit 7 to enable posted write operation. This posted write option allows the data to be buffered before updating to the main memory. The system performance is therefore increased, since the processor can start a new cycle before the write cycle to the main memory is completed.

Cache Burst and Line Size

The 2046 supports a flexible line size structure and cache burst. The 2046 supports 32 bit, 64 bit or, 128 bit line sizes. Configuration register 4h, bits 2 and 1 determine the line size. In the case of a cache read hit cycle, the 2046 will pull the burst ready signal, /BRDY, low and fill the 486 internal cache lines quickly. A 128 bit line size requires only 5 cycles to fill the cache lines. A 64 bit line size requires 3 cycles.

In the case of a read miss cycle, the 2046 burst mode will generate four continuous DRAM read cycles for a 128 bit line size to fill both 486 internal and external cache. For a 64 bit line size, the 2046 burst mode will generate two burst cycles instead of four.

Cache Memory Organization Examples

The 2046 Direct Mapped Cache architecture is so flexible that a cost effective cache system can be organized to suit each system manufacturer's specific needs.

Designers can use either off-the-shelf Tag RAMS or standard fast SRAM coupled with comparators to compare the tag address to determine a hit or a miss.

Example 1:
Design a 32K cache for an 8 Mbyte cacherange.

Cacheable Range:	8 Mbyte (A2-A22)
Line size:	32 bit
Address index to TAG RAM:	A2-A14
TAG field:	A15-A22
TAG RAM required:	one 8K x 8
Data RAM required:	four 8K x 8
DRAM size:	8 Mbyte

Since the cacheable range is 8 Mbyte, it is recommended that the DRAM size not exceed the cacheable size.

Example 2:
Design a 64K cache for a 16 Mbyte cache range

Cacheable Range:	16 Mbyte (A3-A23)
Line size:	64 bit
Address Index to TAG RAM:	A3-A15
TAG field:	A16-A23
TAG RAM required:	one 8K x 8
Data RAM required:	eight 8K x 8
DRAM size:	16 Mbyte

Example 3:
Design a 128K cache for a 32 Mbyte cache range

Cacheable Range:	32 Mbyte (A4-A24)
Line size:	128 bit
Address Index to TAG RAM:	A4-A16
TAG field:	A17-A24
TAG RAM required:	One 8K x 8
Data RAM required:	sixteen 8K x 8
DRAM size:	32 Mbyte

Example 4:
Design a 128K cache for a 16 Mbyte cache range

Cacheable Range:	16 Mbyte (A4-A23)
Line size:	128 bit
Address Index to TAG RAM:	A4-A16
TAG field:	A17-A23
TAG RAM required:	one 8K x 8
Data RAM required:	sixteen 8K x 8
DRAM size:	16 Mbyte

TAG RAM and Data RAM Speed Requirement

System Speed	25 MHz	33 MHz	40 MHz
DRAM speed	80 ns	80 ns	80 ns
DRAM wait speed	0	1	1
SRAM	30 ns	25 ns	20 ns
TAG RAM	25 ns	20 ns	16 ns

Cache RAM circuit example

The 2046 has two different cache RAM application circuits depending on the CPU clock running mode.

In double phase clock mode, the 2046 supports four banks of cache RAM. Signals /KROE, /KRWE, TGLA2, and TGLA3 will be multiplexed to generate the necessary control signals (/KROE A-D and /KRWE A-D) for each bank of cache RAM. Please refer to Figure 1.5, cache RAM application circuit in double phase clock mode.

In single phase clock mode, the 2046 supports two bank interleaved cache RAM memory. Cache RAM enable signals /KROE A-B and /KRWE A-B are generated by 2046 directly. Please refer to Figure 1.6.

Fig. 1.5 Cache RAM application circuit in double phase clock mode

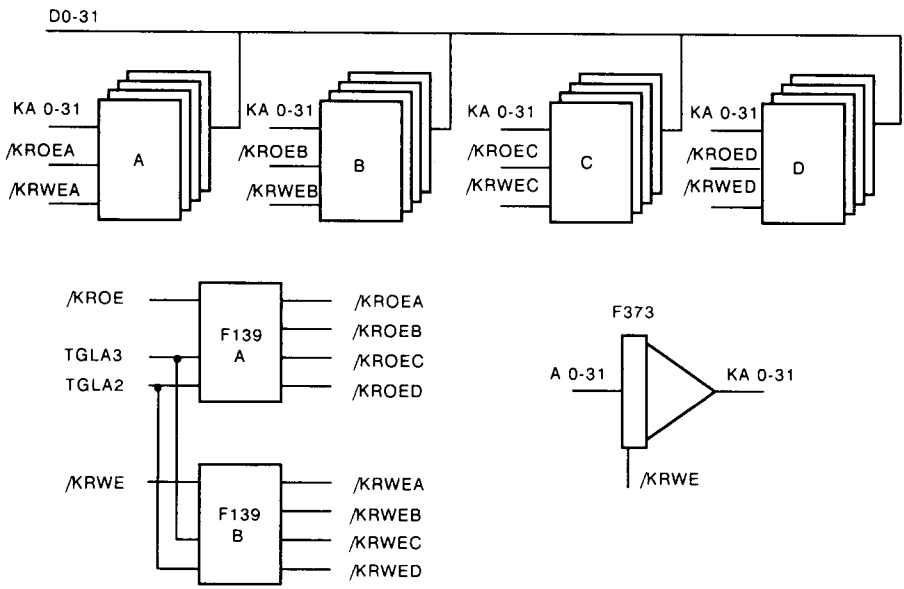
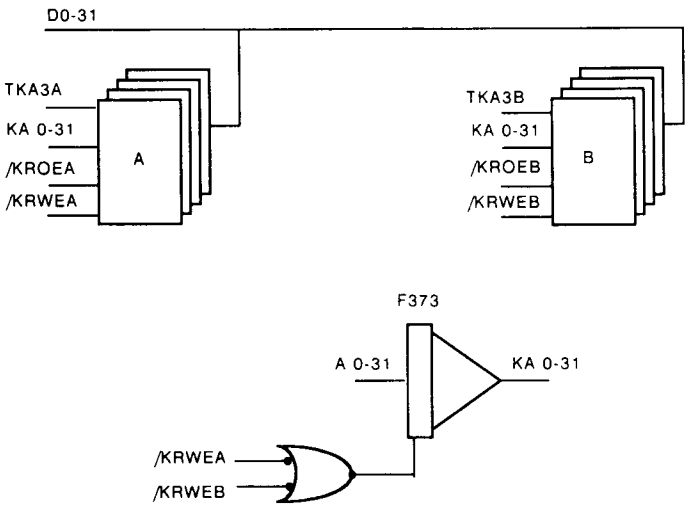


Fig. 1.6 Cache RAM application circuit in single phase clock mode



Non-Cacheable Area

The 2046 built-in cache controller allows three programmable blocks to be defined as non-cacheable area. The three non-cacheable block sizes are defined by configuration register, Ch, Eh, 10h, 0Ch and 0Eh, bits 0-3. The block size can be 16K, 32K, 64K, 128K, 256K, 512K, or 1Mbyte. The starting address of the non-cacheable block are defined by configuration registers Dh, Fh, 11h, 0Ch, 0Dh, 0Eh, and 0Fh respectively which set the non-cacheable address bits from A14 to A25.

Non-cacheable locations are necessary for memory-mapped I/O device, network interface board, dual port memory, hard disk controller, or any other memory that should not be cached.

Reset and Shutdown Logic

The reset and shutdown logic contains the circuitry for the RESETDRV and CPURSTsignals. Reset circuitry generates two resets. One is for the general system reset with power on and the other is for the CPU, or for taking the CPU out of protected mode when a warm software reset request is generated by the 8042 keyboard controller.

The CPURST signal generates a system reset and is synchronized to CPUCLK. When the keyboard reset signal is generated from the 8042 keyboard controller (called a warm reset), CPURST is activated to reset the CPU. CPURST is asserted for at least sixteen CPUCLK cycles and then deactivated for proper CPU operation.

Suspend and Resume Function

The 2046 along with the power management chip ACC Micro 2020 supports a power conservation feature-- Suspend and Resume. Necessary hardware is provided to monitor the activity of power hungry devices such as microprocessor, fixed disk drive, LCD display, etc. All defined register bits in the 2046 and the 2020 are readable and writeable to support this feature.

Through software task, a device can be powered off when no activity is detected for a reasonable length of time which can be programmed in set-up program. The device then can be powered back on to the same state as the last power off when it is desired. This suspend and resume capability minimizes system's battery power consumption.

Configuration Registers

The 2046 contains configuration registers which provide a variety of functions. These functions are concerned with system initialization, software control of advanced memory control and power saving features. For system initialization, these configuration registers implement a no-cost, no-space alternative to system board DIP switches. For advanced memory control, these registers provide maximum flexibility and convenience for programming. Configuration registers are programmed with an indirect addressing scheme using I/O addresses F2 and F3. I/O address F2 contains the write-only configuration index register. F2 selects the corresponding configuration register accessed at I/O address F3. To write a value of "E8" into configuration register 2Ah, the configuration index register at I/O address F2 must first be written with a value of "2A," then register at I/O address F3 with a value of "E8."

Configuration registers are selected by the configuration index register at I/O address F2. Table 1.3 contains a summary of configuration registers 0h - 1Ch.

Table 1.3 ACC 2046 Configuration Registers 0h-1Ch

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0h	MAPEN	MIDROM	ROME	ENROM	< memory configuration select >			
1h	WR1WS	WR0WS	--	TIMEOUT	--	--	ENRAS	ENRD
2h	--	KSHEN	SHRD	ESHF	ESHE	ESHD	ESHC	ESHC0
3h	--	--	--	DISPCK	/NPWS	/NPSEQ	/WETK	/E387
4h	EBFW	BMW0	K1WS	BURST	KB486	<cache line size>		ECACHE
5h	ROM8	M386	PHASE2	EPMSEQ	--	--	SLREF1	SLREF0
6h	--	--	--	<	Bus clock select and divider			>
7h	--	--	--	<	MUX clock select and divider			>
8h	--	--	--	--	ENSLM	<SLM frequency divisor		>
9h	--	--	--	--	--	--	ENPW	EKBRS
0Ah	--	--	--	--	--	--	ENA25	ENA24
0Bh	RPW1	RPW0	CPW	CPT	RCSW1	RCS0	WCSW1	WCSW0
0Ch	CA17	CA16	CA15	CA14	BST3	BST2	BST1	BST0
0Dh	CA25	CA24	CA23	CA22	CA21	CA20	CA19	CA18
0Eh	CA17	CA16	CA15	CA14	BST3	BST2	BST1	BST0
0Fh	CA25	CA24	CA23	CA22	CA21	CA20	CA19	CA18
10h	CA17	CA16	CA15	CA14	BST3	BST2	BST1	BST0
11h	CA25	CA24	CA23	CA22	CA21	CA20	CA19	CA18
12h	ERCDT	--	PMROM	ETSW	EDRM	--	<mem.con.sel>	
18h	--	--	DSD	EP0WS	--	--	BURST	DATR
19h	RASA1	RASA0	RASP1	RASP0	--	BR2	BR1	BR0
1Ah	EADS	D486K	D386P	EKH	EKM	MPOL	EDDMA	EFDMA
1Bh	DCAS3	DCAS2	DCAS1	--	DRAS3	DRAS2	DRAS1	TTI
1Ch	RKBST	--	--	--	--	<revision control register >		

The specific functions of each configuration register are detailed below.

All reserved and unused bits should be written as zero. Any read back from reserved bits can be ignored.

Memory Configuration and ROM Setup Configuration Register 0h, R/W

Bit	Function
7	Enable remap.
6	ROM at 16M.
5	Enable ROM range from segment E.
4	Enable ROM to include C0000-C7FFF.
3-0	Memory configuration bits.

Bit 7 When set to one, this bit enables remap memory within the 640 KB to 1 MB range to memory address above the actual installed memory size. Default is zero.

Bit 6 When set to one, this bit enables middle BIOS ROM in page interleaved mode. The size of the enabled middle BIOS is determined by bit 5. If bit 5 is set to 0, middle BIOS in FF0000- FFFFFF will be enabled. If bit 5 is set to 1, middleBIOS FE0000-FFFFFF will be enabled. Default is zero.
This bit works in conjunction with Register 12h, Bit 6 to set the ROM size for middle BIOS in page mode operation.

Bit 5 When set to 0, ROM BIOS will be located in 0F0000-0FFFFF. When set to 1, ROM BIOS will be extended from 0E0000-0FFFFF. Default is zero.

Bit 4 When set to one, this bit enables ROM to include C0000-C7FFF for video BIOS. Default is zero.

Bits 3-0 These bits are memory configuration bits 3-0.

The 2046 memory controller supports two operation modes, the Page Interleaved mode for double phase CPU clock and the Page mode for the double and single phase CPU clocks.

When Register 12h, bit 3 is set to zero, these four bits are the memory configuration bit for Page Interleaved mode memory options. Refer to the Page Interleaved memory options table below.

Page Interleaved Memory Options

For ENMIX = 0 (Register 12h, bit 3) Memory Configuration 3 2 1 0	# of Banks	Type of DRAM	Total Memory
0 0 0 0	1	256K	1M
0 0 0 1	2	256K	2M
0 0 1 0	4	256K	4M
0 0 1 1	1	1M	4M
0 1 0 0	2	1M	8M
0 1 0 1	4	1M	16M
0 1 1 0	1	4M	16M
0 1 1 1	2	4M	32M
1 0 0 0	4	4M	64M
others		reserved	

When Register 12h, bit 3 is set to one, these four bits plus bits 1 and 0 of Register 12h, set the page mode memory options. Refer to the following table for Page mode memory options

Page Mode Memory Options

for ENMIX = 1 (Register 12h, bit 3)

Option	Memory Configuration 5*4*3 2 1 0	Bank 0	Bank 1	Bank 2	Bank 3	Total Memory
1	0 0 0 0 0 0	256K				1M
2	0 0 0 1 0 0	256K	256K			2M
3	0 0 0 1 1 1	256K	256K	256K		3M
4	0 0 1 0 0 1	256K	256K	256K	256K	4M
5	0 1 0 0 0 0	1M				4M
6	0 1 0 0 0 1	256K	1M			5M
7	0 1 0 0 1 0	256K	256K	1M		6M
8	0 1 0 0 1 1	256K	256K	256K	1M	7M
9	0 1 0 1 0 0	1M	1M			8M
10	0 1 0 1 0 1	256K	1M	1M		9M
11	0 1 0 1 1 0	256K	256K	1M	1M	10M
12	0 1 0 1 1 1	1M	1M	1M		12M
13	0 1 1 0 0 0	256K	1M	1M	1M	13M
14	0 1 1 0 0 1	1M	1M	1M	1M	16M
15	1 0 0 0 0 0	4M				16M
16	1 0 0 0 0 1	1M	4M			20M
17	1 0 0 0 1 0	1M	1M	4M		24M
18	1 0 0 0 1 1	1M	1M	1M	4M	28M
19	1 0 0 1 0 0	4M	4M			32M
20	1 0 0 1 0 1	1M	4M	4M		36M
21	1 0 0 1 1 0	1M	1M	4M	4M	40M
22	1 0 0 1 1 1	4M	4M	4M		48M
23	1 0 1 0 0 0	1M	4M	4M	4M	52M
24	1 0 1 0 0 1	4M	4M	4M	4M	64M

** Memory configuration bits 5 and 4 are located in Register 12h, bits 1 and 0.*

Page Interleave Setup
Configuration Register 1h, R/W

Bit	Function
7	Write wait state control bit 1.
6	Write wait state control bit 0.
5	Reserved.
4	Disable RAS time out.
3	Reserved.
2	Reserved.
1	Enable RAS precharge time
0	Enable read 0 wait state.

Bit 7,6 These two bits are the write wait state control bits. Default is zero.

Bit 7	Bit 6	Wait State Non-Pipeline	Wait State Pipeline
0	0	1	1
0	1	1	0
1	0	2	1
1	1	2	1

Bit 4 When set to one, this bit disables RAS time out. When set to zero, this bit enables RAS time out. Default is zero.

Bit 1 When set to one, this bit enables RAS precharge time to 2 cycles. When set to zero, set RAS precharge time to 3 cycles. Default is 0.

Bit 0 When set to one, this bit enables read 0 wait state. When set to zero, set to read 1 wait state. Default is 0.

Shadow Setup
Configuration Register 2h, R/W

Bit	Function
7	Reserved
6	Enable shadow cache.
5	Shadow read only, write protect.
4	Enable shadow segment F0000- FFFFF.
3	Enable shadow segment E0000- EFFFF.
2	Enable shadow segment D0000- DFFFF.
1	Enable shadow segment C8000- CFFFF.
0	Enable shadow segment C0000- C7FFF.

Bit 6 When set to one, this bit enables shadow area to be cacheable. Default is zero.

Bit 5 When set to one, this bit places the shadow segment into read only, write protect mode. Default is zero.

Bit 4 When set to one, this bit enables shadow segment F0000-FFFFF. Default is zero.

Bit 3 When set to one, this bit enables shadow segment E0000-EFFFF. Default is zero.

Bit 2 When set to one, this bit enables shadow segment D0000-DFFFF. Default is zero.

Bit 1 When set to one, this bit enables shadow segment C8000-CFFFF. Default is zero.

Bit 0 When set to one, this bit enables shadow segment C0000-C7FFF. Default is zero.

Coprocessor and Parity Configuration Register 3h, R/W

Bit	Function
7	Reserved
6	Reserved
5	Reserved
4	Disable parity check.
3	NP in 1 wait state.
2	Disable NP sequencer.
1	Disable Weitek, becomes AT cycle.
0	Disable 387, becomes AT cycle.

Bit 4 When set to one, this bit disables parity check. Default is zero.

Bit 3 When set to one, the numeric processor operates in 1 wait state. When set to zero, the numeric processor operates in 2 wait state. Default is zero.

Bit 2 When set to one, this bit disables the numeric processor's sequencer. Default is zero.

Bit 1 When set to one, this bit disables access to the Weitek 3167 coprocessor. All access to Weitek will become AT Bus cycles. Default is zero.

Bit 0 When set to one, this bit disables access to the 387 processor. All access to 387 will become AT Bus cycles. Default is zero.

Cache Setup Configuration Register 4h, R/W

Bit	Function
7	Enable post write.
6	Enable memory write 0 wait in486 mode.
5	Cache 1 wait state.
4	Enable DRAM burst mode.
3	Enable cache burst mode for 486.
2	Set cache line size bit 0.
1	Set cache line size bit 1.
0	Enable cache.

Bit 7 When set to one, this bit enables post write. Default is zero.

Bit 6 When set to one, this bit enables memory write 0 wait for 486 non- cache operation in page hit cycle. When set to zero, this bit enables memory write 1 wait for 486 non-cache operation in page hit cycle. Default is zero.

Bit 5 When set to one, this bit enables cache 1 wait state. When set to zero, this bit enables cache zero wait state. Default is zero.

Bit 4 When set to one, this bit enables DRAM burst mode. Default is zero.

Bit 3 When set to one, this bit enables cache burst mode to update the 486 internal cache. Default is zero.

Bit 2,1 These two bits set the cache line size as follows:

Bit 2	Bit 1	Line Size
0	0	32
1	0	32
0	1	64
1	1	128

Bit 0 When set to one, this bit enables the 2046 cache controller. Default is zero.

Power Up Select and Slow Refresh Configuration Register 5h R, R/W

Bit	Function
7	8-bit ROM
6	386/486 mode select
5	Double/single phase clock select
4	Enable page mode
3	Reserved
2	Reserved
1	Set slow refresh divisor
0	Set slow refresh divisor

Bit 7 This is a read only bit. When read as one, this bit indicates an 8-bit ROM is installed. When read as zero, this bit indicates a 16-bit ROM is installed.

Bit 6 This is a read only bit. When read as one, it indicates 386 mode is selected. When read as zero, it indicates 486 mode is selected. Read only.

Bit 5 This is a read only bit. When read as one, it indicates double phase clock is selected. When zero, a single phase clock is selected. Read only.

Bit 4 When set to one, this bit enables page mode sequencer. This bit is a read only bit when the 2046 is enabled in single phase CPU clock mode. Default is zero.

Bit 1,0 Bits 1 and 0 select the slow refresh divisor (Read/Write) as follows:

Bits 1	0	Divided by
0	0	1
0	1	2
1	0	4
1	1	8

AT Bus Clock Source Select Configuration Register 6h, R/W

Bit	Function
7	Reserved
6	Reserved
5	Reserved
4-0	Select clock source for SYSCLK

Bits 4-0 Select clock source for AT Bus clock (SYSCLK). The 2046 supports three clock sources for the AT Bus clock. SYSCLK is half of the AT bus clock. When bit 4 is set at zero (default), the SYSCLK is derived from X14M1 (14.318 MHz). When bits 4, 3 are set at one, the SYSCLK is derived from EXT16M (16 MHz). When bit 4 is one and bit 3 is zero, CLKSRC provides the clock source. In addition, bits 2-0 set a divisor to divide down CLKSRC for the use of SYSCLK.

Bits 4	3	2	1	0	AT Bus clock source
0	X	X	X	X	X14M1, default.
1	1	X	X	X	EXT16M
1	0	0	0	0	CLKSRC/5
1	0	0	0	1	CLKSRC/3
1	0	0	1	0	CLKSRC/2.5
1	0	0	1	1	CLKSRC/1.5
1	0	1	0	0	CLKSRC/1
1	0	1	0	1	CLKSRC/4
1	0	1	1	0	CLKSRC/1
1	0	1	1	1	CLKSRC/2

MUX Clock Source Select Configuration Register 7h, R/W

Bit	Function
7	Reserved
6	Reserved
5	Reserved
4-0	Select clock source for internal mux clock.

Bit 4-0 Select clock source for internal mux clock to be used along with multiplex select pins SEL0, SEL1, and SEL2. When bit 4 is set at zero (default), the mux clock is derived from X14M1 (14.318 MHz). When bits 4 and 3 and 0 are set at one, the mux clock is derived from EXT16M (16 MHz). When bit 4 is one and bit 3 is zero, CLKSRC provides the mux clock source. In addition, bits 2-1 set a divisor to divide down CLKSRC for the use of internal mux clock.

Bits 4 3 2 1 0	Mux clock source
0 X X X X	X14M1, default.
1 1 X X 1	EXT16M
1 0 X X 0	CLKSRC/5
1 0 1 0 1	CLKSRC/4
1 0 0 0 1	CLKSRC/3
1 0 1 1 1	CLKSRC/2
1 0 0 1 1	CLKSRC/1

Sleep Mode Control Configuration Register 8h, R/W

Bit	Function
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Enable Sleep mode
2-0	Set Sleep mode frequency divisor

Bit 3 When set to one, this bit enables sleep mode. If sleep mode is enabled, the system clock source will be switched from CLKSRC to AT bus clock which is divided down to a sleep mode frequency. Default is zero.

Bit 2-0 These bits select the divisor to divide the AT bus clock source to the sleep mode clock.

Bits 2 1 0	Divisor	Sleep Mode Clock
1 1 1	16	1 MHz
1 1 0	8	2 MHz
1 0 1	4	4 MHz
1 0 0	2	8 MHz
0 X X	1	16 MHz

Enable Keyboard Reset Configuration Register 9h, R/W

Bit	Function
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Should be set to one
0	Enable keyboard reset

Bit 1 This bit, *along with Register 4, bit 7* should be set to one to enable post write. Default is zero.

Bit 0 When set to one, this bit enables keyboard reset. Default is zero.

DMA High Address 24, 25
Configuration Register 0Ah, R/W

Bit	Function
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Address bit 25 for non CPU cycle.
0	Address bit 24 for non CPU cycle.

Bit 1 When set to one, this bit enables the address bit 25 for non CPU cycle. Default is zero.

Bit 0 When set to one, this bit enables the address bit 24 for non CPU cycle. Default is zero.

Page Mode Setup
Configuration Register 0Bh, R/W

Bit	Function
7-6	Set RAS precharge time.
5	Set RAS to CAS delay time.
4	Set CAS precharge time.
3-2	Set CAS width in read cycle.
1-0	Set CAS width in write cycle.

Bit 7-6 Set RAS precharge time. Default is 2T.

Bits 7 6	RAS precharge time
0 0	2T
0 1	3T
1 0	4T
1 1	5T

Bit 5 When this bit is set to one, the RAS to CAS delay is 3 cycles in write cycle. When set to zero, the RAS to CAS delay time is 2 cycles for both read and write cycles. Default is 0.

Bit 4 When this bit is set to one, the CAS precharge time is 2 cycles. When set to zero, the CAS precharge time is one cycle. Default is 0.

Bit 3,2 These two bits define CAS width for read cycle time. Default is one cycle.

Bits 3 2	CAS width in read cycle
0 0	1T
0 1	2T
1 0	3T
1 1	4T

Bit 1,0 These two bits define CAS width for write cycle. The default is one cycle.

Bits 1 0	CAS width in write cycle
0 0	1T
0 1	2T
1 0	3T
1 1	4T

Non-cacheable block 1
Configuration Register 0Ch, R/W

Bit	Function
7	Non-cacheable block 1 address A17
6	Non-cacheable block 1 address A16
5	Non-cacheable block 1 address A15
4	Non-cacheable block 1 address A14
3-0	Set non-cacheable block 1 size

Bit 7 When set to one, this bit enables non-cacheable block 1 address A17. Default is zero.

Bit 6 When set to one, this bit enables non-cacheable block 1 address A16. Default is zero.

Bit 5 When set to one, this bit enables non-cacheable block 1 address A15. Default is zero.

Bit 4 When set to one, this bit enables non-cacheable block 1 address A14. Default is zero.

Bit 3-0 These bits enable set non-cacheable block 1 size as follows:

Memory 3210	Addr. compared	Non-cacheable block size
0000	don't care	all cacheable
0001	14-25	16K
0010	15-25	32K
0011	16-25	64K
0100	17-25	128K
0101	18-25	256K
0110	19-25	512K
0111	20-25	1M
1000	21-25	2M
1001	22-25	4M
1010	23-25	8M
1011	24-25	16M
1100	25	32M
1XXX		disable cache

Configuration Register 0Dh, R/W

Bit	Function
7	Non-cacheable address A25
6	Non-cacheable address A24
5	Non-cacheable address A23
4	Non-cacheable address A22
3	Non-cahceable address A21
2	Non-cacheable address A20
1	Non-cacheable address A19
0	Non-cacheable address A18

Bit 7 When set to one, this bit enables non-cacheable block 1address A25. Default is zero.

Bit 6 When set to one, this bit enables non-cacheable block 1 address A24. Default is zero.

Bit 5 When set to one, this bit enables non-cacheable block 1 address A23. Default is zero.

Bit 4 When set to one, this bit enables non-cacheable block 1 address A22. Default is zero.

Bit 3 When set to one, this bit enables non-cacheable block 1 address A21. Default is zero.

Bit 2 When set to one, this bit enables non-cacheable block 1 address A20. Default is zero.

Bit 1 When set to one, this bit enables non-cacheable block 1 address A19. Default is zero.

Bit 0 When set to one, this bit enables non-cacheable block 1 address A18. Default is zero.

Non-cacheable block 2
Configuration Register 0Eh, R/W

Bit	Function
7	Non-cacheable block 2 address A17
6	Non-cacheable block 2 address A16
5	Non-cacheable block 2 address A15
4	Non-cacheable block 2 address A14
3-0	Set non-cacheable block 2 size

Bit 7 When set to one, this bit enables non-cacheable block 2 address A17. Default is zero.

Bit 6 When set to one, this bit enables non-cacheable block 2 address A16. Default is zero.

Bit 5 When set to one, this bit enables non-cacheable block 2 address A15. Default is zero.

Bit 4 When set to one, this bit enables non-cacheable block 2 address A14. Default is zero.

Bit 3-0 These bits set non-cacheable block 2 size as follows:

Memory 3210	Addr. compared	Non-cacheable block size
0000	don't care	all cacheable
0001	14-25	16K
0010	15-25	32K
0011	16-25	64K
0100	17-25	128K
0101	18-25	256K
0110	19-25	512K
0111	20-25	1M
1000	21-25	2M
1001	22-25	4M
1010	23-25	8M
1011	24-25	16M
1100	25	32M
1XXX		disable cache

Configuration Register 0Fh, R/W

Bit	Function
7	Non-cacheable block 2 address A25.
6	Non-cacheable block 2 address A24.
5	Non-cacheable block 2 address A23.
4	Non-cacheable block 2 address A22.
3	Non-cacheable block 2 address A21.
2	Non-cacheable block 2 address A20.
1	Non-cacheable block 2 address A19.
0	Non-cacheable block 2 address A18.

Bit 7 When set to one, this bit enables non-cacheable block 2 address A25. Default is zero.

Bit 6 When set to one, this bit enables non-cacheable block 2 address A24. Default is zero.

Bit 5 When set to one, this bit enables non-cacheable block 2 address A23. Default is zero.

Bit 4 When set to one, this bit enables non-cacheable block 2 address A22. Default is zero.

Bit 3 When set to one, this bit enables non-cacheable block 2 address A21. Default is zero.

Bit 2 When set to one, this bit enables non-cacheable block 2 address A20. Default is zero.

Bit 1 When set to one, this bit enables non-cacheable block 2 address A19. Default is zero.

Bit 0 When set to one, this bit enables non-cacheable block 2 address A18. Default is zero.

Memory 3210	Addr. compared	Non-cacheable block size
0000	don't care	all cacheable
0001	14-25	16K
0010	15-25	32K
0011	16-25	64K
0100	17-25	128K
0101	18-25	256K
0110	19-25	512K
0111	20-25	1M
1000	21-25	2M
1001	22-25	4M
1010	23-25	8M
1011	24-25	16M
1100	25	32M
1XXX		disable cache

Configuration Register 10h, R/W

Bit	Function
7	Non-cacheable block 3 address A17.
6	Non-cacheable block 3 address A16.
5	Non-cacheable block 3 address A15.
4	Non-cacheable block 3 address A14.
3-0	Set non-cacheable block 3 size.

Bit 7 When set to one, this bit enables non-cacheable block 3 address A17.

Bit 6 When set to one, this bit enables non-cacheable block 3 address A16.

Bit 5 When set to one, this bit enables non-cacheable block 3 address A15.

Bit 4 When set to one, this bit enables non-cacheable block 3 address A14.

Bit 3-0 These bits set non-cacheable block 3 size.

Configuration Register 11h, R/W

Bit	Function
7	Non-cacheable block 3 address A25.
6	Non-cacheable block 3 address A24.
5	Non-cacheable block 3 address A23.
4	Non-cacheable block 3 address A22.
3	Non-cacheable block 3 address A21.
2	Non-cacheable block 3 address A20.
1	Non-cacheable block 3 address A19.
0	Non-cacheable block 3 address A18.

Bit 7 When set to one, this bit enables non-cacheable block 3 address A25.

Bit 6 When set to one, this bit enables non-cacheable block 3 address A24.

Bit 5 When set to one, this bit enables non-cacheable block 3 address A23.

Bit 4 When set to one, this bit enables non-cacheable block 3 address A22.

Bit 3 When set to one, this bit enables non-cacheable block 3 address A21.

Bit 2 When set to one, this bit enables non-cacheable block 3 address A20.

Bit 1 When set to one, this bit enables non-cacheable block 3 address A19.

Bit 0 When set to one, this bit enables non-cacheable block 3 address A18.

Configuration Register 12h, R/W
Mix Mode and Control

Bit	Function
7	Enable RAS to CAS delay time.
6	Reserved.
5	Page mode ROM size selection bit.
4	Enable Turbo-Sleep switch
3	Enable mix DRAM mode
2	Reserved
1	Page mode memory configuration bit 5
0	Page mode memory configuration bit 4

Bit 7 When set to one, the RAS to CAS delay time is 3 cycles for read cycles in Page mode. When set to zero, the RAS to CAS delay time is 2 cycles. Default is zero.

Bit 5 This bit *in conjunction with bit 6, Register 0h* sets the ROM size for middle BIOS in Page mode operation.

Reg. 18h Bit 5	*Reg. 0h Bit 6*	Middle ROM size
0	0	Disabled
0	1	64K (FF0000-FFFFFF)
1	0	256K (FC0000-FFFFFF)
1	1	512K (F80000-FFFFFF)

Bit 4 When set to one, this bit enables the Turbo pin (pin 75) to switch the operation speed between Turbo clock CLKSRC and Sleep mode clock (defined by Register 8h, bits 2-0). When set to zero, Turbo pin will toggle the operation speed between Turbo clock (CLKSRC) and Normal clock.

Bit 3 When set to one, this bit enables the Page mode operation. Default is zero.

Bit 1-0 These two bits are Page mode memory configuration bits 5,4. Refer to Page mode memory configuration table of Register 0h.

Configuration Register 18h, R/W

Bit	Function
7-6	Reserved
5	Disable sampling delay 1T.
4	Enable post write 0 wait state. Default is 1WS.
3-2	Reserved
1	Enable burst refresh
0	Disable AT refresh

Bit 5 When set to one, this bit disables the sampling delay of 1 cycle time. Default is zero.

Bit 4 When set to one, this bit enables post write zero wait state. When set to zero, this bit enables post write one wait state. Default is zero.

Bit 1 When set to one, this bit enables hidden burst refresh. Default is zero.

Bit 0 When set to one, this bit disables ATstandard refresh. Default is zero.

Configuration Register 19h, R/W

Bit	Function
7	Burst refresh RAS active cycle width bit 1.
6	Burst refresh RAS active cycle width bit 0.
5	Burst refresh RAS precharge cycle width bit 1.
4	Burst refresh RAS precharge cycle width bit 0.
3	Reserved.
2	Burst refresh count bit 2.
1	Burst refresh count bit 1.
0	Burst refresh count bit 0.

Bit 7-6 These two bits define the burst refresh RAS active cycle width. Default is zero.

Bits 7	6	Cycle width
0	0	4T
0	1	3T
1	0	2T
1	1	1T

Bit 5-4 These two bits define the burst refresh RAS precharge cycle width. Default is zero.

Bits 5	4	Cycle width
0	0	4T
0	1	3T
1	0	2T
1	1	1T

Bit 2-0 These three bits define the burst refresh count. Default is zero.

Bits 2	1	0	Burst number
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

Configuration Register 1Ah, R/W

Bit	Function
7	Enable ADS delay at front end.
6	Disable 486 internal cache.
5	Disable 386 pipeline.
4	Enable cache always hit, for initialization.
3	Enable cache always miss, for initialization.
2	Set match polarity. Default is active high.
1	Enable DMA delay line to 3T. Default is 2T.
0	Enable fast DMA, use CPU clock. Default use 16M.

Bit 7 When set to one, this bit enables ADS delay at front end. Default is zero.

Bit 6 When set to one, this bit disables 486 internal cache. When set to zero, this bit enables 486 internal cache. Default is zero.

Bit 5 When set to one, this bit disables the 386 pipeline. When set to zero, this bit enables the 386 pipeline. Default is zero.

Bit 4 When set to one, cache will always hit. Default is zero.

Bit 3 When set to one, cache will always miss. Default is zero.

Bit 2 When set to one, this bit sets active low match input. When set to zero, this bit sets active high match input. Default is zero.

Bit 1 When set to one, the DMA delay line is 3 cycle times. When set to zero, the DMA delay line is 2 cycle times. Default is 2 cycle times.

Bit 0 When set to one, this bit enables fast DMA and uses CPU clock. When set to zero, DMA uses AT Bus clock source. Default is zero.

Configuration Register 1Bh

Bit	Function
7	Disable CAS3 output, only for double phase clock mode.
6	Disable CAS2 output, only for double phase clock mode.
5	Disable CAS1 output, only for double phase clock mode.
4	Reserved.
3	Disable RAS3 output.
2	Disable RAS2 output.
1	Disable RAS1 output.
0	Toggle turbo input.

Bit 7 In double phase clock mode, when this bit is set to one, it disables CAS3 output. When set to zero, CAS3 output is enabled. Default is zero.

Bit 6 In double phase clock mode, when this bit is set to one, it disables CAS2 output. When set to zero, the CAS2 output is enabled. Default is zero.

Bit 5 In double phase clock mode, when this bit is set to one, it disables CAS1 output. When set to zero, the CAS1 output is enabled. Default is zero.

Bit 4 Reserved

Bit 3 When set to one, this bit disables RAS3 output. When set to zero, this bit enables RAS3 output. Default is zero.

Bit 2 When set to one, this bit disables RAS2 output. When set to zero, this bit enables RAS2 output. Default is zero.

Bit 1 When set to one, this bit disables RAS1 output. When set to zero, this bit enables RAS1 output. Default is zero.

Bit 0 *This bit works in conjunction with Register 1Ch, bit 7* to set the turbo or normal speed according to the following table through software (keyboard) control:

Reg. 1Ch bit 7	*Reg. 1Bh bit 0*	System Speed
0	0	Normal
0	1	Turbo
1	0	Turbo
1	1	Normal

Configuration Register 1Ch, Rea Only

Bit	Function
7-4	Reserved
3	Read only keyboard turbo pin status.
2	Read only ver. I.D. bit 2.
1	Read only ver. I.D. bit 1.
0	Read only ver. I.D. bit 0.

Bit 3 This bit reads the status of the turbo pin to allow the keyboard to control the turbo and normal speed.

Bit 2-0 Bits 2-0 are revision control register bits.

OS/2 Optimization
Port 92h

Bit	Function
7-2	Reserved
1	Fast Gate A20.
0	Fast reset.

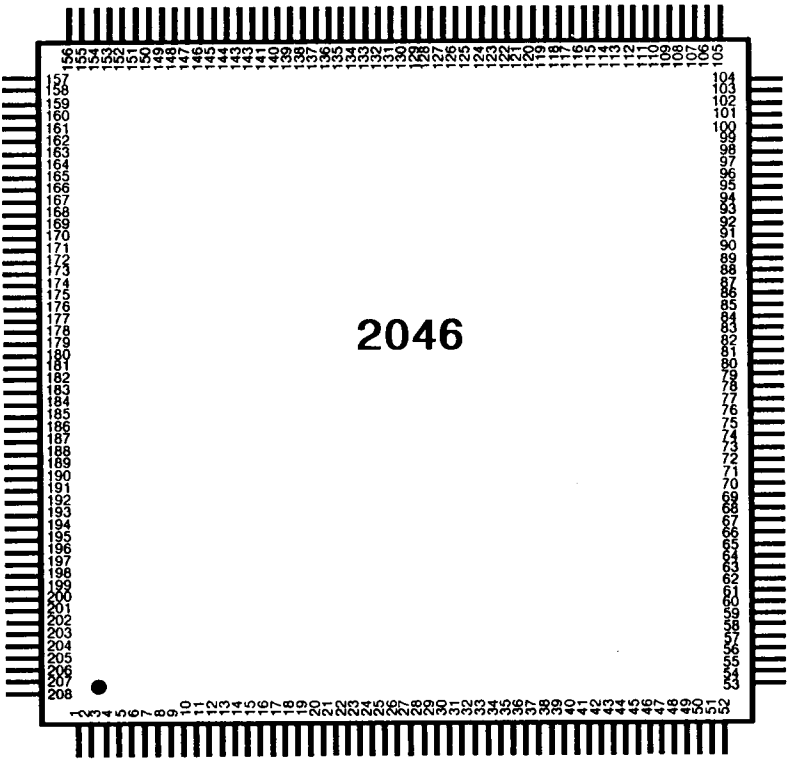
Bit 1 This bit controls CPU address bit A20. When set to 1, it enables A20. When set to 0, this bit makes the A20 Signal inactive, thus preventing the Address bus from going beyond the 0FFFFFh boundary in Real Mode.

Although it has the same function as the keyboard controller's GATE-A20 signal, it is much faster because it is just a simple I/O write operation. Default is 0.

Bit 0 By setting this bit to 1, application software can reinitialize the microprocessor and switch the operation from Protected Mode to Real Mode. Setting this bit does not reset the whole system, it only affects the CPU. This reset function is the same as that of the keyboard controller's "KBRST" signal. However, it provides a faster reset sequence. This bit can be read by application software to determine if it is a hot rest or cold boot. It can only be set to 0 by writing a 0 to bit 0 of the register or by system reset. Default is 0.

These two bits, bit 1 and 0, are logic-ORed with keyboard signals "A20GATE" and "KBRST."

Pin Diagram



1 VSS	69 A24	89 VSS	109 /CAS3	129 AEN	149 /SMEMW	169 SD13	189 D5
2 D23	70 A25	90 MA3*	110 /RAS0	130 /SBHE	150 DAC0	170 SD14	190 D6
3 D24	71 A31	91 MA4	111 /RAS1	131 /IOCS16	151 DAC2	171 SD15	191 D7
4 D25	72 PWRGD	92 MA5	112 VSS	132 /MEMCS16	152 DAC1	172 PAR0	192 D8
5 D26	73 HLDA	93 MA6	113 /RAS2	133 IOCHRDY	153 VSS	173 PAR1	193 D9
6 D27	74 /NPBZY	94 /KTGWE	114 VDD	134 /MASTER	154 SD4	174 VSS	194 D10
7 D28	75 TURBO	95 /MBE0*	115 /RAS3	135 VSS	155 SD5	175 PAR2	195 D11
8 D29	76 /BE0	96 VSS	116 SA0	136 SEL0	156 SD6	176 PAR3	196 D12
9 D30	77 /BE1	97 VDD	117 SA1	137 SEL1	157 MUXI0	177 /READYO	197 D13
10 VDD	78 /BE2	98 MA7	118 SA17	138 SEL2	158 MUXI1	178 VDD	198 D14
11 D31	79 /BE3	99 MA8	119 VSS	139 /ENMAX	159 MUXI2	179 SD0	199 D15
12 CPURST	80 LA20	100 MA9	120 SA18	140 /MEMR	160 NPEREQ*	180 SD1	200 VSS
13 CLKI	81 VSS	101 MA10	121 SA19	141 /MEMW	161 SD7	181 SD2	201 VDD
14 CLKOUT	82 /KRMOE*	102 /MBE1*	122 SPEAKER	142 VSS	162 SD8	182 SD3	202 D16
15 VSS	83 /KRMWE*	103 /MBE2*	123 /ZWS	143 X14M2	163 SD9	183 VSS	203 D17
16 CLKSRC	84 /WEN	104 VSS	124 /IOR	144 X14M1	164 VSS	184 D0	204 D18
17 /KEN	85 MA0	105 /MBE3*	125 /IOW	145 RESETDRV	165 VDD	185 D1	205 D19
18 / RDY	86 MA1*	106 /CAS0	126 BALE	146 /REF	166 SD10	186 D2	206 D20
19 /NA	87 VDD	107 /CAS1	127 VSS	147 VDD	167 SD11	187 D3	207 D21
20 MATCH2	88 MA2*	108 /CAS2	128 SYSCLK	148 /SMEMR	168 SD12	188 D4	208 D22
21 /CPUBZY*							
22 TGLA2*							
23 INTR							
24 M/-IO							
25 D/-C							
26 W/-R							
27 TC							
28 /XDIR*							
29 /ENABUS*							
30 NMI							
31 CPUPEREQ*							
32 /PHOLD							
33 TGLA3*							
34 GA20OUT							
35 MDLAT							
36 /MDIR							
37 486CLK							
38 VSS							
39 EXT16M							
40 RTCAS							
41 A2							
42 A3							
43 VDD							
44 A4							
45 A5							
46 A6							
47 A7							
48 /ADS							
49 /NPERR							
50 MATCH1							
51 A8							
52 A9							
53 A10							
54 A11							
55 A12							
56 A13							
57 A14							
58 A15							
59 A16							
60 VSS							
61 VDD							
62 A17							
63 A18							
64 A19							
65 A20							
66 A21							
67 A22							
68 A23							

* Signals are multifunction or multiplexed pins. Please see pin descriptions.

Pin Descriptions

1. Signal names beginning with '/' are Low-Active
2. '*2' at the end of a signal indicates multiplexed pins
3. '*3' at the end of a signal indicates single phase mode signals

Symbol	Pin	Type	Description
Clock Pins			
CLKSRC	16	I	CPU internal clock source input to 2046, it is two times of the system frequency for 386DX system; and one time or two of the system clock for the 486 systems.
EXT16M	39	I	Alternative bus clock input. This clock provides an optional 16 MHz input clock asynchronous to the CLKSRC.
SYSCLK	128	O	Peripheral clock. This clock can be derived from either X14M, CLKSRC, or EXT16M to provide a system clock source for the AT Bus.
CLKOUT	14	O	Clock output providing the clock for the 386DX and 486.
CLKI	13	I	Clock feedback from CLKOUT.
X14M1	144	I	14.318 MHz crystal input.
X14M2	143	O	14.318 MHz crystal input.
486CLK	37	O	Times 1 clock for 486.
Reset Pins			
PWRGD	72	I	"Power Good" signal from the power supply. When low, a power-up reset is generated.
CPURST	12	O	CPU reset output.
RESETDRV	145	I/O	System reset. Active high. This reset signal is for the bus devices to reset or initialize system logic upon power-up or during a low line voltage.

Symbol	Pin	Type	Description
CPU Pins			
/ADS	48	I	/ADS from CPU. Active low. /ADS is driven directly by the CPU /ADS pin.
M/-IO	24	I	M/-IO from CPU. When M/-IO is high, it indicates current bus cycle is a memory access cycle. When M/-IO is low, it indicates that current bus cycle is a I/O access cycle.
D/-C	25	I	D/-C from CPU. D/-C is designed to connect directly with the D/-C pin of CPU. It indicates whether the bus is a data cycle or a control cycle.
W/-R	26	I	W/-R from CPU. W/-R is designed to connect directly to the W/-R pin of the CPU. When W/-R is high, it indicates that the current bus cycle is a write cycle. When W/-R is low, it indicates that the current bus cycle is a read cycle.
/RDY	18	O	Ready signal to CPU.
/NA	19	O	This pin connects to the 386 CPU directly to request address pipelining.
PHOLD	32	O	CPU HOLD Request. Active high.
HLDA	73	I	Hold acknowledge input signal from CPU. Active high. This signal is usually driven directly by the HLDA pin of CPU. HLDA is used to indicate to 2046 that CPU will grant the control of bus in response to HOLD request.
INTR	23	O	Interrupt to the CPU. Active high.
NMI	30	O	Non-maskable interrupt to the CPU generated by memory parity error, or IOCHCK error. Active high.
/KEN	17	O	486 cache enable. It indicates to the 486 that the current cycle is cacheable.

Symbol	Pin	Type	Description
NPU Signal Pins			
/NPBZY	74	I	This is a multifunction pin. In 386 mode, this pin signals math coprocessor busy, from 80387. In 486 mode, this is reserved and should be tied high by a pull-up resistor.
/NPERR	49	I	Math coprocessor error, from 80387 in 386 mode or 486 CPU in 486 mode..
NPEREQ, /BLAST*[3]	160	I	This is a multifunction pin. In 386 mode, it connects to 387 . In 486 mode, it is the burst last signal indicating the last cycle of burst mode from the 486. This signal is active low.
/CPUBZY, /IGNNE*[3]	21	O	In 386 mode, this is the busy signal to the CPU. In the 486 mode, this is the ignore numeric error signal. When asserted, the 486 microprocessor ignores a numeric error and continues executing non-control floating point instructions. When /IGNNE is deasserted, the 486 microprocessor will freeze on a non-control floating point instruction, if a previous floating point instruction caused an error. Active low.
CPUPEREQ, /BRDY*[3]	31	O	This is a multifunction pin. In the 386 mode, it goes to 386 directly. In 486 mode, it is the burst ready output to 486 CPU signal. /BRDY indicates that during a burst cycle the external system has presented valid data in response to a read.
/READYO	177	I	Coprocessor Ready input to 2046.
/BE0	76	I/O	Byte Enable for D0-D7 during read and write cycles. Connects directly to the CPU.
/BE1	77	I/O	Byte Enable for D8-D15 during read and write cycles. Connects directly to the CPU.
/BE2	78	I/O	Byte Enable for D16-D23 during read and write cycles. Connects directly to the CPU.
/BE3	79	I/O	Byte enable for D24-D31 during read and write cycles. Connects directly to the CPU.

Symbol	Pin	Type	Description
A2	41	I/O	Local Address bus. These pins define the physical area of the input/output space accessed.
A3	42		
A4	44		
A5	45		
A6	46		
A7	47		
A8	51		
A9	52		
A10	53		
A11	54		
A12	55		
A13	56		
A14	57		
A15	58		
A16	59		
A17	62		
A18	63		
A19	64		
A20	65		
A21	66		
A22	67		
A23	68		
A24	69		
A25	70		
A31	71		
GA20OUT	34	O	Gated A20 output to 486. This pin is connected to the 486 to force the 486 CPU to mask off A20 in real mode applications.
LA20	80	I/O	This is the gated A20, which becomes the AT slot A20 signal through a 245 tranceiver.
D0	184	I/O	CPU data bus.
D1	185		
D2	186		
D3	187		
D4	188		
D5	189		
D6	190		
D7	191		
D8	192		
D9	193		
D10	194		

Symbol	Pin	Type	Description
D11	195		
D12	196		
D13	197		
D14	198		
D15	199		
D16	202		
D17	203		
D18	204		
D19	205		
D20	206		
D21	207		
D22	208		
D23	2		
D24	3		
D25	4		
D26	5		
D27	6		
D28	7		
D29	8		
D30	9		
D31	11		
Parity Pins			
PAR0	172	I/O	These pins are set to generate parity check for each byte. The parity bit and parity check are done during the DRAM access.
PAR1	173		
PAR2	175		
PAR3	176		
DRAM Pins			
/RAS0	110	O	DRAM row address strobe for DRAM Bank 0.
/RAS1	111	O	DRAM row address strobe for DRAM Bank 1.
/RAS2	113	O	DRAM row address strobe for DRAM Bank 2.
/RAS3	115	O	DRAM row address strobe for DRAM Bank 3.
/CAS0	106	O	DRAM column address strobe. In double phase clock

Symbol	Pin	Type	Description
/CAS1 /CAS2 /CAS3	107 108 109		mode, these signals are one for each bank and should be gated with /MBE0-3 to generate individual CAS for each byte. In single phase clock mode, these signals are one for each byte and are shared for all banks.
/MBE0 /KRMOEA*3	95	O	This is a multifunction pin. The signal indicates DRAM byte enable in double phase clock mode for byte 0. In single phase clock mode, this signal indicates cache RAM output enable for SRAM bank A.
/MBE1 /KRMOEB*3	102	O	This is a multifunction pin. The signal indicates DRAM byte enable in double phase clock mode for byte 1. In single phase clock mode, this signal indicates cache RAM output enable for SRAM bank B.
/MBE2 /LOCK*3	103	I/O	This is a multifunction pin. The signal indicates DRAM byte enable in double phase clock mode for byte 2. In single phase clock mode, this signal becomes the /LOCK input signal from the 486CPU to indicate that the current bus cycle is locked.
/MBE3 /EADS*3	105	O	This is a multifunction pin. This signal indicates DRAM byte enable in double phase clock mode for byte 3. In single phase mode, this signal becomes the /EADS output signal to the 486CPU to indicate that a valid external address has been driven onto the 486CPU.
Cache Pins			
/KTGWE	94	O	Cache TAG write enable.
/KRMWE, /KRMWEA*3	83	O	This is a multifunction pin. In double phase clock mode, this signal is cache RAM write enable. In single phase clock mode, this signal indicates cache RAM bank A write enable.
/KRMOE, /KRMWEB*3	82	O	This is a multifunction pin. In double phase clock mode, this signal is cache RAM output enable. In single phase clock mode, this signal indicates cache RAM Bank B write enable.
TGLA2,	22	O	This is a multifunction pin. In double phase clock mode,

Symbol	Pin	Type	Description
TKA3A*3			the signal is toggle Address bit 2. In single phase clock mode, this signal is address A3 for cache RAM bank A.
TGLA3, TKA3B*3	33	O	This is a multifunction pin. In double phase clock mode, this signal is toggle Address bit 3. In single phase clock mode, this signal is address A3 for cache RAM bank B.
MATCH1	50	I	Cache hit 1. It indicates whether the data in the cache is valid or not. This pin can be programmed to be active high or active low.
MATCH2	20	I	Cache hit 2. It indicates whether the data in the cache is valid or not. This pin will have the same polarity as MATCH1.
/MDIR	36	O	MD Bus Direction Control for post write operation.
MDLAT	35	O	MD Latch for post write operation.
/WEN	84	O	DRAM write enable.
MUX Pins			
MA0, /ROMOE*2	85	O	This pin is a multiplexed pin. When in memory cycle, this pin is DRAM Address bit 0. When in AT bus cycle, this pin is ROM output enable.
MA1, /CS8042*2	86	O	This pin is a multiplexed pin. When in memory cycle, this pin is DRAM Address bit 1. When in I/O cycle, this pin is keyboard chip select.
MA2, /RTCDS*2	88	O	This pin is a multiplexed pin. When in memory cycle, this pin is DRAM Address bit 2. When in I/O cycle, this pin is Real Time Clock DS.
MA3, /RTCWR*2	90	O	This pin is a multiplexed pin. When in memory cycle, this pin is DRAM Address bit 3. When in I/O cycle, this pin is Real Time Clock WR.
MA4	91	O	This pin is DRAM Address bit 4.

Symbol	Pin	Type	Description
MA5	92	O	This pin is DRAM Address bit 5.
MA6	93	O	This pin is DRAM Address bit 6.
MA7	98	O	This pin is DRAM Address bit 7.
MA8	99	O	This pin is DRAM Address bit 8.
MA9	100	O	This pin is DRAM Address bit 9.
MA10	101	O	This pin is DRAM Address bit 10.
SD Bus Pins			
SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7 SD8 SD9 SD10 SD11 SD12 SD13 SD14 SD15	179 180 181 182 154 155 156 161 162 163 166 167 168 169 170 171	I/O	System data bus.
/XDIR, CLKM*[2]	28	I/O	This is a multiplexed pin. It is the XD Bus direction control. On power up, this signal also selects the clock mode . When pulled down it selects the single phase clock, and when pulled high it selects the times two clock.
/ENABUS, (/BS16) CPUM*[2]	29	I/O	This is a multiplexed pin. Enable address buffer for bus quiet operation. It is also used as /BS16 output signal to the CPU to indicate this is not a 32-bit cycle. On power-up, the CPU mode can also be selected . When pulled high it selects the 386 mode, and when pulled low it selects the 486 mode.

Symbol	Pin	Type	Description
SA Bus Pins			
SA0 SA1	116 117	I/O	System Address Bit. SA0-SA1 are the least significant bits of the bus address.
SA17 SA18 SA19	118 120 121	O	System Address Bit.
MUXI0	157	I	This signal is for multiplexed input for KBINT, IRQ3-9 and /RTC INT.
MUXI1	158	I	This signal is for multiplexed input for IRQ10-12, Weitek interrupt, IRQ14-15, KGA20, /IOCHCK
MUXI2	159	I	This signal is for multiplexed input for DRQ0-7, /KBRST.
SEL0 SEL1 SEL2	136 137 138	O	These are select pins for the multiplexer.
DAC0 DAC1 DAC2	150 152 151	O	These pins are for multiplexed DMA acknowledge to generate /DACK0-3, /DACK5-7.
BALE	126	I/O	Address latch enable.
/MEMR	140	I/O	AT Bus Memory Read command. Active low. When HLDA is inactive, /MEMR will act as an output pin, and it is activated only when the current bus cycle is an AT memory read cycle that is not referenced to the local DRAM. When HLDA is active, /MEMR will be an output in DMA mode and will act as an input pin in master mode driven by the bus master. Moreover, for an aligned 16-bit memory transfer with an 8-bit device, /MEMR will be activated twice before the end of the current cycle.
/MEMW	141	I/O	AT Bus Memory Write Command. Active low. When

Symbol	Pin	Type	Description
			HLDA is inactive, /MEMW will act as an output pin, and it is activated only when the current bus cycle is an AT memory write cycle that is not referenced to the local DRAM. When HLDA is active, /MEMW will be an output in DMA mode and will act as an input pin in master mode driven by the bus master. Moreover, for an aligned 16-bit memory transfer with an 8-bit device, /MEMW will be activated twice before the end of the current cycle.
/IOR	124	I/O	I/O read strobe. AT Bus I/O Read Command. Active low. When HLDA is inactive, /IOR acts as an output signal and is active in AT bus I/O read cycle. When HLDA is active, /IOR will be an output in DMA mode and will act as an input pin in master mode driven by the bus master.
/IOW	125	I/O	I/O write strobe. AT Bus I/O Write Command. Active low. When HLDA is inactive, /IOW acts as an output signal and is active in AT bus I/O write cycle. When HLDA is active, /IOW will be an output in DMA mode and will act as an input pin in master mode driven by the bus master.
/SMEMR	148	O	System Bus Memory Read Command. Active low. /SMEMR is active if the current bus cycle is an AT memory read cycle with address location below the first megabyte. /SMEMR is derived from /MEMR and is tristated when accessed above 1M location. /SMEMR is tristated and it needs an external pull high resister.
/SMEMW	149	O	System Bus Memory Write Command. Active low. /SMEMW is active if the current bus cycle is an AT memory write cycle with address location below the first megabyte. /SMEMW is derived from /MEMW and is tristated when access is above 1M location. /SMEMW is tristated and it needs an external pull high resister.
/MEMCS16	132	I	Memory 16-bit chip select.
/IOCS16	131	I	I/O 16-bit chip select.
/ZWS	123	I	Zero wait state. Active low. This signal is pulled low when an AT bus device wants to complete the AT bus cycle in zero wait state.

Symbol	Pin	Type	Description
IOCHRDY	133	I	I/O channel Ready from Expansion bus. Active high. IOCHRDY is used by slow device to extend the access cycle time. 2046 will sample IOCHRDY by 16 MHz. A sample low data will insert wait state into the current bus cycle. Note that if the current cycle is an aligned 16-bit data transfer with an 8-bit device, the cycle will split into 2 subcycles each of which needs to sample a high state of IOCHRDY before terminating the subcycle. After the second sample high state of IOCHRDY, the whole cycle will also be terminated.
AEN	129	O	Bus hold acknowledge. When asserted, I/O devices ignore the address bus to allow DMA transfers to take place. Active high.
/REF	146	I/O	Refresh Cycle. Active Low. This signal goes to slot to indicate that a refresh cycle is ongoing. The slot memory can use this for refresh.
/MASTER	134	I	AT Bus Master Input. Active low. /MASTER indicates to 2046 that the current bus cycle is controlled by a bus master from the expansion slot.
/SBHE	130	I/O	System Bus High Byte Enable. Active low. When HLDA is inactive, /SBHE will act as an output pin which is decoded from the byte enable signals /BE0-3 from CPU. When HLDA is active, /SBHE will act as an output in DMA mode or input pin in Master mode. In Master mode, together with SA0 and SA1 is used to decode the byte enable signal.
SPEAKER	122	O	Output to drive speaker.
TC	27	O	When high, it indicates the terminal count of any DMA channel is reached.
TURBO	75	I	Turbo Speed Control. TURBO is used to switch the operation speed of the system. When TURBO is high, the frequency of CLKOUT is equal to pin CLKSRC input. When TURBO is low, the frequency of CLKOUT is equal to Bus clock.

Symbol	Pin	Type	Description
RTCAS	40	O	Address strobe for 146818 Real Time Clock. Falling edge causes address to be latched in 146818.
/ENMAX*2	139	I/O	MA0-3 MUX enable. This pin also selects 16 bit ROM or 8 bit ROM on power up. It is pulled high for 8 bit ROM and pulled low for 16 bit ROM.

Power & Ground Pins

VDD	10, 43, 61, 87, 97, 114, 147, 165, 178, 201		
VSS	1, 15, 38, 60, 81, 89, 96, 104, 112, 119, 127, 135, 142, 153, 164, 174, 183, 200		
Reserved			

Rating Specifications

Absolute Maximum Ratings *

Parameter	Symbol	Condition	Min	Max	Unit
Power supply voltage	VDD	Ta = 25° C	VSS-0.3	7.0	V
Input voltage	VI		VSS-0.3	VDD + 0.5	V
Output voltage	VO		VSS-0.3	VDD + 0.5	V
Operating temperature	Top		0	70	°C
Storage temp	Tstg		-65	150	°C

* Exposing the device to stress above these limits can cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Capacitance Limits

TA = +25° C, VDD = 5V

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Input capacitance	CI		4		pF	fc = 1 MHz unmeasured pins at GND
Output capacitance	CO		6			
I/O capacitance	CIO		10		pF	

DC Specifications

TA = 0°C to 70°C, VDD = +5V +/- 5%V

Group 1 INPUT

X14M1

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	1.0	V	VDD = 5 V +/- 0.25 V
Input High voltage	VIH	3.5	VDD	V	VDD = 5 V +/- 0.25 V
Input low current	IIL	-1	1	uA	VIN = VSS
Input high current	IIH	-1	1	uA	VIN = VDD

PWRGD

Parameter	Symbol	Min	Max	Unit	Test Condition
Schmitt trigger Input low voltage	VIL	0.6		V	VDD = 5 V
Schmitt trigger Input High voltage	VIH		3.0	V	VDD = 5 V
Input low current	IIL	-1	1	uA	VIN = VSS
Input high current	IIH	-1	1	uA	VIN = VDD

DC Characteristics

TA = 0° C to +70° C, VDD = +5 V +/- 5%

M/-IO, D/-C, W/-R, EXT16M, /ADS, /NPERR, MATCH1, MATCH2, /NPBZY, TURBO, /IOCS16, / MEMCS16, IOCHRDY, /MASTER, /READY0, /ZWS

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VDD = 5 +/- 0.25 V
Input high voltage	VIH	2.0	VDD	V	VDD = 5 +/- 0.25 V
Input low current	IIL	-105	-25	uA	VIN = VSS
Input high current	IIH	-1	1	uA	VIN = VDD

Group 2 OUTPUT

/CPUBZY

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		VSS+0.4	V	IOL = 6.0 mA
Output high voltage	VOH	VDD-0.4		V	IOH = -2.0 mA

CLKI, CLKSRC, HLDA, MUX10, MUX11, MUX12, NPEREQ

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VDD = 5 +/- 0.25 V
Input high voltage	VIH	2.0	VDD	V	VDD = 5 +/- 0.25 V
Input low current	IIL	-1	1	uA	VIN = VSS
Input high current	IIH	-1	1	uA	VIN = VDD

SA17-SA19, /SMEMR, /SMEMW

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		VSS+0.4	V	IOL = 12.0 mA
Output High voltage	VOH	VDD-0.4		V	IOH = -4.0 mA
Tristate leakage current	IOZ	-1	1	uA	VOUT = VDD or VSS

CLKOUT, CPURST, /KEN, /RDY, /NA, TC, TGLA3, MDLAT, /MDIR, 486CLK, MA0-MA3, /WEN, SYSCLK, AEN, BALE

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		VSS+0.4	V	IOL = 12.0 mA
Output High voltage	VOH	VDD-0.4		V	IOH = -4.0 mA

NMI, /PHOLD, RTCAS, SPEAKER, CPUPEREQ

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		VSS+0.4	V	IOL = 2.0 mA
Output High voltage	VOH	VDD-0.4		V	IOH = -1.0 mA

X14M2

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		VSS+0.4	V	IOL = 50 uA
Output high voltage	VOH	VDD-0.4		V	IOH = -50 uA

/XDIR, /ENABUS

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		VSS+0.4	V	IOL = 2.0 mA
Output high voltage	VOH	VDD-0.4		V	IOH = -1.0 mA
Tristate leakage current	IOZ	-1	1	uA	VOUT = VDD or VSS

INTR, DAC0-DAC2

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VDD = 5 V +/- 0.25 V
Input high voltage	VIH	2.0	VDD	V	VDD = 5 V +/- 0.25 V
Input low current	IIL	-105	-25	uA	VIN = VSS
Input high current	IIH	-1	1	uA	VIN = VDD
Output low voltage	VOL		VSS+0.4	V	IOL = 2.0 mA
Output high voltage	VOH	VDD-0.4		V	IOH = -1.0 mA
Tristate Leakage current	IOZ	-105	-25	uA	VOUT = VDD or VSS

D0-D32, A2-A25, A31, /BE0-/BE3, LA20, SEL0-SEL2, GA20OUT, /MBE0-/MBE3, /CAS0-/CAS3

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VDD = 5 V +/- 0.25 V
Input high voltage	VIH	2.0	VDD	V	VDD = 5 V +/- 0.25 V
Input low current	IIL	-105	-25	uA	VIN = VSS
Input high current	IIH	-1	1	uA	VIN = VDD
Output low voltage	VOL		VSS+0.4	V	IOL = 6.0 mA
Output high voltage	VOH	VDD-0.4		V	IOH = -2.0 mA
Tristate Leakage current	IOZ	-105	-25	uA	VOUT = VDD or VSS

TGLA2, /KRMOE, /KRMWE, MA4-MA10, /KTGWE, /RAS0-/RAS3, SA0, SA1, /IOR, /IOW, /SBHE, /MEMR, /MEMW, RESETDRV, /REF, SD0-SD15, PAR0-PAR3

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VDD = 5 V +/- 0.25 V
Input high voltage	VIH	2.0	VDD	V	VDD = 5 V +/- 0.25 V
Input low current	IIL	-105	-25	uA	VIN = VSS
Input high current	IIH	-1	1	uA	VIN = VDD
Output low voltage	VOL		VSS+0.4	V	IOL = 12.0 mA
Output high voltage	VOH	VDD-0.4		V	IOH = -4.0 mA
Tristate Leakage Current	IOZ	-105	-25	uA	VOUT = VDD or VSS

AC Specifications

The default load of output signal is 100 pf. The output load which is not 100 pf will specify in load item.

Symbol	Parameter	Min	Max	Units
t1	DRQ to SYSCLK high setup time	0		ns
t2	HOLD valid from CLKI high delay time	11	30	ns
t5	Low byte ADDR float to active from SYSCLK high	9.8	22.5	ns
t6	Low byte ADDR active to float delay from SYSCLK high	8.4	19.9	ns
t7	High byte ADDR float to active delay from SYSCLK high	19.9		ns
t8	High byte add active to float from HLDA low	18.9		ns
t9	/DAC_x valid from SYSCK high delay time	16.7	40	ns
t10	/IOR, /IOW, /MEMR, /MEMW active from SYSCLK high delay time	9.2	23.4	ns
t11	/IOR, /IOW, /MEMR, /MEMW inactive from SYSCLK high delay time	16.4		ns
t12	TC active from SYSCLK high delay time	8.4	20.3	ns
t13	TC inactive from SYSCLK high delay time	8.4	20.4	ns
t14	IOCHRDY input setup time to SYSCLK high	26		ns
t15	IOCHRDY input hold time from SYSCLK high	6		ns
t16	SYSCLK pulse width low	50	83.3	ns
t17	SYSCLK pulse width high	50	83.3	ns
t18	SYSCLK cycle time	100	166	ns
t19	SYSCLK rise/fall time			
t25	REFRESH address valid delay from /REF	6.9	16.8	ns

AC Specifications

The default load of output signal is 100 pf. The output load which is not 100 pf will specify in load item.

Symbol	Parameter	Min	Max	Units
t26	Refresh address hold time from /REF inactive	1.3	2.9	ns
t27	SA17-SA23 float from /MASTER low delay time	9.3	24.4	ns
t28	SA17-SA23 active from /MASTER high delay time	8.8	23.4	ns
t29	Interrupt request pulse width low	60 + latency		ns
t30	Interrupt output delay + Latency: 8 Mux clock period	15.2	36.6	ns
t31	SPEAKER valid from /IOW high delay time			

AC Specifications

The default load of output signal is 100 pf. The output load which is not 100 pf will be specified in load item.

Symbol	Description	Min	Type	Max	Units	Load (pf)
t32	RESETDRV deactive delay from PWRGD active	6.6		16.0	ns	
t33	CPURST deactivate from CLKI	6.9		16.8	ns	
t34	CPURST active delay from CLKI in software reset and shut down	6.8		16.5	ns	
t35	CPURST active period in software reset and shunt down		16		us	
t36	CPURST deactivate delay from CLKI in software reset and shunt down	6.9		16.8	ns	
t40	/IOCS16 setup time from SYSCLK rising edge		0		us	
t41	/IOCS16 hold time from SYSCLK rising edge	1		3	ns	
t42	/MCS16 setup time from SYSCLK rising edge		0		us	
t43	/MCS16 hold time from SYSCLK rising edge	1		3	ns	
t44	BALE active from CLKI	10.2		25.4	ns	
t45	BALE deactivate from 16 MHz	3.1		7.2	ns	
t46	/ENABUS, /ENMAX active from CLKI	18.7		45.8	ns	
t47	/ENABUS, /ENMAX deactivate from 16 MHz	16.1		39.2	ns	
t48	/SBHE, SA0-1, SA17-19 active from CLKI	11		28	ns	
t50	/MEMR, /MEMW active from SYSCLK	10		24	ns	
t51	/IOR, /IOW active from SYSCLK	10		25	ns	
t52	/MEMR, /MEMW, /IOR, /IOW deactivate from SYSCLK	2		5	ns	

AC Specifications

The default load of output signal is 100 pf. The output load which is not 100 pf will specify in load item.

Symbol	Description	Min	Type	Max	Units	Load (pf)
t53	/RDY active from CLKI	10.1		24.3	ns	
t54	/RDY deactivate from CLKI	11		26.4	ns	
t55	SD setup time in Bus Read cycle		0		us	
t56	SD hold time in Bus Read cycle	2		4	ns	
t57	D delay time in Bus Read cycle	21.3		52.4	ns	
t58	D hold time in Bus Read cycle	15.2		35.6	ns	
t59	SD delay in Bus Write cycle	30.4		77.0	ns	
t60	SD hold time in Bus Write cycle	13.7		39.8	ns	
t61	/SMEMW, /SMEMR active from SYSCLK	18.9		38.6	ns	
t62	/SMEMW, /SMEMR deactivate from SYSCLK	15.5		37.4	ns	
t63	SA0 deactive from SYSCLK in Bus conversion	10.3		24.2	ns	
t66	Decoded signal active delay to command	6.9		16.3	ns	
t67	Decoded signal deactive delay to command	5.5		13.3	ns	
t68	/8042CS setup time to /ENMAX	18.9		46.2	ns	
t69	/8042CS hold time to /ENMAX	9.6		23.7	ns	
t70	GA20OUT active to /ADS	8.5		20.7	ns	

AC Specifications

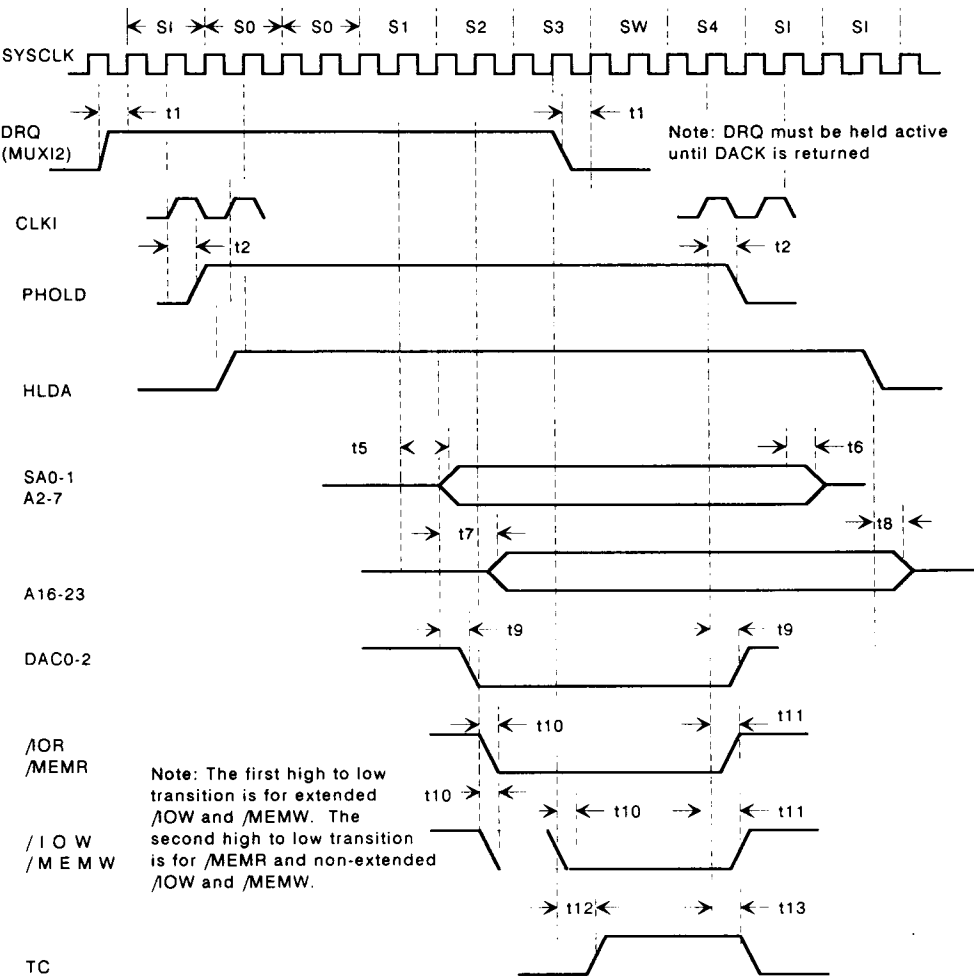
The default load of output signal is 100 pf. The output load which is not 100 pf will specify in load item.

Symbol	Description	Min	Typ	Max	Units	Load (pf)
t100	/RAS active from CLKI	7.4		17.5	ns	
t101	/RAS deactivate from CLKI	9.5		15.4	ns	
t102	/MBE0-3 active from CLKI	15		36.6	ns	
t103	/WEN active from CLKI	8.7		20.9	ns	
104	/WEN deactive from CLKI	7.6		19.2	ns	
t105	/CAS active from CLKI	10.3		24.6	ns	
t106	/CAS deactivate from CLKI	9.5		22.9	ns	
t107	/NA active from CLKI	6.8		16.4	ns	
t108	/NA deactivate from CLKI	6.4		15.3	ns	
t109	ROW address valid from ADDRESS valid	7.9		20.6	ns	
t110	Column address valid from CLKI	14.5		34.6	ns	
t111	ROW address valid from column address	9.7		25.0	ns	
t112	/RDY active from CLKI	9		20.5	ns	
t113	/RDY deactive from CLKI	9.3		20.9	ns	
t114	/KEN active or deactive from CLKI valid	9.4		22.6	ns	
t115	/RAS active from in Refresh cycle	8.9		24.4	ns	
t115a*	Stagger delay in Refresh cycle		3		ns	
t116	/RAS deactive from SYSCLK in Refresh cycle	10		24.5	ns	
t117	ROW address active from address valid (in DMA cycle)	6.5		15.4	ns	
t118	Column address valid from /MEMW, /MEMR active (in DMA cycle)		50		ns	

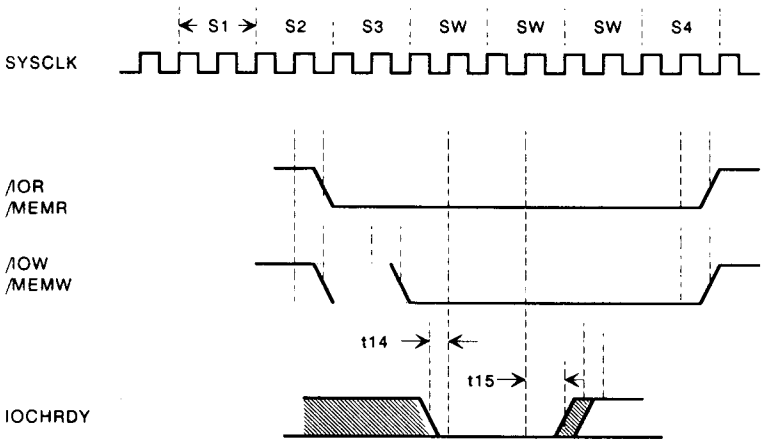
The default load of output signal is 100 pf. The output load which is not 100 pf will specify in load item.

Symbol	Description	Min	Typ	Max	Units	Load (pf)
t119	/RAS active from /MEMR or /MEMW active (in DMA cycle)	7		17.5	ns	
t120	/RAS deactive from /MEMR or /MEMW (in DMA cycle)	5.4		13.5	ns	
t121	/CAS active from /MEMR or /MEMW active (in DMA cycle)		80		ns	
t122	/CAS deactive from /MEMR or /MEMW deactive	9.1		21.9	ns	
t125	MATCH1 setup time		0		ns	
t126	TGLA3 valid delay from address valid	6.4		16.0	ns	
t127	TGLA2 valid delay from address valid	7.1		17.8	ns	
t128	TGLA2 valid delay from rising edge of CLKI	9.5		23.6	ns	
t129	/BRDY activates delay from rising edge of CLKI	13.1		32.0	ns	
t130	/BRDY deactivates delay from rising edge of CLKI	8.0		19.4	ns	
t131	/KRMOE active from falling edge of /ADS	8.1		19.1	ns	
t132	/KRMWE activates delay from rising edge of CLKI	10.1		24.6	ns	
t133	/KRMWE deactivates delay from rising edge of CLKI	9.5		23.4	ns	
t134	/KRMOE deactive from CLKI	8.0		19.4	ns	
t135	TKA3A, TKA3B active from Ax valid.	8.5		16.0	ns	
t136	/KRMOEA, KRMOEB, /KRMWEA, KRMWEB active from CLKI	6.4			ns	
t137	/KRMOEA, KRMOEB, /KRMWEA, KRMWEB deactive from CLKI	9.3		22.5	ns	

DMA Bus Timing

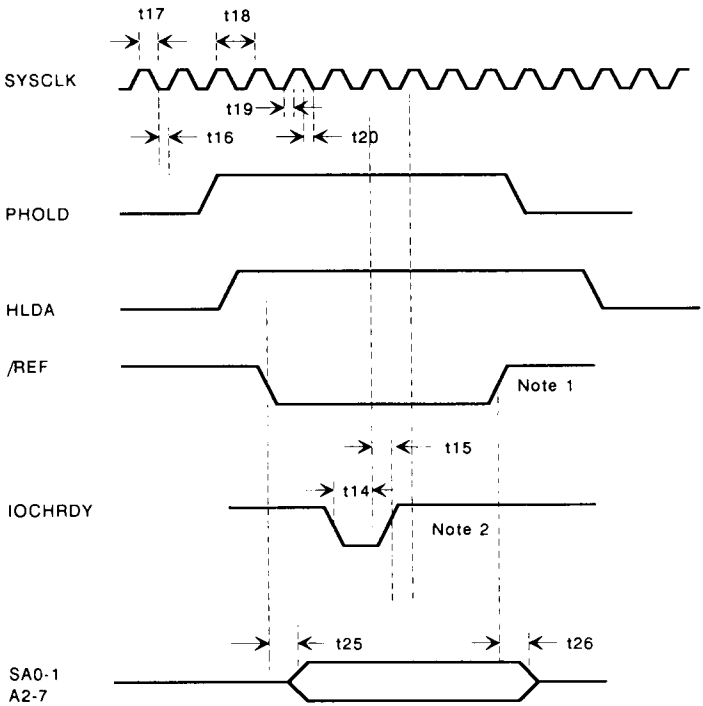


IOCHRDY Timing



The first wait state is inserted by the internal circuitry of the 2046
Additional wait states must be inserted using IOCHRDY.

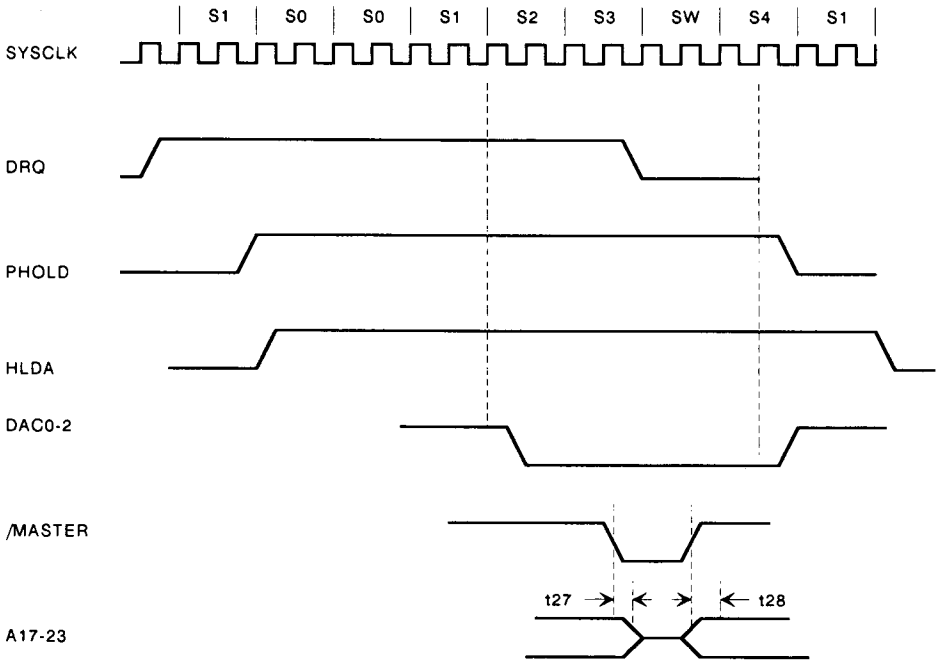
Refresh Timing



Notes

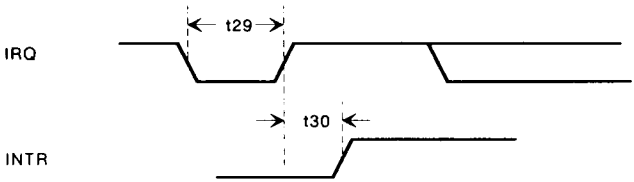
1 A /REF pulse is normally four SYSCLK cycles long.
2 /REF cycles can be extended by inserting wait states using IOCHRDY.

/MASTER Timing

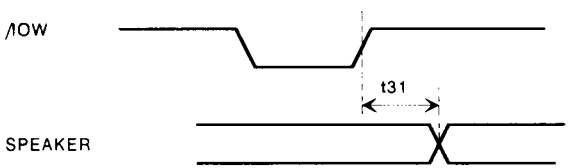


Note: A new bus master must be programmed in Cascade mode.
The new master must not pull /MASTER low until it has received the corresponding DAC signal.

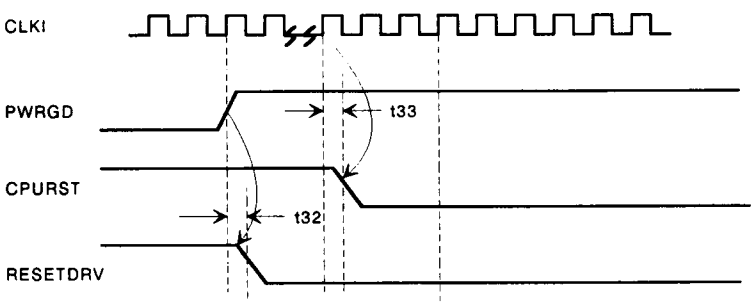
Interrupt Timing



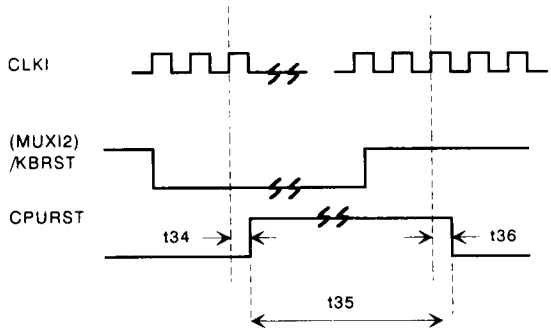
Speaker Timing



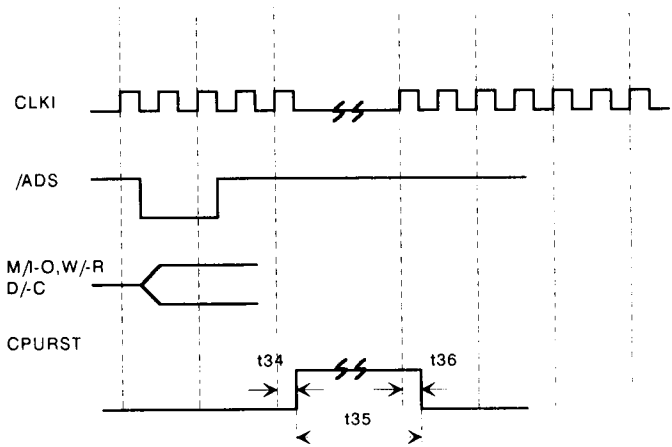
Power On Reset Timing



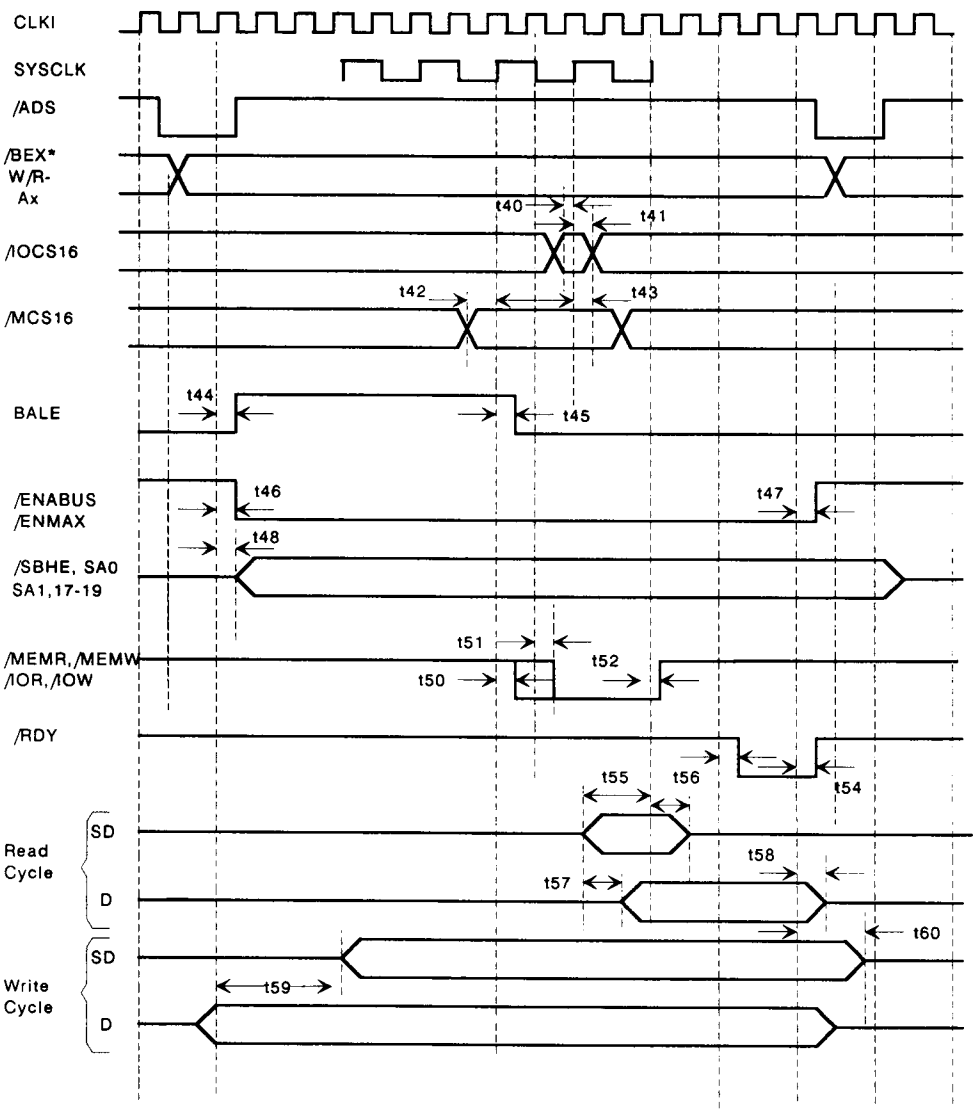
Reset Timing



Shutdown Timing

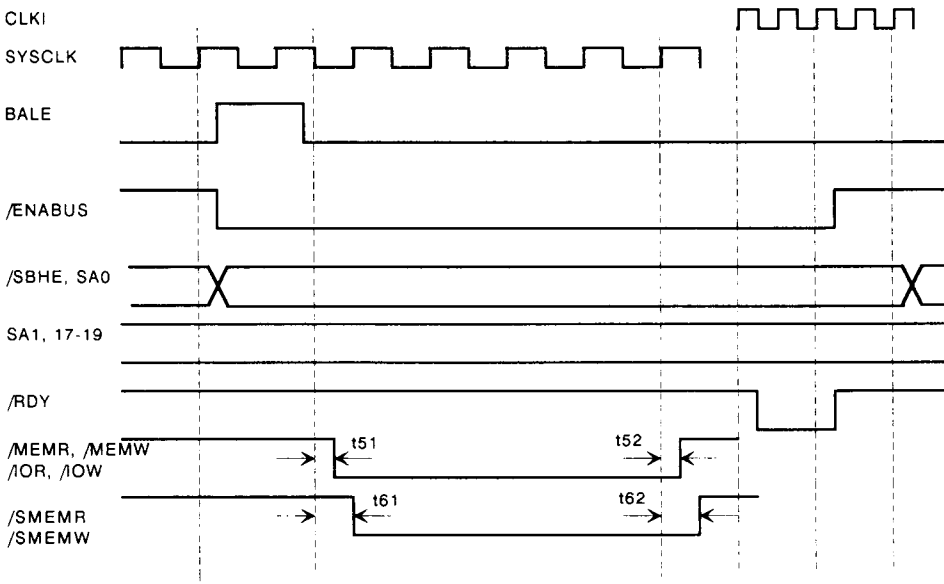


AT Bus 16 Bit Access Timing

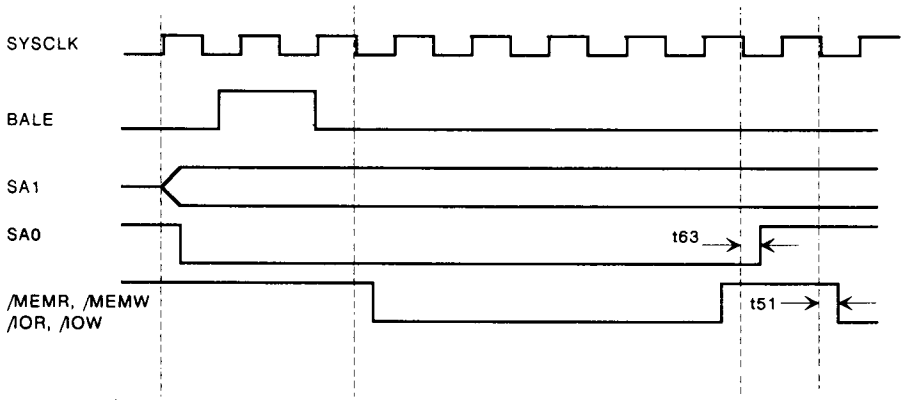


*/BEX indicates /BE0, /BE1, /BE2. and /BE3.

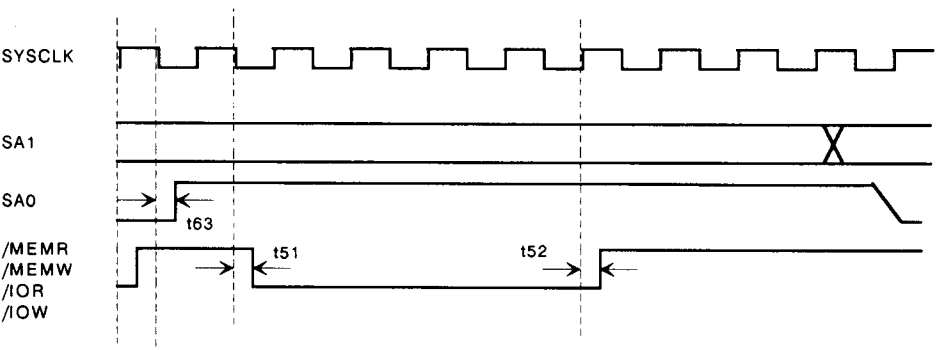
AT Bus 8 Bit Access Timing



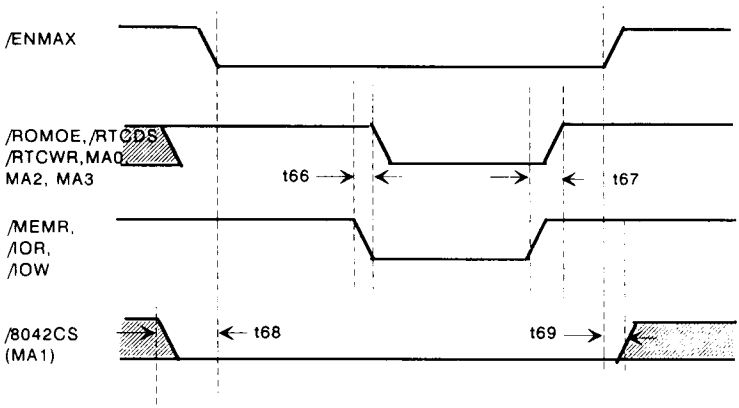
AT Bus Bus Cycle Conversion
(split in two lengthwise and continued as following diagram)



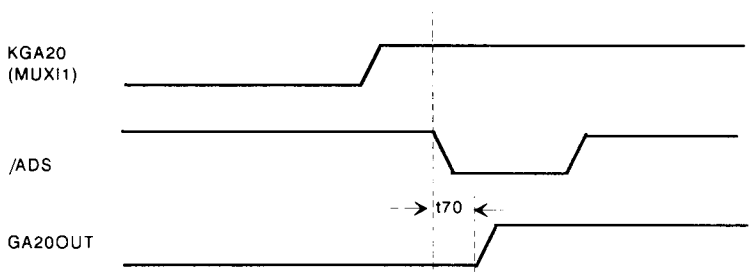
AT Bus Bus Cycle Conversion
(continued from previous diagram)



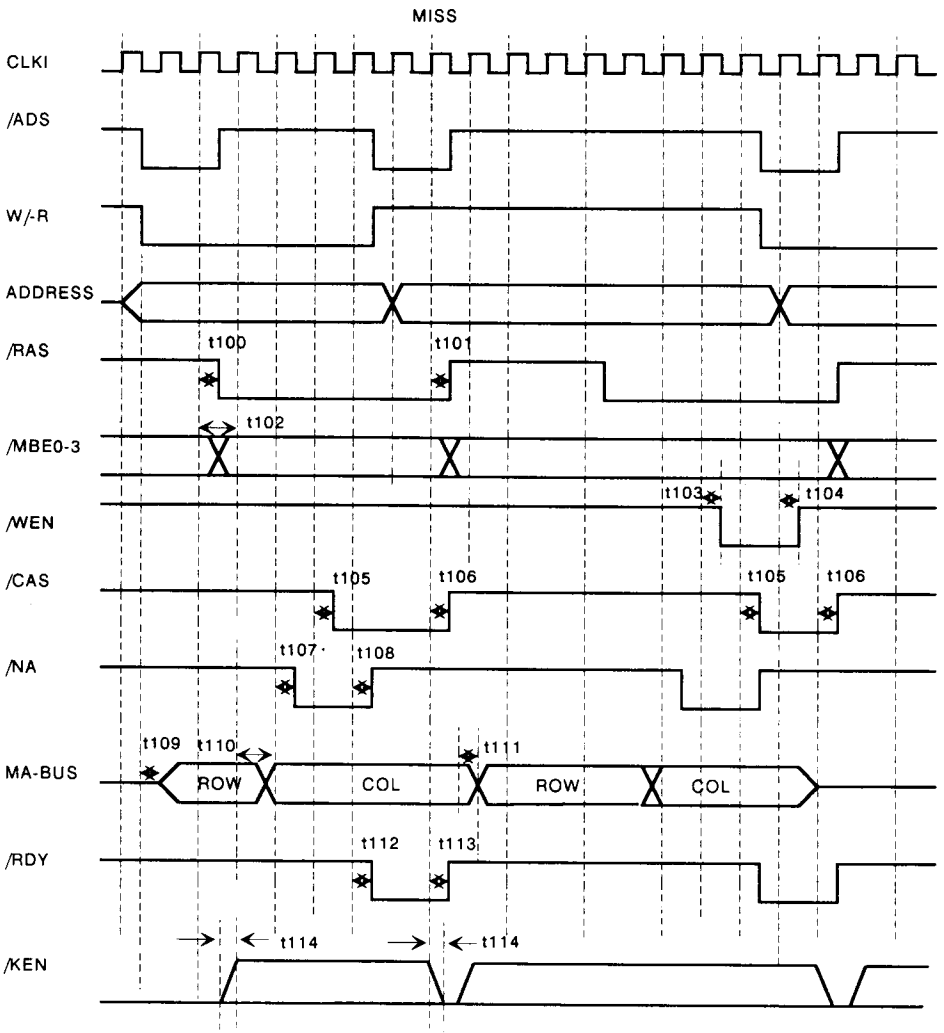
Decoding Signal Timing



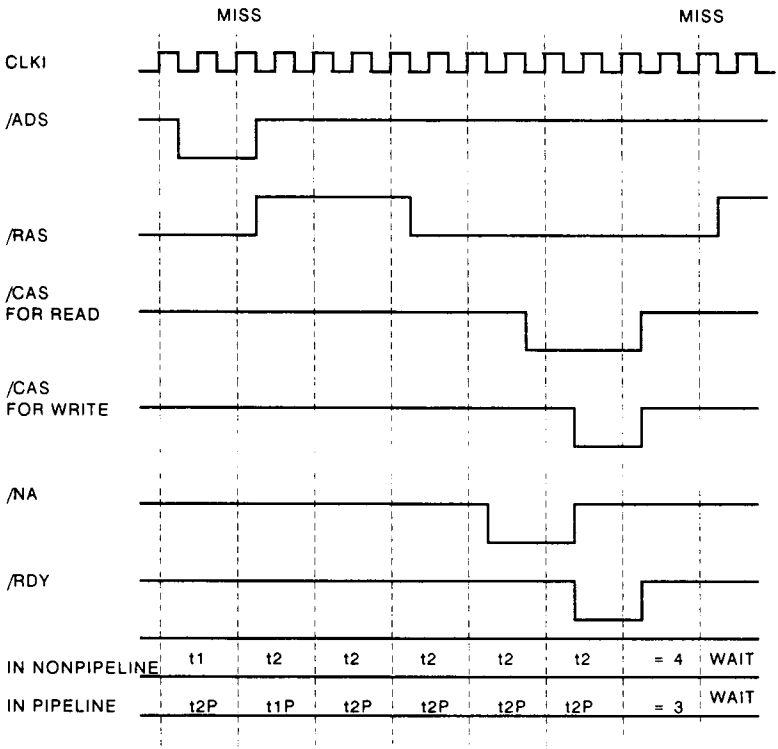
A20 Gate Timing



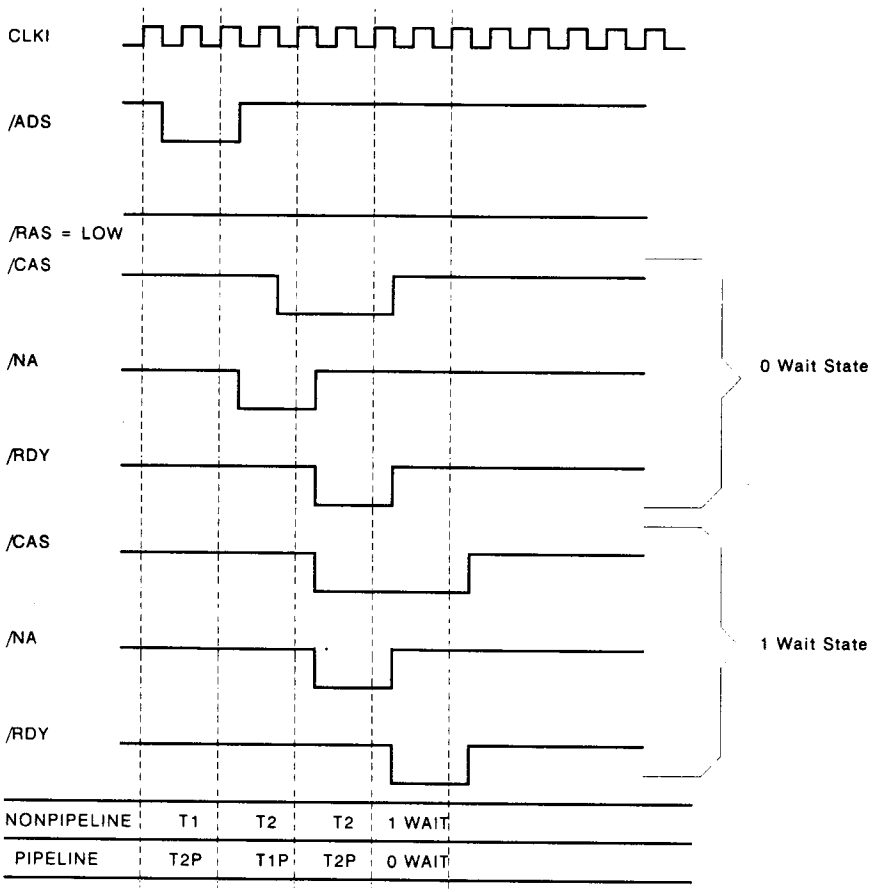
Page Interleaved Mode Local RAM Access
Page Miss Cycle 1



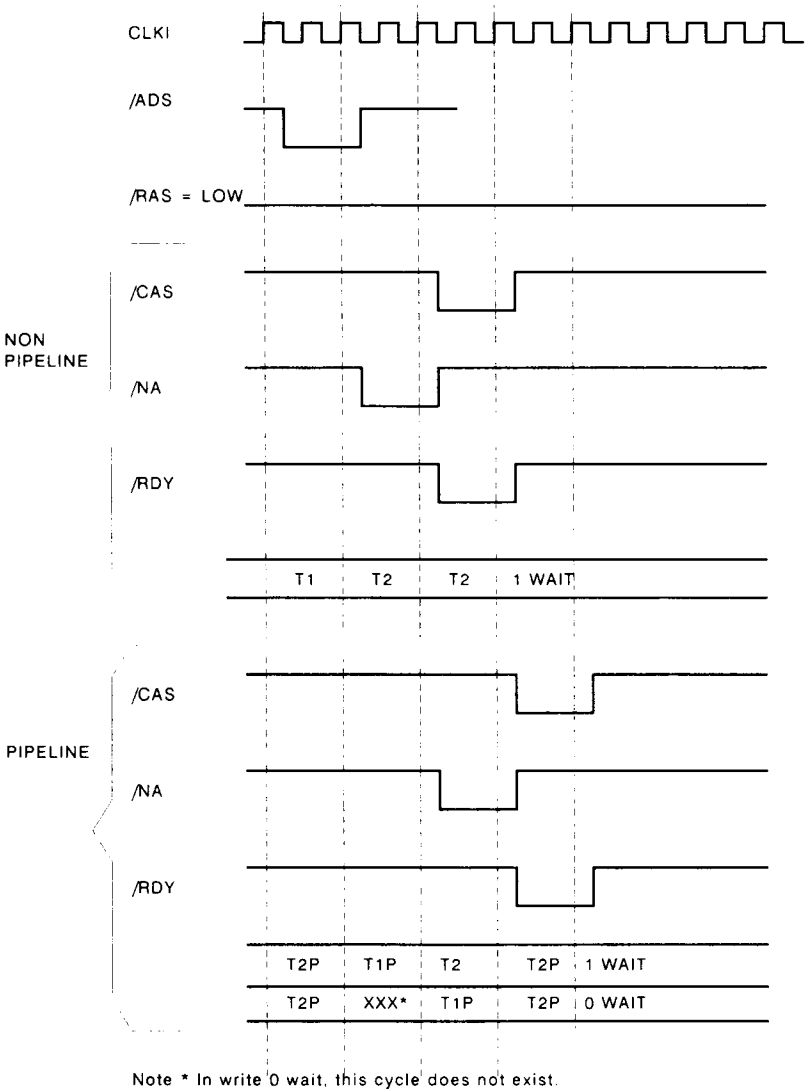
Page Interleaved Mode Local RAM Access
Page Miss Cycle 2



Page Interleaved Mode
Page Hit (Read) Cycle

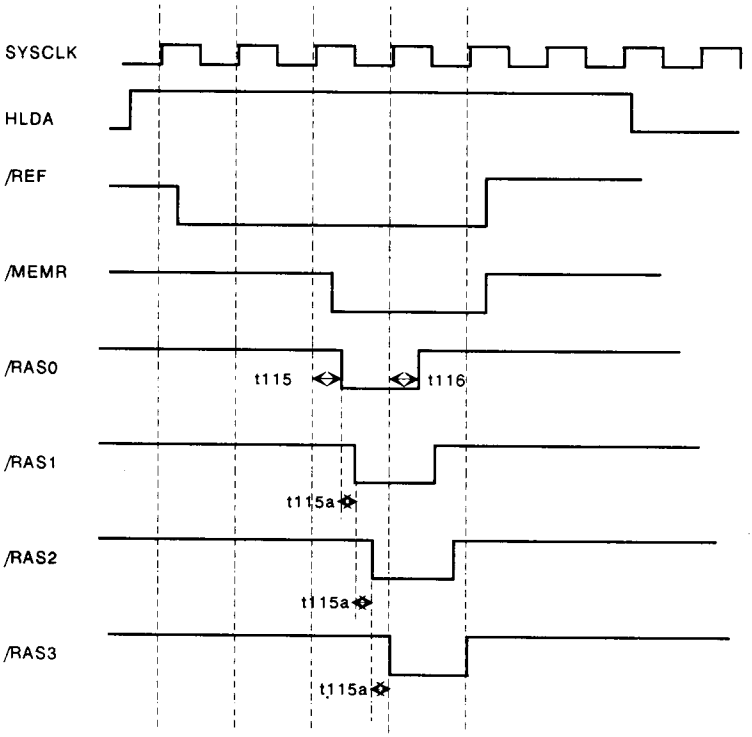


Page Interleaved Mode
Page Hit (Write) Cycle

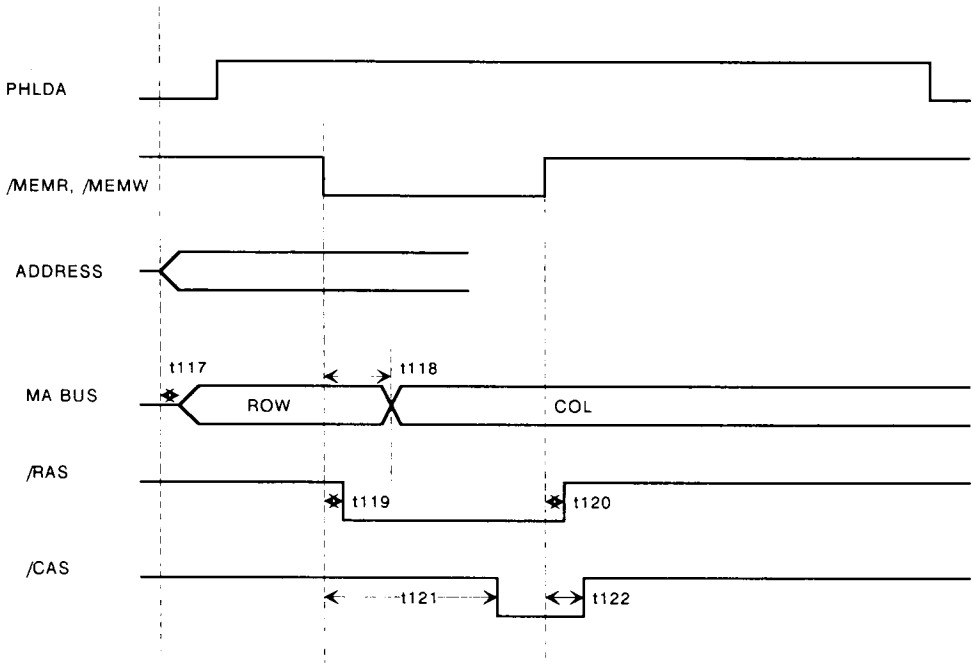


Note * In write 0 wait, this cycle does not exist.

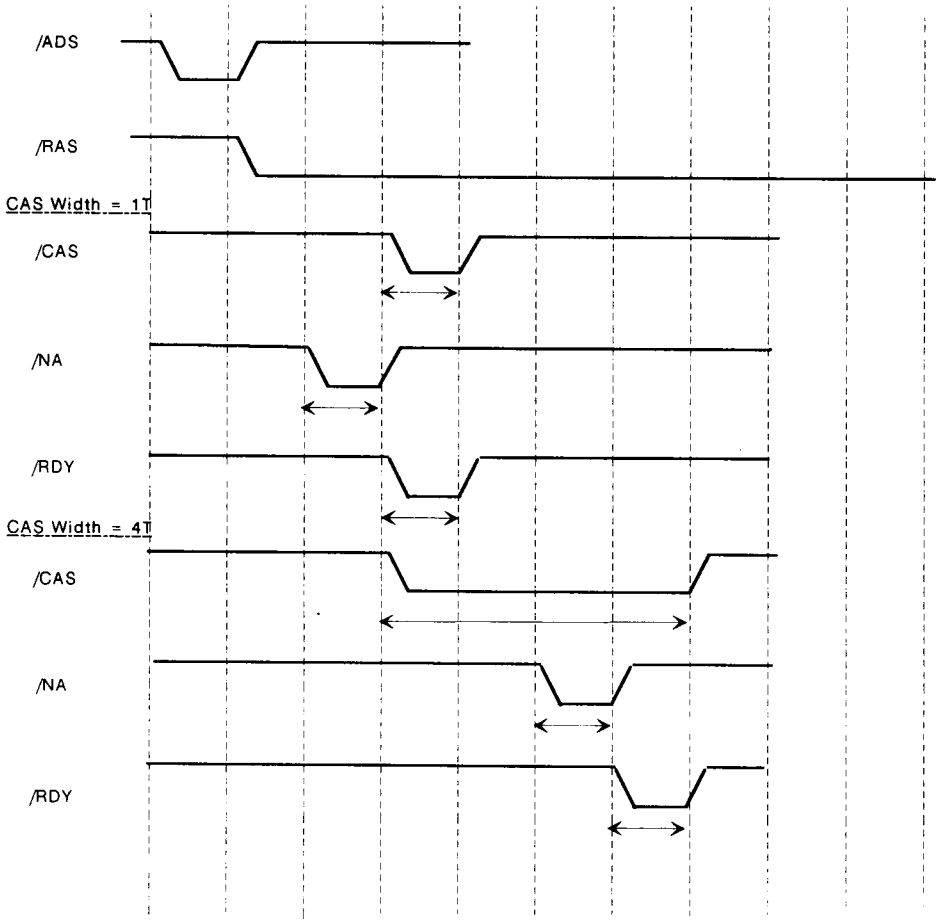
DRAM Refresh Timing



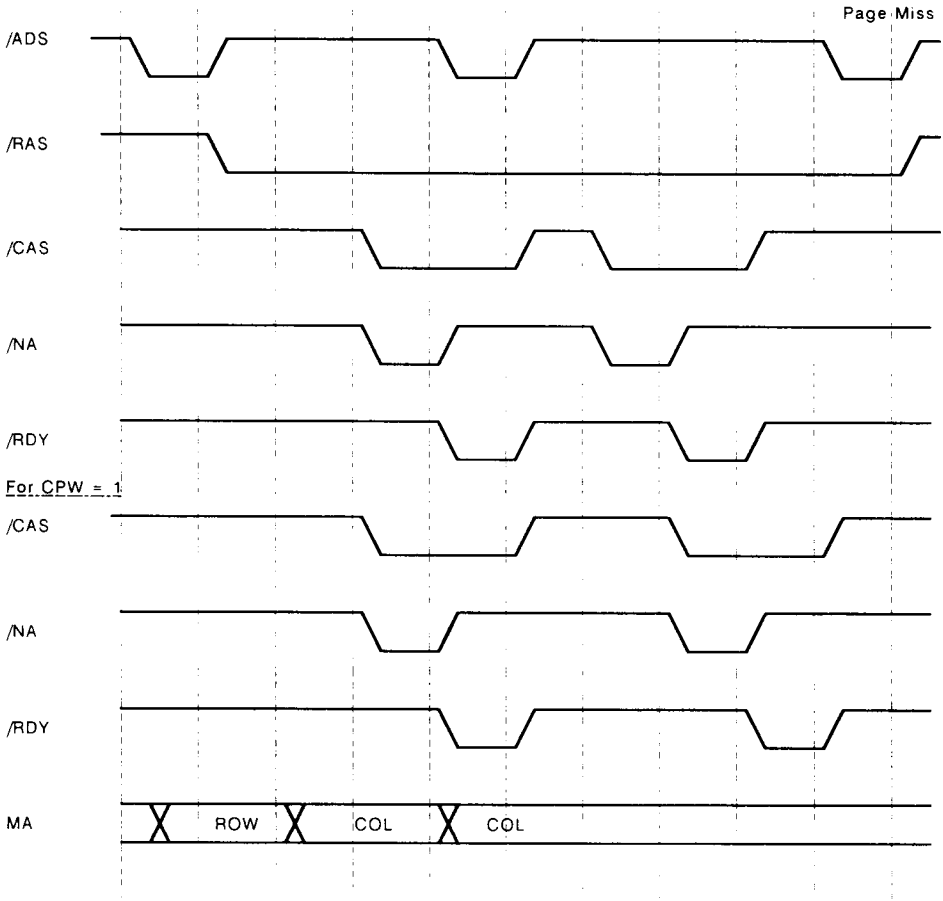
DMA DRAM Timing



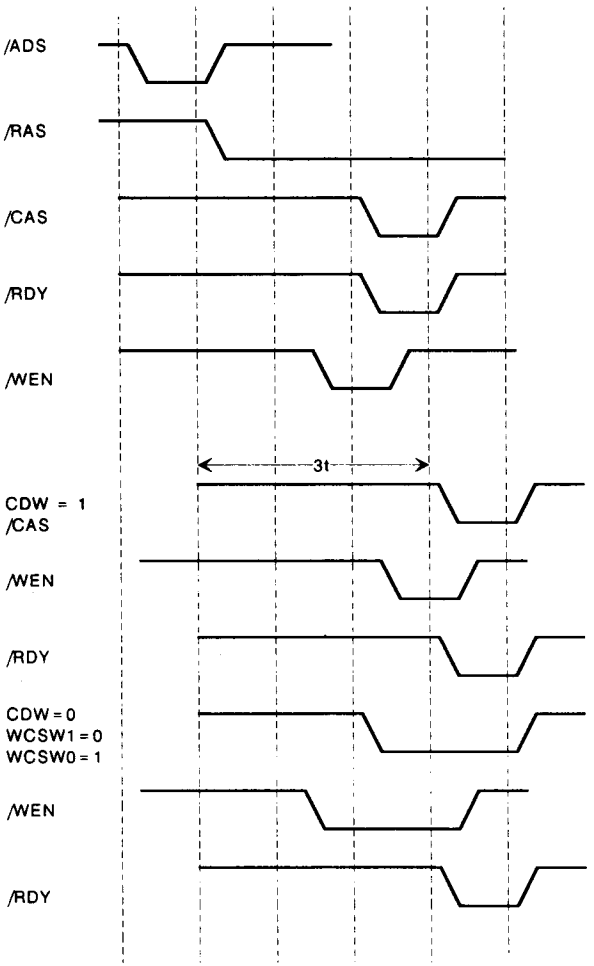
Page Mode Access Timing



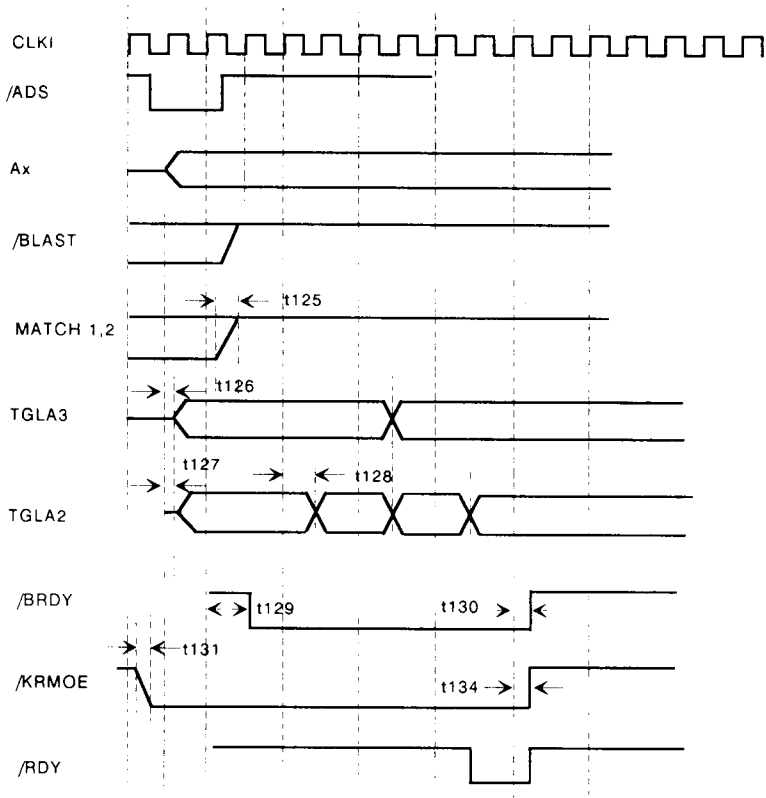
Page Mode Access Timing Wave Form



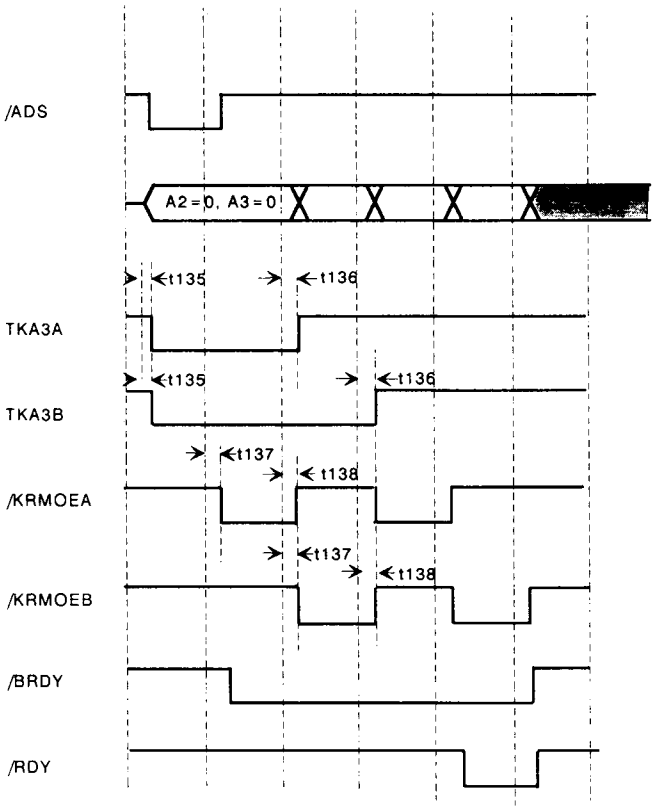
Page Mode Access Timing
Write Cycle Wave Form



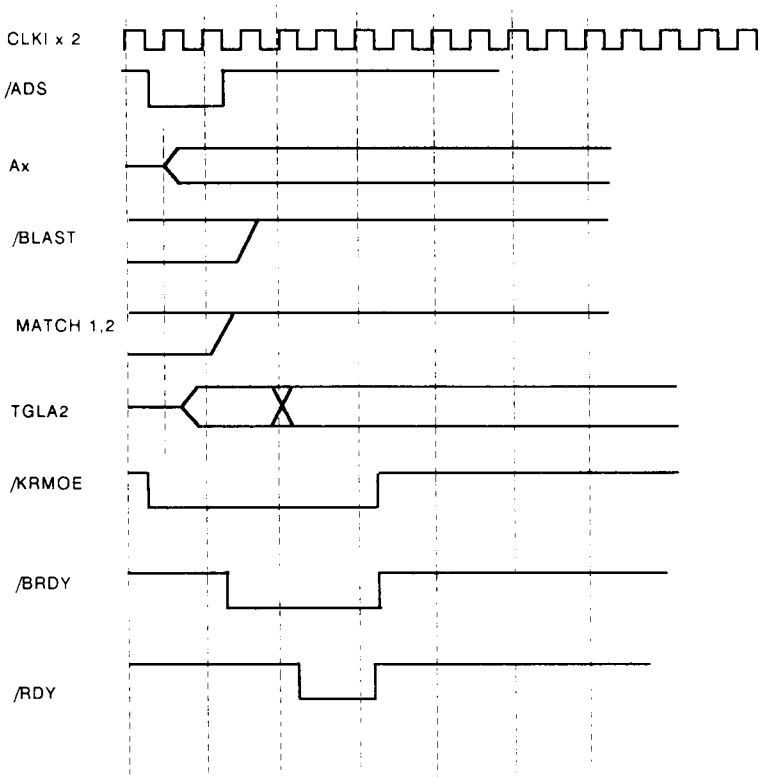
Cache Read Hit
Cache Burst (128 Bit) Line Double Phase



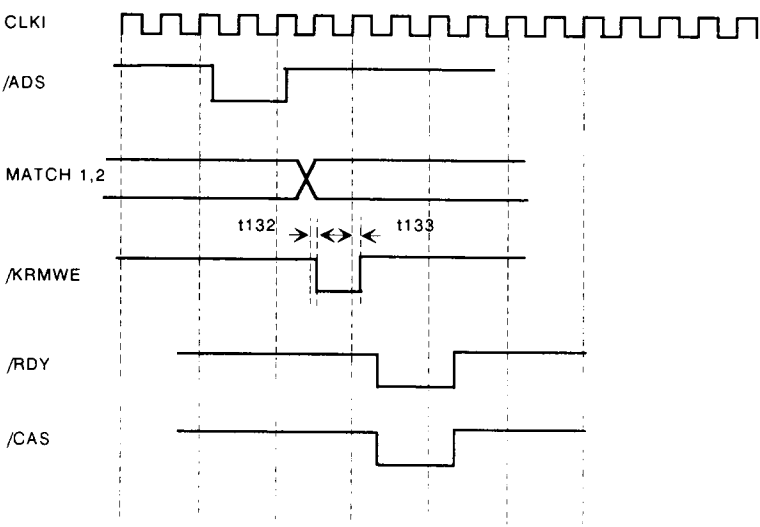
Cache Read Hit
Cache Burst (128 Bit) Line Single Phase



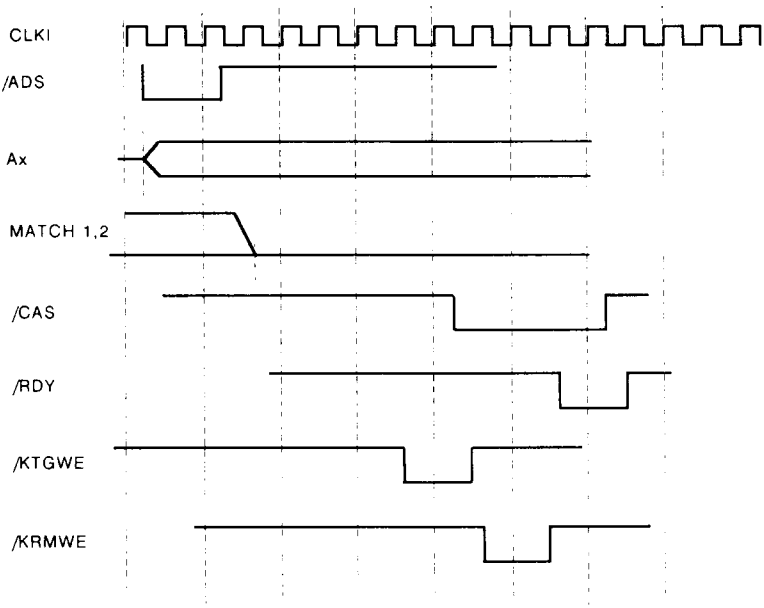
Cache Read
Cache Burst (64 Bit) Line



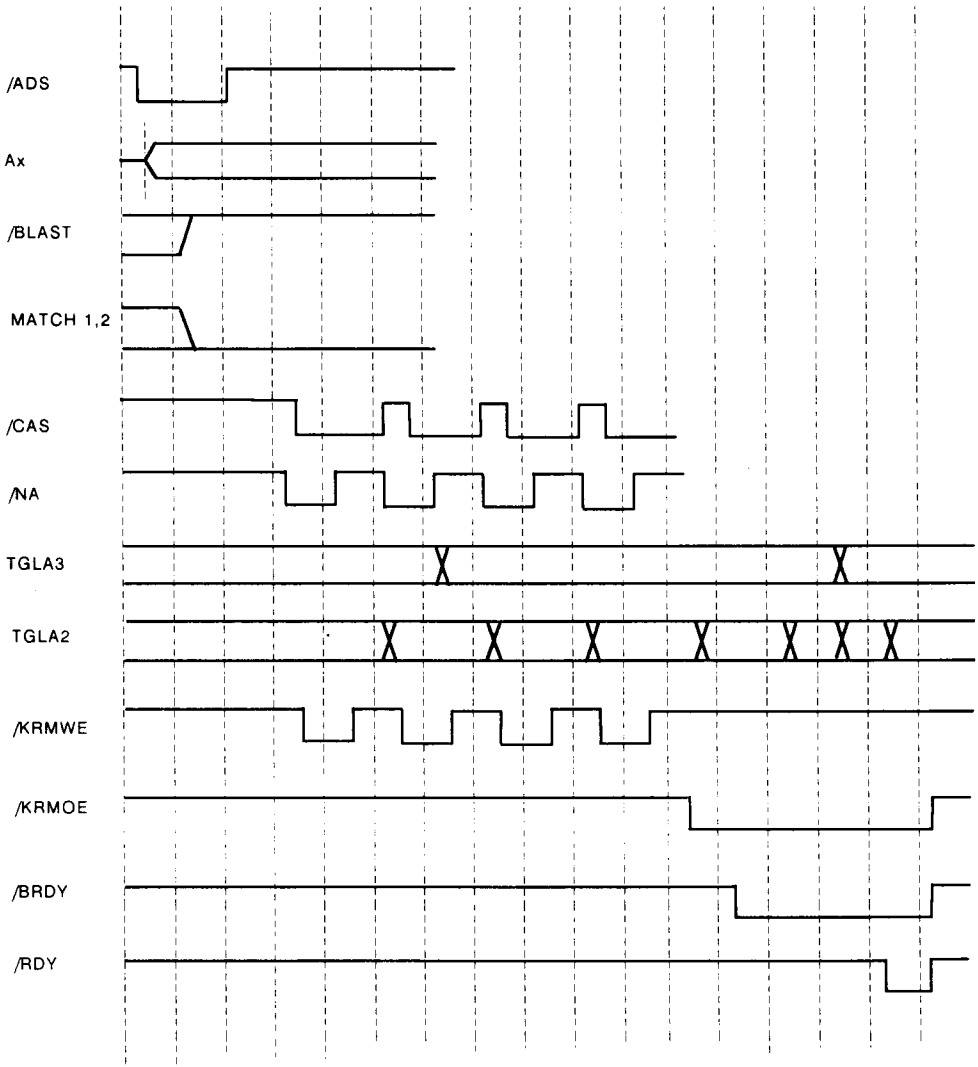
Cache Write Hit
DRAM Page Hit without Buffer Write



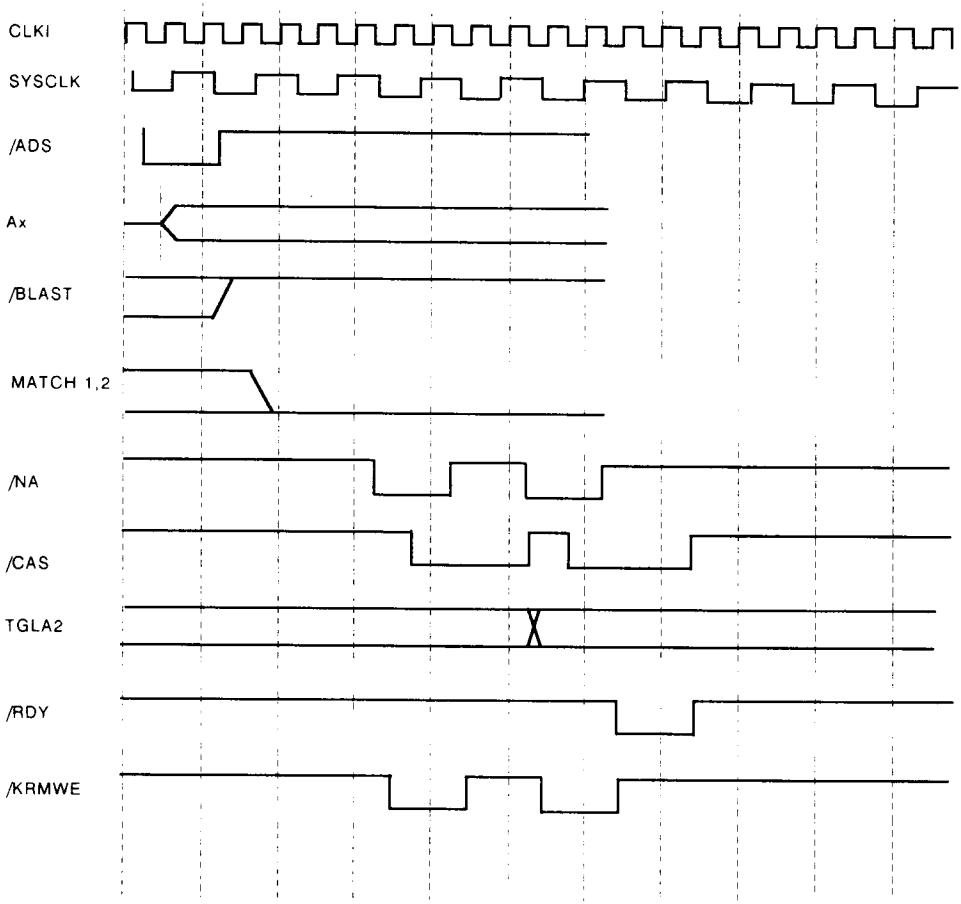
Cache Read Miss (32 Bit) Double Phase



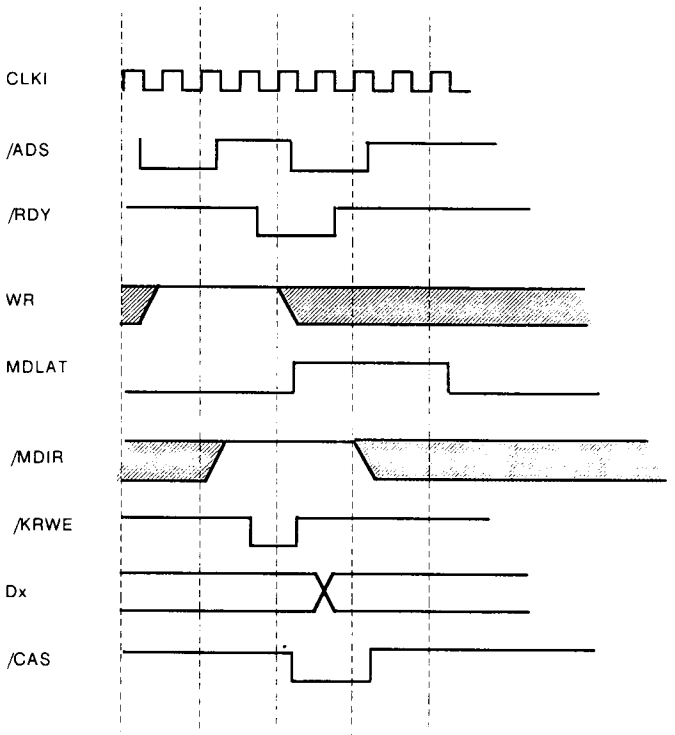
Cache Read Miss
RAM Burst in (128 Bit) Line Fill Double Phase



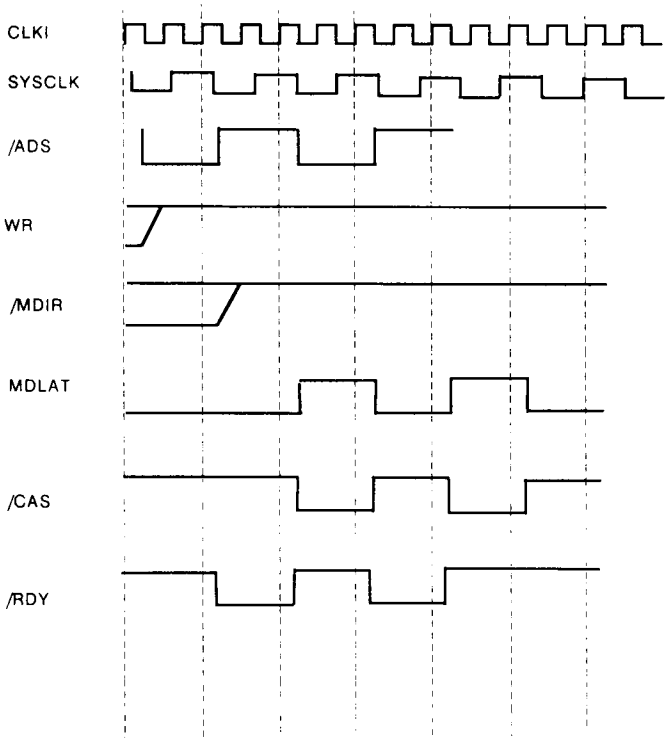
Cache Read Miss
RAM Burst in (64 Bit) Line Fill Double Phase



Cache Write Hit in Buffer Write
DRAM Page Hit



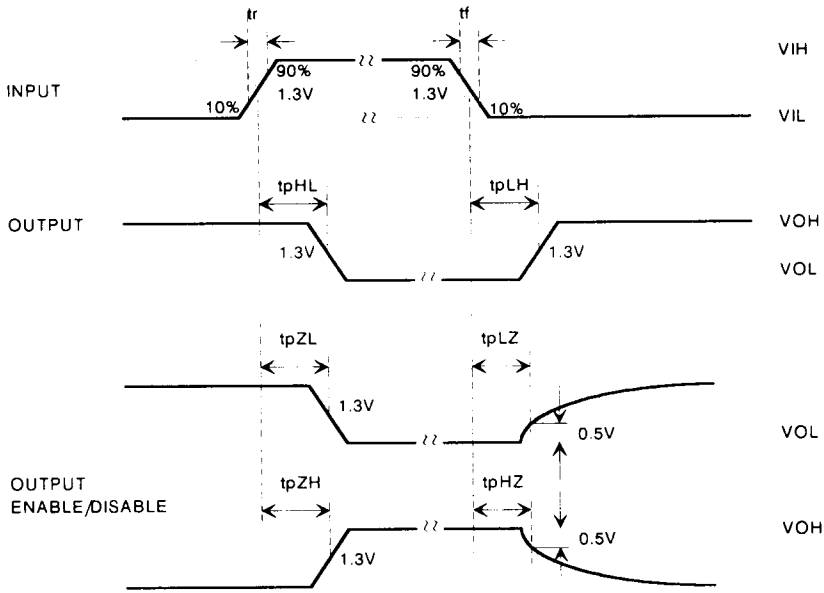
Buffered Write followed by a Write Cycle
DRAM Page Hit



Load Circuit and AC Characteristics Measurement

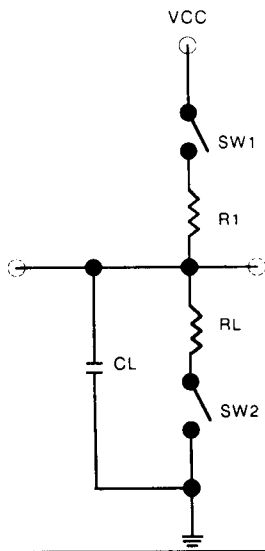
Parameter	Output Type	Symbol	CL(pF)	R1	RL	SW1	SW2
Propagation Delay	Totem pole 3-state	tPLH	100		1.0K	off	on
		tPHL	100		1.0K	off	on
Time	Bidirectional						
Propagation Delay time	Open drain or Open collection	tPLH	100	0.5K		on	off
		tPHL	100	0.5K		on	off
Disable time	3-state Bidirectional	tPLZ	100	0.5K	1.0K	on	on
		tPHZ	100	0.5K	1.0K	off	on
Enable time	3-state Bidirectional	tPZL	100	0.5K	1.0K	on	on
		tPZH	100	0.5K	1.0K	off	on

AC Characteristics Measurement



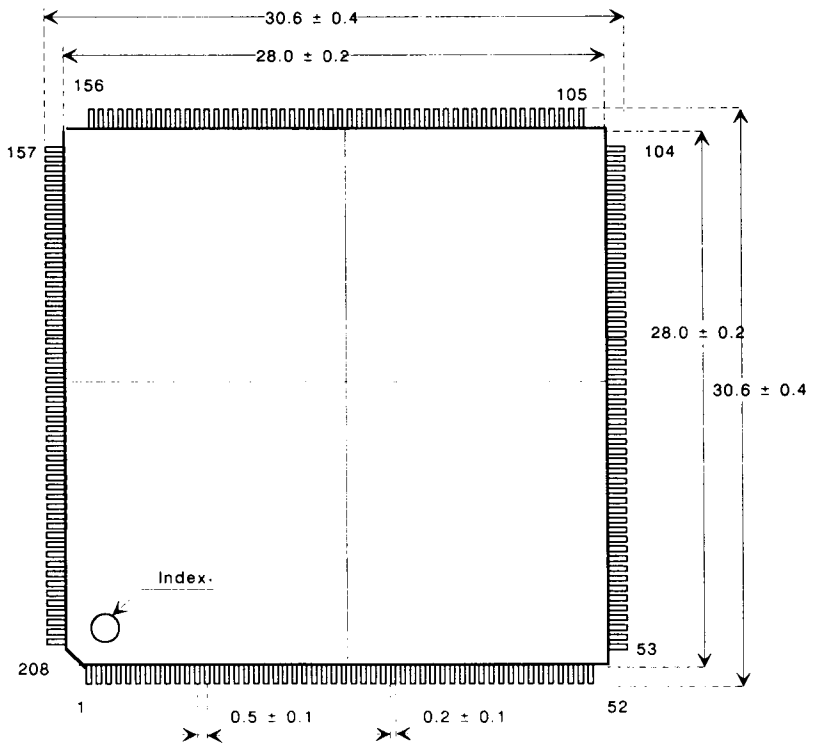
VIH = 3 V, VIL = 0, tr ≤ 10 ns, tf ≤ 5 ns

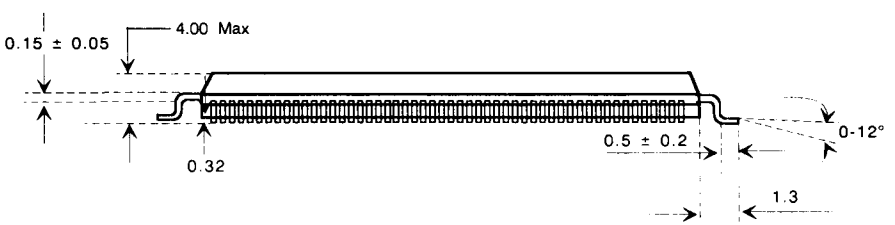
Load Circuit



Production Package Specification

Package: 208-pin PQFP
Unit: (mm)
Chip: 2046





ACC Microelectronics Corporation

2500 Augustine Dr.
Santa Clara, CA 95054
Phone: 408-980-0622 FAX: 408-980-0626

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