ACC MICRO

Single Chip Solution™ 2036

The Single Chip Solution™ 2036 integrates all the logic and high performance of a 386SX and 286 AT system into a single chip. It includes peripheral control logic, bus and memory control logic, and data and address buffer logic.

* 100% hardware and software compatible with the IBM PC/AT
* Fully compatible with

  Intel 8237 DMA controller
  Intel 8259 interrupt controller
  Intel 8254 timer/counter
  Intel 82284 clock generator
  Intel 82288 bus controller
  TI 74LS612 memory mapper
  ACC 82021 AT chipset

* Functions include

  7 DMA channels
  3 timer/counter channels
  14 external interrupt channels
  Advanced memory controller
  Power management features

* Supports 286 and 386SX micro- processors with up to 33 MHz system clock
* Supports 287 and 387SX coprocessors
* 4-way or 2-way page interleaved memory controller
* Direct Access Memory Controller
* Supports EMS 4.0
* Shadow RAM for BIOS and video
* Simultaneous EMS and shadow RAM
* Supports up to 512K EPROM
* Supports single 8-bit EPROM
* Supports 64Kx1, 256Kx1, 256Kx4, 1Mx1, 1Mx4, 4M x1 DRAM memories up to 16 MB
* Supports up to 8 banks of Memory
* Supports mixed type of DRAM memories from one bank to another
* On board 128K-640K RAM can be disabled
* Speed change via hardware or software
* Supports dynamic remapping of 640K through 1M memory range
* Supports pipelined mode operation
* Programmable wait states for ROM
* Built-in bus conversion logic for 16-bit to 8-bit transfers
* Quick software switch from protected mode to real mode for OS/2 optimization
* Programmable I/O address decoder
* Supports standby mode operation at as low as 1MHz
* Power-saving features:

  Selectable operating frequency.
  Unused RAS lines can be shut off.
  Optional slow DRAM refresh.
  Detect video display activities.
  CLKSER and CLK8042 can be shut off.

* Data and address buffers
* Parity bit can be disabled
* 1.0/0.8 micron high performance CMOS technology
* 208-pin PQFP package

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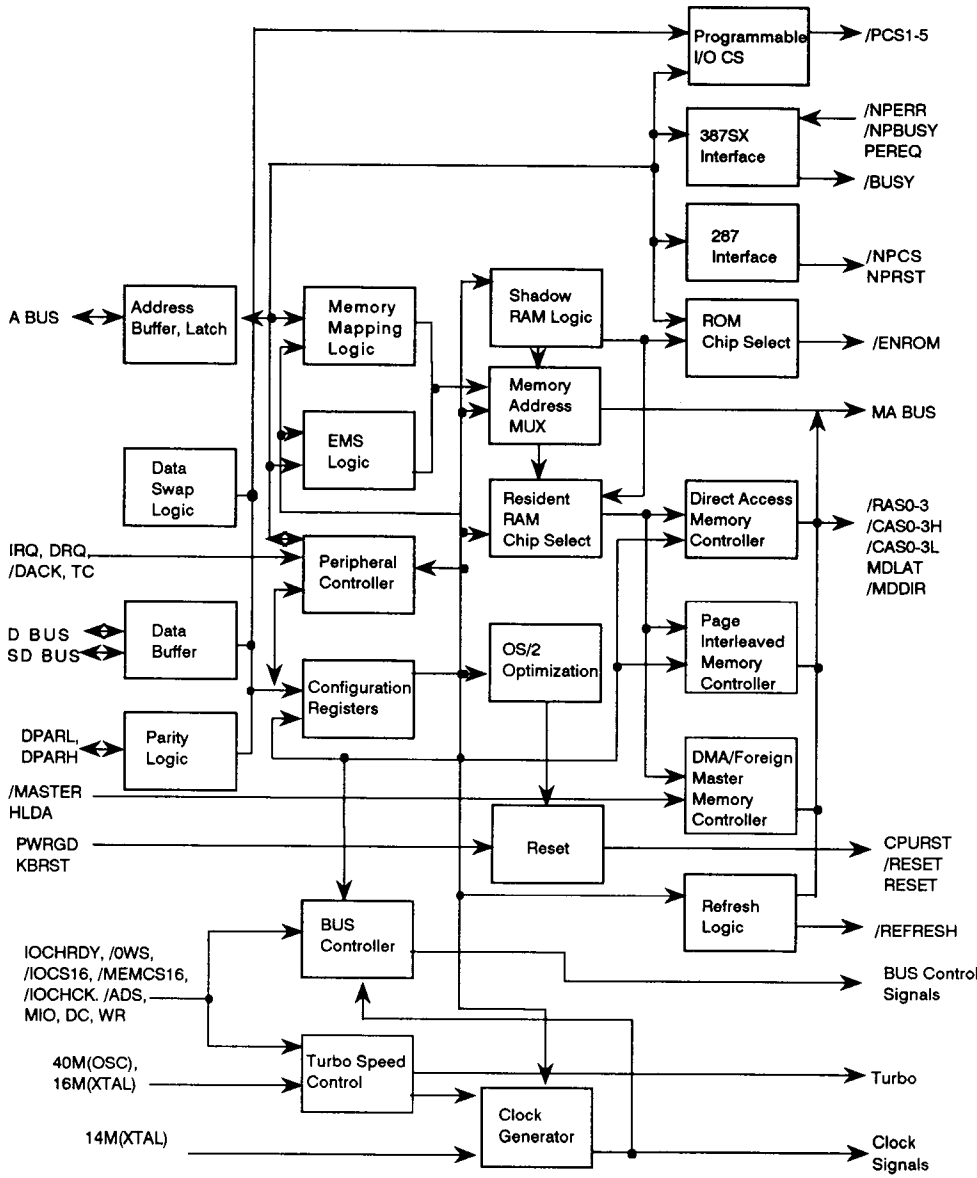
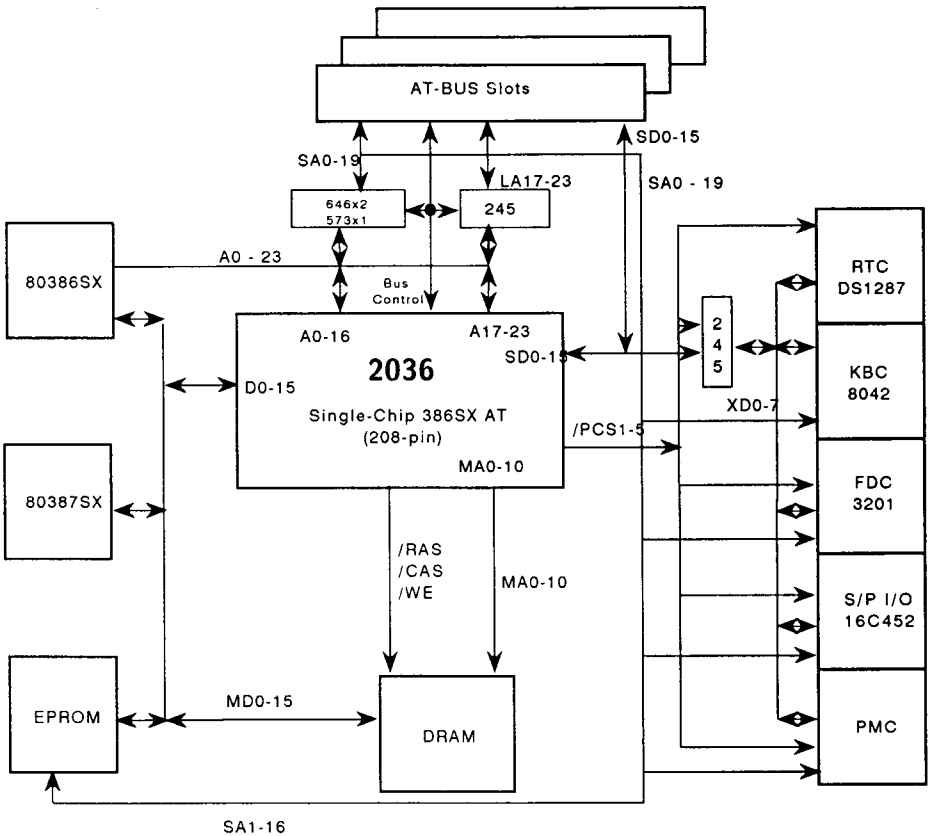
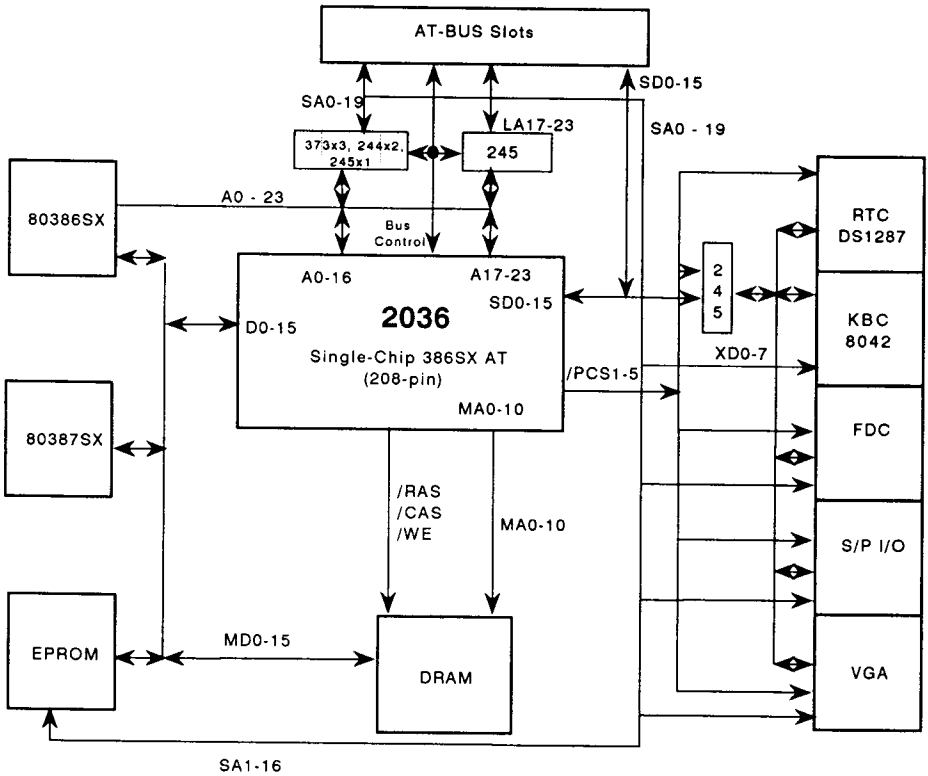
ACC Micro 2036 Block Diagram



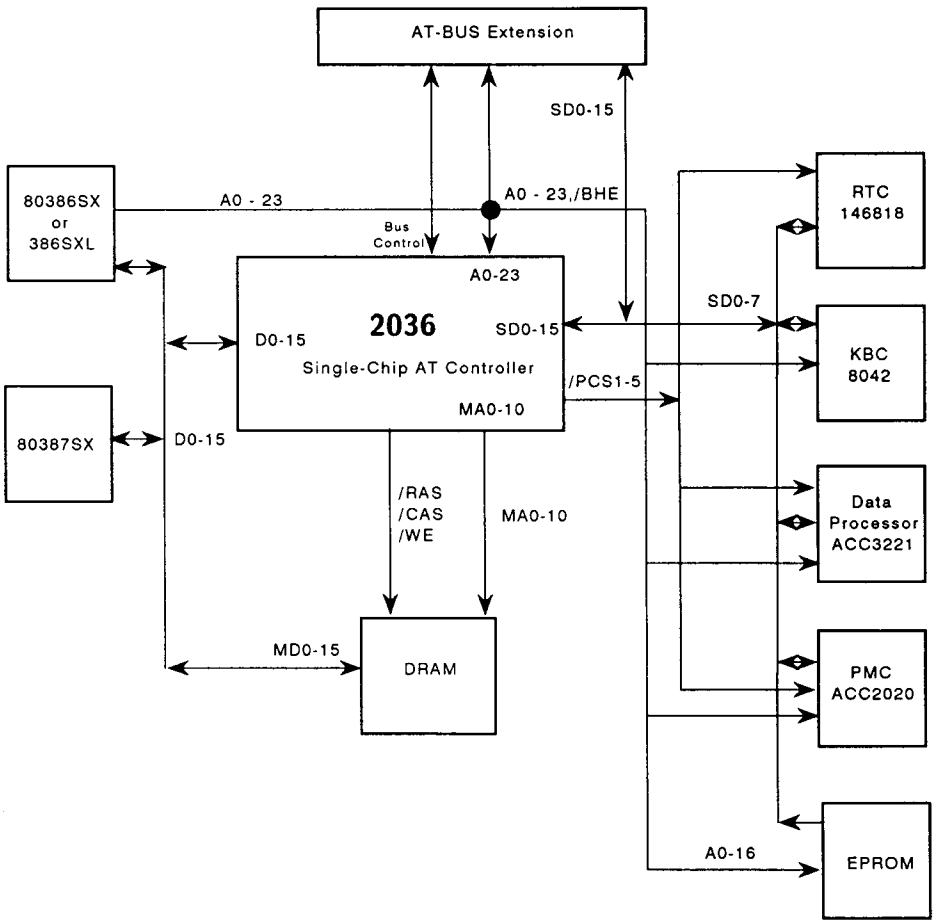
System Block Diagram
(386SX Desktop Computer Application)



System Block Diagram
(286 Systems Application)



System Block Diagram
(386SX Notebook Computer Application)



Functional Description

Interrupt Controllers

There are two programmable interrupt controllers for the 2036. They are fully compatible with Intel's 8259 controller, providing up to 15 interrupt sources (14 external and 1 internal). The internal line connects to the 8254 Counter 0 output.

These interrupt controllers prioritize interrupt requests to the CPU.

DMA

The 2036 has two DMA controllers, compatible with the Intel 8237, which provide a total of seven external DMA channels.

Combined with the Memory Mapper, each DMA channel has a 24-bit address output to access data throughout the entire 16 megabyte system address space. Channel 0 through channel 3 support 8-bit peripherals, transferring data to or from an 8 or 16-bit memory. Each channel can transfer data in 64 Kbyte pages. Channel 4 is used for cascading and is not available externally. Channel 5 through channel 7 support 16-bit I/O adapters, transferring data a word at a time. These channels can transfer in 128 Kbyte pages.

All address latching functions for DMA operation are done inside the 2036.

Features include

- Address increment or decrement.
- Seven independent DMA channels with independent auto initialization for each channel.
- Each DMA request can be controlled individually to enable or disable.

Memory Mapper

The 2036 has equivalent logic to the 74LS612, generating the upper address bits during a DMA cycle.

Source Memory Mapper		8237
	(for DMA Channels 0 - 3)	
Address	A23 ⟷ A16	A15 ⟷ A0
	(for DMA Channels 5 - 7)	
Address	A23 ⟷ A17	A16 ⟷ A1

Timer/Counter

The 2036 provides three internal counters which are compatible with the 8254. The clock input for each counter is tied to a clock of 1.19 MHz, which is derived by dividing the

14.318 MHz crystal input by 12. The output of Counter 0 is connected to the IRQ1 input of interrupt controller 1. Counter 1 initiates a refresh cycle and Counter 2 generates sound waveforms for the speaker.

Features:

- Three independent 16-bit counters
- Count binary or BCD

2036 I/O Address Map

The 2036 I/O address decode is fully compatible to the IBM PC/AT requirements. The 2036 has more fully decoded the I/O address range from 000 to 0FF (refer to the 2036 I/O address map table) to allow users to use the I/O areas not used by the IBM PC/AT.

2036 I/O Address Map Table

Hex Range	Device
000-00F	DMA controller 1, 8237A-5
020-021	Interrupt controller 1, 8259A,Master
040-043	Timer, 8254
060-064	8042 (Keyboard)
070-071	Real-time clock, NMI (non-maskable interrupt) mask
080-08F	DMA page register, 74LS612
092	Alternative Gate A20 and FAST RESET Register.
0A0-0A1	Interrupt controller 2, 8259A
0C0-0DF	DMA controller 2, 8237A-5
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F2	2036 Configuration Register Index
0F3	2036 Configuration Register Data
0F8-0FF	Math Coprocessor

PIO

The PIO is the system configuration to control the speaker port. It also has circuitry to detect refresh. This condition can be read back as Bit 4 of I/O Port 61h.

Refresh Generation Logic

Refresh circuitry contains an 8-bit counter for address SA0-7 during a refresh. In addition, two more address counter bits are present inside the 2036 to support refresh for DRAMs up to 4M bits.

Refresh/DMA Arbitration Logic

The 2036 contains circuitry to control a refresh cycle.

There are two possible sources for a hold request to the CPU. Either the DMA controller issues a hold request or the output of Counter 1 in the 8254 makes a low to high transition. The HOLD line is active when either source is requesting a hold. The hold request from the DMA controller is sampled on the rising edge of the DMA clock and the request from the timer is sampled on the falling edge of the DMA clock.

If the DMA controller's hold wins the arbitration, the HOLD is asserted, and it waits for a signal back from the CPU. When the DMA controller is finished, it negates its hold request signal to the arbiter. The arbitration then switches to a REFRESH cycle if there is a pending hold from the Counter/Timer, otherwise the arbiter inactivates the HOLD line and returns control to the CPU.

If a refresh cycle wins the arbitration, the HOLD is asserted and the 2036 pulls the /REFRESH pin low. /REFRESH remains low for four SYSCLK rising edges. On the fourth

rising edge of SYSCLK, the HOLD line is inactivated. However, if there is a pending hold request from the DMA controller on the fourth rising edge of SYSCLK, the REFRESH cycle is extended for one more SYSCLK cycle. The hold request arbiter then acknowledges the hold request from the DMA controller.

NMI and Port B Logic

The 2036 contains non-maskable interrupt (NMI) signal generation logic. An NMI can be caused by an I/O error or by a parity error. Port B indentifies the source of the error. At power up, the NMI signal is masked off. NMI is enabled by writing to I/O address 070 hex with Bit 7 low; NMI is disabled by writing to I/O addresss 070 hex with Bit 7 high.

Bus Controller and Converter

The 2036 CPU bus controller is functionally equivalent to Intel's 82288 multi-bus adapter, providing CPU bus and signal control for both system and peripheral buses. The D/-C, W-R and M/-IO signals carry data from the CPU, announcing a bus cycle and defining its type. Table 1 lists and defines the different types of bus cycles.

Table 1.1a ACC Micro 2036 386SX Bus Cycle Definitions

/ADS	M/-IO	D/-C	W-R	Bus Cycle Initiated
0	0	0	0	Interrupt acknowledge
0	0	0	1	Does not occur.
0	0	1	0	I/O data read.
0	0	1	1	I/O data write.
0	1	0	0	Memory code read.
0	1	0	1	Halt if A1=1; shut down if A1=0.
0	1	1	0	Memory data read.
0	1	1	1	Memory data write.

Table 1.1b ACC Micro 2036 286 Bus Cycle Definitions

COD, /INTA	M/-IO	/S1	/S0	Bus Cycle Initiated
0 (low)	0	0	0	Interrupt acknowledge
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	Not a status cycle
0	1	0	0	If A1=1, then halt; else, shutdown
0	1	0	1	Memory data read
0	1	1	0	Memory data write
0	1	1	1	Not a status cycle
1 (high)	0	0	0	Reserved
1	0	0	1	I/O read
1	0	1	0	I/O write
1	0	1	1	Not a status cycle
1	1	0	0	Reserved
1	1	0	1	Memory instruction read
1	1	1	0	Reserved
1	1	1	1	Not a status cycle

The CPU bus controller has four operation modes.

AT CPU Mode

This mode is active when HLDA is low. The CPU bus controller generates /IOR, /IOW, /INTA, /MEMR, and /MEMW signals.

DMA Mode

DMA mode is active if HLDA and AEN are active. The DMA controller drives the /IOR, /IOW, /MEMR, and /MEMW signals.

Refresh Mode

Refresh mode is active when HLDA and /REFRESH are active. /MEMR becomes active at this time to perform a refresh on both AT bus and local DRAM.

Master Mode

Master mode is active when HLDA is active and a card in the AT slot pulls /MASTER low. The card controls system address, data line and control line.

Bus Conversion

The 2036 contains logic to convert between 16-bit and 8-bit data accessing. During a bus conversion cycle, the AT bus command strobe (/MEMR, /MEMW, /IOR, or /IOW) is activated two times.

287 Interface Control

Additional circuitry supports the decoding required to select and reset the numeric coprocessor. /NPCS is a chip select decoded at addresses 0F8-0FF hex. The NPRST signal resets the math coprocessor. NPRST is activated by a system reset or by performing a write operation to I/O port 0F1 hex.

80387SX Interface Control

The 80387SX interfaces directly to the 80386SX with the error-reporting logic built in the 2036. A coprocessor error is sent to the 2036, generating an interrupt request to the CPU, followed by a service request. A write operation to I/O port 0F0 will clear the interrupt request.

Clock Generator

The 2036 Clock Generator provides clock signals to support internal and external timing requirements. It provides clock outputs for the CPU, the NPU, the Keyboard Controller, and the UART. Clock signals are generated from three clock sources. X14M1, X14M2, X16M1, and X16M2 are inputs for 14.318 MHz and 16 MHz crystal oscillators respectively. CLKIN is the doubled clock input for running the CPU in turbo mode. This pin is driven by an external oscillator. The 14.318 MHz input is used to derive clocks for the NPU, and the UART, as well as providing the OSC signal for the AT bus.

Turbo Speed Control Logic

The CPUCLK frequency can be switched between CLKIN and one other lower speed signal, X16M. The frequency switch can be generated through either hardware or software.

A SPDSW pin is provided to support a front panel turbo speed switch. SPDSW high selects CLKIN as the CPU clock. When that occurs, the TLED output sinks current to engage a turbo mode LED on the front panel. SPDSW low selects normal mode clock, X16M.

Configuration register 21h, bit 4, is the turbo mode select bit. If this bit is programmed to 1, the system is set at Turbo mode (CLKIN clock). If this bit is set to 0, the system is set at normal mode (X16M clock). The default value for this bit is zero.

For power conservation, a standby mode clock control is provided. A system needs to pre-select the standby mode available (set bit 4 of configuration register 35h = 1) first, then an intelligent BIOS will monitor the activity of the system. If all pre-defined conditions of the standby mode are satisfied, the system will go into the standby mode by pulling down the /LOSPD pin or set the bit 3 of configuration register 35h to 1.

The standby mode operating frequency can be pre-set by programming bit 4 and bit 3 of configuration register 33h. The standby frequencies are set as following:

Bit 4	Bit 3	Frequency
0	0	8 MHz
0	1	4 MHz
1	0	2 MHz
1	1	1 MHz

Table 1.2 DRAM Speed Selection Guide

	Page Interleaved		Direct Access (1WS)		Direct Access (0WS)	
	1M/4M	256K	1M/4M	256K	1M/4M	256K
33 Mhz	60	53	---	---	---	---
25 MHz	70	60	60	---	---	---
20 MHz	100	80	70	60	40	---
16 MHz	120	100	85	80	57	57
12.5 Hz	<150	150	120	100	80	80
10 MHz	<150	<150	150	120	100	100

Memory Controller

The Memory Controller is a key feature of the 2036. This versatile circuit provides complete control of up to 16 megabytes of system DRAM. In any control mode, it generates up to eight Row Address Strobes (/RAS0-7) and one Memory Write Enable signal (/WEN). The Memory Controller also provides the interface to transfer control to a DMA controller or an AT Bus master.

Memory Control Modes

The 2036 features two memory control modes: Page Interleaved Mode and Direct Access mode. These options provide flexibility and optimize system performance.

Page Interleaved mode has system performance, approximately 0.4 to 0.7 average wait states, but operate with slower and less expensive DRAM.

Table 1.2 lists the minimum access time required by a DRAM for each of the two memory control modes. This table presents the varying requirements relative to CPU speed and memory type. The most appropriate combination of CPU speed, DRAM speed, and memory control mode can be selected based on the system's application, depending on speed and cost requirements. Whatever the requirement, the 2036 is designed to provide maximum flexibility and optimum system efficiency.

Page Interleaved Memory Controller

The 2036 implements a 4-way, 2-way, and 1-way page interleaved memory controller, providing optimum system performance for high speed CPUs. This option offers near Direct Access performance (approximately 0.4 to 0.7 wait state average), while operating with a slower and less expensive DRAM. The Page Interleaved Memory Controller operates on two principles: Page Mode Memory access, which is much faster than random access, and the sequential and localized patterns it follows.

The Page Interleaved Memory Controller organizes the memory array into interleaved pages by banks, operating up to four banks simultaneously in Page mode. Each bank of memory consists of 18 bits of DRAM (two 8-bit bytes plus two parity bits).

The size of a memory page is determined by the type of DRAM installed. A 256K DRAM provides a page size of 1K bytes (512 column bits per DRAM row times 16 DRAMs per bank), 1M DRAM provides a 2K byte page size, and 4M DRAM provides a 4K byte page size. These page sizes are a result of the physical architecture of the DRAM. Once page mode is selected, a row can be kept active (/RAS low) almost indefinitely (up to 10uS), allowing any number of column accesses along that same row. Each row, and any intersecting column access along that same row, is defined as a "Page Hit." This results in a zero wait state access. If any subsequent memory access selects a new row, it is defined as a "Page Miss" and results in a three wait state access.

The organization and operation of the memory array is dependent on the type and quantity of memory installed (See "Configuration Registers" section). Memory performance is improved when a greater number of open pages, up to four, are used. This provides a larger and more flexible "zero wait state" work space. The open page on each bank retains the last row address selected on that particular bank.

The 2036 offers flexible memory bank configurations supporting one bank, two banks, four banks, six banks, and eight banks. When more than four banks of memory are

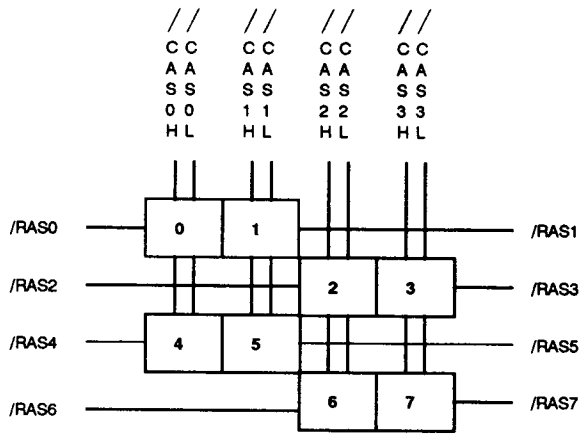


Figure 1.1 ACC Micro 2036 Memory Bank Configurations

installed, Banks 0 and 4, 1 and 5, 2 and 6, and 3 and 7 are paired so that CAS lines can be shared. This means that only one bank of each pair can be active at any given time. For example, if six banks of memory are installed, Banks 0 and 4, and Banks 1 and 5 share the same CAS lines. Banks 2 and 3 have their own CAS lines. The four simultaneously open pages can reside in either banks 0, 1, 2, 3, banks 0, 5, 2, 3, banks 4, 1, 2, 3, or banks 4, 5, 2, 3 while in the 4-Way Page Interleaved mode.

Direct Access Memory Controller

The Direct Access Memory Controller provides the highest level of system performance for slower systems in the 8, 10, 12.5, 16, and 20 MHz range. Direct Access initiates all CPU cycles to system RAM, with one or zero wait states. When memory access is under the control of the DMA Controller or AT I/O Bus, process time is slower, but this seldom occurs.

Memory Mapping

Memory Mapping translates system RAM within the 640 KB to 1MB range, which cannot be accessed normally, to an accessible address range, above the physical RAM space.

Memory address space between the 640 KB to 1MB range, which is reserved for system ROM and BIOS application, cannot be used to access physical DRAM. Memory Mapping translates physical RAM space within the 640 KB to 1MB range to memory addresses above the actual installed memory size. For example, if 4 MB of memory are installed, and the memory mapping feature is on, the DRAMs in the 640 KB to 1MB range are mapped to an address above 4 MB.

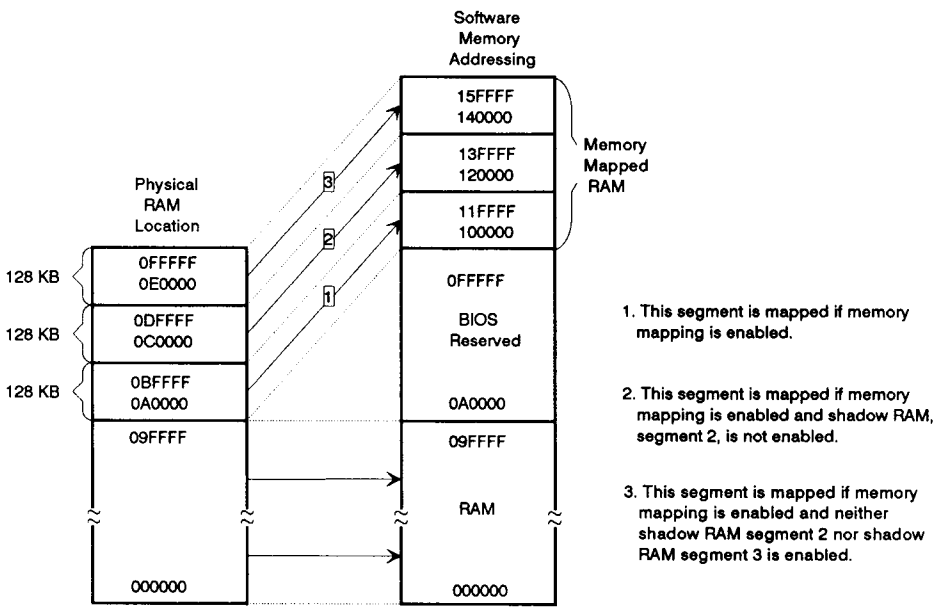


Figure 1.2 Memory Mapping for a 1 MB System

Memory Mapping is enabled by a bit in the configuration registers. When Shadow RAM is enabled simultaneously with Memory Mapping, the quantity of RAM available for Memory Mapping is reduced. If Shadow RAM segment 3 is enabled, 256 KB of RAM can be mapped. If Shadow RAM segment 2 is enabled, only 128 KB of RAM can be mapped. See Figure 1.2 for the memory mapping involved in a 1MB system and Figure 1.3 for a 2 MB system.

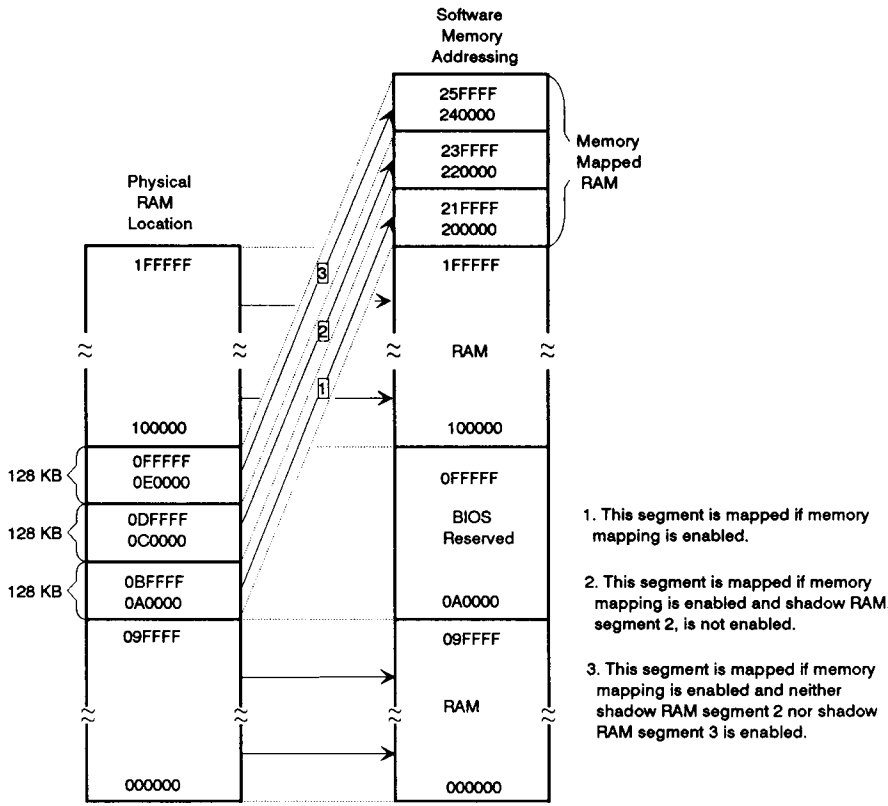


Figure 1.3 Memory Mapping for a 2 MB System

512K Memory Remapping

The 2036 supports 640 KB or 512 KB of base memory when 1 MB is configured. When configuration register 22, bit 4 is set to one, the system will be set to have 512 KB of base memory and will remap the other 512 KB above the 1 MB area. See Figure 1.4 for 512 KB memory mapping above 1 MB.

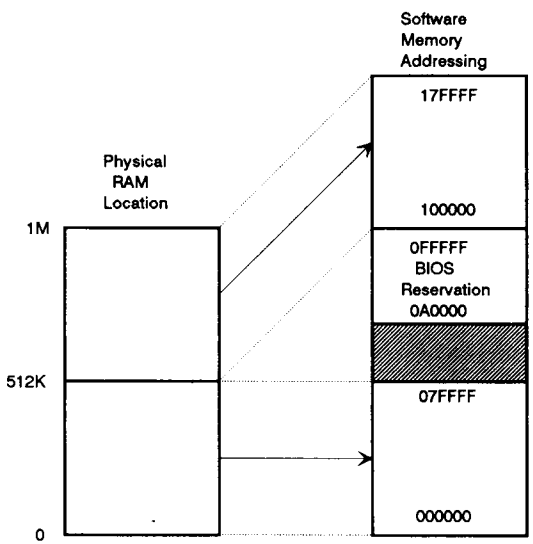


Figure 1.4 512 KB Memory Remapping for a 1 MB system

EMS 4.0

EMS (Expanded Memory Specification) is a method of indirectly addressing an extended area of RAM. EMS uses a window in the 384 KB address range dedicated to the system, and indirectly addresses memory through that window. There are four EMS registers in the 2036.

The main application for EMS is in DOS systems whose programs can only access 1MB because the address range has only 20 address bits. (The 8086 had only 20 bits). If a system has more than 1MB of RAM, and DOS can only address 1MB, the remaining memory can only be used by addressing the memory indirectly.

The EMS window, for example between 0D0000 to 0DFFFF, is broken into four 16 KB segments. Each of these segments has one associated EMS register (see Figure 1.5), where each EMS page register represents ten address bits (A23 to A14). When the EMS window is selected, these bits represent physical address bits A23 to A14 and A13 to A0 which are represented by the corresponding software address bits. This, gives EMS software the ability to redirect memory addresses from the four EMS windows to anywhere in the resident RAM address range.

EMS is enabled in a Configuration Register The four EMS address registers are also programmed within the Configuration Registers.

For example, to access memory at location 230FFF, EMS must be enabled and an address register must be programmed using the upper ten bits of memory address. Address Register 0 is programmed with 0010-0011-00 and the 16 KB block of memory from 230000 to 233FFF is available for Register 0 (located between 0D0000 to 0D3FFF). A memory access to software address 0D0FFF is directed to 230FFF.

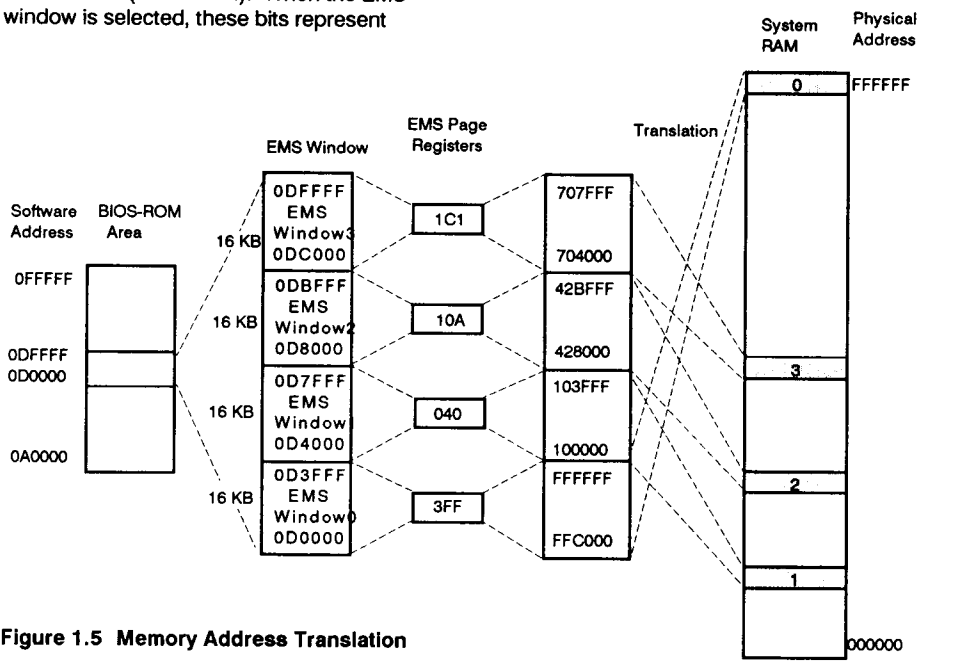


Figure 1.5 Memory Address Translation

Extended Memory

The 2036 supports Extended Memory, allowing up to 16 MB in protected mode applications.

Extended Memory refers to additional memory added to a system which is above one megabyte. In DOS, because it emulates the 8086, the 80286 can only access 1 MB of memory in real mode. Consequently, the Extended Memory is used for applications such as print buffers or disk cache which do not require direct CPU accesses.

In an OS/2 environment however, the CPU can access up to 16 MB in protected mode. Therefore, Extended Memory is most valuable for OS/2 applications.

Simultaneous Extended and Expanded Memory

The 2036 provides the ability to access Extended Memory and Expanded Memory (EMS) simultaneously at the same address location. Generally, systems require a selection of one or the other, but not both at the same time. This unique feature of the 2036 allows more flexibility with systems where switching from DOS to OS/2 is required.

When the EMS window locations are selected by the CPU or DMA, and EMS is enabled, EMS SEL goes active (refer to figure 1.6). An EMS page register will then be assigned to a location between MEMA14 and MEMA23, allowing memory above 1 MB to be accessed through the EMS window. A14 and A15 are used to select one of the four EMS page registers.

When neither the CPU nor DMA device chooses an address location above the 1 MB range, the EMS window is not selected, and the CPU address becomes the memory address, allowing Extended Memory to be accessed.

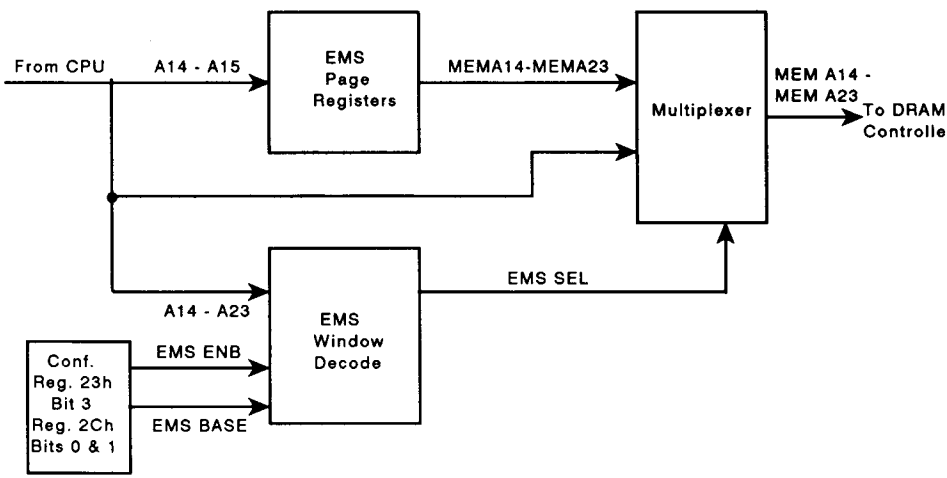


Figure 1.6 ACC Micro 2036 EMS Logic Block Diagram

Shadow RAM

Shadow RAM provides an option to transfer BIOS or video-extension BIOS program codes into system RAM. This option provides significant performance improvement for applicatons requiring intensive BIOS calls.

Shadow RAM implements an alternate BIOS source by copying the complete EPROM program code into system RAM. This is referred to a "shadowing" because the DRAM and EPROM are both located at the same physical address space. This change is transparent to the rest of the system. ROM can be disabled, allowing the RAM to respond in its place. The advantage of this procedure is that DRAM access time is typically much faster than EPROM access time.

The 2036 Shadow RAM is configured in two independent segments (see Figure 1.7). Segment 3 shadows the BIOS ROM at addresses 0E0000 to 0FFFFF, and Segment 2 shadows the BIOS video-extension ROM at addresses 0C0000 to 0DFFFF. Both Shadow RAM segments are written and enabled using four control bits in Configuration Register 22h.

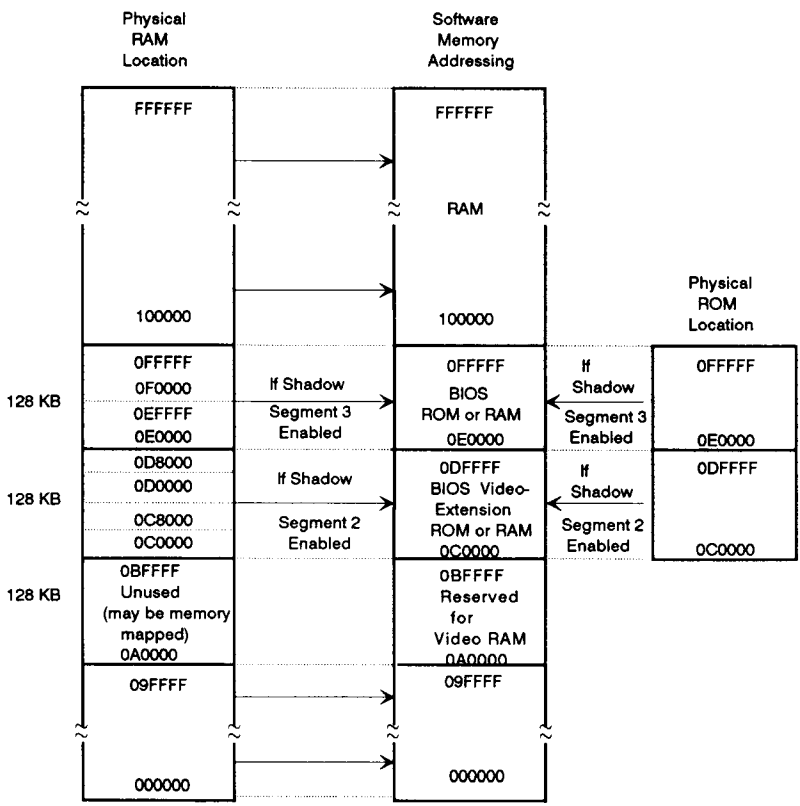


Figure 1.7 ACC Micro 2036 Shadow RAM Address Map

Segment 3 can be divided into two 64-KB subsegments. Subsegments can be enabled for shadow operation individually or simultaneously. Segment 2 can be divided into four 32-KB subsegments and enabled for shadow RAM operation.

Enabling Shadow RAM segments requires two steps. The "Shadow RAM Write Mode" for Segment 2 or 3 must be activated to allow the transfer of BIOS program code from EPROM to DRAM. Transfer is made by a read from EPROM and a write to system DRAM at the same address. The second step activates the "Shadow RAM Enable" of the corresponding segment, disables that segment's EPROM, and places that segment's DRAM in read-only mode.

Each Shadow RAM segment is completely independent and can be enabled individually or at the same time. Note that enabling Shadow RAM segments reduces the quantity of memory that can be remapped using the Memory Mapping feature.

OS/2 Optimization

The 2036 implements OS/2 optimization, which is a more efficient way to switch back and forth between real and protected mode in an OS/2 environment when frequent DOS calls are made. Conventional methods require the processor to issue two commands to the keyboard controller in switching to protected mode and activating gate A20.

With OS/2 optimization, the 2036 allows control of software CPU reset and A20 gating through the configuration register 31h or through Port 92h.

Configuration Register Port 92h, Fast A20 Gate, and Alternative RESET Control

Bit	Function
7-2	Reserved
1	A20 Gate
0	Alternate CPU reset

Bit 1 This bit controls CPU address bit A20. When set to 1, it enables A20. When set to 0, this bit makes the A20 Signal inactive, thus preventing the Address bus from going beyond the 0FFFFFh boundary in Real Mode.

Although it has the same function as the keyboard controller's GATE-A20 signal, it is much faster because it is just a simple I/O write operation. Default is 0.

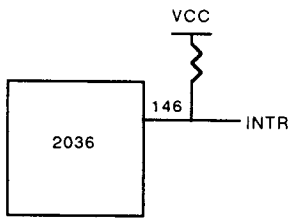
Bit 0 By setting this bit to 1, application softwares can reinitialize the microprocessor and switch the operation from Protected Mode to Real Mode. Setting this bit does not reset the whole system, it only affects the CPU. This reset function is the same as that of the keyboard controller's "KBRST" signal. However, it provides a faster reset sequence. This bit can be read by application software to determine if it is a hot rest or cold boot. It can only be set to 0 by writing a 0 to bit 0 of the register or by system reset. Default is 0.

These two bits, bit 1 and 0, are logic-ORed with Configuration Register 31h bits 1 and 0 and hardware signals "A20GATE" and "KBRST."

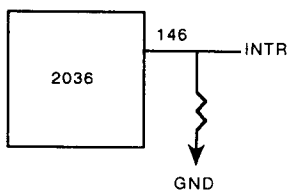
8-bit/16-bit ROM Options

The 2036 supports both 8-bit and 16-bit ROM Data buses. It is configured by a pull-up or a pull-down resistor on pin 146 (INTR) as demonstrated below:

16-bit ROM configuration



8-bit ROM configuration



The 16-bit ROM is located in the local memory bus (MD) and treated as local memory. It can be accessed more efficiently and it takes less time to finish a cycle.

The 8-bit ROM is located in the local I/O Bus (XD) and treated as an AT Bus device. Due to its narrow data path and long cycle, the performance of ROM cycles will not be as efficient as that of the 16-bit option. However, as the 2036 provides BIOS shadow capability, this inefficiency can be avoided by moving the BIOS code from the 8-bit ROM to a 16-bit local RAM.

128K/64K ROM BIOS Range

The system ROM BIOS range can be set to two different sizes--64K or 128K--to accommodate various application requirements. Refer to configuration 2Ch definition to configure the size of the ROM BIOS Range.

512K EPROM Support

The 2036 allows the system designer to porgram the memory from F80000 to FEFFFF as ROM cycle. The system BIOS at location 0E0000 to 0FFFFF will be duplicated to FE0000-FFFFFF.

Single EPROM Support

Pin /ENROM is a ROM chip select signal. This signal can select EPROM locations at 0C0000-0CFFFF, 0E0000-0FFFFF and F80000-FFFFFF. When bits 7 and 6 of Register 27h are set to one, /ENROM can select both the system BIOS and VGA BIOS. Therefore, the system BIOS and Video BIOS can be combined into a single 8-bit EPROM. To enable the Single EPROM support, the system needs to be set to run at Normal mode (8MHz).

Local base memory decode

The memory range between 0 and 640K can be selectively disabled. so that the 2036 does not generate local DRAM cycles for the selected ranges. Instead, the 2036 generates AT Bus cycles for those ranges. This feature makes the 2036 fully compatible with some memory boards which have to be located within conventional memory range. This feature is achieved by programming the Configuration Register 21h, bit 3 and 0.

Staggered Refresh Logic

The 2036 refresh logic works to perform a periodic refresh for both system DRAM and extended RAM on the AT Bus. The 2036 initiates a refresh cycle by driving its /REFRESH output low, and driving the refresh address onto the MA Bus, simultaneously generating staggered refresh pulses on the eight RAS outputs. The RAS outputs are staggered to reduce the current drain caused by the refresh operation.

During each refresh cycle, the 2036 drives the current refresh address onto the AT address bus. This provides the refresh address for extended memory. The refresh pulse for extended memory is from the /MEMR signal.

Reset and Shutdown Logic

The reset and shutdown logic contains the circuitry for the RESET and /CPURDY signals. Reset circuitry generates two resets. One is for the general system reset with power on and the other is for the CPU, or for taking the 80286 out of protected mode when a warm software reset request is generated by the 8042 keyboard controller.

The PWRGOOD signal generates a system reset and is synchronized to CPUCLK. When the /SWRESET signal is generated from the 8042 keyboard controller (called a warm reset), CPURST is activated to reset the CPU. CPURST is asserted for at least sixteen CPUCLK cycles and then deactivated for proper CPU operation.

Suspend and Resume Function

The 2036 along with the power management chip ACC Micro 2020 supports a power conservation feature-- Suspend and Resume. Necessary hardware is provided to monitor the activity of power hungry devices such as microprocessor, fixed disk drive, LCD display, etc. All defined register bits in the 2036 and the 2020 are readable and writeable to support this feature.

Through software task, a device can be powered off when no activity is detected for a reasonable length of time which can be programmed in set-up program. The device then can be powered back on to the same state as the last power off when it is desired. This suspend and resume capability minimizes system's battery power consumption.

Configuration Registers

The 2036 contains configuration registers which provide a variety of functions. These functions are concerned with system initialization, software control of advanced memory control and power saving features. For system initialization, these configuration registers implement a no-cost, no-space alternative to system board DIP switches. For advanced memory control, these registers provide maximum flexibility and convenience for programming. Configuration registers are selected by the configuration index register at I/O address F2. Table 1.3 contains a summary of configuration registers.Configuration registers are programmed with an indirect addressing scheme using I/O addresses F2 and F3. I/O address F2 contains the write-only configuration index register. F2 selects the corresponding configuration register accessed at I/O address F3. To write a value of "E8" into configuration register 2Ah, the configuration index register at I/O address F2 must first be written with a value of "2A," then register at I/O address F3 with a value of "E8." Configuration registers are selected by the configuration index register at I/O address F2. Table 1.3 contains a summary of configuration registers 20h - 31h. Table 1.4 contains a summary of configuration registers 32h-3Fh.

Table 1.3 ACC 2036 Configuration Registers 20h-31h

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
20h	R*	FEFROM	R	TPI	< memory configuration select >			
21h	FD8ROM	FD0ROM	R	CHF	LRAM3	<memory mode select>		LRAM1
22h	FC8ROM	FC0ROM	R	MM512K	SH2WR	SH2EN	SH3WR	SH3EN
23h	FB8ROM	D80ROM	R	MMEN	EMSEN	R/WE	ROM wait state select	
24h	FA8ROM	FA0ROM	R	ER0A23	ER0A22	ER0A21	ER0A20	ER0A19
25h	F98ROM	F90ROM	R	ER0A18	ER0A17	ER0A16	ER0A15	ER0A14
26h	F88ROM	F80ROM	R	ER1A23	ER1A22	ER1A21	ER1A20	ER1A19
27h	0C8ROM	0C0ROM	R	ER1A18	ER1A17	ER1A16	ER1A15	ER1A14
28h	R	R	R	ER2A23	ER2A22	ER2A21	ER2A20	ER2A19
29h	R	MAMUX	R	ER2A18	ER2A17	ER2A16	ER2A15	ER2A14
2Ah	R	R	R	ER3A23	ER3A22	ER3A21	ER3A20	ER3A19
2Bh	R	R	R	ER3A18	ER3A17	ER3A16	ER3A15	ER3A14
2Ch	R	R	R	ROM size	SH32	SH31	< EMS base	>
2Dh	R	R	R	R	SH24	SH23	SH22	SH21
2Eh	R	R	R	1	NO387SX	RAST	REFCLK	0
31h	R	R	R	R	R	R	HOTSWR	ENGA20

R = Reserved Bits

The specific functions of each configuration register are detailed below.

An unused bit is ignored by the system and is always read back as a one.

Note that all reserved bits must be written to zero, even though they can read back as ones. Any readback from reserved bits can be ignored.

Configuration Register 20h

Bit	Function
7	Reserved
6	Enable FE0000-FEFFFF as EPROM cycle
5-4	Reserved
3-0	Memory configuration select

Bit 6 When set to 1, memory location from FE0000 to FEFFFF is set for EPROM cycle. When set to 0, memory location from FE0000 to FEFFFF is set for DRAM cycle. Default is zero.

Bits 3-0
These bits are encoded to select the type and quantity of system board DRAM. Refer to following table. Default for these bits is 2 hex.

Note that system board memory is organized in banks consisting of 18 bits of DRAM each (two 8-bit bytes plus two parity bits).

Bits 3 2 1 0	Option	Bank	Type	Total DRAM
0 0 0 0	0	0	256K	
		1	64K	640K*
0 0 0 1	1	0	256K	512K
0 0 1 0	2	0,1	256K	1M
0 0 1 1	3	0-3	256K	2M
0 1 0 0	4	0-5	256K	3M
0 1 0 1	5	0-7	256K	4M
0 1 1 0	6		Reserved	
0 1 1 1	7	0	1M	2M
1 0 0 0	8	0,1	1M	4M
1 0 0 1	9	0-3	1M	8M
1 0 1 0	10	0-5	1M	12M
1 0 1 1	11	0-7	1M	16M
1 1 0 0	12	0	4M	8M
1 1 0 1	13	0-1	4M	16M
1 1 1 0	14	0,1	256K	
		2	1M	3M*
1 1 1 1	15	0,1	256K	
		2,3	1M	5M*

Memory option definition

* Option 0,14 and 15 have two different types of memory, to obtain a total of 640K, 3M and 5M RAM.

Configuration Register 21h

Bit	Function
7	Enable FD8000-FDFFFF as EPROM cycle
6	Enable FD0000-FD7FFF as EPROM cycle
5	Reserved
4	Turbo mode select
3	Local base memory decode
2-1	Memory Mode Selections
0	Local base memory decode

Bit 7 When set to 1, memory location from FD8000 to FDFFFF is set for EPROM cycle. When set to 0, memory location from FD8000 to FDFFFF is set for DRAM cycle. Default is zero.

Bit 6 When set to 1, memory location from FD0000-FD7FFF is set for EPROM cycle. When set to 0, memory location from FD0000-FD7FFF is set for DRAM cycle. Default is zero.

Bit 4 When set to 1, this bit selects the Turbo frequency mode. When this bit is set high, the system is placed in Turbo mode. Default is zero.

Bit 3,0 The system base memory can be disabled to as low as 128K bytes by programming bits 3 and 0 as follows:

Bit 3	Bit 0	Local base memory range
0	0	000000-09FFFF (Default, 640K Base memory)
0	1	000000-01FFFF (128K Base Memory)
1	0	000000-03FFFF (256K Base Memory)
1	1	000000-07FFFF (512K Base Memory)

Bit 2-1 When both bit 2 and bit 1 are set to zero, this bit selects the Page interleaved memory control mode. Page interleaved mode reduces performance to 0.4 or 0.7 wait states, but functions with slower and less expensive DRAMs. When bit 2 is set to zero and bit 1 is set to one, it indicates Direct Access mode 0WS. When both bit 2 and bit 1 are set to one, it indicates Direct Access mode 1WS. Default for Bits 1 and 2 is zero.

Bit 2	Bit 1	Memory Mode
0	0	Page Interleaved
0	1	Direct Access, 0WS
1	0	Reserved
1	1	Direct Access, 1WS

Configuration Register 22h

Bit	Function
7	Enable FC8000-FCFFFF as EPROM cycle
6	Enable FC0000-FC7FFF as EPROM cycle
5	Reserved
4	512K memory mapping enable
3	Shadow RAM write only mode, Segment 2
2	Shadow RAM enable, Segment 2
1	Shadow RAM write only mode, Segment 3
0	Shadow RAM enable, Segment 3

Bit 7 When set to 1, memory location from FC8000-FCFFFF is set for EPROM cycle. When set to 0, memory location from FC8000-FCFFFF is set for DRAM cycle. Default is zero.

Bit 6 When set to 1, memory location from FC0000-FC7FFF is set for EPROM cycle. When set to 0, memory location from FC8000-FCFFFF is set for DRAM cycle. Default is zero.

Bit 4 When set to 1, this bit enables the 512 KB memory remapping feature. This feature can only be activated when the system board memory is configured as option 2. Default is 0.

Bit 3 When set to 1, this bit places the Shadow RAM for Segment 2 (0C0000 to 0DFFFF) into write mode. Refer to the Shadow RAM description. Default is zero.

Bit 2 When set to 1, this bit enables the Shadow RAM at Segment 2 (0C0000 to 0DFFFF). Default is zero.

Bit 1 When set to 1, this bit places the Shadow RAM at Segment 3 (0E0000 to 0FFFFF) into write mode. Default is zero.

Bit 0 When set to 1, this bit enables the Shadow RAM at Segment 3 (0E0000 to 0FFFFF). Default is zero.

Configuration Register 23h

Bit	Function
7	Enable FB8000-FBFFFF as EPROM cycle
6	Enable FB0000-FB7FFF as EPROM cycle
5	Reserved
4	Memory mapping enable
3	EMS enable
2	E-segment R/W control
1-0	ROM wait state select

Bit 7 When set to 1, memory location from FB8000-FBFFFF is set for EPROM cycle. When set to 0, memory location from FB8000-FBFFFF is set for DRAM cycle. Default is zero.

Bit 6 When set to 1, memory location from FB0000-FB7FFF is set for EPROM cycle. When set to 0, memory location from FB0000-FB7FFF is set for DRAM cycle. Default is zero.

Bit 4 When set to 1, this bit enables the memory mapping feature. Default is zero.

Bit 3 When set to 1, this bit enables the EMS feature. Default is zero.

Bit 2 When set to 1 and when 0E0000-0EFFFF is programmed as Shadow RAM, it is Read/Write memory. When set to 0, and 0E0000-0EFFFF is programmed as Shadow RAM, it is Read Only memory. Default is 0.

Bits 1-0

These bits select the number of wait states that are inserted for all ROM read cycles. These bits default to the 4 wait state select.

Bits 1	Bits 0	Select
0	0	4 wait states (default)
0	1	1 wait state
1	0	2 wait states
1	1	3 wait states

Configuration Registers 24h-2Bh

The 2036 supports four EMS registers. Configuration register pairs 24h and 25h, 26h and 27h, 28h and 29h, 2Ah and 2Bh, each constitute one EMS register. These pairs are defined as EMS registers 0 through 3. The contents of these pairs provide alternate address bits for A14-23 during EMS accesses. All EMS registers default to zero.

EMS Register 0
Configuration Register 24h

The 16 KByte EMS window for EMS register 0 is located at address range 0D0000 to 0D3FFF at default.

Bit	Definition
7	Enable FA8000-FAFFFF as EPROM cycle
6	Enable FA0000-FA7FFF as EPROM cycle
5	Reserved
4	ER0, A23
3	ER0, A22
2	ER0, A21
1	ER0, A20
0	ER0, A19

Bit 7 When set to 1, memory location from FA8000-FAFFFF is set for EPROM cycle. When set to 0, memory location from FA8000-FAFFFF is set for DRAM cycle. Default is zero.

Bit 6 When set to 1, memory location from FA0000-FA7FFF is set for EPROM cycle. When set to 0, memory location from FA0000-FA7FFF is set for DRAM cycle. Default is zero.

Bits 4-0 EMS register 0. EMS address lines A23-A19.

Configuration Register 25h

Bit	Definition
7	Enable F98000-F9FFFF as EPROM cycle
6	Enable F90000-F97FFF as EPROM cycle
5	Reserved
4	ER0, A18
3	ER0, A17
2	ER0, A16
1	ER0, A15
0	ER0, A14

Bit 7 When set to 1, memory location from F98000-F9FFFF is set for EPROM cycle. When set to 0, memory location from F98000-F9FFFF is set for DRAM cycle. Default is zero.

Bit 6 When set to 1, memory location from F90000-F97FFF is set for EPROM cycle. When set to 0, memory location from F90000-F97FFF is set for DRAM cycle. Default is zero.

Bits 4-0 EMS register 0. EMS address lines A18-A14.

EMS Register 1
Configuration Register 26h

The 16 KByte EMS window for EMS register 1 is located at address range 0D4000 to 0D7FFF.

Bit	Definition
7	Enable F88000-F8FFFF as EPROM cycle
6	Enable F80000-F87FFF as EPROM cycle
5	Reserved
4	ER1, A23
3	ER1, A22
2	ER1, A21
1	ER1, A20
0	ER1, A19

Bit 7 When set to 1, memory location from F88000-F8FFFF is set for EPROM cycle. When set to 0, memory location from F88000-F8FFFF is set for DRAM cycle. Default is zero.

Bit 6 When set to 1, memory location from F80000-F87FFF is set for EPROM cycle. When set to 0, memory location from F80000-F87FFF is set for DRAM cycle. Default is zero.

Bits 4-0 EMS register 1. EMS address lines A23-A19.

Configuration Register 27h

Bit	Definition
7	Enable 0C8000-0CFFFF as /ENROM cycle
6	Enable 0C0000-0C7FFF as /ENROM cycle
5	Reserved
4	ER1, A18
3	ER1, A17
2	ER1, A16
1	ER1, A15
0	ER1, A14

Bit 7 When set to 1, /ENROM selects 0C8000-0CFFFF as part of EPROM enable areas. When set to 0, 0C8000-0CFFFF is not included in the EPROM enable areas.

Bit 6 When set to 1, /ENROM selects 0C0000-0C7FFF as part of EPROM enable areas. When set to 0, 0C0000-0C7FFF is not included in the EPROM enable areas.

Bits 4-0 EMS register 1, EMS address lines A18-A14.

EMS Register 2
Configuration Register 28h

The 16 KByte EMS window for EMS register 2 is located at address range 0D8000 to 0DBFFF.

Bit	Definition
7-5	Reserved
4	ER2, A23
3	ER2, A22
2	ER2, A21
1	ER2, A20
0	ER2, A19

Bits 4-0 EMS register 2. EMS address lines A23-A19.

Configuration Register 29h

Bit	Definition
7	Reserved
6	MA Mux control
5	Reserved
4	ER2, A18
3	ER2, A17
2	ER2, A16
1	ER2, A15
0	ER2, A14

Bit 6 When set to 1, MA mux sets an early column address timing which makes column address coming out earlier than the normal column address timing. When set to 0, MA mux sets a normal column address timing. Default is zero.

Bits 4-0 EMS register 2. EMS address lines A18-A14.

EMS Register 3
Configuration Register 2Ah

The 16 KB EMS window for EMS register 3 is located at address range 0DC000 to 0DFFFF.

Bit	Definition
7-5	Reserved
4	ER3, A23
3	ER3, A22
2	ER3, A21
1	ER3, A20
0	ER3, A19

Bits 4-0 EMS register 3. EMS address lines A23-A19.

Configuration Register 2Bh

Bit	Definition
7-5	Reserved
4	ER3, A18
3	ER3, A17
2	ER3, A16
1	ER3, A15
0	ER3, A14

Bits 4-0 EMS register 3. EMS address lines A18-A14.

Segment 3 Shadow Register Configuration Register 2Ch

Bit	Definition
7-5	Reserved
4	BIOS decode range
3	Shadow the second 64 KB of the BIOS segment
2	Shadow the first 64 KB of the BIOS segment
1-0	EMS base address

Bit 4 When set to 0, ROM BIOS will be located in (0F0000-0FFFFF) when set to 1, ROM BIOS will extend to (0E0000-0FFFFF). Default is zero.

Bit 3 When set to 1, this bit indicates that the second 64 KB of the BIOS segment (0F0000-0FFFFF) is available for shadow operation. Default is zero.

Bit 2 When set to 1, this bit indicates that the first 64 KB of the BIOS segment (0E0000-0EFFFF) is available for shadow operation. Default is zero.

Bits 1-0 These bits indicate the base starting address of the EMS window. Default base address is 0D0000.

Bits 1 0	Base address
0 0	0C0000
0 1	0C8000
1 0	0D0000
1 1	0E0000

Segment 2 Shadow Register Configuration Register 2Dh

Bit	Definition
7-4	Reserved
3	Shadow the fourth 32K of segment 2
2	Shadow the third 32K of segment 2
1	Shadow the second 32K of segment 2
0	Shadow the first 32K of segment2

Bit 3 When Bit 3 of register 2D is set to 1, shadow RAM is enabled at location (0D8000-0DFFFF). Default is zero.

Bit 2 When Bit 2 of register 2D is set to 1, shadow RAM is enabled at location (0D0000-0D7FFF). Default is zero.

Bit 1 When Bit 1 of register 2D is set to 1, shadow RAM is enabled at location (0C8000-0CFFFF). Default is zero.

Bit 0 When Bit 0 of register 2D is set to 1, shadow RAM is enabled at location (0C0000-0C7FFF). Default is zero.

Configuration Register 2Eh

Bit	Definition
5-7	Reserved
4	Reserved, hard code to 1
3	No 387SX
2	RAS Timeout
1	Refresh clock
0	Reserved, (Default = 0)

Bit 4 Hard code to 1. Default is one.

Bit 3 When set to zero, this bit indicates that 387SX exists. When set to one, this bit indicates that 387SX does not exist. Default is zero.

Bit 2 When set to zero, this bit indicates that RAS Timeout is disabled. When set to one, this bit indicates that RAS Timeout is enabled. Default is zero.

Bit 1 When set to zero, this bit indicates the CPUCLK is 8 MHz during refresh period. When set to one, this bit indicates Turbo CLK during refresh period. Default is zero.

Bit 0 Default is zero.

Configuration Register 31h

Bit	Function
7-2	Reserved
1	Hot software reset
0	Enables gate A20

Bit 1 This bit triggers a CPU reset when set to 1. Default is zero.

Bit 0 This bit enables address A20 when set to 1. Default is one.

Table 1.4 ACC Micro 2036 Configuration Registers 32h - 3Fh

Register	Pin Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
32h	/PCS1	SA9	SA8	SA7	SA6	SA5	SA4	SA3	SA2
33h	/PCS1	ENB	XD	16BIT	< Divisor >		< Decode Size >		
34h	/PCS2	SA9	SA8	SA7	SA6	SA5	SA4	SA3	SA2
35h	/PCS2	ENB	XD	16BIT	STBYE	STBYI	< Decode Size >		
36h	/PCS3	SA9	SA8	SA7	SA6	SA5	SA4	SA3	SA2
37h	/PCS3	ENB	XD	16BIT	Pari	PASS	< Decode Size >		
38h	/PCS4	SA9	SA8	SA7	SA6	SA5	SA4	SA3	SA2
39h	/PCS4	ENB	XD	16BIT	OSCM	M287	< Decode Size >		
3Ah	/PCS5	SA9	SA8	SA7	SA6	SA5	SA4	SA3	SA2
3Bh	/PCS5	ENB	XD	16BIT	R	P131	< Decode Size >		
3Ch	/PMCS	PBA	PBA	PBA	PBA	PBA	PBA	PBA	PBA
3Dh	/PMCS	ENB	XD	16BIT	PBA	PBA	MASK	MASK	MASK
3Eh	CLK42	CLK42	SER	SLRF	SLRF	VRE	VRS	NMIS	NMI
3Fh	/VRAM	BC	B8	B4	B0	AC	A8	A4	A0

Programmable Chip Selects

To support an all-in-one board, the 2036 supports five programmable chip selects. These PCSs can be used to initialize peripheral devices such as serial ports, parallel ports, floppy, hard disk, etc. Each programmable chip select pin is defined by two registers. For example, chip select pin /PCS1 is defined by registers 32h and 33h, and pin /PCS2 is defined by registers 34h and 35h.

The 2036 also supports a separate register 3C to select the Power Management Chip.

The typical application for these chip select pins are used for peripheral chip select. The 2036 chip selects support all the standard peripheral I/O map range.

Standard Peripheral I/O Map

Hex Range	Device
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel printer port 2
2F8-2FF	Serial port 2
300-31F	Prototype card
360-36F	Reserved
378-37F	Parallel printer port 1
380-38F	SDLC, bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome Display and Printer Adapter
3C0-3CF	Reserved
3D0-3DF	Color/Graphics Monitor Adapter
3F0-3F7	Diskette controller
3F8-3FF	Serial port 1

Programmable Chip Select /PCS1 Configuration Registers 32h

Bit	Function
7-0	Indicate base address A9-A2 of /PCS1. Default is 00h.

Configuration Register 33h

Bit	Function
7	Enables decode.
6	Device attached to XD bus.
5	16-bit device.
4-3	Standby mode clock frequency
2-0	Indicate /PCS1 block size

Bit 7 Set to one, this bit enables decoding of /PCS1. Default is zero.

Bit 6 Set to one, /PCS1 device is attached to XD bus. Default is one.

Bit 5 Set to one, /PCS1 selects a 16-bit device. Default is zero.

Bits 4-3
Select standby mode clock divider frequency for standby mode operation:
00 = divided by 2
01 = " 4
10 = " 8
11 = " 16
Defaut is 00b.

Bits 2-0
Indicate size of /PCS1 block:

000	4 bytes
001	8 bytes
010	16 bytes
011	32 bytes
100	64 bytes
101	128 bytes
11x	Reserved

Default is 000b

Programmable Chip Select /PCS2 Configuration Register 34h

Bit	Function
7-0	Indicate address A9-A2 of /PCS2. Default is 00h.

Configuration Register 35h

Bit	Function
7	Enables decode.
6	Device attached to XD bus.
5	16-bit device.
4	Selects standby mode.
3	Go to standby mode.
2-0	Indicate /PCS2 block size.

Bit 7 Set to one, this bit enables decode of /PCS2. Default is zero.

Bit 6 Set to one, /PCS2 device is attached to XD bus. Default is one.

Bit 5 Set to one, /PCS2 selects a 16-bit device. Default is zero.

Bit 4 Set to one, this bit enables standby mode; set to zero, this bit disables standby mode. Bit 4 overwrites bit 3. Default is zero.

Bit 3 Set to one, the 2036 goes to standby mode. Default is zero.

Bits 2-0

Indicate size of /PCS2 block:

000	4 bytes
001	8 bytes
010	16 bytes
011	32 bytes
100	64 bytes
101	128 bytes
11x	Reserved.

Default is 000b.

Programmable Chip Select /PCS3 Configuration register 36h

Bit	Function
7-0	Indicates address A9-A2 of /PCS3. Default is 00h.

Configuration Register 37h

Bit	Function
7	Enables decode.
6	Device attached to XD bus.
5	16-bit device attached.
4	Disable parity check
3	Lock password
2-0	Indicate /PCS3 block size

Bit 7 Set to one, this bit enables decoding of /PCS3. Default is zero.

Bit 6 Set to one. /PCS3 device is attached to XD bus. Default is one.

Bit 5 Set to one, /PCS3 selects a 16-bit device. Default is zero.

Bit 4 Set to one to disable on-board memory parity check function. Default is 0.

Bit 3 Set to one to lock password stored in RTC CMOS RAM. 78h - 7Fh. Default is 0.

Bits 2-0

Indicate size of /PCS3 block:

000	4 bytes
001	8 bytes
010	16 bytes
011	32 bytes
100	64 bytes
101	128 bytes
11x	Reserved.

Default is 000b.

Programmable Chip Select /PCS4 Configuration Register 38h

Bit	Function
7-0	Indicates address A9-A2 of /PCS4. Default is 00h.

Configuration Register 39h

Bit	Function
7	Enables decode.
6	Device attached to XD bus.
5	16-bit device.
4	OSC MASK
3	Reserved
2-0	Indicates /PCS4 block size

Bit 7 Set to one, this bit enables decoding of /PCS4. Default is zero.

Bit 6 Set to one, /PCS4 device is attached to XD bus. Default is one.

Bit 5 Set to one, /PCS 4 selects a 16-bit device. Default is zero.

Bit 4 Set to one to mask 14.318 MHz. Default is zero.

Bits 2-0

Indicate size of /PCS4 block:

000	4 bytes
001	8 bytes
010	16 bytes
011	32 bytes
100	64 bytes
101	128 bytes
11x	Reserved.

Default is 000b.

Programmable Chip Select /PCS5 Configuration Register 3Ah

Bit	Function
7-0	Indicate base address A9-A2 of /PCS5. Default is 00h.

Configuration Register 3Bh

Bit	Function
7	Enables decode.
6	Device attached to XD bus.
5	16-bit device.
4	Reserved.
3	Pin 131 definition.
2-0	Indicate /PCS5 block size

Bit 7 Set to one, this bit enables decoding of /PCS5. Default is zero.

Bit 6 Set to one, /PCS5 device is attached to XD bus. Default is one.

Bit 5 Set to one, /PCS5 selects a 16-bit device. Default is zero.

Bit 3 When set to 1, multifunction pin 131 is defined as /SBHE. When set to zero, pin 131 is defined as /PCS4. Default is one.

Bits 2-0

Indicate size of /PCS5 block:

000	4 bytes
001	8 bytes
010	16 bytes
011	32 bytes
100	64 bytes
101	128 bytes
11x	Reserved.

Default is zero.

Programmable Power Management Chip Select /PMCS Configuration Register 3Ch

Bit	Function
7-0	Indicate base address A7-A0 of /PMCS. Default is 22h.

Configuration Register 3Dh

Bit	Function
7	Enables decode of /PMCS.
6	Attached to XD bus.
5	16-bit PMC.
4-3	Indicates base address A9-A8 of /PMCS decode. Default is 00b.
2-0	Mask [2..0] of /PMCS decode.

Bit 7 Set to one, this bit enables decoding of /PMCS. Default is one.

Bit 6 Set to one, PMC attached to XD bus. Default is one.

Bit 5 Set to one, PMC is a 16-bit device. Set to zero, PMC is an 8-bit device. Default is zero.

Bit 4-3 Indicates base address A9-A8 of /PMCS decode. Default is 00b.

Bit 2 Set to one, /PMCS will not decode SA2. Default is one.

Bit 1 Set to one, /PMCS will not decode SA1. Default is zero.

Bit 0 Set to one, /PMCS will not decode SA0. Default is zero.

Configuration Register 3Eh

Bit	Function
7	Enables CLK42 MASK.
6	Enables CLKSER MASK.
5-4	Slow Refresh divider.
3	Enables /VRAM decoder.
2	/VRAM read/write cycle select.
1	Indicates /NMIIN status; READ ONLY.
0	/NMIIN enable

Bit 7 Set to zero, this bit enables CLK42; set to one, disables CLK42. Default is zero.

Bit 6 Set to zero, enables CLKSER; set to one, this bit disables CLKSER. Default is zero.

Bits 5-4
Slow REFRESH divisor:

54	Divided by	Refresh period
00	1	15 us.
01	2	30 us.
10	3	60 us.
11	4	120 us.

Default is 00b.

Bit 3 Set to one, this bit enables /VRAM decoder. Set to zero, this bit disables /VRAM decoder. /VRAM replaces /PCS5, if set to one. Default is zero.

Bit 2 Set to one, /VRAM is asserted on WRITE cycles only; set to zero, /VRAM is asserted on both READ and WRITE cycles. Default is zero.

Bit 1 /NMIIN status, READ ONLY. This bit is connected to /NMIIN pin. Default is zero.

Bit 0 Set to one, this bit enables /NMIIN; set to zero, this bit disables /NMIIN. Default is zero. When there is an active low signal inserted to /NMIIN pin and this bit is enabled, the /NMIIN will generate NMI ouput to CPU. Default is zero.

/VRAM Map Register
Configuration Register 3Fh

Bit	Function
7	0BC000h-0BFFFFh
6	0B8000h-0BBFFFh
5	0B4000h-0B7FFFh
4	0B0000h-0B3FFFh
3	0AC000h-0AFFFFh
2	0A8000h-0ABFFFh
1	0A4000h-0A7FFFh
0	0A0000h-0A3FFFh

The 3Fh register is designed to monitor the activity of the display subsystem. When there is an access to the video display area, the /VRAM will send out an active low signal. This feature is very useful for a system designer to determine when to disable video display to save the system power consumption.

Bit 7 When set to one, this bit monitors video data area 0BC000h-0BFFFFh. Default is zero.

Bit 6 When set to one, this bit monitors video data area 0B8000h-0BBFFFh. Default is zero.

Bit 5 When set to one, this bit monitors video data area 0B4000h-0B7FFFh. Default is one.

Bit 4 When set to one, this bit monitors video data area 0B0000h-0B3FFFh. Default is one.

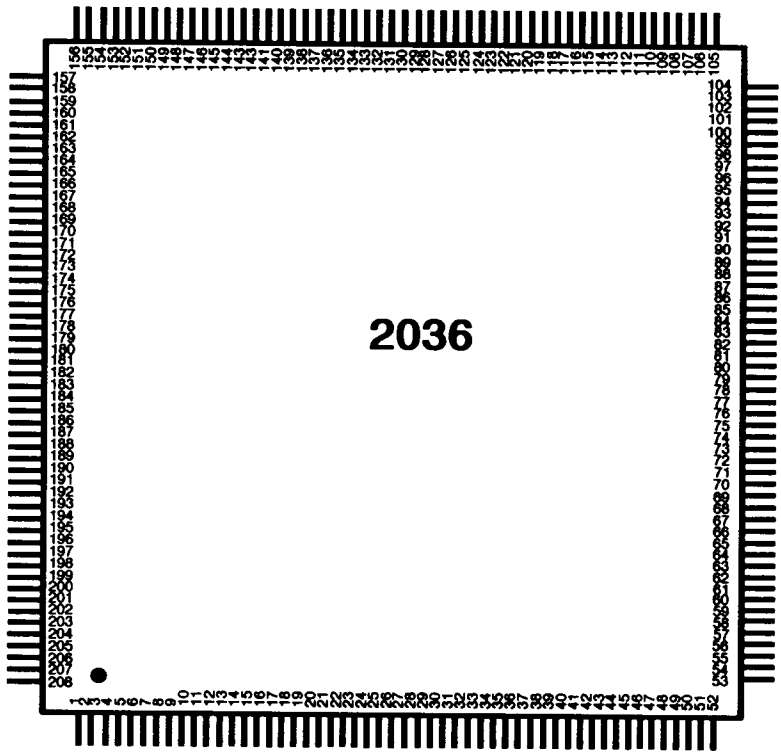
Bit 3 When set to one, this bit monitors video data area 0AC000h-0AFFFFh. Default is zero.

Bit 2 When set to one, this bit monitors video data area 0A8000h-0ABFFFh. Default is zero.

Bit 1 When set to one, this bit monitors video data area 0A4000h-0A7FFFh. Default is zero.

Bit 0 When set to one, this bit monitors video data area 0A0000h-0A3FFFh. Default is zero.

Pin Diagram



1 VSS	69 A20	89 /CAS0L	109 VSS	129 /PCS2	149 /NMIIN	169 IRQ4	189 DRQ7
2 X14M1	70 W-R*	90 /CAS1L	110 MA9	130 /PCS3	150 SD13	170 IRQ5	190 /DACK0
3 X14M2	71 A21	91 /CAS2L	111 MA10	131 /PCS4	151 SD14	171 IRQ6	191 /DACK1
4 RESETDRV	72 SYSCLK	92 /CAS3L	112 /ENROM	132 /PCS5	152 SD15	172 IRQ7	192 /DACK2
5 CPUA20	73 /RDY	93 /CAS0H	113 MDLAT	133 VSS	153 BALE	173 IRQ9	193 /DACK3
6 /RESET	74 X 16M2	94 /CAS1H	114 VDD	134 SD1	154 /MEMR	174 IRQ10	194 /DACK5
7 CLK42	75 X16M1	95 /CAS2H	115 DPARL	135 SD2	155 XDIR	175 IRQ11	195 /DACK6
8 CPURST	76 VSS	96 VSS	116 DPARH	136 SD3	156 VSS	176 SD7	196 /DACK7
9 CLKSER	77 /SX	97 VDD	117 /CS8042	137 /ZWS	157 VSS	177 SD8	197 AEN
10 VDD	78 VSS	98 VSS	118 KBINT	138 SD4	158 /MEMW	178 SD9	198 TC
11 TLED	79 /RAS0	99 SD0	119 VSS	139 /IOCS16	159 /IOW	179 SD10	199 /REFRESH
12 /NPERR	80 /RAS1	100 HLDA	120 RTCAS	140 SD5	160 /IOR	180 SD11	200 VSS
13 CPUCLK	81 /RAS2	101 /MASTER	121 MDDIR	141 SD6	161 /SMEMR	181 SD12	201 VDD
14 /LOSPD	82 /RAS3	102 PWRGD	122 /RTCDS	142 VSS	162 /SMEMW	182 DRQ0	202 /WEN
15 VSS	83 /RAS4	103 HOLD	123 A20GATE	143 IRQ12	163 /MEMC16	183 DRQ1	203 MA0
16 /KBRST	84 /RAS5	104 MA4	124 RTCRW	144 IRQ14	164 VSS	184 DRQ2	204 MA1
17 SPDSW	85 /RAS6	105 MA5	125 /RTCINT	145 IRQ15	165 VDD	185 DRQ3	205 MA2
18 D0	86 /RAS7	106 MA6	126 SPEAKER	146 INTR	166 IOCHRDY	186 VSS	206 MA3
19 D1	87 VSS	107 MA7	127 /PMCS	147 VDD	167 /IOCHCK	187 DRQ5	207 / CPUBZY
20 D2	88 /CAS3H	108 MA8	128 /PCS1	148 NMI	168 IRQ3	188 DRQ6	208 CPUPEREQ*
21 D3							
22 D4							
23 CLKIN							
24 D5							
25 /BLE							
26 D6							
27 D7							
28 D8							
29 D9							
30 D10							
31 D11							
32 D12							
33 D13							
34 D14							
35 D15							
36 A0							
37 A1							
38 VSS							
39 A2							
40 A3							
41 A4							
42 A5							
43 VDD							
44 A6							
45 A7							
46 A8							
47 A9							
48 A10							
49 A11							
50 A12							
51 A13							
52 NPEREQ*							
53 /NPBZY							
54 A14							
55 A15							
56 A16							
57 A17							
58 A18							
59 A19							
60 VSS							
61 VDD							
62 A22							
63 A23							
64 /BHE							
65 OSC							
66 /ADS							
67 M/-IO							
68 D/-C*							

* Signals have different meanings with 286 CPU. Please see pin descriptions.

Pin Descriptions

Symbol	Pin	Type	Description
Clock Pins			
X14M1	2	I	14.318 MHz crystal input.
X14M2	3	O	14.318 MHz crystal output.
X16M1	75	I	16 MHz crystal input.
X16M2	74	O	16 MHz crystal crystal output.
CLKIN	23	I	System clock oscillator input
OSC	65	O	14.318 MHz oscillator output.
CLK42	7	O	8042 clock.
SYSCLK	72	O	Peripheral clock.
CLKSER	9	O	UART clock. 1.84 MHz.
CPUCLK	13	O	CPU clock.
SPDSW	17	I	Hardware turbo mode select.
TLED	11	O	Output turns on LED turbo mode indicator. Driven low for memory cycles.
/LOSPD	14	I	Standby mode clock control.
Reset Pins			
PWRGD	102	I	"Power Good" indicator from the power supply. When low, a power-up reset is generated.
/KBRST	16	I	Keyboard reset input.
CPURST	8	O	Reset output from keyboard controller.
RESETDRV	4	O	System reset. Active high.
/RESET	6	O	System reset. Active low.

Pin Descriptions

Symbol	Pin	Type	Description
CPU Interface Pins			
D0	18	I/O	CPU data bus.
D1	19		
D2	20		
D3	21		
D4	22		
D5	24		
D6	26		
D7	27		
D8	28		
D9	29		
D10	30		
D11	31		
D12	32		
D13	33		
D14	34		
D15	35		
A0	36	I/O	Local Address bus.
A1	37		
A2	39		
A3	40		
A4	41		
A5	42		
A6	44		
A7	45		
A8	46		
A9	47		
A10	48		
A11	49		
A12	50		
A13	51		
A14	54		
A15	55		
A16	56		
A17	57		
A18	58		
A19	59		
A20	69		
A21	71		
A22	62		
A23	63		

Pin Descriptions

Symbol	Pin	Type	Description
CPU Interface Pins (contd.)			
/BHE	64	I/O	CPU byte high enable.
/BLE	25	I	CPU byte low enable.
/ADS	66	I	Address status.
M/-IO	67	I	Memory/IO.
D/-C or /S0	68	I	CPU status.
W-R or /S1	70	I	CPU status.
CPUA20	5	I	80386SX A20.
/RDY	73	O	Ready signal to CPU.
/CPUBZY	207	O	Coprocessor Busy indicator.
CPUPEREQ or NPRST	208	O	Request for 386SX mode; NPU RESET for 286 mode.
/SX	77	I	CPU TYPE; High: 286, Low: 386SX.
NPU Interface Pins			
NPEREQ or /NPCS	52	I/O	387 PEREQ for 386SX mode; NPU chip select for 286 mode.
/NPBZY	53	I	Math coprocessor busy, from 80387SX.
/NPERR	12	I	Math coprocessor error, from 80387SX.

Pin Descriptions

Symbol	Pin	Type	Description
Memory Interface Pins			
/RAS0	79	O	DRAM row address strobe.
/RAS1	80		
/RAS2	81		
/RAS3	82		
/RAS4	83		
/RAS5	84		
/RAS6	85		
/RAS7	86		
/CAS0L	89	O	DRAM column address strobe, low byte.
/CAS1L	90		
/CAS2L	91		
/CAS3L	92		
/CAS0H	93	O	DRAM column address strobe, high byte.
/CAS1H	94		
/CAS2H	95		
/CAS3H	88		
/WEN	202	O	DRAM write enable.
MA0	203	O	DRAM address (multiplexed).
MA1	204		
MA2	205		
MA3	206		
MA4	104		
MA5	105		
MA6	106		
MA7	107		
MA8	108		
MA9	110		
MA10	111		
/ENROM	112	O	ROM chip select. Active low.
MDLAT	113	O	Memory data latch.
MDDIR	121	O	Control for MD bus transceiver.
DPARL	115	I/O	Low byte parity.
DPARH	116	I/O	High byte parity.

Pin Descriptions

Symbol	Pin	Type	Description
On-Board Peripheral Interface Pins			
/CS8042	117	O	Keyboard chip select. Active low.
KBINT	118	I	Keyboard interrupt.
A20GATE	123	I	Gate A20 enable.
RTCAS	120	O	Address strobe for 146818 Real Time Clock. Falling edge causes address to be latched in 146818.
/RTCDS	122	O	Data strobe for Real Time Clock. Identifies the cycle when the RTC and RAM drive the bus with read data..
RTCRW	124	O	Read or write select for Real Time Clock.
/RTCINT	125	I	Interrupt from RTC.
SPEAKER	126	OD	Output to drive speaker.
/PMCS	127	O	Power Management Chip select.
/PCS1	128	O	Programmable Chip select.
/PCS2	129		
/PCS3	130		
/PCS4 or /SBHE	131	O	Programmable chip select or /SBHE.
/PCS5 or /VRAM	132	O	Programmable Chip select; Video Activity Detector.
AT Bus Interface Pins			
SD0	99	I/O	System data bus.
SD1	134		
SD2	135		
SD3	136		
SD4	138		
SD5	140		
SD6	141		
SD7	176		
SD8	177		
SD9	178		
SD10	179		
SD11	180		
SD12	181		
SD13	150		
SD14	151		
SD15	152		

Pin Descriptions

Symbol	Pin	Type	Description
AT BUS Interface Pins (contd.)			
XDIR	155	O	XD direction control.
BALE	153	O	Address latch enable
/MEMR	154	I/O	Memory read strobe.
/MEMW	158	I/O	Memory write strobe.
/IOR	160	I/O	I/O read strobe.
/IOW	159	I/O	I/O write strobe.
/SMEMR	161	O	System memory read strobe.
/SMEMW	162	O	System memory write strobe.
/MEMCS16	163	I	Memory 16-bit chip select.
/ZWS	137	I	Zero wait state.
/IOCS16	139	I	I/O 16-bit chip select.
IOCHRDY	166	I	I/O channel ready from expansion bus.
/IOCHCHK	167	I	Error from expansion bus. Active low.
Interrupt Pins			
IRQ3	168	I	Interrupt request from expansion bus. Active high.
IRQ4	169	I	
IRQ5	170	I	
IRQ6	171	I	
IRQ7	172	I	
IRQ9	173	I	
IRQ10	174	I	
IRQ11	175	I	
IRQ12	143	I	
IRQ14	144	I	
IRQ15	145	I	

Pin Descriptions

Symbol	Pin	Type	Description
Interrupts (contd.)			
INTR	146	I/O	This pin is a multifunction pin. At power up INTR is an input pin used to determine the BIOS data bus width. 1: 16-bit BIOS on MD Bus 0: 8-bit BIOS on XD Bus At other times, INTR is an output pin generating interrupt request to CPU. Active high.
NMI	148	O	Non-maskable interrupt to the CPU generated by math coprocessor, memory parity error, or IOCHCK error. Active high.
/NMIIN	149	I	Suspend/resume NMI input. When there is an active low signal inserted to /NMIIN pin and /NMIIN bit in Configuration Register 3Eh is enabled, the /NMIIN will generate NMI ouput to CPU.
DMA Pins			
DRQ0	182	I	DMA Request line. Active high.
DRQ1	183	I	
DRQ2	184	I	
DRQ3	185	I	
DRQ5	187	I	
DRQ6	188	I	
DRQ7	189	I	
/DACK0	190	O	DMA Acknowledge
/DACK1	191	O	
/DACK2	192	O	
/DACK3	193	O	
/DACK5	194	O	
/DACK6	195	O	
/DACK7	196	O	
AEN	197	O	Bus hold acknowledge. When asserted, I/O devices ignore address bus. Active high.
TC	198	O	DMA Terminal count pulses when terminal count is reached.
/REFRESH	199	I/O	DRAM refresh cycle. Active low.
/MASTER	101	I	Signal to gain system control.

Pin Descriptions

Symbol	Pin	Type	Description
HOLD	103	O	Hold request for CPU. Active high.
HLDA	100	I	Hold acknowledge from CPU.

Power & Ground Pins

VDD	10,43,61, 97,114,147, 165,201	System power.
VSS	1,15,38, 60,76,78, 87,96,98, 109,119,133, 142,156,157, 164,186,200	System ground.

Rating Specifications

Absolute Maximum Ratings *

Parameter	Symbol	Condition	Min	Max	Unit
Power supply voltage	VDD	Ta=25° C	VSS-0.3	7.0	V
Input voltage	VI		VSS-0.3	VDD+0.5	V
Output voltage	VO		VSS-0.3	VDD+0.5	V
Operating temperature	Top		0	70	°C
Storage temp	Tstg		-65	150	°C

* Exposing the device to stress above these limits can cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Capacitance Limits

TA = +25° C, VDD = 5V

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Input capacitance	CI		4		pF	fc = 1 MHz unmeasured pins at GND
Output capacitance	CO		6			
I/O capacitance	CIO		10		pF	

DC Specifications

TA = 0°C to 70°C, VDD = +5V +/- 0.25V

Group 1 INPUT

X14M1, X16M1,CLKIN

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VDD = 5 V +/- 0.25 V
Input High voltage	VIH	2.0	VDD	V	VDD = 5 V +/- 0.25 V
Input low current	IIL	-1	1	uA	VIN = VSS
Input high current	IIH	-1	1	uA	VIN =VDD

PWRGD, /KBRST

Parameter	Symbol	Min	Max	Unit	Test Condition
Schmitt trigger Input low voltage	VIL	0.6		V	VDD = 5 V
Schmitt trigger Input High voltage	VIH		3.0	V	VDD = 5 V
Input low current	IIL	-105	-25	uA	VIN = VSS
Input high current	IIH	-1	1	uA	VIN = VDD

DC Characteristics

TA = 0° C to +70° C, VDD = +5 V +/- 5%

IRQ 3-7, , KBINT, /RTCINT, /IOCHCK, /KBINT, /BLE, /ADS, M/-IO, D/-C, W-R, SPDSW, /LOSPD, /NPBZY, /NPERR, A20GATE, /IOCS16, /ZWS, IOCHRDY, DRQ 0-3, DRQ 5-7, /MASTER, HLDA, TEST, NMIIN, IRQ 9-12, IRQ 14-15, /SX, MEMCS16

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VDD = 5 +/- 0.25 V
Input high voltage	VIH	2.0	VDD	V	VDD = 5 +/- 0.25 V
Input low current	IIL	-105	-25	uA	VIN = VSS
Input high current	IIH	-1	1	uA	VIN = VDD

Group 2 OUTPUT

CLK42, CLKSER, /RESET, /CPUBZY, CPUPEREQ, MDLAT, /CS8042, MDDIR, RTCAS, /RTCDS, RTCRW, /PMCS, XDIR, INTR, NMI, DACK0-3, DACK 5-7

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		VSS+0.4	V	IOL = 6.0 mA
Output high voltage	VOH	VDD-0.4		V	IOH = -2.0 mA

X14M2, X16M2

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		VSS+0.4	V	IOL = 50 μA
Output high voltage	VOH	VDD-0.4		V	IOH = -50 μA

/PCS5, TLED

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		VSS+0.4	V	IOL = 6.0 mA
Output high voltage	VOH	VDD-0.4		V	IOH = -2.0 mA
Tristate leakage current	IOZ	-1	1	uA	VOUT = VDD or VSS

/RAS0-7, /CAS0H, /CAS1H, /CAS2H, /CAS3H,/CAS0L, /CAS1L, /CAS2L, /CAS3L, CPUCLK, CPURST, /RDY, /ENROM, TC

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		VSS+0.4	V	IOL = 12.0 mA
Output high voltage	VOH	VDD-0.4		V	IOH = -4.0 mA

/SMEMR, /SMEMW

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		VSS+0.4	V	IOL = 12.0 mA
Output High voltage	VOH	VDD-0.4		V	IOH = -4 mA
Tristate leakage current	IOZ	-1	1	uA	VOUT = VDD or VSS

OSC, SYSCLK, RESETDRV, /WEN, MA0-10, BALE, AEN

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		VSS+0.4	V	IOL = 12.0 mA
Output High voltage	VOH	VDD-0.4		V	IOH = -4.0 mA

SPEAKER

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		VSS+0.4	V	IOL = 24.0 mA
Tristate Leakage current	IOZ	-1	0	uA	VOUT = VDD

CPUA20

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VDD = 5 V +/- 0.25 V
Input high voltage	VIH	2.0	VDD	V	VDD = 5 V +/- 0.25 V
Input low current	IIL	-105	-25	uA	VIN = VSS
Input high current	IIH	-1	1	uA	VIN = VDD
Output low voltage	VOL		VSS+0.4	V	IOL = 2.0 mA
Output high voltage	VOH	VDD-0.4		V	IOH = -1.0 mA
Tristate Leakage current	IOZ	-105	-25	uA	VOUT = VDD or VSS

D0-15, A0-23, HOLD, NPEREQ, /PCS 1-4

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VDD = 5 V +/- 0.25 V
Input high voltage	VIH	2.0	VDD	V	VDD = 5 V +/- 0.25 V
Input low current	IIL	-105	-25	uA	VIN = VSS
Input high current	IIH	-1	1	uA	VIN = VDD
Output low voltage	VOL		VSS+0.4	V	IOL = 6.0 mA
Output high voltage	VOH	VDD-0.4		V	IOH = -2.0 mA
Tristate Leakage current	IOZ	-105	-25	uA	VOUT = VDD or VSS

DPARL, DPARH, SD0-15, /MEMR, /MEMW, /IOR, /IOW, /REFRESH

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS	0.8	V	VDD = 5 V +/- 0.25 V
Input high voltage	VIH	2.0	VDD	V	VDD = 5 V +/- 0.25 V
Input low current	IIL	-105	-25	uA	VIN = VSS
Input high current	IIH	-1	1	uA	VIN = VDD
Output low voltage	VOL		VSS+0.4	V	IOL = 12.0 mA
Output high voltage	VOH	VDD-0.4		V	IOH = -4.0 mA
Tristate Leakage Current	IOZ	-105	-25	uA	VOUT = VDD or VSS

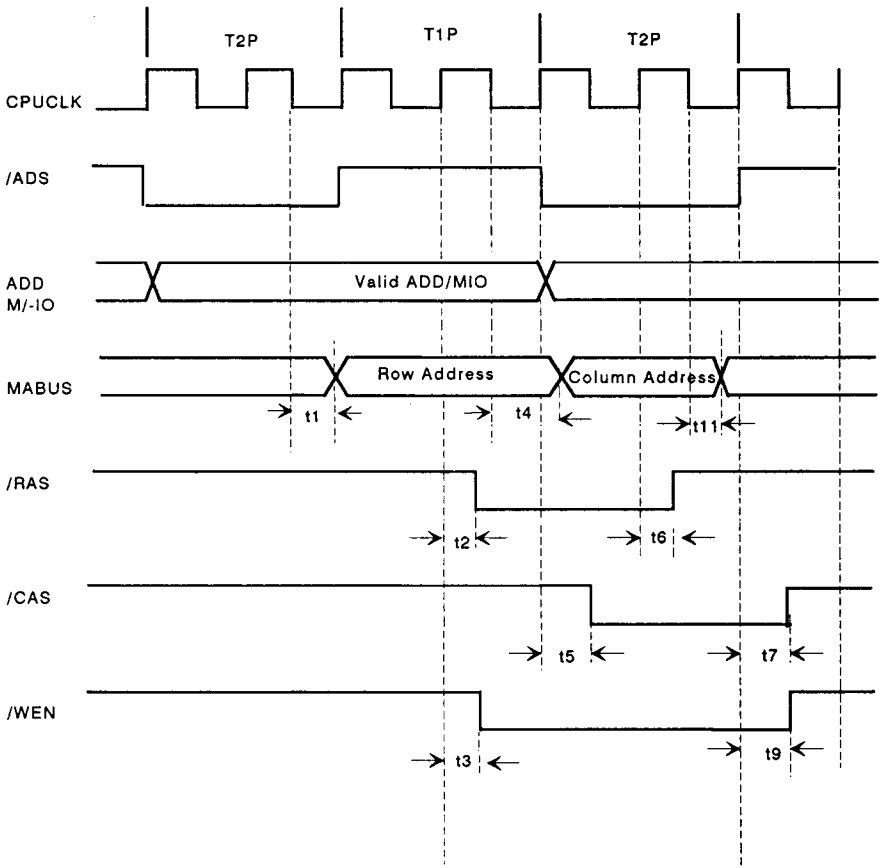
AC Specifications

VDD = 5 Volts ± 5% **Temperature = 0° - 70°** **Output Capacitance = 100PF**

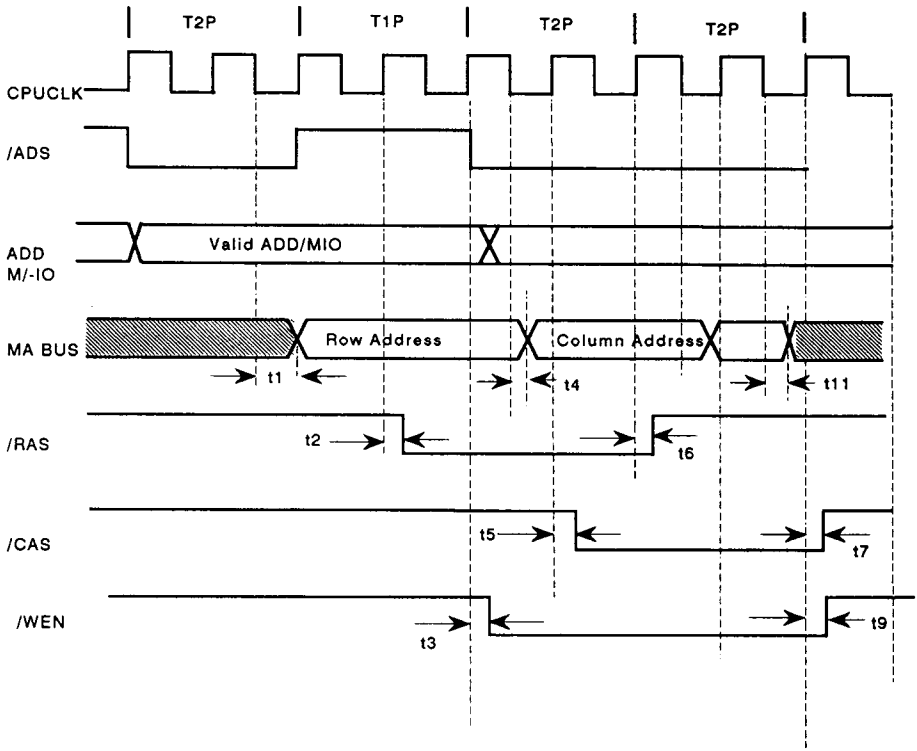
Symbol	Description	16 MHz		20 MHz		25 MHz*		33 MHz*		
		Max	Min	Max	Min	Max	Min	Max		Units
t1	Row address stable from CPUCLK falling edge	44.5	21.0	31.8	16.0	25.0	14	20		ns
t2	/RAS active delay from CPUCLK rising edge	25.5	7.6	18.2	7.6	18.2	6	13		ns
t3	/WEN active delay from CPUCLK rising edge	24.9	7.6	17.8	7.6	17.8	6	13		ns
t4	Column address stable from CPUCLK falling edge	30.3	10.3	20.0	8.0	16.0	6	13		ns
t5	/CAS active delay from CPUCLK rising edge	25.5	7.6	18.2	7.6	18.2	6	13		ns
t6	/RAS inactive delay from CPUCLK rising edge	26.0	6.9	18.6	6.9	18.6	6	13		ns
t7	/CAS inactive delay from CPUCLK rising edge	20.7	6.3	14.8	6.3	14.8	6	13		ns
t9	/WEN inactive delay from CPUCLK rising edge	21.0	7.0	15.0	7.0	15.0	6	13		ns
t11	Column address invalid from CPUCLK falling edge	42.6	21.5	30.4	16.0	25.0	14	20		ns

* 25 MHz and 33 MHz run at 1 wait state.

Direct Access (0WS) Memory Control Timing



Direct Access (1 WS) Memory Control Timing



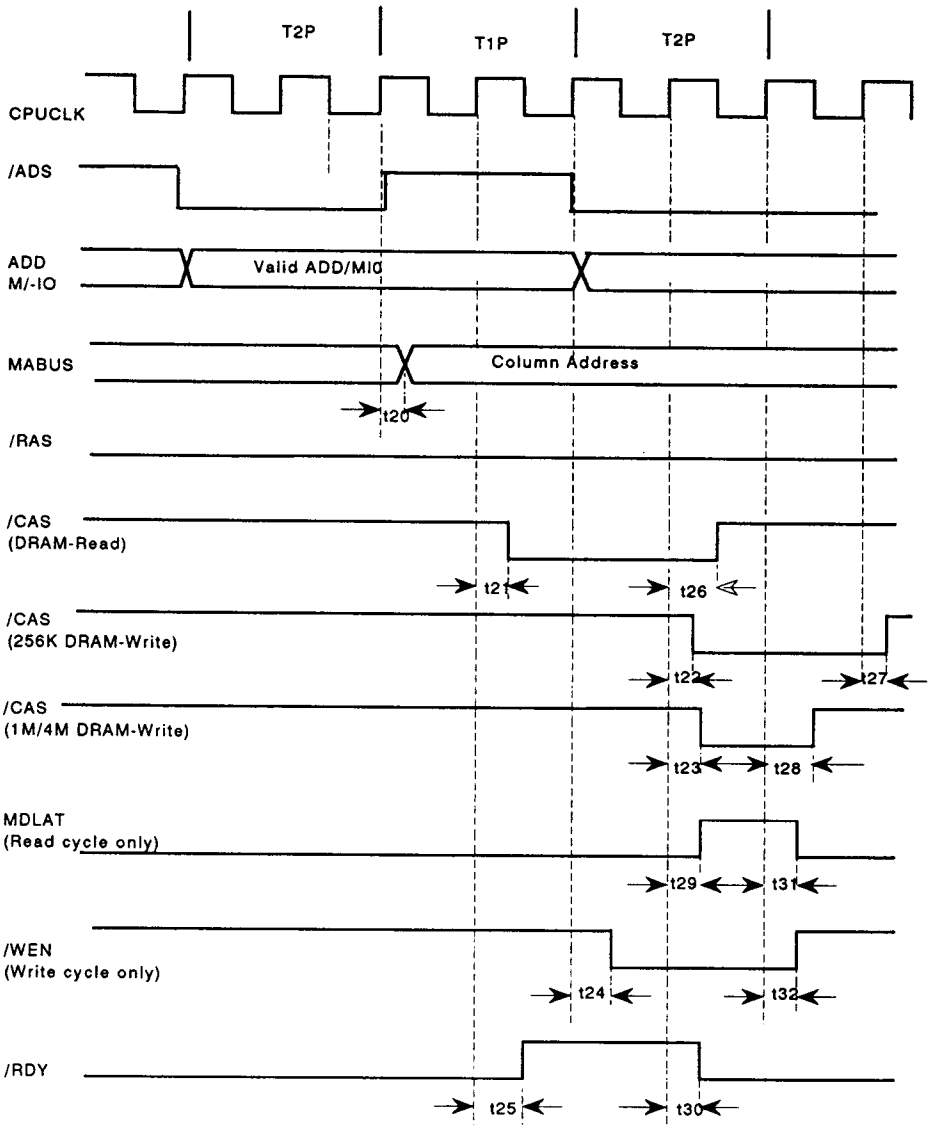
AC Specifications

VDD = 5 Volts ± 5% **Temperature = 0° - 70°** **Output Capacitance = 100PF**

Symbol	Description	16 MHz		20 MHz		25 MHz	33 MHz		Units
		Max	Min	Max	Min	Max	Min	Max	
t20	Column address stable from CPUCLK rising edge	24.4	8.2	17.4	8.2	17.4	6	12	ns
/CAS active delay from CPUCLK rising edge									
t21	In case of DRAM read cycle	25.8	7.8	18.4	7.8	18.4	6	15	ns
t22	In case of 256 DRAM write cycle	20.7	7.6	14.8	7.6	14.8	6	14	ns
t23	In case of 1M/4M DRAM write cycle	24.8	7.5	17.7	6.5	14.6	6	12	ns
t24	/WEN active delay from CPUCLK rising edge	25.2	7.6	18.0	7.6	18.0	6	15	ns
t25	/RDY inactive delay from CPUCLK rising edge*	9.3	3.2	5.0	3.2	5.0	3	5	ns
/CAS inactive delay from CPUCLK rising edge									
t26	In case of DRAM read cycle	22.1	6.3	15.8	6.3	15.8	6	15	ns
t27	In case of 256K DRAM write cycle	25.2	5.2	18.0	5.2	18.0	5	14	ns
t28	In case of 1M/4M DRAM write	20.4	6.5	14.6	6.5	14.6	6	15	ns
t29	MDLAT active delay from CPUCLK rising edge*	20.7	4.3	10.4	4.3	10.4	4	10	ns
t30	/RDY active delay from CPUCLK rising edge*	10.0	3.7	8.3	3.7	8.3	3	6	ns
t31	MDLAT inactive delay from CPUCLK rising edge*	20.9	4.1	11.4	4.1	11.4	4	10	ns
t32	/WEN inactive delay from CPUCLK rising edge	23.0	7.0	16.4	7.0	16.4	6	15	ns

* Tested under 25 pf.

Page Interleaved Memory Control Timing
Page Hit Cycle



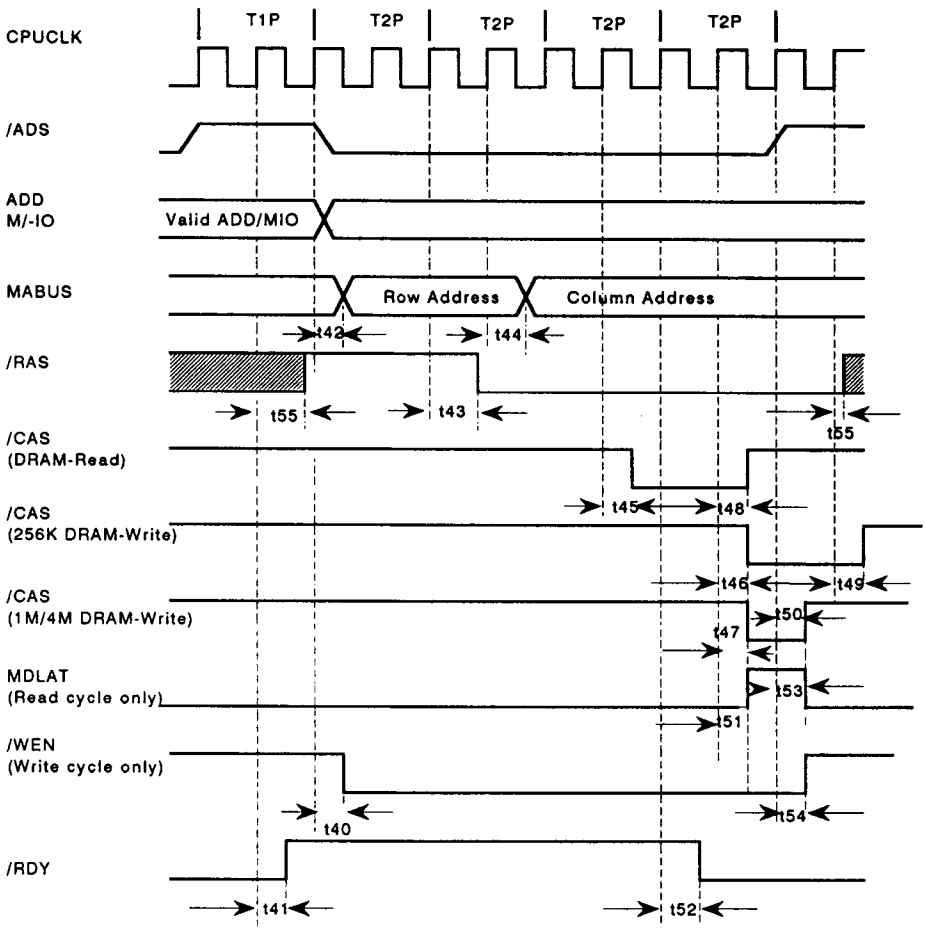
AC Specifications

VDD = 5 Volts ± 5% **Temperature = 0° - 70°** **Output Capacitance = 100PF**

Symbol	Description	16 MHz		20 MHz		25 MHz		33 MHz		Units
		Max	Min	Max	Min	Max	Min	Max		
t40	/WEN active delay from CPUCLK rising edge	23.2	7.6	16.6	7.6	16.6	6	15		ns
t41	/RDY inactive delay from CPUCLK rising edge*	10.0	2.3	5.0	2.3	5.0	2	5		ns
t42	Row address stable from CPUCLK rising edge	25.8	9.2	18.4	9.2	18.4	7	13		ns
t43	RAS active delay from CPUCLK rising edge	44.9	21.0	32.1	18.0	25.0	14	20		ns
t44	Column address stable from CPUCLK rising edge	28.9	18.5	27.8	16.4	22.4	14	20		ns
/CAS active delay from CPUCLK falling edg										
t45	DRAM - read cycle	24.5	7.3	17.5	7.3	17.5	6	13		ns
t46	256K DRAM - write cycle	24.5	7.6	17.6	7.6	17.6	6	13		ns
t47	1M/4M DRAM - write cycle	25.2	7.8	18.0	7.8	18.0	6	12		ns
/CAS inactive delay from CPUCLK rising edge										
t48	DRAM - read cycle	21.6	6.3	14.4	6.3	14.4	6	13		ns
t49	256K DRAM - write cycle	18.8	4.8	13.4	4.8	13.4	4	13		ns
t50	1M/4M DRAM - write cycle	20.2	5.9	14.4	5.9	14.4	6	15		ns
t51	MDLAT active delay from CPUCLK rising edge*	20.7	3.5	9.7	3.5	9.7	3	9		ns
t52	/RDY active delay from CPUCLK rising edge*	35.0	17.4	23.7	17.4	23.7	15	20		ns
t53	MDLAT inactive delay from CPUCLK*	20.7	4.0	10.7	4.0	10.7	4	9		ns
t54	/WEN inactive delay from CPUCLK	25.5	7.4	18.2	7.4	18.2	6	13		ns
t55	/RAS inactive delay from CPUCLK	22.7	6.8	16.2	6.8	16.2	6	13		ns

* Tested under 25 pf.

Page Interleaved Memory Control Timing
Page Miss Cycle



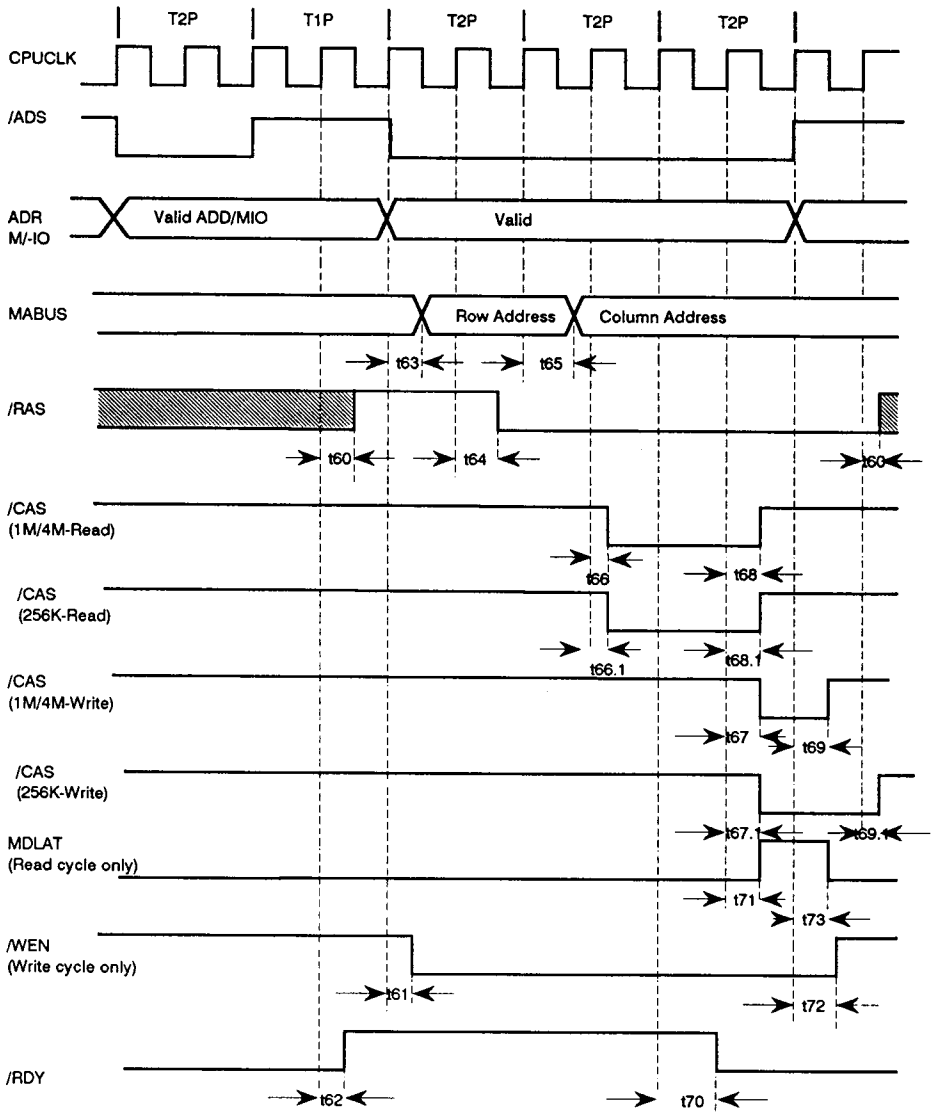
AC Specifications

VDD = 5 Volts ± 5% Temperature = 0° - 70° Output Capacitance = 100PF

Symbol	Description	16 MHz Max	20 MHz Min	20 MHz Max	25 MHz Min	25 MHz Max	33 MHz Min	33 MHz Max	Units
t60	/RAS inactive delay from CPUCLK rising edge	22.8	6.8	16.3	6.8	16.3	6	13	ns
t61	/WEN active delay from CPUCLK rising edge	23.2	8.4	16.6	8.4	16.6	6	15	ns
t62	/RDY inactive delay from CPUCLK rising edge*	10.0	2.3	5.0	2.3	5.0	2	5	ns
t63	Row address stable from CPUCLK rising edge	25.8	9.4	18.4	9.4	18.4	7	13	ns
t64	/RAS active delay from CPUCLK rising edge	44.9	25.4	32.1	18.0	25.0	14	20	ns
t65	Column address stable from CPUCLK rising edge	29.3	22.1	28.1	16.4	22.4	14	20	ns
	/CAS active delay from CPUCLK falling edge								
t66	In case of 1M/4M read cycle	25.5	7.3	18.2	7.3	18.2	6	14	ns
t66.1	In case of 256K read cycle	25.6	7.3	18.1	7.3	18.1	6	14	ns
t67	In case of 1M/4M write cycle	25.2	6.4	14.4	6.4	14.4	6	12	ns
t67.1	In case of 256K write cycle	25.6	7.6	18.1	7.6	18.1	6	14	ns
	/CAS inactive delay from CPUCLK falling edge								
t68	In case of 1M/4M read cycle	20.0	6.4	14.8	6.4	14.8	6	14	ns
t68.1	In case of 256K read cycle	18.4	3.9	13.0	3.9	13.3	6	14	ns
t69	In case of 1M/4M write cycle	20.2	6.4	14.4	6.4	14.4	6	15	ns
t69.1	In case of 265K write cycle	18.6	3.9	13.3	3.9	13.3	3	14	ns
t70	/RDY active delay from CPUCLK*	35.0	17.4	23.7	17.4	23.7	16	20	ns
t71	MDLAT active delay from CPUCLK*	20.1	3.5	9.7	3.5	9.7	3	9	ns
t72	/WEN inactive delay from CPUCLK	25.5	8.1	18.2	8.1	18.2	6	13	ns
t73	MDLAT inactive delay from CPUCLK*	21.1	4.0	10.7	4.0	10.7	4	9	ns

* Tested under 25 pf.

Turbo Page Interleaved Memory Control Timing
Page Miss Cycle



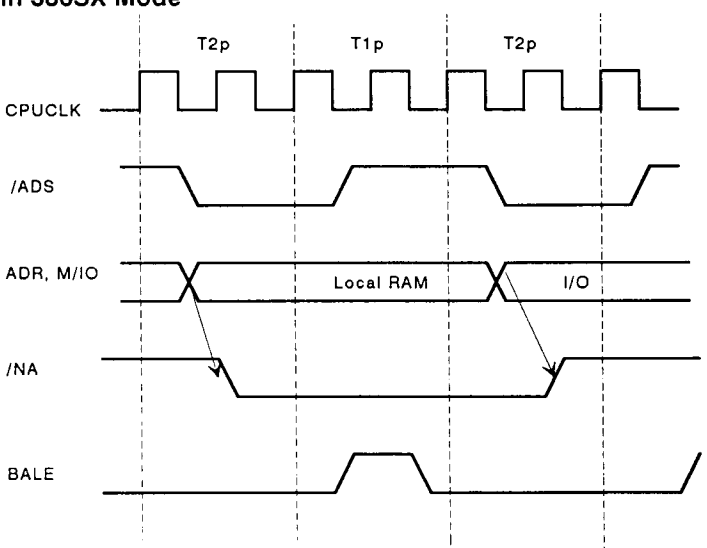
AC Specifications

VDD = 5 Volts ± 5% **Temperature = 0° - 70°** **Output Capacitance = 100PF**

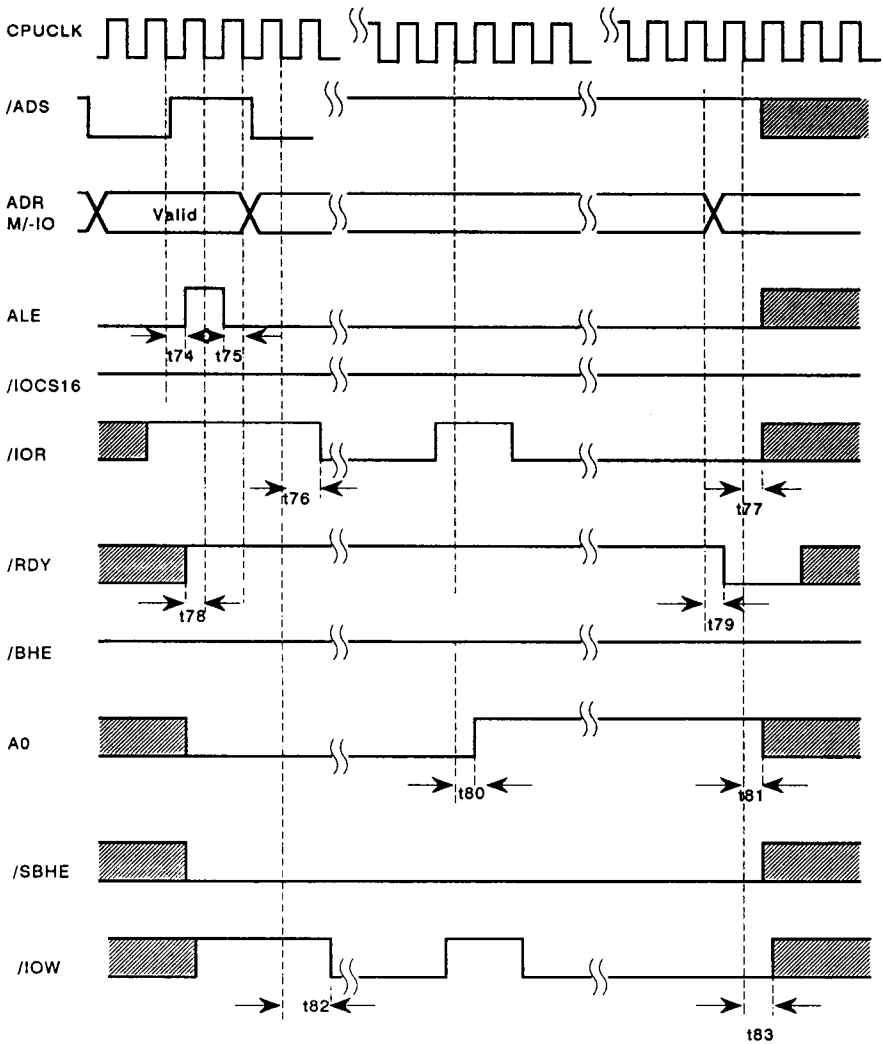
Symbol	Description	16 MHz Max	20/25 MHz Min	20/25 MHz Max	33 MHz Min	33 MHz Max	Unit
t74	ALE active delay from CPUCLK falling	13.4	3.9	9.6	3	10	ns
t75	ALE inactive delay from CPUCLK falling	17.9	5.3	12.8	5	13	ns
t76	/IOR active delay from CPUCLK rising	35	10.2	25	6	20	ns
t77	/IOR inactive delay from CPUCLK rising	25	10.4	25	6	20	ns
t78	/RDY inactive delay from CPUCLK rising*	19.0	2.3	8.4	2	9	ns
t79	/RDY active delay from CPUCLK rising*	14.7	3.4	5.3	3	6	ns
t80	A0 rising from CPUCLK rising	44.7	13.2	31.9	10	26	ns
t81	A0 falling from CPUCLK falling	44.1	12.8	31.5	10	26	ns
t82	/IOW active delay from CPUCLK rising	35	10.2	25	8	20	ns
t83	/IOW inactive delay from CPUCLK rising	39.2	10.4	26.1	8	21	ns

* Tested under 25 pf.

In 386SX Mode



BUS Conversion



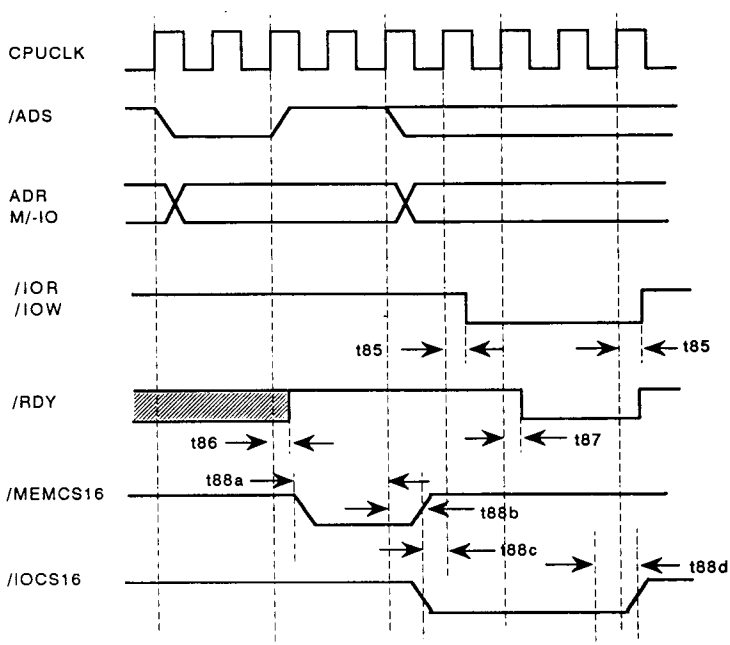
AC Specifications

VDD = 5 Volts ± 5% **Temperature = 0° - 70°** **Output Capacitance = 100PF**

Symbol	Description	16 MHz Max	20/25 MHz Min	20/25 MHz Max	33 MHz Min	33 MHz Max	Unit
t84	/IOR, /IOW active delay from CPUCLK rising	34.4	10	24.6	8	20	ns
t85	/IOR, /IOW inactive delay from CPUCLK	32.5	10	23.2	8	20	ns
t86	/RDY inactive delay from CPUCLK*	9.6	3.2	5.4	3	6	ns
t87	/RDY active delay from CPUCLK *	13.8	3.8	8.4	3	9	ns
t88a	/MEMCS16 set up time from CPUCLK		20		10		
t88b	/MEMCS16 hold time from CPUCLK		15		10		
t88c	/IOCS16 set up time from CPUCLK		30		30		
t88d	/IOCS16 hold time from CPUCLK		20		10		

* Tested under 25 pf.

I/O Read/Write

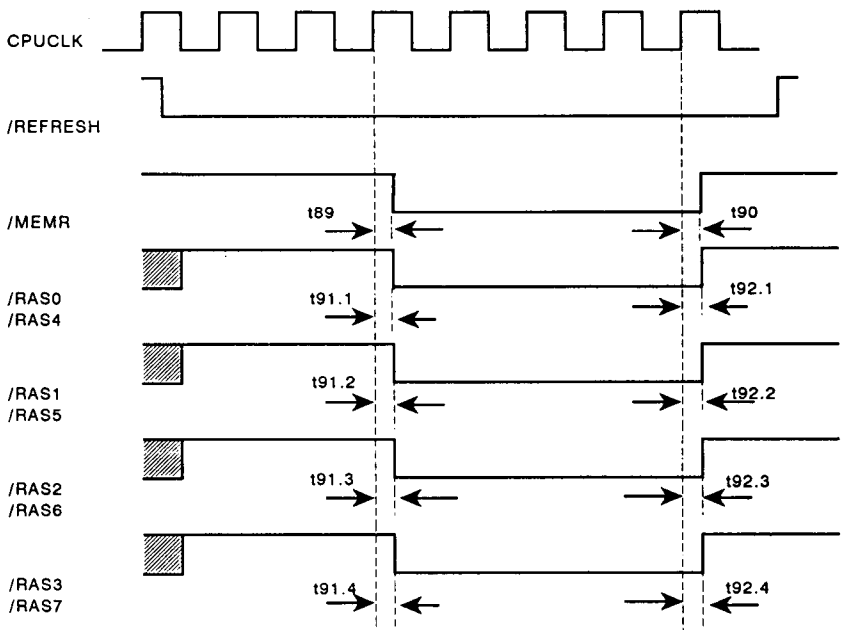


AC Specifications

VDD = 5 Volts ± 5% Temperature = 0° - 70° Output Capacitance = 100PF

Symbol	Description	16 MHz Max	20/25 MHz Min	20/25 MHz Max	33 MHz Min	33 MHz Max	Unit
t89	/MEMR active delay from CPUCLK rising	43.5	12.7	31.1	9	25	ns
t90	/MEMR inactive delay from CPUCLK rising	36.0	10.8	25.7	9	21	ns
t91.1	/RAS0, /RAS4 active delay from CPUCLK rising	32.1	10.2	21.4	8	18	ns
t91.2	/RAS1, /RAS5 active delay from CPUCLK rising	30.5	9.5	21.8	8	18	ns
t91.3	/RAS2, /RAS6 active delay from CPUCLK rising	31.9	9.6	22.8	8	19	ns
t91.4	/RAS3, /RAS7 active delay from CPUCLK rising	33.6	10.2	24.0	8	21	ns
t92.1	/RAS0, /RAS4 inactive delay from CPUCLK rising	26.3	7.8	18.8	8	16	ns
t92.2	/RAS1, /RAS5 inactive delay from CPUCLK rising	26.9	8.2	19.2	8	17	ns
t92.3	/RAS2, /RAS6 inactive delay from CPUCLK rising	29.1	8.9	20.8	8	17	ns
t92.4	/RAS3, /RAS7 inactive delay from CPUCLK rising	30.0	9.1	21.4	8	18	ns

REFRESH

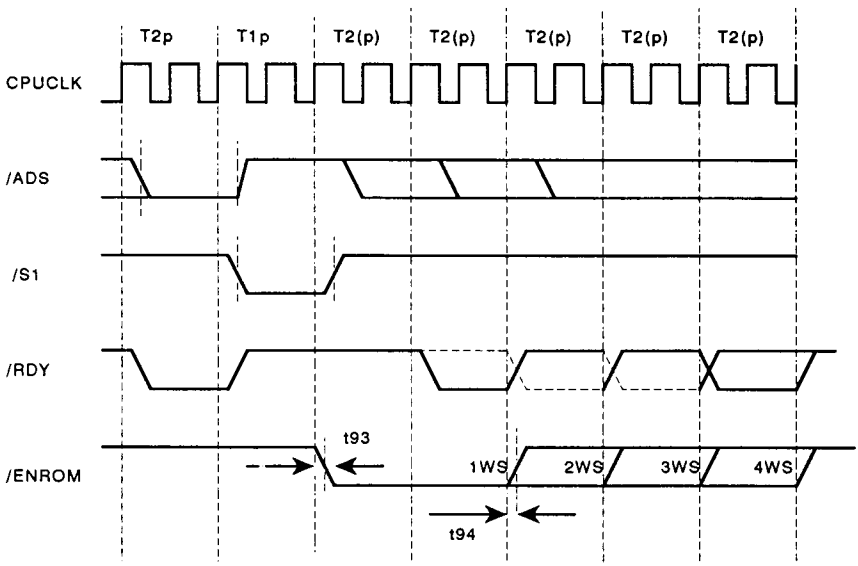

CPUCLK
/REFRESH
/MEMR
t89
t90
/RAS0
/RAS4
t91.1
t92.1
/RAS1
/RAS5
t91.2
t92.2
/RAS2
/RAS6
t91.3
t92.3
/RAS3
/RAS7
t91.4
t92.4

AC Specifications

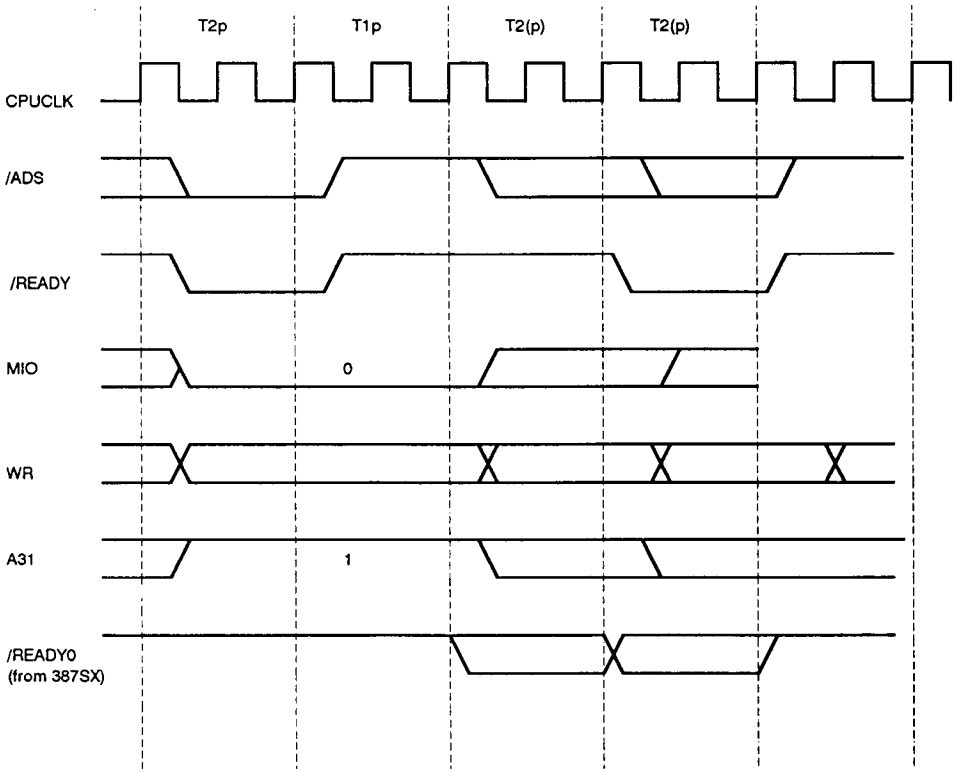
VDD = 5 Volts ± 5% Temperature = 0° - 70° Output Capacitance = 100PF

Symbol	Description	16 MHz Max	20/25 MHz Min	20/25 MHz Max	33 MHz Min	33 MHz Max	Unit
t93	/ENROM active delay from CPUCLK rising	21.4	5.9	15.3	5	15	ns
t94	/ENROM inactive delay from CPUCLK rising	18.6	6.1	13.1	5	13	ns

ROM Cycles



386SX Mode 387SX Coprocessor Timing



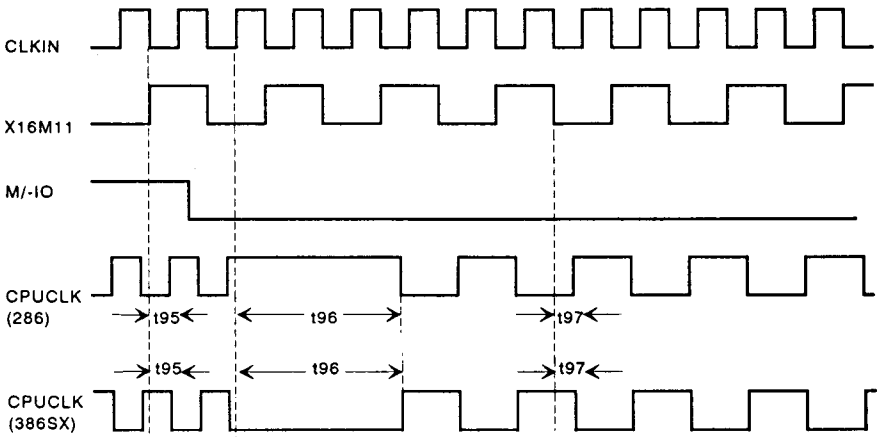
AC Specifications

VDD = 5 Volts ± 5% **Temperature = 0° - 70°** **Output Capacitance = 100PF**

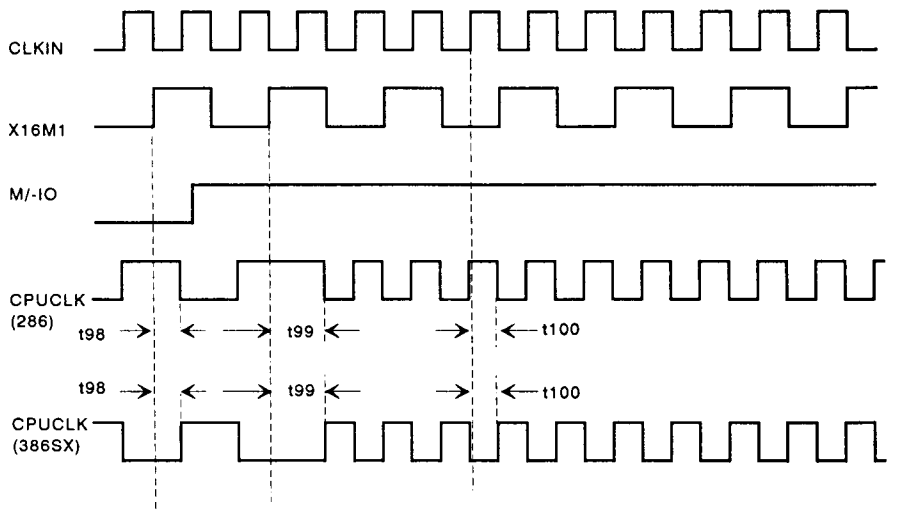
Symbol	Description	16 MHz	20/25 MHz		33 MHz		Unit
		Max	Min	Max	Min	Max	
t95	CPUCLK falling delay from CLKIN falling*	32.0	8.8	21.4	8	18	ns
t96	CPUCLK rising switching delay from CLKIN rising*	115.0	69.2	80.8	60	80	ns
t97	CPUCLK falling delay from X16M1 falling*	47.8	13.2	32.7	12	32	ns
t98	CPUCLK rising delay from X16M1 rising*	42.7	11.6	29.1	10	29	ns
t99	CPUCLK rising switching delay from X16M1 rising*	30.6	9.2	20.4	9	20	ns
t100	CPUCLK rising delay from CLKIN rising*	27.8	7.4	18.4	7	18	ns

* Tested under 25 pf.

Clock Switching from High to Low



Clock Switching from Low to High

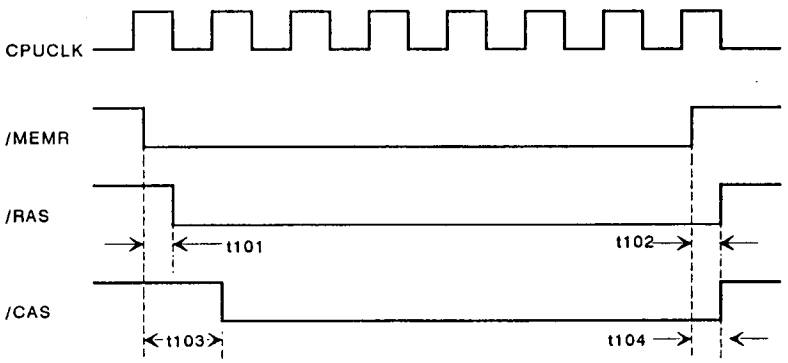


AC Specifications

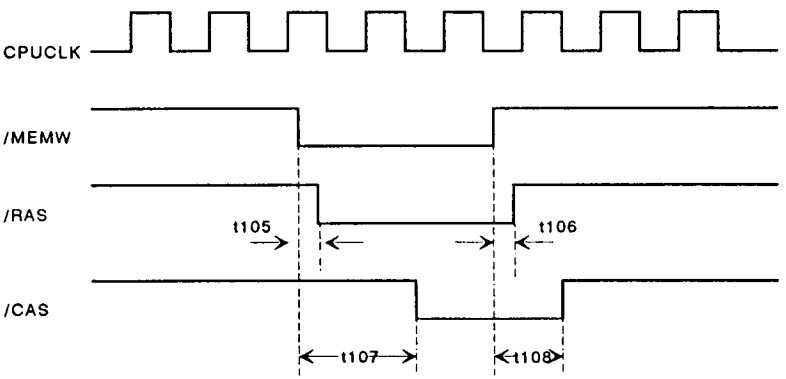
VDD = 5 Volts ± 5% Temperature = 0° - 70° Output Capacitance = 100PF

Symbol	Description	16 MHz Max	20/25 MHz Min	20/25 MHz Max	33 MHz Min	33 MHz Max	Unit
DMA Memory Read							
101	/RAS active delay from /MEMR falling	17.5	5.6	12.5	5	12	ns
t102	/RAS inactive delay from /MEMR rising	16.8	5.3	12	5	12	ns
t103	/CAS active delay from /MEMR falling	175.0	110.9	125.0	110	120	ns
t104	/CAS inactive delay from /MEMR rising	14.8	51	10.6	5	11	ns
DMA Memory Write							
t105	/RAS active delay from /MEMW falling	21.0	6.7	15	6	15	ns
t106	/RAS inactive delay from /MEMW rising	18.5	5.3	13.2	5	13	ns
t107	/CAS active delay from /MEMW falling	173.2	107.6	123.7	107	120	ns
t108	/CAS inactive delay from /MEMW rising	82.7	41	59.1	40	48	ns

DMA
Memory Read



DMA
Memory Write

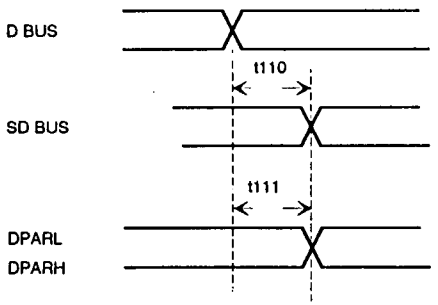


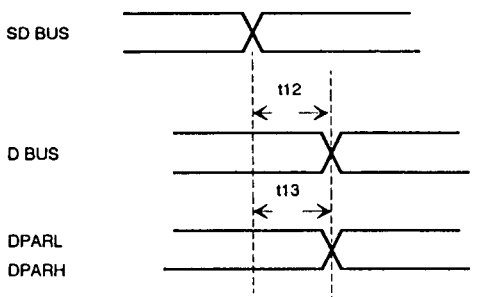
ACC 2036 Data Buffer AC Specifications

VDD = 5 Volts ± 5% **Temperature = 0° - 70°** **Output Capacitance = 100PF**

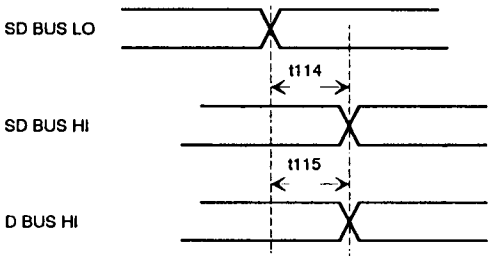
Symbol	Description	16 MHz	20/25 MHz		33 MHz		Unit
		Max	Min	Max	Min	Max	
t110	D BUS in to SD BUS out	41.2	13.5	29.4	12	25	ns
t111	D BUS in to DPARL or DPARH (CPU to memory access)	43.4	11.4	31	10	25	ns
t112	SD BUS in to D BUS out	54.9	16.2	39.2	15	32	ns
t113	SD BUS in to DPARL or DPARH (DMA memory access)	33.6	6.2	24	5	20	ns
t114	SD BUS low to SD BUS high data out	48.4	14.2	34.6	13	30	ns
t115	SD BUS low to D BUS high data out	70	20.5	50	18	42	ns
t116	A20 active to A20GATE delay	52.5	15.6	37.5	13	32	ns

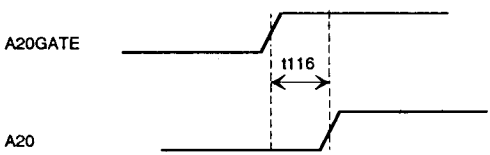
ACC 2036 Data Buffer Timing





ACC 2036 Data Buffer Timing



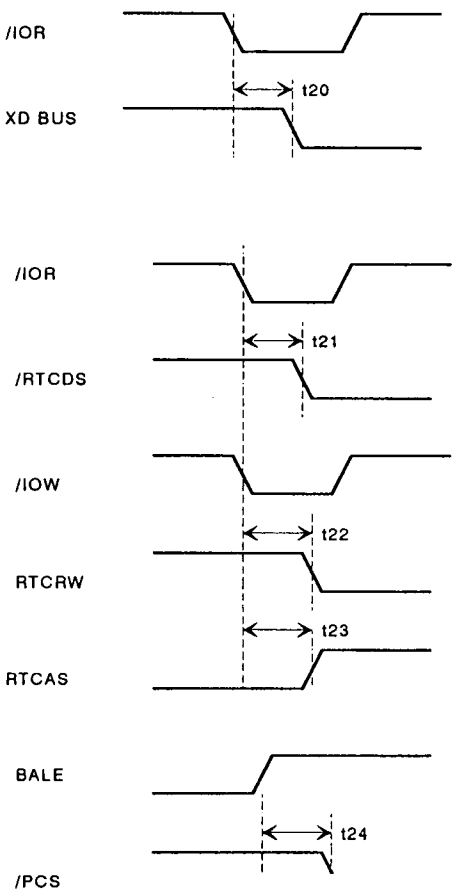


ACC 2036 Address Buffer AC Specifications

VDD = 5 Volts ± 5% Temperature = 0° - 70° Output Capacitance = 100PF

Symbol	Description	16 MHz	20/25 MHz		33 MHz		Unit
		Max	Min	Max	Min	Max	
t120	/IOR to D OUT (Read config Reg 0F3H)	60.2	18.5	43.2	16	35	ns
t121	/IOR to /RTCDS	37.0	11.1	26.4	10	20	ns
t122	/IOW to RTCRW	35.3	10.8	25.2	10	20	ns
t123	/IOW to RTCAS	35.3	10.8	25.2	10	20	ns
t124	CPU address valid to chip select output (/PCS)	46.5	13.5	33.2	12	26	ns

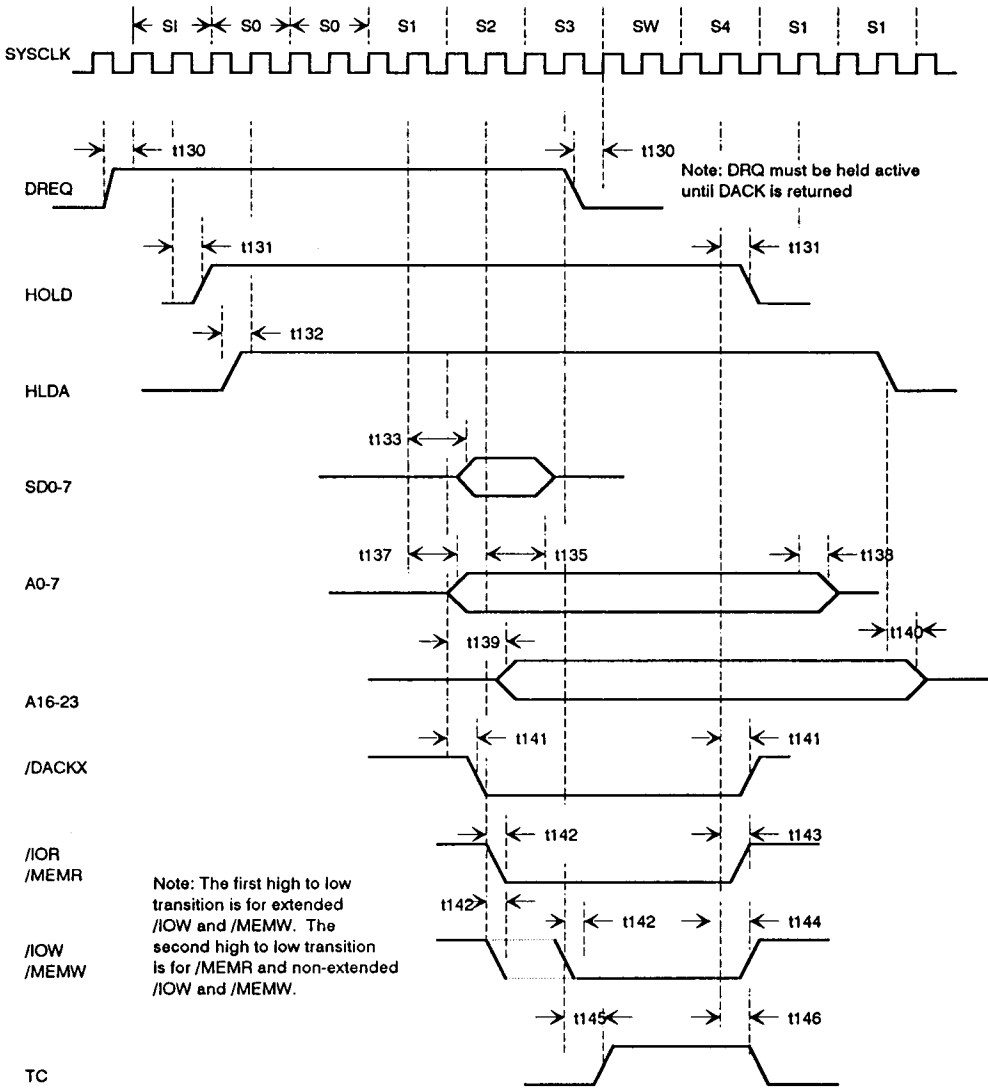
ACC 2036 Address Buffer Timing



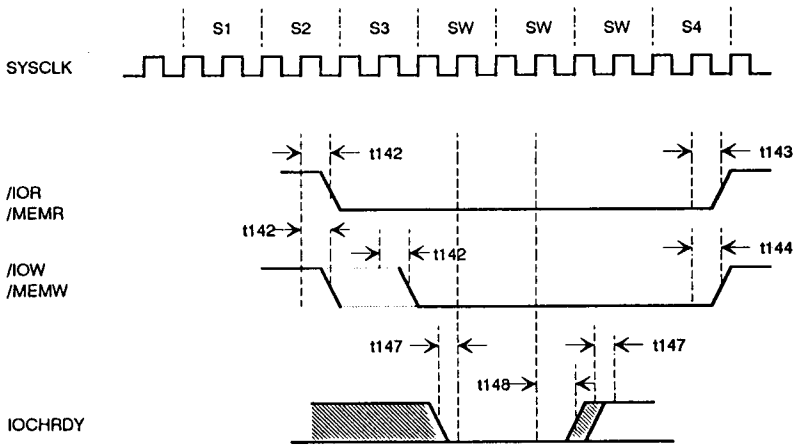
AC Specifications

Symbol	Parameter	Min	Max	Units
t130	DRQ to SYSCLK high setup time	0		ns
t131	HOLD valid from SYSCLK high delay time		50	ns
t132	HLDA to SYSCLK high setup time	25		ns
t133	Data float to active delay from SYSCLK high		93	ns
t135	Data active to float delay from SYSCLK high		92	ns
t137	low byte ADDR float to active from SYSCLK high		180	ns
t138	low byte ADDR active to float delay from SYSCLK high		70	ns
t139	high byte ADDR float to active delay from SYSCLK high		123	ns
t140	high byte add active to float from HLDA low		35	ns
t141	/DACK valid from SYSCK high delay time		83	ns
t142	/IOR, /IOW, /MEMR, /MEMW active from SYSCLK high delay time		53	ns
t143	/IOR and /MEMR inactive from SYSCLK high delay time		97	ns
t144	/IOW and /MEMW inactive from SYSCLK high delay time		80	ns
t145	TC active from SYSCLK high delay time		82	ns
t146	TC inactive from SYSCLK high delay time		82	ns
t147	IOCHRDY input setup time to SYSCLK high	26		ns
t148	IOCHRDY input hold time from SYSCLK high	15		ns

DMA Timing


SI
S0
S0
S1
S2
S3
SW
S4
S1
S1
SYSCLK
t130
t130
DREQ
Note: DRQ must be held active until DACK is returned
t131
t131
HOLD
t132
HLDA
t133
SD0-7
t137
t135
t138
A0-7
t140
t139
A16-23
t141
t141
/DACKX
t142
t143
/IOR
/MEMR
t142
t142
t144
/IOW
/MEMW
t145
t146
TC
Note: The first high to low transition is for extended /IOW and /MEMW. The second high to low transition is for /MEMR and non-extended /IOW and /MEMW.

IOCHRDY Timing

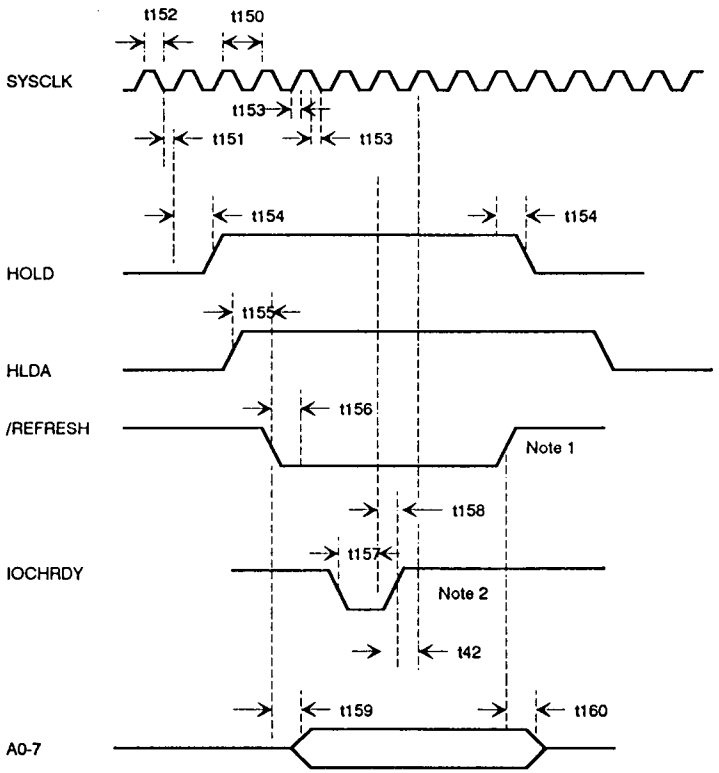


The first wait state is inserted by the internal circuitry.
Additional wait states must be inserted using IOCHRDY.

AC Specifications

Symbol	Parameter	Min	Max	Units
t150	SYSCLK cycle time	62		ns
t151	SYSCLK pulse width low	25		ns
t152	SYSCLK pulse width high	25		ns
t153	SYSCLK rise/fall time	10		ns
t154	HOLD valid from SYSCLK high delay time		50	ns
t155	/REFRESH low delay from HLDA		40	ns
t156	/REFRESH low to SYSCLK high setup time		20	ns
t157	IOCHRDY input setup time to SYSCLK high	26		ns
t158	IOCHRDY input hold time from SYSCLK high	15		ns
t159	Refresh address valid delay from /REFRESH		92	ns
t160	Refresh address hold time from /REFRESH inactive		88	ns

Refresh Timing



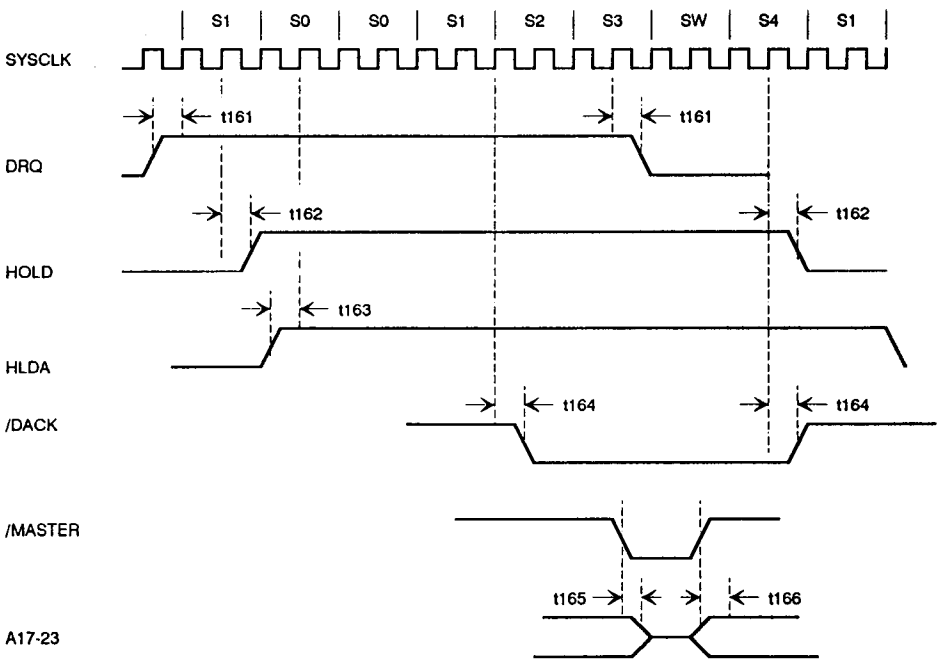
Notes

1 A /REFRESH pulse is normally four SYSCLK cycles long.
2 /REFRESH cycles can be extended by inserting wait states using IOCHRDY.

AC Specifications

Symbol	Parameter	Min	Max	Units
t161	DRQ to SYSCLK high setup time	0		ns
t162	HOLD valid from SYSCLK high delay time		50	ns
t163	HLDA to SYSCLK high set up time	25		ns
t164	/DACK valid from SYSCLK high delay time		83	ns
t165	A17-A23 float from /MASTER low delay time	11	36	ns
t166	A17-A23 active from /MASTER high delay time	11	36	ns

/MASTER Timing

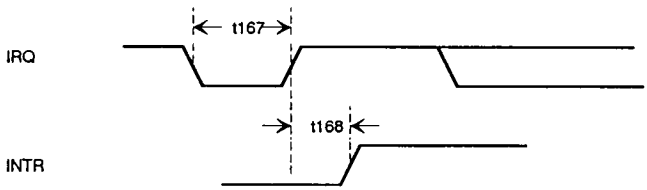


Note: A new bus master must be programmed in Cascade mode.
The new master must not pull /MASTER low until it has received the corresponding /DACK signal.

AC Specifications

Symbol	Parameter	Min	Max	Units
t167	Interrupt request pulse width low	60		ns
t168	Interrupt output delay		63	ns

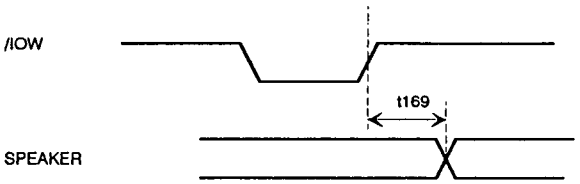
Interrupt Timing



AC Specifications

Symbol	Parameter	Min	Max	Units
t59	SPEAKER valid from /IOW high delay time		100	ns

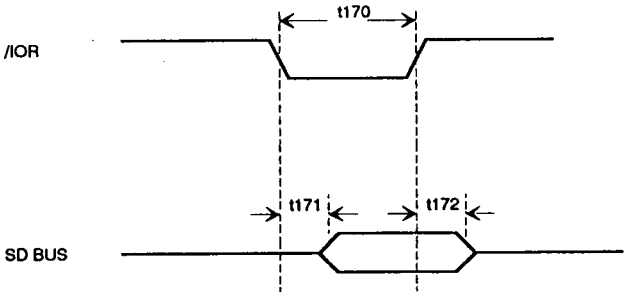
8254 Timing



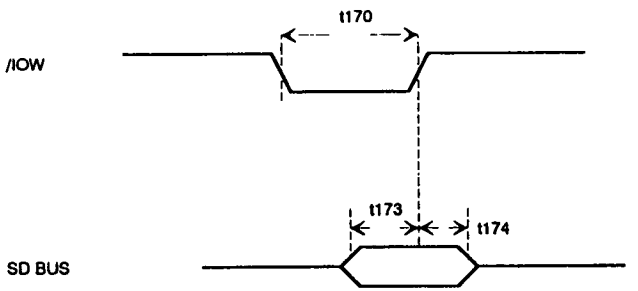
AC Specifications

Symbol	Parameter	Min	Max	Units
t170	/IOR or /IOW pulse width	110		ns
t171	D data valid delay from /IOR low		110	ns
t172	D data float delay from /IOR high	0	90	ns
t173	D data valid to /IOW high setup time	70		ns
t174	D data hold time from /IOW high	15		ns
t175	RESET high pulse width	250		ns
t176	RESET inactive to first /IOR or /IOW command	4		SYSCLK Cycle
t177	Command recovery time between successive /IOR or /IOW pulses	125		ns
t178	NMI output delay		68	ns

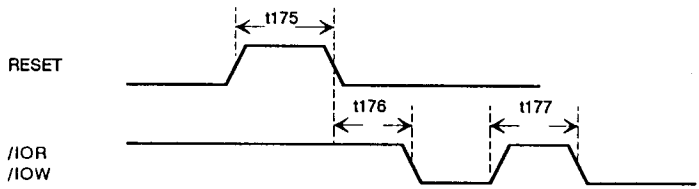
Peripheral Read Timing



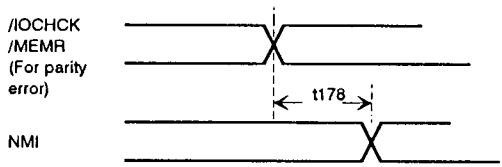
Peripheral Write Timing



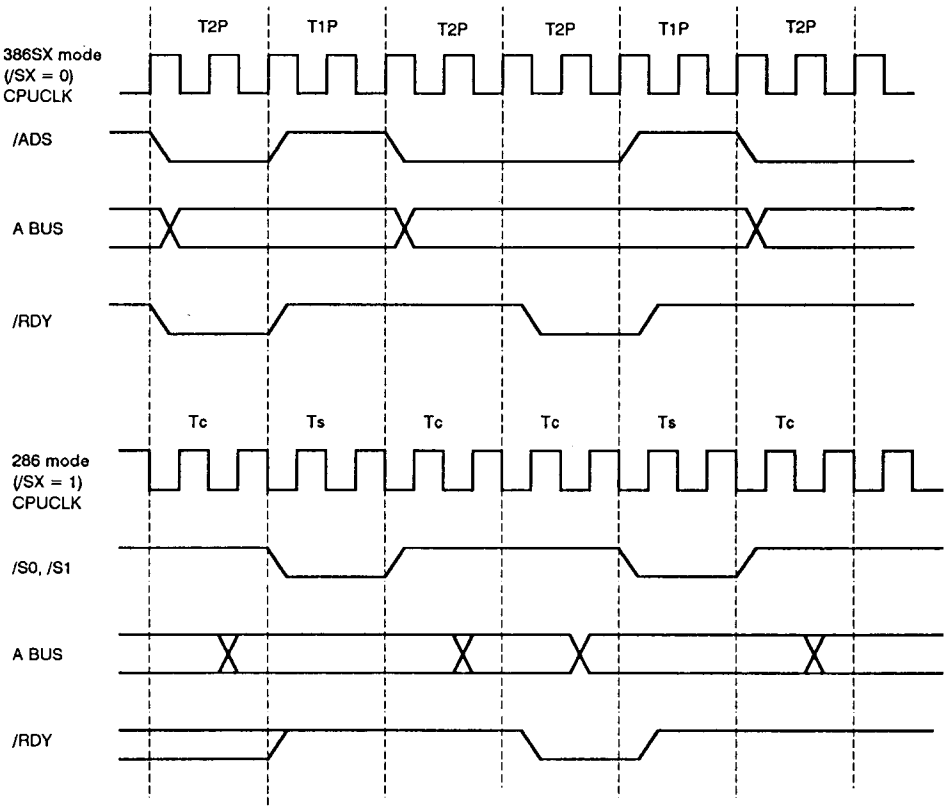
Command and Reset Timing



Other Timing Waveforms



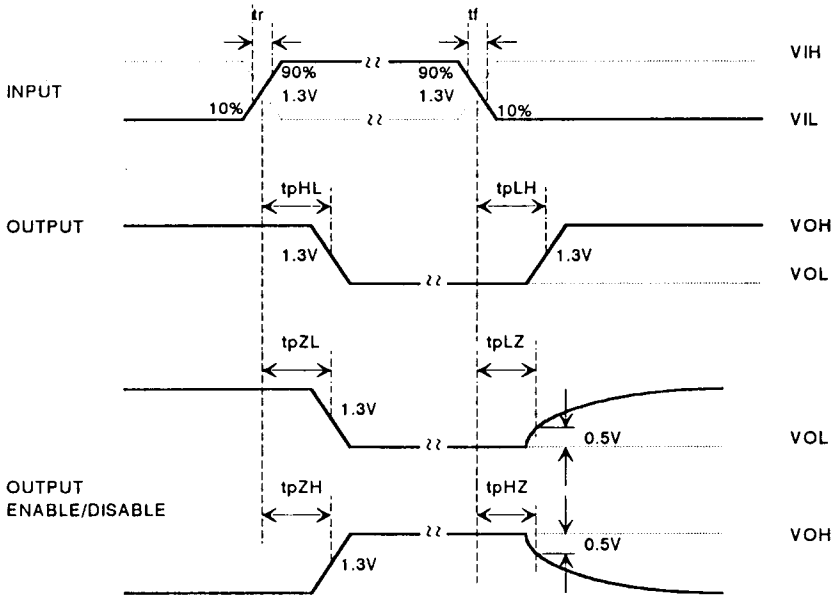
Relationship between 386SX Mode and 286 Mode



Load Circuit and AC Characteristics Measurement

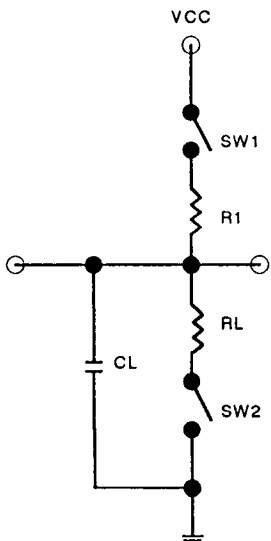
Parameter	Output Type	Symbol	CL(pF)	R1	RL	SW1	SW2
Propagation	Totem pole						
Delay	3-state	tPLH	100		1.0K	off	on
		tPHL	100		1.0K	off	on
Time	Bidirectional						
Propagation	Open drain or	tPLH	100	0.5K		on	off
Delay time	Open collector	tPHL	100	0.5K		on	off
Disable time	3-state	tPLZ	100	0.5K	1.0K	on	on
	Bidirectional	tPHZ	100	0.5K	1.0K	off	on
Enable time	3-state	tPZL	100	0.5K	1.0K	on	on
	Bidirectional	tPZH	100	0.5K	1.0K	off	on

AC Characteristics Measurement



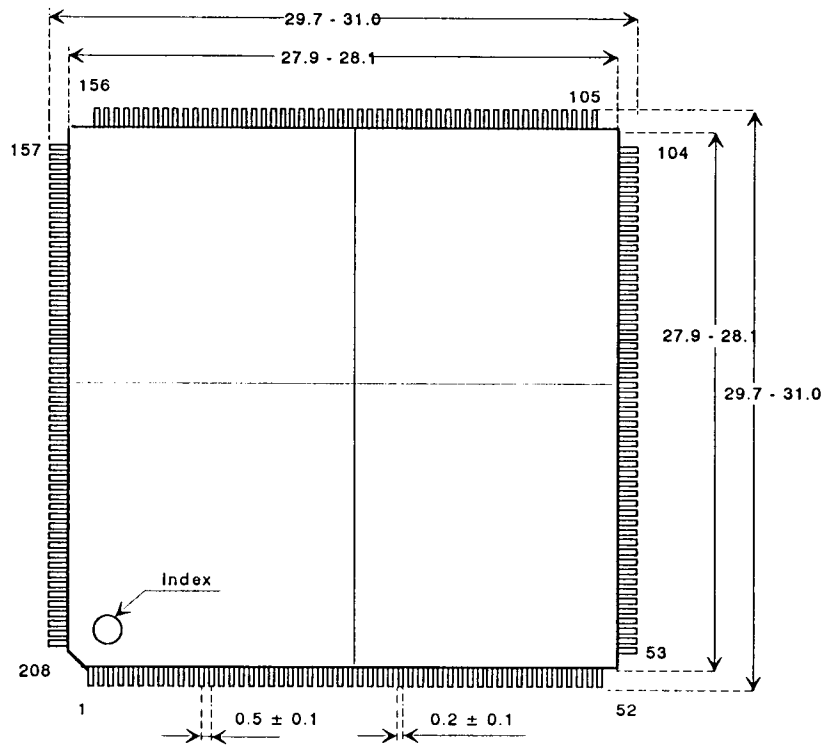
VIH = 3 V, VIL = 0, tr ≤ 10 ns, tf ≤ 5 ns

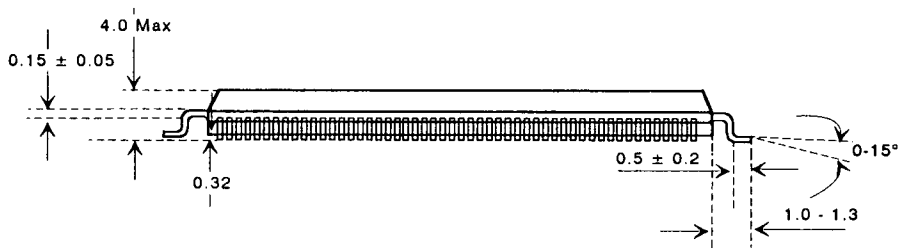
Load Circuit



Production Package Specification

Package: 208-pin PQFP
Unit: (mm)
Chip: 2036





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